Second Edition

Microwave and Wireless Synthesizers

Theory and Design

Ulrich L. Rohde
Enrico Rubiola
Jerry C. Whitaker

WILEY

Microwave and Wireless Synthesizers: Theory and Design, Second Edition.
Ulrich L. Rohde, Enrico Rubiola, and Jerry C. Whitaker.
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MICROWAVE AND WIRELESS SYNTHESIZERS

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Theory and Design

SECOND EDITION

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CONTENTS

Author Biography xii

Preface xvi

Important Notations xx

1 Loop Fundamentals 1

1-1 Introduction to Linear Loops / 1
1-2 Characteristics of a Loop / 3
1-3 Digital Loops / 7
1-4 Type 1 First-Order Loop / 10
1-5 Type 1 Second-Order Loop / 12
1-6 Type 2 Second-Order Loop / 20
1-6-1 Transient Behavior of Digital Loops Using Tri-state Phase Detectors / 22
1-7 Type 2 Third-Order Loop / 27
1-7-1 Transfer Function of Type 2 Third-Order Loop / 28
1-7-2 FM Noise Suppression / 35
1-8 Higher-Order Loops / 36
1-8-1 Fifth-Order Loop Transient Response / 36
1-9 Digital Loops with Mixers / 40
1-10 Acquisition / 44
Example 1 / 48
1-10-1 Pull-in Performance of the Digital Loop / 49
1-10-2 Coarse Steering of the VCO as an Acquisition Aid / 52
1-10-3 Loop Stability / 54
References / 62
Suggested Reading / 62

2 Almost all About Phase Noise 65

2-1 Introduction to Phase Noise / 65
2-1-1 The Clock Signal / 65
2-1-2 The Power Spectral Density (PSD) / 68
2-1-3 Basics of Noise / 71
2-1-4 Phase and Frequency Noise / 78

2-2 The Allan Variance and Other Two-Sample Variances / 88
2-2-1 Frequency Counters / 89
2-2-2 The Two-Sample Variances AVAR, MVAR, and PVAR / 94
2-2-3 Conversion from Spectra to Two-Sample Variances / 96
2-3 Phase Noise in Components / 100
2-3-1 Amplifiers / 100
2-3-2 Frequency Dividers / 104
2-3-3 Frequency Multipliers / 112
2-3-4 Direct Digital Synthesizer (DDS) / 117
2-3-5 Phase Detectors / 128
2-3-6 Noise Contribution from Power Supplies / 132
2-4 Phase Noise in Oscillators / 133
2-4-1 Modern View of the Leeson Model / 134
2-4-2 Circumventing the Resonator's Thermal Noise / 144
2-4-3 Oscillator Hacking / 146
2-5 The Measurement of Phase Noise / 153
2-5-1 Double-Balanced Mixer Instruments / 154
2-5-2 The Cross-Spectrum Method / 166
2-5-3 Digital Instruments / 171
2-5-4 Pitfalls and Limitations of the Cross-Spectrum Measurements / 180
2-5-5 The Bridge (Interferometric) Method / 187
2-5-6 Artifacts and Oddities Often Found in the Real World / 190
References / 193
Suggested Readings / 197

3 Special Loops **201**

3-1 Introduction / 201
3-2 Direct Digital Synthesis Techniques / 201
3-2-1 A First Look at Fractional *N* / 202
3-2-2 Digital Waveform Synthesizers / 203
3-2-3 Signal Quality / 220
3-2-4 Future Prospects / 235
3-3 Loops with Delay Line as Phase Comparators / 236
3-4 Fractional Division *N* Synthesizers / 237
3-4-1 Example Implementation / 240
3-4-2 Some Special Past Patents for Fractional Division *N* Synthesizers / 253
References / 255
Bibliography / 256
Fractional Division *N* Readings / 256

4 Loop Components **259**

4-1 Introduction to Oscillators and Their Mathematical Treatment / 259
4-2 The Colpitts Oscillator / 259

4-2-1 Linear Approach / 260
4-2-2 Design Example for a 350 MHz Fixed-Frequency Colpitts Oscillator / 269
4-2-3 Validation Circuits / 282
4-2-4 Series Feedback Oscillator / 314
4-2-5 2400 MHz MOSFET-Based Push–Pull Oscillator / 319
4-2-6 Oscillators for IC Applications / 336
4-2-7 Noise in Semiconductors and Circuits / 337
4-2-8 Summary / 339
4-3 Use of Tuning Diodes / 339
4-3-1 Diode Tuned Resonant Circuits / 340
4-3-2 Practical Circuits / 344
4-4 Use of Diode Switches / 345
4-4-1 Diode Switches for Electronic Band Selection / 346
4-4-2 Use of Diodes for Frequency Multiplication / 347
4-5 Reference Frequency Standards / 351
4-5-1 Specifying Oscillators / 351
4-5-2 Typical Examples of Crystal Oscillator Specifications / 352
4-6 Mixer Applications / 354
4-7 Phase/Frequency Comparators / 357
4-7-1 Diode Rings / 357
4-7-2 Exclusive ORs / 358
4-7-3 Sample/Hold Detectors / 362
4-7-4 Edge-Triggered JK Master/Slave Flip-Flops / 368
4-7-5 Digital Tri-State Comparators / 369
4-8 Wideband High-Gain Amplifiers / 378
4-8-1 Summation Amplifiers / 378
4-8-2 Differential Limiters / 382
4-8-3 Isolation Amplifiers / 382
4-8-4 Example Implementations / 387
4-9 Programmable Dividers / 393
4-9-1 Asynchronous Counters / 393
4-9-2 Programmable Synchronous Up-/Down-Counters / 394
4-9-3 Advanced Implementation Example / 405
4-9-4 Swallow Counters/Dual-Modulus Counters / 407
4-9-5 Look-Ahead and Delay Compensation / 411
4-10 Loop Filters / 421
4-10-1 Passive RC Filters / 421
4-10-2 Active RC Filters / 422
4-10-3 Active Second-Order Low-Pass Filters / 423
4-10-4 Passive LC Filters / 426
4-10-5 Spur-Suppression Techniques / 427
4-11 Microwave Oscillator Design / 430
4-11-1 The Compressed Smith Chart / 432
4-11-2 Series or Parallel Resonance / 434

4-11-3 Two-Port Oscillator Design / 435
4-12 Microwave Resonators / 444
4-12-1 SAW Oscillators / 445
4-12-2 Dielectric Resonators / 445
4-12-3 YIG Oscillators / 448
4-12-4 Varactor Resonators / 452
4-12-5 Ceramic Resonators / 455
References / 461
Suggested Readings / 464

5 Digital PLL Synthesizers 471

5-1 Multiloop Synthesizers Using Different Techniques / 471
5-1-1 Direct Frequency Synthesis / 471
5-1-2 Multiple Loops / 473
5-2 System Analysis / 477
5-3 Low-Noise Microwave Synthesizers / 484
5-3-1 Building Blocks / 485
5-3-2 Output Loop Response / 489
5-3-3 Low Phase Noise References: Frequency Standards / 490
5-3-4 Critical Stage / 493
5-3-5 Time Domain Analysis / 503
5-3-6 Summary / 508
5-3-7 Two Commercial Synthesizer Examples / 512
5-4 Microprocessor Applications in Synthesizers / 518
5-5 Transceiver Applications / 523
5-6 About Bits, Symbols, and Waveforms / 526
5-6-1 Representation of a Modulated RF Carrier / 527
5-6-2 Generation of the Modulated Carrier / 529
5-6-3 Putting It all Together / 533
5-6-4 Combination of Techniques / 535
Acknowledgments / 537
References / 540
Bibliography and Suggested Reading / 540

6 A High-Performance Hybrid Synthesizer 543

6-1 Introduction / 543
6-2 Basic Synthesizer Approach / 544
6-3 Loop Filter Design / 548
6-4 Summary / 556
Bibliography / 557

A Mathematical Review 559

A-1 Functions of a Complex Variable / 559
A-2 Complex Planes / 561
A-2-1 Functions in the Complex Frequency Plane / 565
A-3 Bode Diagram / 568
A-4 Laplace Transform / 582
A-4-1 The Step Function / 583
A-4-2 The Ramp / 584
A-4-3 Linearity Theorem / 584
A-4-4 Differentiation and Integration / 585
A-4-5 Initial Value Theorem / 585
A-4-6 Final Value Theorem / 585
A-4-7 The Active Integrator / 585
A-4-8 Locking Behavior of the PLL / 587
A-5 Low-Noise Oscillator Design / 590
A-5-1 Example Implementation / 590
A-6 Oscillator Amplitude Stabilization / 594
A-7 Very Low Phase Noise VCO for 800 MHZ / 602
References / 605

B A General-Purpose Nonlinear Approach to the Computation of Sideband Phase Noise in Free-Running Microwave and RF Oscillators 607

B-1 Introduction / 607
B-2 Noise Generation in Oscillators / 608
B-3 Bias-Dependent Noise Model / 609
B-3-1 Bias-Dependent Model / 617
B-3-2 Derivation of the Model / 617
B-4 General Concept of Noisy Circuits / 619
B-4-1 Noise from Linear Elements / 620
B-5 Noise Figure of Mixer Circuits / 622
B-6 Oscillator Noise Analysis / 624
B-7 Limitations of the Frequency-Conversion Approach / 625
B-7-1 Assumptions / 626
B-7-2 Conversion and Modulation Noise / 626
B-7-3 Properties of Modulation Noise / 626
B-7-4 Noise Analysis of Autonomous Circuits / 627
B-7-5 Conversion Noise Analysis Results / 627
B-7-6 Modulation Noise Analysis Results / 627
B-8 Summary of the Phase Noise Spectrum of the Oscillator / 628
B-9 Verification Examples for the Calculation of Phase Noise in Oscillators Using Nonlinear Techniques / 628
B-9-1 Example 1: High-Q Case Microstrip DRO / 628
B-9-2 Example 2: 10 MHz Crystal Oscillator / 629
B-9-3 Example 3: The 1-GHz Ceramic Resonator VCO / 630

B-9-4 Example 4: Low Phase Noise FET Oscillator / 632
B-9-5 Example 5: Millimeter-Wave Applications / 636
B-9-6 Example 6: Discriminator Stabilized DRO / 639
B-10 Summary / 641
References / 643

C Example of Wireless Synthesizers Using Commercial ICs 645

D MMIC-Based Synthesizers 665

D-1 Introduction / 665
Bibliography / 668

E Articles on Design of Dielectric Resonator Oscillator 671

E-1 The Design of an Ultra-Low Phase Noise DRO / 671
E-1-1 Basic Considerations and Component Selection / 671
E-1-2 Component Selection / 672
E-1-3 DRO Topologies / 675
E-1-4 Small Signal Design Approach for the Parallel Feedback Type DRO / 677
E-1-5 Simulated Versus Measured Results / 683
E-1-6 Physical Embodiment / 685
E-1-7 Acknowledgments / 685
E-1-8 Final Remarks / 688
References / 692
Bibliography / 692
E-2 A Novel Oscillator Design with Metamaterial-MöBius Coupling to a Dielectric Resonator / 692
E-2-1 Abstract / 692
E-2-2 Introduction / 693
References / 699

F Opto-Electronically Stabilized RF Oscillators 701

F-1 Introduction / 701
F-1-1 Oscillator Basics / 701
F-1-2 Resonator Technologies / 701
F-1-3 Motivation for OEO / 704
F-1-4 Operation Principle of the OEO / 704
F-2 Experimental Evaluation and Thermal Stability of OEO / 705
F-2-1 Experimental Setup / 705
F-2-2 Phase Noise Measurements / 708
F-2-3 Thermal Sensitivity Analysis of Standard Fibers / 709
F-2-4 Temperature Sensitivity Measurements / 710
F-2-5 Temperature Sensitivity Improvement with HC-PCF / 712
F-2-6 Improve Thermal Stability Versus Phase Noise Degradation / 712

F-2-7 Passive Temperature Compensation / 713
F-2-8 Improving Effective Q with Raman Amplification / 714
F-3 Forced Oscillation Techniques of OEO / 718
F-3-1 Analysis of Standard Injection-Locked (IL) Oscillators / 718
F-3-2 Analysis of Self-Injection Locked (SIL) Oscillators / 720
F-3-3 Experimental Verification of Self-Injection Locked (SIL) Oscillators / 721
F-3-4 Analysis of Standard Phase Locked Loop (PLL) Oscillators / 723
F-3-5 Analysis of Self Phase Locked Loop (SPLL) Oscillators / 725
F-3-6 Experimental Verification of Self-Phase Locked Loop (SPLL) Oscillators / 726
F-3-7 Analysis of Self-Injection Locked Phase Locked Loop (SILPLL) Oscillators / 728
F-4 SILPLL Based X- and K-Band Frequency Synthesizers / 731
F-4-1 X-Band Frequency Synthesizer / 732
F-4-2 19″ Rack-Mountable K-Band Frequency Synthesizer / 737
F-5 Integrated OEO Realization Using Si-Photonics / 742
F-6 Compact OEO Using InP Multi-Mode Semiconductor Laser / 744
F-6-1 Structure of Multi-mode InP Laser / 744
F-6-2 Multi-mode Laser and Inter-Modal RF Oscillation / 745
F-6-3 Self-Forced Frequency Stabilizations / 747
F-7 Discussions / 752
Acknowledgments / 753
References / 754

G Phase Noise Analysis, then and Today 761

G-1 Introduction / 761
G-2 Large-Signal Noise Analysis / 762
References / 769

H A Novel Approach to Frequency and Phase Settling Time Measurements on PLL Circuits 771

H-1 Introduction / 771
H-2 Settling Time Measurement Overview / 771
H-2-1 Theoretical Background of Frequency Settling Time / 771
H-2-2 Frequency Settling Measurement in the Past / 772
H-3 R&S FSWP Phase Noise Analyzer / 774
H-3-1 Phase Noise Analyzer Architecture / 774
H-3-2 Typical Test Setup for Settling Time Measurements / 776
H-4 Frequency Hopping and Settling Time Measurements in Practice / 776
H-4-1 Trigger on Wideband Frequency Hopping Signals / 776
H-4-2 Frequency and Phase Settling Time Measurement / 777
H-5 Conclusion / 780

Index 783

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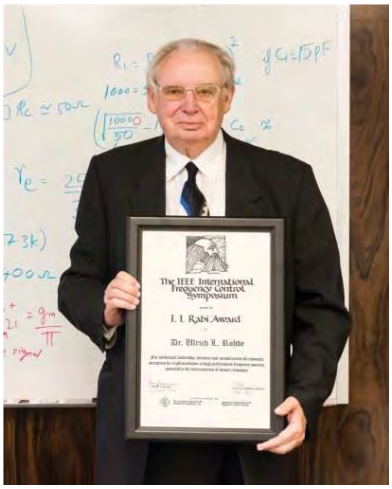

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"I like solving problems in my field of expertise where others have failed. Most people lack the drive or staying power to see things through."

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- Recipient of the 2017 RCA (Radio Club of America) Lifetime achievement award for "For significant achievements and a major body of work accomplished over a lifetime that has advanced the art and science of radio and wireless technology."
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In 2006, Dr. Rohde was honored as Microwave Legend by *Microwave & RF* Magazine; the selection was based on global voting. In 2009, Dr. Rohde was selected in the list of Divine Innovators of November 2011, *Microwave Journal*. Based on Dr. Rohde's five-decade of scientific creativity and pioneer contributions in the field of microwave and antenna, IEEE has established three awards on his name:

- IEEE Ulrich L. Rohde Innovative Conference Paper Award on Antenna Measurements and Applications
- IEEE Ulrich L. Rohde Innovative Conference Paper Award on Computational Techniques in Electromagnetics
- IEEE Ulrich L. Rohde Humanitarian Technical Field Award.

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His hobbies include building high-end vacuum tube audio amplifiers, restoring vintage radio broadcast hardware, and attending his children's numerous school sporting events. Mr. Whitaker lives with his wife and daughters (and two dogs) in Morgan Hill, CA.

PREFACE

Since 1997 when the first edition of *Microwave and Wireless Synthesizers* was published, enormous progress has been made both in semiconductors (discrete devices and integrated circuits) and in fundamental technologies. Specifically, much better implementations of direct digital synthesis (DDS) architectures have helped to improve performance in a number of key areas, notably reduced spurious elements and noise. Another critical part of a synthesizer is the voltage-controlled oscillator (VCO). New insights into its functionality have made the out-of-loop bandwidth much better. This also applies in the understanding of crystal and other high-Q based oscillators. These portions of the first edition have been greatly enhanced and updated in this Second Edition.

The radio frequency (RF)/microwave synthesizer text has also been expanded considerably, and the very important element of signal generation has been added, for example, arbitrary waveform generation and vector signal generation with very fast switching and high frequency resolution, and low noise/low spurious response.

TECHNOLOGY ADVANCEMENTS

In order to properly set the stage for the Second Edition, some introductory comments are warranted on the topic of signal generation. Today, the trend is toward full digital generation of modulated RF signals, that is, the traditional analog VCO and phase-locked loop (PLL) are no longer always necessary. Currently, the required functionality and the subsequent digital-to-analog converter (DAC) are incorporated into large-scale application-specific integrated circuits (ASICs). The following two links are to datasheets of such devices[1]: http://www.analog.com/media/en/technical-documentation/data-sheets/AD9164.pdf and http://www.ti.com/lit/ds/symlink/dac38j84.pdf.

From Analog Devices, the authors would like to thank John Morrissey and Ian Collins for their technical contribution and permission to use the Analog Devices material.

Modern waveform synthesis is based on the approach that the DAC directly generates complex modulated signals, that is, subsequent analog modulation is no longer required. The field programmable gate array (FPGA) generates the I/Q modulation data as a digital data stream. High-speed serial interfaces are used to transmit the I/Q data from the FPGA to the DAC, for example, in accordance with the JESD204B standard. To improve data efficiency, only the baseband data is transmitted, not the sampled RF signal. To achieve the DAC's final sampling rate, which at $2.5 \times f_{rf}$ typically lies significantly above the sampling rate for baseband data, the baseband data is interpolated up to the DAC sampling rate (i.e., initially greatly oversampled). The carrier is generated by a numerically controlled oscillator (NCO). Today's state-of-the-art phase accumulators have resolutions of 48 bit (or higher). If the NCO's frequency resolution is insufficient, the remaining frequency difference can be pre-calculated in baseband to achieve the required final resolution. A digital multiplier mixes the up-sampled baseband data with the NCO carrier to yield the digital modulated RF signal. This digital RF data is then fed into the RF DAC and output as an analog signal.

The maximum frequency of the RF signal is limited by the Nyquist rate (DAC sampling rate). If the required RF frequency lies above this frequency, the signal can be up-converted with a scalar mixer.

Overall, this results in very compact solutions for digitally generating RF signals without impairments. Additional advantages are the option of very fast frequency hopping, including phase-locked frequency hopping, that is,

[1]The hyperlinks in this book were functional at the time of publication. Some hyperlinks change over time, and so it may be necessary to search on the document filename to resolve a modified link.

phase-accurate hopping back to the previous frequency. Because this method of signal generation is mathematically deterministic, clock synchronization allows very efficient multiple-in/multiple-out (MIMO) signal generation.

Digital synthesis has the disadvantage of inherent spurs (DAC nonlinearities, finite resolution, and power source timing in the DAC). Depending on the RF frequency, these spurs show up between 40 and 80 dBc and need to be eliminated through appropriate frequency planning and filtering.

A very good clock source is necessary to achieve good phase noise in high-performance DACs. From a system theory perspective, a DAC functions as a frequency divider, delivering very good phase noise values close to the carrier. Unlike traditional synthesizers, there is no "noise shoulder" in the region of the PLL bandwidth. Another advantage of an RF DAC compared with a traditional PLL is that the clock is generated with a narrowband, high-quality oscillator instead of a tunable broadband VCO.

A MAJOR REVISION

Preparation of the Second Edition of *Microwave and Wireless Synthesizers* has included a comprehensive review of all of the original text and the addition of new updated text and illustrations. The new edition has been a collective effort among the authors. Jerry C. Whitaker took charge of the organization of the book, streamlining it for easy reading and attending to the details of publication, and Enrico Rubiola added his insightful knowledge of noise and noise contribution in circuits and system to the new edition. Another useful item we introduced is a clear mathematical method to treat the oscillators design for best noise performance, both at RF and microwave frequencies. This is of great value since most companies still prefer to design their oscillators or have them custom-optimized.

In addition, Prof. Afshin Daryoush agreed to write a theoretical introduction about opto-electric synthesizer based on fiber optic cable. Also, some of our joint publications on this topic are included.

Rohde & Schwarz Munich provided some of the important material including photographs. They came from the Business Unit, Measurement and Test Equipment, specifically from Mr. Pauly and Mr. Pointner. Also, our colleagues at Synergy Microwave Corp., NJ, USA, helped with important contributions, specifically Dr. Ajay Poddar.

This book is based on theoretical and practical work done over many years, courses given at George Washington University 1983, very recent developments done at Synergy Microwave Corp., and mathematical treatments found in the Ansys HFSS circuit analysis program (which was supported by a variety of government contracts). We have used mostly software from Ansys Corp. and Keysight. There are other suppliers of similar high-performance software; however, we tend to have less access to those.

For individuals who are getting acquainted with oscillators and synthesizers, we strongly recommend purchasing the *ARRL Handbook for Radio Communications*, annually published by the American Radio Relay League, 225 Main Street, Newington, CT 06111. The chapter on oscillators and synthesizers is a complete and well written first-time introduction to this topic.

Microwave and Wireless Synthesizers, Second Edition, is divided into six chapters beginning with Chapter 1 on loop fundamentals, which provides detailed insight into settling time and other characteristics of the loop. The clear differentiation between analog and digital loops has proven to be quite useful, and topics such as pull-in performance and acquisition are discussed in detail. This mathematically based presentation remains very much up to date.

Chapter 2 outlines noise and spurious responses of the loops. The linear approach of oscillator phase noise is very detailed and walks the reader through all the important steps and contributions, both inside and outside the loop. We also look at the noise contribution of the various parts of the loop, such as frequency dividers, phase detectors, and even power supplies. Finally, the noise analysis of the entire system and its measurements are covered. We added clarification and guidance to many parts. Here, modern IC design has helped to substantially improve the PLL.

In Chapter 3 we look at special loops. Here, the DDS technique—explained in detail—should prove most interesting to the reader. The fractional division *N* synthesizer technology (FN) competes with DDS. Details regarding a mixed approach are also shown in the appendices. Most of these FN loops can be found in cell phones and battery-operated two-way radios.

The fractional division *N* synthesis principle is quite complex. This is best seen from the various patent applications. Most RF and microwave companies now use this technique. The digital implementation of the accumulator and its compensating network has the greatest influence on performance. This area is very exciting, but only major

houses will be able to afford the large-scale custom integrated circuits (LSIs) and gate arrays that will solve these problems. The appearance of high performance fractional-*N* synthesizer chips for low-power applications further illustrates this trend when cost and power consumption are an issue. However, when highest performance is more critical than cost and power consumption (e.g., test equipment applications), modern DDS system implementations clearly win. If the readers are interested in CMOS PLL Synthesizers, there is an interesting book by Keliu Shu and Edgar Sánchez-Sinencio, published by Springer, ISBN 0-387-23668-6. © 2005. Also we found a PhD dissertation on the topic, "Low Phase Noise CMOS PLL Frequency Synthesizer—Design and Analysis," by Xinhua He, which can be found at: https://drum.lib.umd.edu/bitstream/handle/1903/7337/umi-umd-4746.pdf?sequence=1&isAllowed=y.

This book does not address foundry designs specifically, but the two examples earlier (the book and the dissertation) require a foundry and provide many useful information about the topic. We are sure there are more and newer publications about Synthesizer CMOS IC-design. The book mentioned previously provides an interesting discussion on Sigma-Delta modulators.

Chapter 4 provides a detailed overview of loop components. Many practical circuit details are found in this chapter as it addresses low-noise oscillator design, including the use of linear CAD tools. The section on reference frequency standards provides thorough insight into the design of crystal oscillators, which are a vital part of synthesizers and which must provide both low aging and optimum phase noise. Other important components include mixers, phase/frequency discriminators, wideband high-gain amplifiers, programmable dividers, and loop filters. The microwave oscillator design section in Chapter 4 is unique because it is the first systematic evaluation of all aspects of microwave design techniques—including different resonators, such surface acoustic wave (SAW) oscillators, dielectric resonators, and ceramic resonators—and addresses the use of tuning diodes. We apply nonlinear time domain analysis to calculate the oscillators, and we employ CAD tools to verify the oscillator noise performance.

Chapter 5 provides in-depth details about multiloop synthesizers. The section on microwave synthesizers deals with analysis, architectures, and trade-offs. Another unique section is the survey of critical stages and the examination of their behavior. Microprocessors are used to optimize parts of the synthesizer architecture. Various techniques are found in synthesizer for military communication equipment.

Chapter 6 is dedicated to practical synthesizer examples, which combine the techniques outlined in previous chapters. The design of a high-performance hybrid synthesizer and the related performance measurement techniques enable the engineer to follow the various design steps and design rules. The core of this chapter teaches the reader to understand the essentials for success in the first go-round of a design.

The appendices comprise eight sections.

- Appendix A provides a mathematical overview for individuals who want to write their own CAD programs. Also, verified designs are provided for very low phase noise very high frequency (VHF) and ultra high frequency (UHF) oscillators. Analog Devices and others provide a set of free CAD tools, such as a SPICE version, to analyze many types of systems, for example: http://www.analog.com/LTSpice.
- Appendix B is a mathematical treatment of the nonlinear time domain approach to calculating phase noise in a free-running oscillator. This may be the first complete treatment of its kind in a book and is based on recent publications by the renowned expert team of Synergy Microwave Corporation.
- Appendix C is a reprint of selected application notes provided by Analog Devices. This is useful to get a feel for the state-of-the-art synthesizer chips available and how to use them.
- Appendix D discusses monolithic microwave integrated circuit (MMIC)-based synthesizers.
- Appendix E is about advanced dielectric resonator oscillator (DRO) design.
- Appendix F describes opto-electronic oscillator/synthesizer.
- Appendix G discusses noise analysis, then and today.
- Appendix H describes a novel approach to frequency and phase settling time measurements on PLL circuits.

The following link documents some interesting frequency synthesizer approaches: https://www.nature.com/articles/ncomms3097.

CONTRIBUTIONS AND RESOURCES

Many renowned experts have contributed to the Second Edition of *Microwave and Wireless Synthesizers*. It is a concise collection of practical and theoretical information, and we are very grateful to have received input from many engineers interested in specific applications.

A note of caution: Currently, it appears that the cleanest and best single or dual-loop synthesizers can be built by using custom made fractional-division *N* ASIC chips. While many companies are competing for the PLL chip market, at the time of publication of this book, it appears that the performance of the Analog Devices family member PLL chips is leading the market. As technology changes, a different company may be leading tomorrow. We strongly advise a thorough evaluation of all available chips (including how long those chips will be in stock) before committing to a final design. Many come and go, and the lifetimes of these devices vary widely.

Since a designer needs to test a whole range of parameters for VCO/PLLs—including VCO tuning characteristics, RF power flatness, PLL transients (both spurious and harmonic), and of course phase noise as well as added phase noise and burst phase noise—having the necessary signal analysis tools is essential. The recently introduced FSWP signal analyzer from R&S® can handle all the needed measurements and more at a frequency range of 1 MHz to 26.5 GHz and higher (e.g., 50 GHz). The FSWP, for example, can measure the phase noise of a 1.8 GHz VCO/PLL in less than a few seconds covering 100+ frequency offset points.

The R&S FSWP phase noise analyzer and VCO tester combines extremely low-noise internal sources and cross-correlation technology, delivering high sensitivity for phase noise measurements. As a result, it takes just seconds to measure even highly stable sources such as those found in radar applications. Additional options such as pulsed signal measurements, additive phase noise (including pulsed) characterization, and integrated high-end signal and spectrum analysis make the analyzer a unique test instrument.

Some additional interesting facts about Synthesizers can be found in U. L. Rohde, Matthias Rudolph, "RF/Microwave Circuit Design for Wireless Applications," 2nd Ed., John Wiley & Sons. pp. 745–746, ISBN 1118431405, New York, 2013.

The completion of this new edition was an enjoyable project. We are very grateful to the various individuals who supported us throughout the work, specifically Prof. Afshin Daryoush, Dr. Ajay Poddar, Anisha Apte from Synergy Microwave, and, of course, thanks to our publisher, John Wiley & Sons, Inc., for their continued support of *Microwave and Wireless Synthesizers*, Second Edition.

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Jerry C. Whitaker, Morgan Hill, CA, USA

IMPORTANT NOTATIONS

Symbol	Meaning
$a_i (i = 1, 2, \ldots, n)$	Loop parameters of nth-order PLL
a_n, a_k	Digital data values
A	Amplifier gain
$A(s)$	Open-loop gain
$A(\omega)$	Amplitude of transfer function
	Amplitude response of network
B_i	Bandwidth of input bandpass filter (Hz)
B_L	Noise bandwidth of PLL (Hz)
$B(s)$	Closed-loop gain of PLL
$E(s)$	Error function
F	Noise figure
f, f_i	Frequency (Hz)
f_c	Corner frequency of flicker noise
f_m	Fourier frequency (sideband, offset, modulation, baseband frequency)
f_o	Carrier frequency
$f(t)$	Instantaneous frequency
Δf	Peak frequency deviation (Hz)
$\Delta f(t)$	Instantaneous frequency fluctuation
Δf_{peak}	Peak deviation of sinusoidal frequency modulation
Δf_{res}	Residual FM
$F(s)$, $F(j\omega)$	Transfer function of loop filter
$G(s)$, $G(j\omega)$	Feedforward function (rad/s)
$G_n(s)$	Transfer characteristic of a divider
$H(s)$, $H(j\omega)$	Feedback transfer function
K	Loop gain (rad/s)
K_d'	Phase detector gain before lock (V/rad)
K_e	Phase detector gain factor (V/rad)
K_m	Multiplier gain
K_o	VCO gain factor (rad/s V)
K_s	Shaper constant
K_v	dc Gain of PLL or velocity error coefficient (rad/s)
k	An integer or an integer index on a sequence
K	1.4×10^{-23} Ws/K
$L(x)$	Laplace transform of x
$\mathcal{L}(f_m)$	Single-sideband phase noise to total signal power in a 1-Hz bandwidth
m	An integer
$m(t)$	Modulation waveshape
M	An integer denoting frequency multiplication or division
n	An integer
n	Loop order
$n(t)$	Noise voltage (V)

Symbol	Meaning
$\overline{n(t)}$	Time average of noise
N, N_i	An integer representing frequency division or multiplication
$P(j\omega)$	Fourier transform of pulse waveshape
P_s	Signal power (W)
P_{ssB}	Power of single sideband
P_{sav}	Available signal power
Q_{unl}	Quality factor of unloaded resonator
$s = \sigma + j\omega$	Laplace transform complex variable
SNR	Signal-to-noise ratio
SNR_L	Signal-to-noise ratio in loop bandwidth $2B_L$
S_o	One-sided spectral density of white noise (dB/Hz)
$S_{\Delta f}(f_m)$	Spectral density of frequency fluctuations
$S_y(f_m)$	Spectral density of fractional frequency fluctuations
$S_{\Delta\theta}(f_m)$	Spectral density of phase perturbation
$S_{\Delta\phi}(f_m)$	Spectral density of phase noise
t	Time (s)
t_{acq}	Acquisition time of a loop
t_{lock}	Lock-in time for phase lock
T	Symbol interval of digital data stream (s)
T_{AV}	Average time to first cycle slip (s)
T_o	Temperature (kelvin, K)
T_p	Pull-in time (s)
v_c, V_c	VCO control voltage (V)
v_d, V_d	Phase detector output voltage (V)
$v(t)$	Instantaneous voltage
V_o	Peak amplitude of VCO voltage (V)
V_s	Peak amplitude of signal voltage (V)
V_{sL}	Peak amplitude of sinusoidal signal at limiting port
$V_{n\,\text{rms}}$	Equivalent noise voltage (1-Hz bandwidth)
V_{sav}	Available signal voltage
W_e	Maximum energy stored in capacitor
W_i	Spectral density of white noise (W/Hz)
$y(t)$	Instantaneous fractional frequency offset from nominal frequency
θ	Phase angle (rad)
θ_i	Phase angle of input signal (rad)
$\theta_\varepsilon = \theta_i - \theta_o$	Phase error between input signal and VCO (rad)
θ_o	VCO phase (rad)
θ_p	Loop phase error caused by oscillator noise (rad)
θ_v	Steady-state phase error (static phase error, loop stress) due to offset of input frequency (rad)
$\Delta\theta$	Phase deviation (rad)
	Amplitude of phase step (rad)
	Peak deviation of phase modulation (rad)
$\Delta\theta(t)$	Instantaneous fluctuation of phase perturbation
ξ	Damping factor of second-order loop
ρ	Signal-to-noise ratio
ρ_{sav}	Input signal-to-noise ratio
σ_n	Standard deviation (rms value) of noise $n(t)$ (V)
$\sigma_y^2(\tau)$	Allan variance
τ	Time constant (s)
τ_1, τ_2, τ_L	Time constants in loop filter (s)
τ_p	Pull-in time constant
$\Delta\phi(t)$	Instantaneous phase fluctuation

Symbol	Meaning
$\Delta\phi_{\text{peak}}$	Peak deviation of sinusoidal phase modulation, also modulation index
ϕ	Loop phase error reduced modulo 2π (rad)
ϕ_{N_o}	Phase fluctuation internal to an oscillator
$\phi(\omega)$	Phase of transfer function of a network
ψ	Phase of a transfer function (rad)
$\omega = 2\pi f$	Angular frequency (rad/s)
$j\omega$	Fourier transform variable
ω_i	Radian frequency of input signal (rad/s)
ω_m	Modulating frequency (rad/s)
ω_n	Natural frequency of second-order loop (rad/s)
$\Delta\omega$	Amplitude of frequency step or of frequency offset (rad/s)
	Peak deviation of frequency modulation (rad/s)
$\Delta\dot{\omega}$	Rate of change of frequency (rad/s^2)
$\Delta\omega_H$	Hold-in limit of PLL (rad/s)
$\Delta\omega_L$	Lock-in limit of PLL (rad/s)
$\Delta\omega_P$	Pull-in limit of PLL (rad/s)
$\Omega(s)$	Laplace transform $L[\Delta\omega(t)]$

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1

LOOP FUNDAMENTALS

1-1 INTRODUCTION TO LINEAR LOOPS

The majority of frequency synthesizers utilize the phase-locked loop (PLL). Indeed, it was the realization of the PLL in an integrated circuit that led to the inexpensive frequency synthesizer. Because an understanding of PLLs is necessary for the design of frequency synthesizers, they are discussed in detail in this chapter. The emphasis here is on the PLL as used in a frequency synthesizer rather than for signal detection. For the latter problem, the PLL input is a relatively low-level signal embedded in noise, and the PLL serves to detect the noisy signal. For PLL applications in frequency synthesizers, the input signal-to-noise ratio is high, and the PLL serves to lock out the output frequency on a multiple of the input frequency.

Although the PLL is a nonlinear device, it can be modeled as a linear device over most of its operating range. This chapter first presents the linearized analysis of the PLL, including its stability characteristics. The design of compensating filters to improve PLL performance is then discussed.

A PLL includes a phase detector, low-pass filter, and voltage-controlled oscillator (VCO), as illustrated in Figure 1-1. The phase detector is a nonlinear device, and its characteristics determine loop performance. The various types of phase detectors are described in Chapter 3. The loop transient performance is discussed in Section 1-10. No generalized results are available for transient performance, but the discussion illustrates one analysis approach that can be used.

Several books have been published on this matter, and for those involved in research or have interest in a more theoretical approach of the PLL principle, the following classic books are recommended:

Best, Roland E., *Phase Locked Loops*: *Design, Simulation, and Applications*, 6th Edition, McGraw-Hill, New York, NY, 2007.

Crawford, James A., *Frequency Synthesizer Design Handbook*, Artech House, Boston-London, 1994.

Egan, William F., *Frequency Synthesis by Phase Lock*, Wiley, New York, NY, 2007. ISBN 978-0-470-17871-3.

Gardner, Floyd M., *Phaselock Techniques*, 3rd edition, Wiley, New York, NY, 2005. ISBN 978-0-471-43063-6.

Gorsky-Popiel, Jerzy, *Frequency Synthesis Techniques and Applications*, IEEE Press, New York, NY, 1975.

Kroupa, Venceslav F, *Phase Lock Loops and Frequency Synthesis*, Griffin, London, 2003, ISBN 978-0-470-86512-5.

Lindsey, William C, and Chie, Chak M., *Phase-Locked Loops and Their Applications*, IEEE Press, New York, NY, 1985.

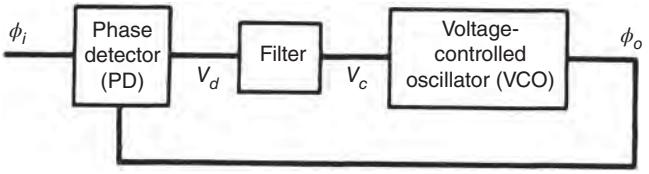


Figure 1-1 Block diagram of a PLL.

Manassewitsch, Vadim, *Frequency Synthesizers Theory and Design*, 3rd edition, Wiley, New York, NY, 2005, ISBN 978-0-471-77263-7.

Robert Bogdan Staszewski and Poras T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, September 2006, ISBN 978-0-471-77255-2.

The term *phase-locked* loop refers to a feedback loop in which the input and feedback parameters of interest are the relative phases of the waveforms. The function of a PLL is to track small differences in phase between the input and feedback signal. The phase detector measures the phase difference between its two inputs. The phase detector output is then filtered by the low-pass filter and applied to VCO. The VCO input voltage changes the VCO frequency in a direction that reduces the phase difference between the input signal and the local oscillator (LO). The loop is said to be in *phase lock or locked* when the phase difference is reduced to zero.

Although the PLL is nonlinear since the phase detector is nonlinear, it can accurately be modeled as a linear device when the loop is in lock. When the loop is locked, it is assumed that the phase detector output voltage is proportional to the difference in phase between its inputs; that is,

$$V_d = K_\theta(\theta_t - \theta_o) \tag{1-1}$$

where θ_t and θ_o are the phases of the input and VCO output signals, respectively.

K_θ is the phase detector gain factor and has the dimensions of volts per radian. It will also be assured that the VCO can be modeled as a linear device whose output frequency deviates from its free-running frequency by an increment of frequency,

$$\Delta\omega = K_o V_e \tag{1-2}$$

where V_e is the voltage at the output of the low-pass filter and K_o is the VCO gain factor, with the dimensions of rad/s per volt. Since frequency is the time derivative of phase, the VCO operation can be described as

$$\Delta\omega = \frac{d\theta_o}{dt} = K_o V_e \tag{1-3}$$

With these assumptions, the PLL can be represented by the linear model shown in Figure 1-2. $F(s)$ is the transfer function of the low-pass filter. The linear transfer function relating $\theta_o(s)$ and $\theta_t(s)$ is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\theta K_o F(s)/s}{1 + K_\theta K_o F(s)/s} \tag{1-4}$$

If no low-pass filter is used, the transfer function is

$$B(s) = \frac{\theta_o}{\theta_i} = \frac{K_\theta K_o}{s + K_\theta K_o} = \frac{K}{s + K} \tag{1-5}$$

which is equivalent to the transfer function of a simple low-pass filter with unity dc gain and bandwidth equal to K.

This is really the minimum configuration of a PLL. Since there is no divider in the chain, the output frequency and the reference frequency are the same. The first PLL built probably used a ring modulator as a phase detector.

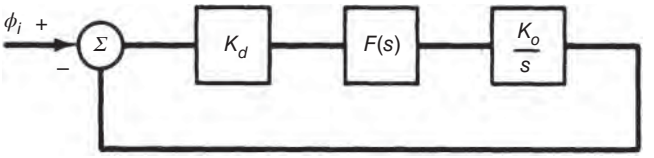


Figure 1-2 Block diagram of a PLL using a linearized model.

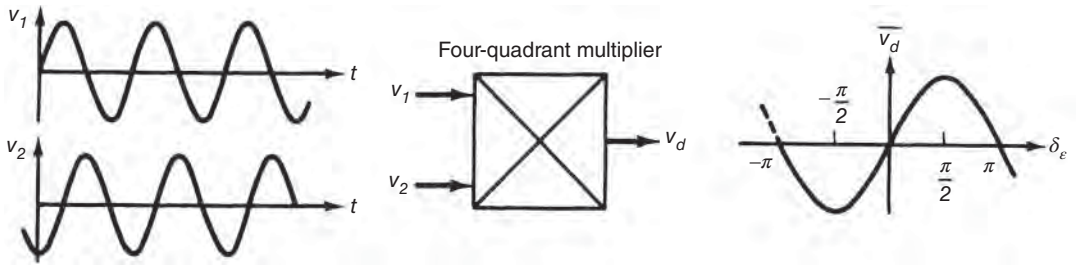


Figure 1-3 Waveform and transient characteristic of a linear phase detector.

The ring modulator or diode bridge is electrically the same as a four-quadrant multiplier and operates from $-\pi$ to $+\pi$ of phase range.

Since the VCO probably has a sine-wave output and the reference frequency also has a sine wave, it is referred to as a *sinusoidal phase detector*. This does not really mean that the phase detector is sinusoidal; it means that the waves applied to the phase detector are sinusoidal.

Since there are no digital components in this basic loop, it is correctly called an *analog phase-locked loop* and, as stated earlier, is the minimum form of a PLL. To model it correctly, a number of assumptions are required.

We have already stated that, for our initial consideration, the loop is locked and that the transfer characteristic of the phase/frequency detector is linear in the area of operation. A four-quadrant multiplier or diode quad has a sinusoidal output voltage, as shown in Figure 1-3, and is only piecewise linear for $\theta = 0$ or in the center of operation.

This minimum configuration of a PLL has several drawbacks. The absence of a filter does not allow one to choose parameters for optimized performance; the diode ring has only several hundred millivolts output, and an additional loop amplifier will add noise to the system. Therefore, for frequency synthesizer applications, a simple analog loop without any filter is rarely used. Such a loop would be called a first-order type 1 loop, and we will deal with it later.

There are some applications for a 1:1 loop, as we will see. The 1:1 loop is used to clean up an existing frequency, whereby the loop bandwidth is kept narrow enough to allow fast locking, and wide enough to permit fast acquisition. However, the loop bandwidth is narrower than the spurious frequencies present at the reference input. The attenuation of the loop filter of such a loop, which should be a second-order loop, will clean up the output signal relative to the reference.

1-2 CHARACTERISTICS OF A LOOP

We have met the minimum-configuration analog PLL and already learned that there are several limitations to this loop. The first step in increasing the output voltage delivered from the diode quad and avoiding an operational amplifier is to use a different phase detector.

If the diode bridge arrangement is changed and the diodes are overdriven by the reference signal and the input signal from the VCO remains sufficiently small relative to the reference, the phase detector is still in a linear operation mode, and the output signal of the phase detector is no longer a sinusoidal curve but rather has a linear

sawtooth form. The range over which the phase detector operates is still from $-\pi$ to $+\pi$, and the circuit is called *quasi-digital*. Later, when dealing with ring modulators, we will learn that it is a major requirement that the reference or LO signal must have a specified range, with a minimum typically 0.5 V for hot carrier diodes, and the VCO voltage should be substantially smaller for linear operation.

As the amplitude of the VCO signal is increased, the diode bridge or double-balanced modulator is overdriven, and a large number of harmonics occur. In a 1:1 loop, this is not very dangerous because all harmonics are phase and frequency coherent and do not generate unwanted signals. If a double-balanced mixer is used in a conversion scheme inside a loop, as we will see later, it is of utmost importance to operate the double-balanced mixer in its linear range and use a double-balanced mixer that has sufficient isolation between all ports.

In the case of the double-balanced mixer, whether overdriven from the LO or not, we refer to it as an analog linear PLL. If the VCO signal also overdrives the double-balanced mixer, we call it quasi-digital.

The digital equivalent of a double-balanced mixer is the exclusive-OR gate. The exclusive-OR gate, when built in CMOS logic, can be operated at 12 V, and therefore the dc output voltage can now be from almost 0 to +12 V, obtained from the integrator. We now have found a way to increase our dc control voltage without the noise sacrifice of an additional operational amplifier.

Both the double-balanced mixer and the exclusive-OR gate are only phase sensitive. The exclusive-OR gate also operates from $-\pi$ to $+\pi$, and the VCO has to be pretuned to be within the capture range.

Both phase detectors can be used for harmonic locking.

When we analyze the various loop components in Chapter 4, we will find some drawbacks that limit the use of the exclusive-OR gate.

The edge-triggered JK master/slave flip-flop can be used as a phase/frequency comparator. It operates from -2π to $+2\pi$. The edge-triggered JK master/slave flip-flop has two outputs. One output supplies pulses to charge a capacitor, and the other can be used to discharge a capacitor.

To use this phase/frequency detector requires an active loop filter or active integrator, commonly referred to as a *charge pump*. This type of phase detector generates a beat frequency at the output, and the average dc voltage generated in the integrator is either negative or positive, relative to half the power supply voltage, depending on whether the signal frequency is higher or lower than the reference. This is a useful feature and explains why we can state that this circuit is not only phase sensitive but also frequency sensitive. Unfortunately, the frequency sensitivity for this type of phase/frequency discriminator is useful only for large differences. For very small differences in frequency, there is very little advantage in choosing this circuit over the exclusive-OR gate or the double-balanced mixer. We will learn more about this circuit in Chapter 4.

The most important circuit for phase/frequency comparators is probably an arrangement of two flip-flops and several gates. This particular circuit will be called a *tri-state phase/frequency comparator*, for reasons we will see later. It has several advantages:

(1) The operating range is linear, from -2π to $+2\pi$.

(2) It has the best possible locking performance and best frequency and phase difference detection.

(3) Regardless of the amount of frequency error, the average output voltage is always above or below half the operating voltage. This results in good locking.

The last two types of phase/frequency detectors, because of their charge/discharge capability, require active filters or summation circuits. It is theoretically possible to avoid the amplifier and use purely resistive circuits, but as we will soon learn, this has disadvantages. So far, we still have only used a loop that has no frequency divider.

The introduction of a frequency divider requires that the input to the divider be a square wave (transistor–transistor logic (TTL)), and we will now define all loops that use digital dividers and phase/frequency comparators as digital loops. This should not be confused with digital synthesizers. A digital frequency synthesizer is most likely a direct synthesizer in which the output frequency is digitally generated with the help of a processor and is not available anywhere in analog or sine wave form. The output frequency is then the summation of several digital signals in a quasi-sine wave at the output generated only by means of digital circuitry. There are several methods besides the one currently used, which employs a lookup table for sine or cosine functions. For very low-frequency application, a complicated arrangement of diodes can be used to generate sine waves out of triangular waveshapes. Table 1-1 shows a comparison of the various phase/frequency detectors.

Table 1-1 Comparison of Various Phase/frequency Comparators

Type	Operating range	Sensitivity
Diode ring	$-\pi$ to π	Phase only
Exclusive-OR gate	$-\pi$ to π	Phase only
Edge-triggered JK flip-flop	-2π to 2π ($-\pi$ to π); See Table 1-2	Phase frequency; undefined for small errors
Tri-state phase/frequency	-2π to 2π	Phase frequency comparator

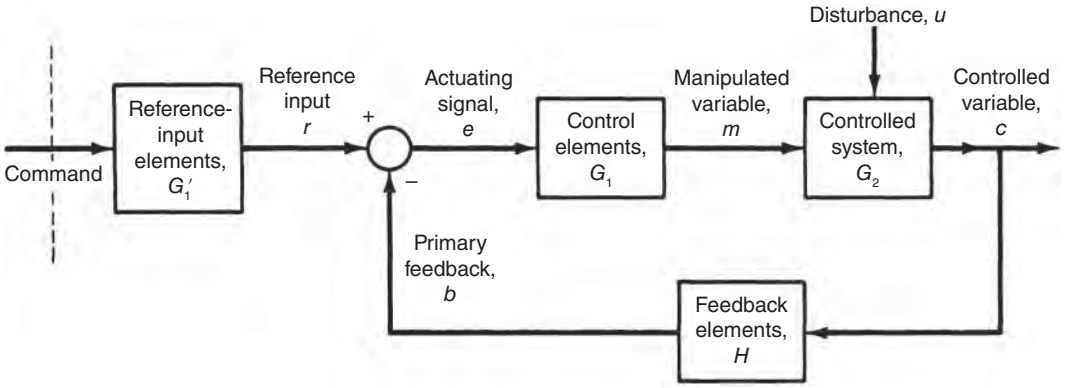


Figure 1-4 Equivalent diagram of a PLL using feedback control system analogy.

We have learned that because of its wider operating range, the PLL using digital phase/frequency comparators offers significant advantages over the analog PLL, and that is the main reason it is used in frequency synthesizers.

A closed loop is really a feedback system, and the various rules for feedback systems apply. We have already written down without further justification the formula that applies for a closed loop:

$$B(s) = \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \tag{1-6}$$

Before we continue, let us take a look at some of the abbreviations and definitions that are used in feedback control systems. Figure 1-4 shows the equivalent block diagram of a feedback system. The gain is equal to the multiplication of the VCO gain K_o times the phase/frequency comparator K_θ and will be abbreviated by K:

$$K = K_o K_\theta \frac{\text{rad/s}}{\text{V}} \frac{\text{V}}{\text{rad}} \tag{1-7}$$

The feedforward function

$$G(s) = \frac{K}{s} F(s) \tag{1-8}$$

takes a filter function $F(s)$ into consideration, and the fact that the VCO itself is a perfect integrator is also taken into consideration.

To close the loop, we have to describe the feedback transfer function

$$H(s) = \frac{1}{N} \tag{1-9}$$

which will describe the divider ratio N and assumes that there is no delay in the divider. If there is delay in the divider, $H(s)$ is expressed in the form

$$H(s)^* = \frac{e^{-T_n s}}{N} \tag{1-10}$$

Therefore, the open-loop gain of the system is written

$$A(s) = G(s)H(s) \tag{1-11}$$

This definition of open-loop gain must not be confused with the open-loop gain K or the feedforward gain. From our definition earlier, the closed-loop gain is

$$\begin{aligned} B(s) &= \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \\ &= \frac{\theta_o(s)}{\theta_i(s)} \\ &= \frac{G(s)}{1 + G(s)H(s)} \\ &= \frac{K(s)F(s)}{s + K(s)F(s)/N} \end{aligned} \tag{1-12}$$

It has become customary to incorporate the divider ratio N in the K, which means that K in most cases can be said to equal

$$\frac{K_o K_\theta}{N}$$

If this substitution is made, the formulas are generally valid, provided that the correct factor of K is selected, and the formulas are generally usable regardless of the actual division ratio. In synthesizer design it is interesting to determine the system's noise bandwidth, B_n, which is defined as

$$B_n = \frac{1}{2\pi} \int_0^\infty B(j\omega)\, d\omega \tag{1-13}$$

The 3-dB bandwidth can be determined by solving the equation substituting

$$|B_n(j\omega)| = 0.707$$

the resulting j_θ would then be the 3-dB bandwidth, the complex variable j deleted. Another important piece of information in feedback control system performance is the *steady-state error*, that is, the error remaining after all transients have died out. The equation for the error function is

$$E(s) = \frac{\theta_e}{\theta_i} = 1 - B(s) = \frac{1}{1 + G(s)H(s)} \tag{1-14}$$

We will compute the steady-state error as a function of the various systems in Section 1-10 and make some predictions on loops of various orders. As previously mentioned, we have classified the loops to be either analog or digital, referring to the phase/frequency detector, and in writing the initial equations, we have already indicated that the loop may or may not have a filter incorporated.

In analyzing the loop, we will find that to describe a loop, we can express it in terms of both the order of the loop and the type of loop. The expression "type of loop" refers to the number of integrators used. A PLL using no active integrator can really only be a type 1 loop. The term "order" refers to the order of the polynomial that is required to express the loop transfer characteristic.

The absolute minimum in a loop is a phase/frequency detector, a VCO, and no filter. By this definition, this would be a first-order type 1 loop. Another way of explaining this is by saying that the *type* of a system refers to the number of poles of the loop transfer function locked at the origin. The *order* of a system refers to the highest degree of the polynomial expression of the denominator that can be expanded into a polynomial expression. In this book we deal with loops of types 1 and 2 from first order up to fifth.

We have now learned that there are two classifications for loops:

(1) Classification by phase detector, characterizing the loop to be analog or digital.

(2) Characterizing the loop by the type of loop filter and number of integrators.

1-3 DIGITAL LOOPS

Using our previous definition, a digital PLL is a PLL system in which the phase/frequency comparator is built from digital components such as gates or flip-flops to form either an exclusive-OR gate, an edge-triggered JK master/slave flip-flop, or what we call a tri-state phase/frequency comparator. In addition, digital PLLs use frequency dividers, and although some circuits using the principle of subharmonic locking for dividers are known, this generally refers to the use of asynchronous or synchronous dividers. Asynchronous dividers are usually ripple counters, and synchronous dividers are counters that are being clocked by a common reset line.

The basic difference between an analog and a digital phase/frequency loop is in the possible delay introduced by the frequency divider and the nonlinear effects of the phase/frequency comparator, and the question of ultimate resolution of the phase/frequency comparator. The phase/frequency comparator using active filters shows some highly nonlinear performance during zero crossings at the output or under perfectly locked conditions. As there is no output from a tri-state phase/frequency comparator under locked conditions, the gain of the loop is zero until there is a requirement to send correcting pulses from the digital phase/frequency comparator, which then results in a jump of loop gain.

We will demonstrate that digital phase/frequency comparators, especially tri-state phase/frequency comparators, have two ranges for acquisition. One is called *pull-in* range, and the other is called *lock-in* range. The acquisition time is the time for both. This total time to acquire both frequency and phase lock is sometimes called the *capture time* or *digital acquisition time*. Depending on the loop filter and the phase/frequency comparator, we will have different time constants.

For reasons of convenience and linearity, we have, so far, assumed that the loop is in the locked condition. Initially, when the loop is switched on for the first time, it is far from being locked, and the VCO frequency can be anywhere within tuning range. *Tuning range* is defined as the frequency range over which the VCO can be tuned with the available control voltage.

There are, however, limitations because of the tuning diodes. The minimum voltage that can be applied is determined by the threshold voltage of the diode itself before it becomes conductive. This voltage is typically 0.7 V, and the maximum voltage is the potential determined by the breakdown voltage of the tuning diode. Even in the case where the familiar back-to-back diode arrangement is used, these are the two limits for the voltage range. In practice, however, this range is even narrower because the voltage sensitivity of the tuning diode is excessive at the very low end and very small at the extreme high end. Even before the breakdown voltage is reached, the noise contribution from the diode already increases because of some zener effects.

As the loop currently is not in locked condition, we have to help it to acquire lock. Very few loops acquire locking by themselves, a process called *self-acquisition*. Generally, the tuning range is larger than the acquisition range. Self-acquisition is a slow, unreliable process. If the loop is closed for the first time, the process called "pull-in" will occur. The oscillator frequency, together with the reference frequency, will generate a beat note and a dc control voltage of such phases that the VCO is pulled in a direction of frequency lock. As the oscillator itself generates noise in the form of a residual frequency modulation (FM), the oscillator is constantly trying to break out of lock, and the loop is constantly monitoring the state and reassuring lock. This results, under normal circumstances, in constant charging and discharging of the holding capacitor responsible for the averaging process.

There is one other phase/frequency comparator that is really more a switch than anything else; it is called a *sample/hold comparator*. The sample/hold comparator, which we will deal with later, has the advantage of very

good reference frequency suppression, introduces a phase shift that reduces the phase margin, and is really useful only up to several hundred kilohertz of frequency. For frequencies higher than this, there is too much leakage. The sample/hold comparator, which has been popular for a number of years, is described in Chapter 4. Modern frequency synthesizers, however, prefer digital phase/frequency comparators because the sample/hold comparator is only a phase comparator and does not recognize frequency offsets. It is too slow to be used for harmonic sampling and, in our opinion, has only limited use.

The sample/hold comparator is used mostly with T networks for additional reference suppression, and although these circuits provide good reference suppression, the phase margin has to be so high that the loops are generally slow in their response.

The switching speed of the loop and its general performance to noise are covered in detail in Section 1-10.

Now let us take a look at a numerical example. Consider a frequency synthesizer using a PLL to synthesize a 1-MHz signal from a 25-kHz reference frequency. To realize an output frequency of 1 MHz, a division of 1 MHz/25 kHz = 40 is necessary.

Let us assume that there is no filtering included, and therefore the closed-loop transfer function will be

$$B(s) = \frac{K}{s + K/N} \tag{1-15}$$

A typical value for K_θ is 2 V/rad and a typical value for the VCO gain factor K_o is 1000 Hz/V. With these values the closed-loop transfer function is

$$B(s) = \frac{K_\theta K_o}{s + K_\theta K_o/N} = \frac{1000 \times 2\pi \times 2}{s + [(1000 \times 2\pi \times 2)/40]} = \frac{4000\pi}{s + 100\pi} \tag{1-16}$$

The 3-dB frequency of the system by definition is

$$\omega_{3\text{dB}} = \frac{K_\theta K_o}{N} \tag{1-17}$$

and therefore

$$\omega_n = 100\pi$$

If this is solved to determine f, we obtain $f = 50$ Hz.

As the reference frequency is 25 kHz, the reference suppression of the simple system can be determined from

$$A = 20\log_{10}\left(\frac{25{,}000}{50}\right) = 20\log_{10}(500)$$

$$= 54 \text{ dB}$$

The loop bandwidth of the system by itself is 50 Hz.

We have, with very little effort, calculated a first-order type 1 loop. We deal more with these loops in Chapter 2.

Table 1-2 shows the input waveforms and the output average voltage of:

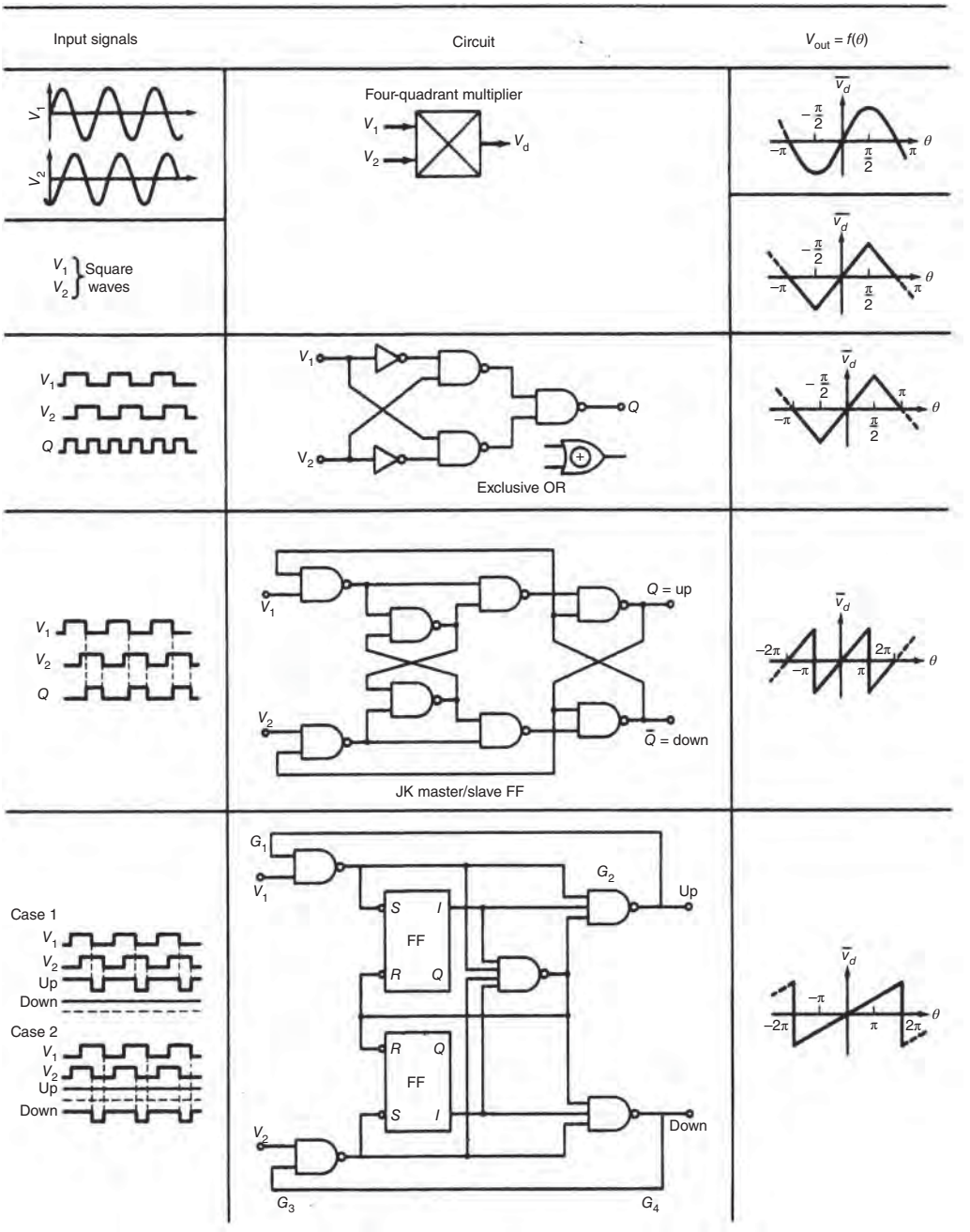
(1) A four-quadrant multiplier or double-balanced mixer being driven either by a sine wave or a square wave.

(2) The input and output voltages for an exclusive-OR gate.

(3) The input and output voltages after the integrator of an edge-triggered JK master/slave flip-flop.

(4) The input and output voltages of a tri-state phase/frequency comparator after the integrator. Notice that the extended operating range is linear from -2π to $+2\pi$.

Table 1-2 Circuit Diagrams and Input and Output Waveforms of Various Phase/frequency Comparators



Source: Courtesy of Fachschriftenverlag, Aargauer Tagblatt AG, Aarau, Switzerland.

1-4 TYPE 1 FIRST-ORDER LOOP

The type 1 first-order loop contains a digital phase/frequency comparator and a digital divider, and throughout the rest of this book, we will deal only with digital loops. This is done on the assumption that the phase/frequency comparator can be modeled as a linear device over the operating range, which is certainly not true. However, as most of the formulas and deviations that deal with PLLs have certain assumptions that have finite accuracy, it is permissible to do so. We realize that a purist will be offended by this statement. However, as many PLLs have been designed by rule of thumb and the final results were within a few percent accurate, we assume that the reader will permit this simplification.

The analog loop, as mentioned earlier, does not provide enough dc output, and for reasons of sideband noise, there is no advantage in using the linear loop in digital frequency synthesizers. Therefore, the PLL without a loop filter, $F(s) = 1$, is called a type 1 first-order loop because it has only one integrator, and the highest power (s) in the denominator of the system transfer function is 1.

The open-loop gain of a type 1 first-order PLL is equal to the forward gain divided by N, $(K_\theta K_o/s)/N$. The transfer function is

$$B(s) = \frac{N}{1 + s[1/(K_\theta K_o/N)]} \tag{1-18}$$

The loop noise bandwidth can be determined from the integration to be

$$B_n = \frac{K_\theta K_o}{4N} \tag{1-19}$$

It should be noted that the noise bandwidth changes as a function of the division ratio N. If there is a large change in the division ratio, the noise bandwidth will change substantially. This is another reason why the type 1 first-order loop is not very popular.

Let us assume that the loop is not in locked condition. The phase/frequency comparator receives two different frequencies at the two inputs. For digital phase/frequency comparators, we will use an exclusive-OR gate, which requires an active integrator.

Because of the limits of the operating range, presteering is required for the VCO to be within the range $-\pi$ to $+\pi$ for a locking condition. It is known that the maximum difference between the VCO free-running frequency and the desired final frequency at which phase lock is possible can be equal to

$$\Delta\omega_{\text{capture}} = \Delta\omega_H = \frac{K_\theta K_o}{N} \text{ rad/s} \tag{1-20}$$

It is important to keep the steady-state phase error small; therefore, high dc loop gain is required. As the increase in loop gain would require an amplifier, this makes the loop noisy and eventually unstable.

We have explained previously that the VCO gain is limited because of the tuning range of the diodes, and we will learn later that it is desirable to keep the VCO gain as low as possible. The input line to the VCO is a high-impedance, and pick-up on this line will result in spurious output at the VCO. To keep the spurious frequencies small, the VCO gain must be kept as small as possible.

The phase detector sensitivity depends mainly on the operating voltage. We recall that the double-balanced modulator with four diodes supplies only several hundred millivolts; instead, the exclusive-OR gate was chosen, as this can be operated from 12 V or even higher if CMOS logic is used.

There are several estimates regarding the acquisition time for the type 1 first-order PLL. Using the exclusive-OR gate, the acquisition time is approximately

$$T_A = \frac{2}{K_\theta K_o/N} \ln \frac{2}{\theta_\varepsilon} \tag{1-21}$$

where ln refers to the natural logarithm and θ_ε refers to the final phase error in radians.

From our previous example, the acquisition time T_A would be determined to be

$$\begin{aligned} T_A &= \frac{2}{50} \ln \frac{2}{0.2} \\ &= 9.2 \times 10^{-2} \text{ s} \end{aligned}$$

Assuming that the initial offset was less than 50 Hz, the loop locks in frequency without skipping cycles. In practice, it is impossible to presteer the loop within 50 Hz; therefore, this formula has only limited use.

We have just determined the acquisition time, but we have to ask ourselves: What does it really mean? Does it mean that the frequency from the initial offset is now the same as the reference frequency? Does it mean that we have reached a certain percentage of final frequency or gotten very close to the final frequency or final phase? Will we ever reach the final value, or is there a residual error?

The *error function*, which we met earlier, provides us with information and insight.

$$E(s) = \frac{\theta_\varepsilon}{\theta_i} = 1 - B(s) = \frac{1}{1 - G(s)H(s)} \tag{1-14}$$

It has been shown that, depending on the type of change of input, we get different results. These results are determined by the use of a transformation from the frequency into the time domain. Section A-4 presents the mathematical background for the Laplace transform and discusses how it is applied. Here, we use only the results. Inserting the known factors into Eq. (1-14), we obtain

$$E(s) = \frac{s\theta_\varepsilon(s)}{s + K} \tag{1-22}$$

with $K = K_\theta K_o/N$. It is customary to analyze the performance of the loop for three different conditions:

(1) To apply a step to the input and see what the output response is.
(2) A ramp voltage.
(3) A parabolic input.

Case 1, the step input, means an instantaneous jump with zero rise time to which the output will respond with a delay. The steady-state phase error resulting from this step change of input phase of magnitude $\Delta\theta$ for a ramp,

$$\theta(s) = \frac{\Delta\theta}{s} \tag{1-23}$$

is

$$\varepsilon = \lim_{s \to 0} \frac{\Delta\omega}{s + K} = \frac{\Delta\theta}{K} \tag{1-24}$$

Case 2, the steady-state error resulting from a ramp of input phase that is the same as a step change in reference frequency in the amount $\Delta\omega[\theta(s) \times \Delta\omega/s^2]$, is

$$\varepsilon = \lim_{s \to 0} \frac{\Delta\omega}{s + K} = \frac{\Delta\omega}{K} \tag{1-25}$$

It is apparent from these two equations that after a certain time, a type 1 first-order loop will track out any step change in input phase within the system hold-in range and will follow a step change in frequency with a phase error that is proportional to the magnitude of the frequency steps and inversely proportional to the dc loop gain. The loop will show the same performance if phase or frequency of the VCO changes rather than the reference.

In case 3, for the type 1 first-order PLL, it is of interest to examine a ramp change in frequency, the case in which the reference frequency is linearly changed with a time rate of $\Delta\omega/dt$ rad/s^2 and $\theta(s) = (2\Delta\omega/dt)/s^3$. Why

is this so important? Let us assume that we sweep a PLL at a constant rate, as is done in some modern spectrum analyzers, and we have to find the final condition for the steady-state phase error. The final phase error is

$$\varepsilon = \lim_{s\to 0} \frac{2\Delta\omega/dt}{s^2 + sK} = \infty \tag{1-26}$$

What does this mean for us? It means that, as there is no infinite value for K in a type 1 first-order loop, this loop is not very attractive for tracking, and it also means that above a certain and critical rate of change of reference frequency or VCO frequency, the loop will no longer stay in locked condition. Therefore, if the loop is swept above a certain rate, it will not maintain lock.

1-5 TYPE 1 SECOND-ORDER LOOP

A type 1 second-order loop is shown in Figure 1-5.

If we insert in our PLL a simple low-pass filter

$$F(s) = \frac{1}{\tau_s + 1} \tag{1-27}$$

the closed-loop transfer function using

$$K = \frac{K_o K_\theta}{N}$$

is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{NK}{s(\tau s + 1) + K} = \frac{N}{(s^2/\omega_n^2) + (2\zeta/\omega_n)s + 1} \tag{1-28}$$

where

$$\omega_n = \sqrt{\frac{K}{\tau}} \tag{1-29}$$

and

$$2\xi = \frac{\omega_n}{K} = \sqrt{\frac{1}{\tau K}} \tag{1-30}$$

The magnitude of the steady-state frequency response is

$$|B(s)| = \left|\frac{\theta_o}{\theta_i}(j\omega)\right| = \frac{1}{[(1 - \omega^2/\omega_n^2)^2 + (2\zeta\omega/\omega_n)^2]^{1/2}} \tag{1-31}$$

and the phase shift is

$$\arg \frac{\theta_o}{\theta_i}(j\omega) = \arctan \frac{2\zeta\omega}{\omega_n(1 - \omega^2/\omega_n^2)^2} \tag{1-32}$$

The frequency response of this second-order transfer function determined in Eq. (1-28) is plotted in Figure 1-6 for selected values of ζ. For $\zeta = 0.07$, the transfer function becomes the second-order "maximally flat" Butterworth response. For values of $\zeta < 0.07$, the gain exhibits peaking in the frequency domain. The maximum value of the frequency response M_P can be found by differentiating the magnitude of Eq. (1-28) (with $s = j\omega$). M_P is found to be

$$M_P = \frac{1}{2\zeta\sqrt{1 - \zeta^2}} \tag{1-33}$$

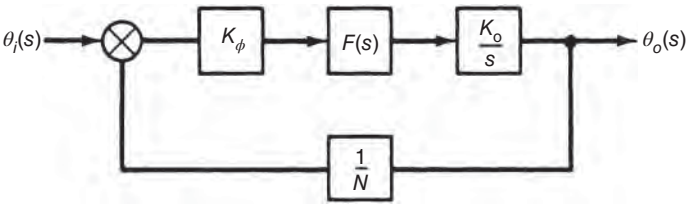


Figure 1-5 Block diagram of the second-order PLL.

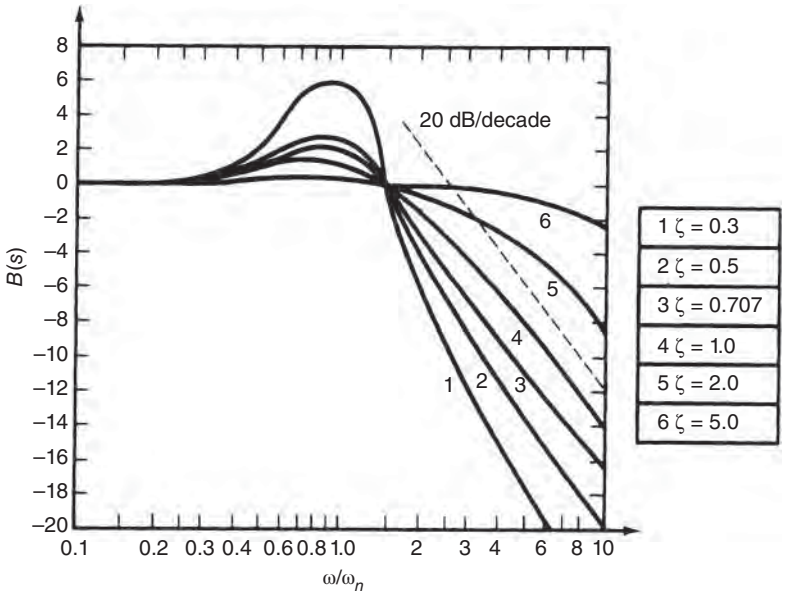


Figure 1-6 Frequency response of the type 1 second-order loop as a function of ζ.

and the frequency ω_p at which the maximum occurs is

$$\omega_p = \omega_n \sqrt{1 - 2\zeta^2} \tag{1-34}$$

The 3-dB bandwidth B can be derived by solving for the frequency ω_h at which the magnitude of Eq. (1-28) (with $s = j\omega$) is equal to 0.707. B is found to be

$$B = \omega_n (1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4})^{1/2} \tag{1-35}$$

The time it takes for the output to rise from 10% to 90% of its final value is called the *rise time* t_r. Rise time is approximately related to the system bandwidth by the relation

$$t_r = \frac{2.2}{B} \tag{1-36}$$

which is exact only for the first-order system described by Eq. (1-5).

The error signal θ_ε, defined as $\theta_i - \theta_o$, can be expressed (in unity feedback systems) as

$$\theta_\varepsilon(s) = \frac{\theta_i(s)}{1 + KG(s)} = \frac{\theta_i(s)}{1 + KF(s)/s} \tag{1-37}$$

If the system is stable, the steady-state error for polynomial inputs $\theta_i(t) = t^n$ can be obtained from the final value theorem,

$$\begin{aligned} \lim_{t\to\infty} \theta_\varepsilon(t) &= \lim_{s\to 0} s\theta_\varepsilon(s) \\ &= \lim_{s\to 0} \frac{2\theta_i}{KF(s)} \end{aligned} \tag{1-38}$$

If $\theta_i(t)$ is a step function representing a sudden increase in phase, $\theta_i(s) = 1/s$ and

$$\lim_{t\to\infty} \theta_\varepsilon(t) = \lim_{s\to 0} \frac{s}{KF(s)} \tag{1-39}$$

$F(s)$ is either a constant or a low-pass filter that may include poles at the origin. That is,

$$\lim_{s\to 0} F(s) = \frac{K^*}{s^n} \neq 0 \tag{1-40}$$

Therefore, Eq. (1-39) can be written

$$\lim_{t\to\infty} \theta_\varepsilon(t) = \lim_{s\to 0} \frac{s^{n+1}K^*}{KK^*} = 0 \tag{1-41}$$

That is, a PLL will track step changes in phase with zero steady-state error.

If there is a constant-amplitude change in the input frequency of A rad/s,

$$\theta_i(s) = \frac{A}{S^2} \tag{1-42}$$

Equation (1-39) becomes

$$\lim_{t\to\infty} \theta_\varepsilon(y) = \lim_{s\to 0} \frac{A}{KF(s)} = \frac{A}{KF(0)} \tag{1-43}$$

If $F(0) = 1$, the steady-state phase error will be inversely proportional to the loop gain K. Recall that the larger K is, the larger will be the closed-loop bandwidth and thus the faster the loop response. To increase the response speed and reduce the tracking error, the loop gain should be as large as possible. If $F(0)$ is finite, there will be a finite steady-state phase error. The frequency error,

$$f_\varepsilon(t) = \frac{d}{dt}\theta_\varepsilon(t) \tag{1-44}$$

will be zero in the steady state. That is, the input and VCO frequencies will be equal ($\omega_i = \omega_o$).

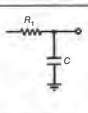
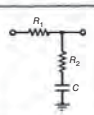
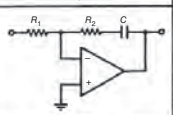
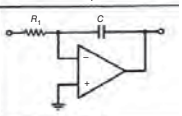
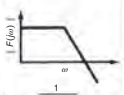
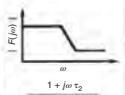
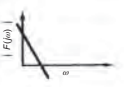
Table 1-3 shows the popular loop filters for the type 2 second-order loop. We have now dealt with case 1, a simple resistor-capacitor (RC) filter. The performance obtained with this loop filter is relatively restricted, mainly because the advantage over the loop with no filter was that we only got one additional parameter, a time constant τ_1.

Let us look at the table and the various filters. The passive filter type 2 uses two resistors and one capacitor, which allows compensation of phase.

The active filter, with which we will be dealing shortly, will add an additional integrator and therefore change this loop from a type 1 second-order to a type 2 second-order. The second-order loops we are currently dealing with are of type 1 because there is only one integrator involved, the VCO.

As we have only the time constant available as the additional parameter, which as we saw previously determines both the natural loop frequency ω_n and the damping factor ζ, we have not made much progress toward improving

Table 1-3 Circuit and Transfer Characteristics of Several PLL Filters

Type	Passive		Active	
	1	2	3	4
Circuit				
Transfer characteristic				
$F(j\omega) =$	$\frac{1}{1 + j\omega\tau_1}$	$\frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$	$\frac{1 + j\omega\tau_2}{j\omega\tau_1}$	$\frac{1}{j\omega\tau_1}$

$\tau_1 = R_1 C$ $\tau_2 = R_2 C$

the loop and choosing independent parameters. If we add a resistor in series with the capacitor and obtain the loop filter shown in Table 1-3, type 2, the transfer function $F(s)$ is

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \tag{1-45}$$

or as it is sometimes defined,

$$F(s) = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)} \tag{1-46}$$

What is the difference? In the first case, we use the abbreviations

$$\tau_1 = (R_1 + R_2)C \tag{1-47}$$

and

$$\tau_2 = R_2 C \tag{1-48}$$

whereas in the second case, and as listed in Table 1-3,

$$\tau_1 = R_1 C \tag{1-49}$$

and

$$\tau_2 = R_2 C \tag{1-50}$$

This fact should be pointed out, as it may cause confusion to the reader. This results in the transfer function of the type 1 second-order PLL using the first-case definition,

$$\begin{aligned} B(s) &= \frac{K(1 + \tau_2 s/1 + \tau_1 s)}{s + K(1 + \tau_2 s/1 + \tau_1 s)} \\ &= \frac{K(1/\tau_1)(1 + \tau_2 s)}{s^2 + (1/\tau_1)(1 + K\tau_2)s + (K/\tau_1)} \end{aligned} \tag{1-51}$$

To be consistent with our previous abbreviations, we now insert the terms of the loop damping factor ζ and the natural frequency ω_n and obtain

$$B(s) = \frac{s\omega_n(2\zeta - \omega_n/K) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1-52}$$

where

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \text{ rad/s} \tag{1-53}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau_1 K}(1 + \tau_2 K)} \tag{1-54}$$

We remember our abbreviation used previously, ω_n. The magnitude of the transfer function of the phase-lag filter magnitude is

$$|F(j\omega)| = \sqrt{\frac{1 + (\omega R_2 C)^2}{1 + [\omega C(R_1 + R_2)]^2}} \tag{1-55}$$

and the phase is

$$\theta(j\omega) = \arctan(\omega\tau_2) - \arctan(\omega\tau_1)$$

When we use the other definition of τ_1 and τ_2 insert the abbreviations

$$\omega_n = \sqrt{\frac{K}{\tau_1 + \tau_2}} \tag{1-56}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K}\right) \tag{1-57}$$

we obtain the expression

$$B(s) = \frac{s\omega_n(2\zeta - \omega_n/K) + \omega_n^2}{s^2 + 2\zeta(\omega_n^s + \omega_n^2)} \tag{1-58}$$

which turns out to give the same result.

As we were interested in the 3-dB bandwidth of the type 1 first-order loop, we now determine the 3-dB bandwidth of the type 1 second-order loop to be

$$B_{3\text{dB}} = \frac{\omega_n}{2\pi}(a + \sqrt{a^2 + 1})^{1/2}\ \text{Hz} \tag{1-59}$$

with the substitution

$$a = 2\zeta^2 + 1 - \frac{\omega_n}{K}\left(4\zeta - \frac{\omega_n}{K}\right) \tag{1-60}$$

The noise bandwidth of the type 1 second-order loop is

$$B_n = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)\ \text{Hz} \tag{1-61}$$

Again, we are interested in the final phase error and information we can gain from the phase error function

$$E(s) = \frac{s(1 + \tau_1 s)\theta(s)}{\tau_1 s^2 + (1 + K\tau_2)s + K} \tag{1-62}$$

As we are still dealing with a type 1 system, we obtain zero steady phase error, for a step in phase, and constant error for a ramp input in phase. One of these cases is shown in Figure 1-7, where the transient phase error due to a step in phase is plotted.

For the loop to stay in lock, the following critical values have to be considered. The maximum rate of change of reference frequency $d\Delta\omega/dt$ should satisfy the equation

$$\left(\frac{d\Delta\omega}{dt}\right)_{\max} = \omega_n^2 \tag{1-63}$$

The maximum rate at which the VCO can be swept must satisfy the condition

$$\left(\frac{d\Delta\omega}{dt}\right)_{\max} < \frac{\omega_n^2}{2} \tag{1-64}$$

to achieve lock. The hold-in range of this loop is

$$\Delta\omega_H = K\ \text{rad/s}$$

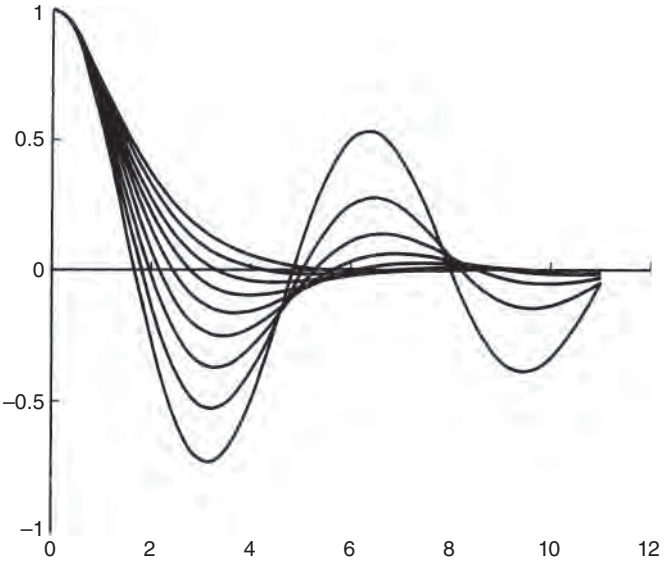


Figure 1-7 Transient phase step response for type 1 second-order loop.

and the capture range is

$$\Delta\omega_C = K\left(\frac{\tau_1}{\tau_2}\right) \text{ rad/s} \tag{1-65}$$

An approximate time required for this type 1 second-order loop to obtain frequency lock is

$$T_{\text{acq}} \simeq \frac{4(\Delta f)^2}{B_n^3} \text{ s} \tag{1-66}$$

A simple numerical example may give some additional insight. Let us assume that we have an oscillator operating at 45 MHz, using a reference frequency of 1 kHz. The tuning range of the oscillator is 5 MHz, which means that the frequency of the VCO in the beginning can be at either 40 or 50 MHz, as an extreme value. If we take the Δf offset worst-case condition of 5 MHz, and to get adequate reference suppression, we use a 50-Hz natural loop frequency and a damping factor ζ of 0.7, the noise bandwidth is

$$\begin{aligned} B_n &= \frac{50}{2}\left(0.7 + \frac{1}{0.7 \times 4}\right) \\ &= 25(0.7 + 0.3571) \\ &= 25 \times 1.0571 \\ &= 26.4 \text{ Hz} \end{aligned}$$

For a 5-MHz offset,

$$T_{\text{acq}} = \frac{4(5 \times 10^6)^2}{26.4^3} = 5.4 \times 10^9 \text{ s}$$

This is a ridiculous value. Unless the loop gets acquisition help, we would lose patience before it has ever acquired lock. Let us assume for a moment that we have a Δf of only 1 kHz or one step size. This still results in an acquisition time of 380 s, much too long for practical values. In Section 1-10 we will learn some acquisition

aids that can speed up the otherwise lengthy procedure. For now, it is sufficient to know that in cases where we do not use a phase/frequency comparator, it generates a beat note that is capable of switching and, therefore, aiding acquisition. Externally switched oscillators can be used, or automatic circuits can be incorporated that change the loop bandwidth before acquisition occurs and therefore can speed up the circuit substantially.

We end our discussion of the type 1 second-order loop here and concentrate on the more popular type 2 second-order loop. Why is the type 2 second-order loop so much more popular?

We found out previously that the freedom of choice of parameters was limited.

(1) In the type 1 first-order loop with no filter, K determined everything.

(2) In the type 1 second-order loop, we had one time constant (τ_1) available, which restricted us in the choice of ω_n and ζ, as these values were related. The type 1 second-order loop has finite dc gain and therefore it is questionable whether the term "PLL" is really justified. By this definition we really should not call it a true PLL system because, from the assumptions made previously, zero phase error requires infinite dc gain.

How do we accomplish the infinite dc gain, and how do we accomplish zero phase error?

If it is necessary to have zero phase error in response to step changes in the input frequency, $\lim_{s\to 0} F(s)$ must be infinite. That is, the dc gain of the low-pass filter must be infinite. This can be realized by including in $F(s)$ a pole at the origin. In this case $F(s)$ will be of the form

$$F(s) = \frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \tag{1-67}$$

The addition of the pole at the origin creates difficulties with the loop stability. In fact, the system will now be unstable unless a lead network is included in $F(s)$. With a passive filter, therefore resulting in a type 1 second-order loop, the condition is generally that we start with specified values for ω_n and ζ and we want to determine the time constants τ_1 and τ_2. This has rarely been shown in the literature, and for those interested, here is the result. We start off with $K_\theta K_o/N = K$ and

$$\omega_n = \sqrt{\frac{K}{\tau_1 + \tau_2}} \tag{1.56}$$

$$\zeta = \frac{1}{2}\left(K + \frac{1}{\tau_1 + \tau_2}\right)^{1/2}\left(\tau_2 + \frac{1}{K}\right) \tag{1-68}$$

By squaring ζ and inserting the value for ω_n, after some manipulation we obtain

$$\tau_2^2 K^2 + \tau_2 2K + 1 - 4\zeta^2\frac{K^2}{\omega_n^2} = 0 \tag{1-69}$$

This equation can be solved with

$$\tau_1 = \frac{K}{\omega_n^2} - \tau_2 \tag{1-70}$$

$$\tau_2 = \frac{-2K + \sqrt{4K^2 - 4K^2[1 - 4\zeta^2(K^2/\omega_n^2)]}}{2K^2} \tag{1-71}$$

and

$$R_1 = \frac{\tau_1}{C} \tag{1-72}$$

and

$$R_2 = \frac{\tau_2}{C} \tag{1-73}$$

1-6 TYPE 2 SECOND-ORDER LOOP

The type 2 second-order loop uses a loop filter in the form

$$F(s) = \frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \tag{1-67}$$

The multiplier $1/s$ indicates a second integrator, which is generated by the active amplifier. In Table 1-3, this is the type 3 filter. The type 4 filter is mentioned there as a possible configuration but is not recommended because, as stated previously, the addition of the pole of the origin creates difficulties with loop stability and, in most cases, requires a change from the type 4 to the type 3 filter. One can consider the type 4 filter as a special case of the type 3 filter, and therefore it does not have to be treated separately. Another possible transfer function is

$$F(s) = \frac{1}{R_1 C}\frac{1 + \tau_2 s}{s} \tag{1-74}$$

with

$$\tau_2 = R_2 C \tag{1-50}$$

Under these conditions, the magnitude of the transfer function is

$$|F(j\omega)| = \frac{1}{R_1 C\omega}\sqrt{1 + (\omega R_2 C)^2} \tag{1-75}$$

and the phase is

$$\theta = \arctan(\omega\tau_2) - 90^\circ$$

Again, as if for a practical case, we start off with the design values ω_n and ζ, and we have to determine τ_1 and τ_2. Taking an approach similar to that for the type 1 second-order loop, the results are

$$\tau_1 = \frac{K}{\omega_n} \tag{1-76}$$

and

$$\tau_2 = \frac{2\zeta}{\omega_n} \tag{1-77}$$

and

$$R_1 = \frac{\tau_1}{C} \tag{1.72}$$

and

$$R_2 = \frac{\tau_2}{C} \tag{1.73}$$

The closed-loop transfer function of a type 2 second-order PLL with a perfect integrator is

$$B(s) = \frac{K(R_2/R_1)[s + (1/\tau_2)]}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{1-78}$$

By introducing the terms ζ and ω_n, the transfer function now becomes

$$B(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1-79}$$

with the abbreviations

$$\omega_n = \left(\frac{K}{\tau_2}\frac{R_2}{R_1}\right)^{1/2} \text{ rad/s} \tag{1-80}$$

and

$$\zeta = \frac{1}{2}\left(K\tau_2\frac{R_2}{R_1}\right)^{1/2} \tag{1-81}$$

and $K = K_\theta K_o/N$.

The 3-dB bandwidth of the type 2 second-order loop is

$$B_{3\text{dB}} = \frac{\omega_n}{2\pi}[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}]^{1/2} \text{ Hz} \tag{1-82}$$

and the noise bandwidth is

$$B_n = \frac{K(R_2/R_1) + 1/\tau_2}{4} \tag{1-83}$$

Again, we ask the question of the final error and use the previous error function,

$$E(s) = \frac{s\theta(s)}{s + K(R_2/R_1)\{[s + (1/\tau_2)]/s\}} \tag{1-84}$$

or

$$E(s) = \frac{s^2\theta(s)}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{1-85}$$

As a result of the perfect integrator, the steady-state error resulting from a step change in input phase or change of magnitude of frequency is zero.

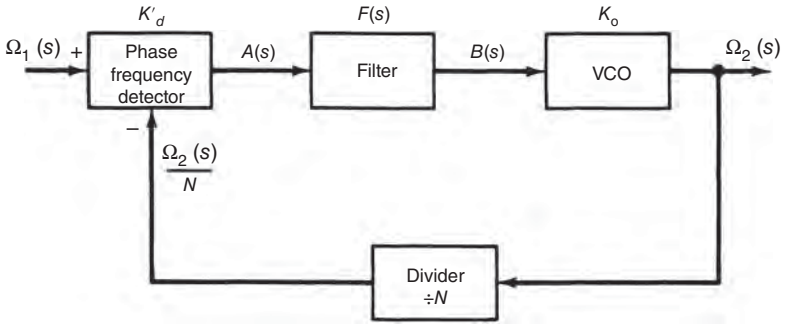
If the input frequency is swept with a constant range change of input frequency ($\Delta\omega/dt$) for $\theta(s) = (2\Delta\omega/dt)/s^3$, the steady-state phase error is

$$E(s) = \frac{R_1}{R_2}\frac{\tau_2(2\Delta\omega/dt)}{K} \text{ rad} \tag{1-86}$$

The maximum rate at which the VCO frequency can be swept for maintaining lock is

$$\frac{2\Delta\omega}{dt} = \frac{N}{2\tau_2}\left(4B_n - \frac{1}{\tau_2}\right) \text{ rad/s} \tag{1-87}$$

The introduction of N indicates that this is referred to the VCO rather than to the phase/frequency comparator. In the previous example of the type 1 first-order loop, we referred it only to the phase/frequency comparator rather than the VCO.



Note: The frequency transfer const. of the VCO = K_o
(not $\frac{K_o}{s}$, which is valid for phase transfer only.)

Figure 1-8 Block diagram of a digital PLL before lock is acquired.

1-6-1 Transient Behavior of Digital Loops Using Tri-state Phase Detectors

Pull-in Characteristic

The type 2 second-order loop is used with either a sample/hold comparator or a tri-state phase/frequency comparator. We will now determine the transient behavior of this loop. Figure 1-8 shows the block diagram.

Very rarely in literature is a clear distinction between pull-in and lock-in characteristics or frequency and phase acquisition made as a function of the digital phase/frequency detector. Somehow, all the approximations or linearizations refer to a sinusoidal phase/frequency comparator or its digital equivalent, the exclusive-OR gate.

The tri-state phase/frequency comparator (which will be explored in greater detail in Chapter 4) follows slightly different mathematical principles.

The phase detector gain

$$K'_d = \frac{V_d}{\omega_0} = \frac{\text{phase detector supply voltage}}{\text{loop idling frequency}}$$

is explained fully in Chapter 4, and we only use the result here. This phase detector gain is valid only in the out-of-lock state and is a somewhat coarse approximation to the real gain, which, due to nonlinear differential equations, is very difficult to calculate. However, practical tests show that this approximation is still fairly accurate.

Definitions:

$$\Omega_1(s) = l[\Delta\omega_1(t)] \quad \text{Reference input to } \delta/\omega \text{ detector}$$

$$\Omega_2(s) = l[\Delta\omega_2(t)] \quad \text{Signal VCO output frequency}$$

$$\Omega_e(s) = l[\Delta\omega_e(t)] \quad \text{Error frequency at } \delta/\omega \text{ detector}$$

$$\Omega_e(s) = \Omega_1(s) - \frac{\Omega_2(s)}{N}$$

$$\Omega_2(s) = [\Omega_1(s) - \Omega_e(s)]/N$$

From the circuit earlier,

$$A(s) = \Omega_e(s)K'_d$$

$$B(s) = A(s)F(s)$$

$$\Omega_2(s) = B(s)K_o$$

The error frequency at the detector is

$$\Omega_e(s) = \Omega_1(s)N\frac{1}{N + K_oK_d'F(s)} \tag{1-88}$$

The signal is stepped in frequency:

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \quad (\Delta\omega_1 = \text{magnitude of frequency step}) \tag{1-89}$$

Active Filter of First Order

If we use an active filter

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{1-90}$$

and insert this in Eq. (1-88), the error frequency is

$$\Omega_e(s) = \frac{1}{s\left(N + K_oK_d'\frac{\tau_2}{\tau_1}\right) + \frac{K_oK_d'}{\tau_1}} \tag{1-91}$$

Utilizing the Laplace transformation, we obtain

$$\omega_e(t) = \Delta\omega_1\frac{1}{1 + K_oK_d'(\tau_2/\tau_1)(1/N)}\exp\left[-\frac{1}{(\tau_1N/K_oK_d') + \tau_2}\right] \tag{1-92}$$

and

$$\lim_{t\to 0}\omega_e(t) = \frac{\Delta\omega_1N}{N + K_oK_d'(\tau_2/\tau_1)} \tag{1-93}$$

$$\lim_{t\to\infty}\omega_e(t) = 0 \tag{1-94}$$

Passive Filter of First Order

If we use a passive filter

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{1-95}$$

for the frequency step

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \tag{1-96}$$

the error frequency at the input becomes

$$\Omega_e(s) = \Delta\omega_1N\left\{\frac{1}{s}\frac{1}{s[N(\tau_1 + \tau_2) + K_oK_d'\tau_2] + (N + K_oK_d')} + \frac{\tau_1 + \tau_2}{s[N(\tau_1 + \tau_2) + K_oK_d'\tau_2] + (N + K_oK_d')}\right\} \tag{1-97}$$

For the first term we will use the abbreviation A, and for the second term we will use the abbreviation B.

$$A = \frac{1/[N(\tau_1 + \tau_2) + K_o K_d' \tau_2]}{s\left[s + \frac{N + K_o K_d'}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}\right]} \tag{1-98}$$

$$B = \frac{\frac{\tau_1+\tau_2}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}}{s + \frac{N+K_o K_d'}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}} \tag{1-99}$$

After the inverse Laplace transformation, our final result becomes

$$\mathscr{L}^{-1}(A) = \frac{1}{N + K_o K_d'}\left\{1 - \exp\left[-t\frac{N + K_o K_d'}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2}\right]\right\} \tag{1-100}$$

$$\mathscr{L}^{-1}(B) = \frac{\tau_1 + \tau_2}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2} \exp\left(-t\frac{N + K_o K_d'}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2}\right) \tag{1-101}$$

and finally

$$\omega_e(t) = \omega_1 N[\mathscr{L}^{-1}(A) + (\tau_1 + \tau_2)\mathscr{L}^{-1}(B)] \tag{1-102}$$

What does the equation mean? We really want to know how long it takes to pull the VCO frequency to the reference. Therefore, we want to know the value of t, the time it takes to be within 2π or less of lock-in range.

The PLL can, at the beginning, have a phase error from -2π to $+2\pi$, and the loop, by accomplishing lock, then takes care of this phase error.

We can make the reverse assumption for a moment and ask ourselves, as we have done earlier, how long the loop stays in phase lock. This is called the *pull-out* range. Again, we apply signals to the input of the PLL as long as the loop can follow and the phase error does not become larger than 2π. Once the error is larger than 2π, the loop jumps out of lock.

We will learn more about this in Section 1-10, but as already mentioned with regard to the condition where the loop is out of lock, a beat note occurs at the output of the loop filter following the phase/frequency detector.

The tri-state phase/frequency comparator, however, works on a different principle, and the pulses generated and supplied to the charge pump do not allow the generation of an ac voltage. The output of such a phase/frequency detector is always unipolar, but, relative to the value of $V_{\text{batt}}/2$, the integrator voltage can be either positive or negative. If we assume for a moment that this voltage should be the final voltage under a locked condition, we will observe that the resulting dc voltage is either more negative or more positive relative to this value, and because of this, the VCO will be "pulled in" to this final frequency rather than swept in, which had been mentioned previously. The swept-in technique applies only in cases of phase/frequency comparators, where this beat note is being generated. A typical case would be the exclusive-OR gate or even a sample/hold comparator. This phenomenon is rarely covered in the literature and was probably discussed in detail for the first time in the book by Roland Best [1].

Let us assume now that the VCO has been pulled in to final frequency to be within 2π of the final frequency, and the time t is known. The next step is to determine the lock-in characteristic.

Lock-in Characteristic

We will now determine lock-in characteristic, and this requires the use of a different block diagram. Figure 1-8 shows the familiar block diagram of the PLL, and we will use the following definitions:

$\theta_1(s) = \mathscr{L}[\Delta\delta_1(t)]$ Reference input to δ/ω detector

$\theta_2(s) = \mathscr{L}[\Delta\delta_2(t)]$ Signal VCO output phase

$$\theta_e(s) = \mathcal{L}[\delta_e(t)] \qquad \text{Phase error at } \delta/\omega \text{ detector}$$

$$\theta_e(s) = \theta_1(s) - \frac{\theta_2(s)}{N}$$

From the block diagram, the following is apparent:

$$A(s) = \theta_e(s)K_d$$

$$B(s) = A(s)F(s)$$

$$\theta_2(s) = B(s)\frac{K_o}{s}$$

The phase error at the detector is

$$\theta_e(s) = \theta_1(s)\frac{sN}{K_oK_dF(s) + sN} \tag{1-103}$$

In Section A-4 we will see that a step in phase at the input, with the worst-case error being 2π, results in

$$\theta_1(s) = 2\pi\frac{1}{s} \tag{1-104}$$

We will now treat the two cases using an active or a passive filter.

Active Filter

The transfer characteristic of the active filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{1.90}$$

This results in the formula for the phase error at the detector,

$$\theta_e(s) = 2\pi\frac{s}{s^2 + (sK_oK_d\tau_2/\tau_1)/N + (K_oK_d/\tau_1)/N} \tag{1-105}$$

The polynomial coefficients for the denominator are

$$a_2 = 1$$

$$a_1 = (K_oK_d\tau_2/\tau_1)/N$$

$$a_0 = (K_oK_d/\tau_1)/N$$

and we have to find the roots W_1 and W_2. Expressed in the form of a polynomial coefficient, the phase error is

$$\theta_e(s) = 2\pi\frac{s}{(s + W_1)(s + W_2)} \tag{1-106}$$

After the Laplace transformation has been performed, the result can be written in the form

$$\delta_e(t) = 2\pi\frac{W_1e^{-W_1t} - W_2e^{-W_2t}}{W_1 - W_2} \tag{1-107}$$

with

$$\lim_{t\to 0}\delta_e(t) = 2\pi$$

and

$$\lim_{t\to\infty} \delta_e(t) = 0$$

The same can be done using a passive filter.

Passive Filter

The transfer function of the passive filter is

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{1.95}$$

If we apply the same phase step of 2π as before, the resulting phase error is

$$\theta_e(s) = 2\pi \frac{[1/(\tau_1 + \tau_2)] + s}{s^2 + s\frac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)} + \frac{K_o K_d}{N(\tau_1 + \tau_2)}} \tag{1-108}$$

Again, we have to find the polynomial coefficients, which are

$$a_2 = 1$$
$$a_1 = \frac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)}$$
$$a_0 = \frac{K_o K_d}{N(\tau_1 + \tau_2)}$$

and finally find the roots for W_1 and W_2. This can be written in the form

$$\theta_e(s) = 2\pi \left[\frac{1}{\tau_1 + \tau_2} \frac{1}{(s + W_1)(s + W_2)} + \frac{s}{(s + W_1)(s + W_2)} \right] \tag{1-109}$$

Now we perform the Laplace transformation and obtain our result:

$$\delta_e(t) = 2\pi \left(\frac{1}{\tau_1 + \tau_2} \frac{e^{-W_1 t} - e^{-W_2 t}}{W_1 - W_2} + \frac{W_1 e^{-W_1 t} - W_2 e^{-W_2 t}}{W_1 - W_2} \right) \tag{1-110}$$

with

$$\lim_{t\to 0} \delta_e(t) = 2\pi$$

and

$$\lim_{t\to\infty 0} \delta_e(t) = 0$$

We will show with the type 2 third-order loop how these roots are being determined, as the roots are going to be fifth order. We assume that determining the roots of a cubic equation is known and easy.

As a result of the last equation for the active as well as for the passive filter, Eqs. (1-107) and (1-110) have the dimension of radians. Although mathematically speaking it is not strictly accurate, it is permissible to multiply these values with the division ratio N and the reference frequency to obtain a final error in the dimension frequency. It has been shown in practical experiments that, if this final error is less than 0.1 Hz, the time (t) it takes to get there can be taken as the lock-in time. In Chapter 2, we will learn that any VCO has a certain residual FM. This means that even under locked condition, the output frequency moves within certain boundaries. Medium-quality synthesizers show a residual FM of 3 Hz, whereas a loop with dividers at the output and low division ratio can have a residual

FM as low as 0.1 Hz or better. This is, at times, also called *incidental FM*, and similar expressions have been found in the literature.

In Table 1-2 we indicated that the exclusive-OR gate and the edge-triggered JK master/slave flip-flop have a different operation mode than that of the tri-state phase/frequency comparator.

We will go into the details in Section 1-10, since the tri-state phase/frequency comparator does not require any acquisition aid.

Let us take a look at a numerical example. We have a PLL with the following parameters:

Reference frequency	5000 Hz
K_o	$2\pi \times 1$ MHz
K_θ	2.1 V/rad
N	1000
ω_n	500 Hz
Phase margin	45°
ζ	0.7
R_1	1336 Ω
R_2	445 Ω
C_1	1E-6 F
Reference suppression	20 dB
Lockup time	8 ms

These values were determined for the type 2 second-order loop with a program.

In Section 1-7 we will find that the type 2 third-order loop, although initially somewhat more difficult to treat mathematically, will show better reference suppression, faster lockup time, and really is better as far as reproducibility is concerned. This is due to the fact that there are always stray capacitors and some other elements in the circuit, which can be incorporated in the type 2 third-order loop, whereas the type 2 second-order loop really does not exist in its pure form.

Some of the dynamics of the type 2 second-order loop and of the type 2 third-order loop are dealt with in Section 1-10. For reasons of consistency, however, the transient behavior of the type 2 second-order loop has already been treated, and the equivalent performance of the type 2 third-order loop will be discussed on the following pages.

1-7 TYPE 2 THIRD-ORDER LOOP

We have stated several times previously that low-order loops really do not exist. The reasons for this are the introduction of phase shift by the operational amplifier, stray capacitors, and other things in the loop.

The type 2 third-order loop is a very good approximation of what is actually happening and can easily be developed from the type 2 second-order loop by adding one more *RC* filter at the output. Most likely, the operational amplifier as part of the active filter has to drive a feed-through capacitor, and for reasons of spike decoupling or additional filtering, one resistor is put in series.

Figure 1-9 shows a loop filter for a type 2 third-order loop. Just a reminder: this loop has two integrators, one being the VCO and one being the operational amplifier and three time constants.

This filter can be redrawn as shown in Figure 1-10. The transfer function for this filter is

$$F(s) = -\frac{1}{s\tau_1}\frac{1 + s\tau_2}{1 + s\tau_3} \tag{1-111}$$

with

$$\tau_1 = C_1 R_1 \tag{1-112}$$

$$\tau_2 = R_2(C_1 + C_2) \tag{1-113}$$

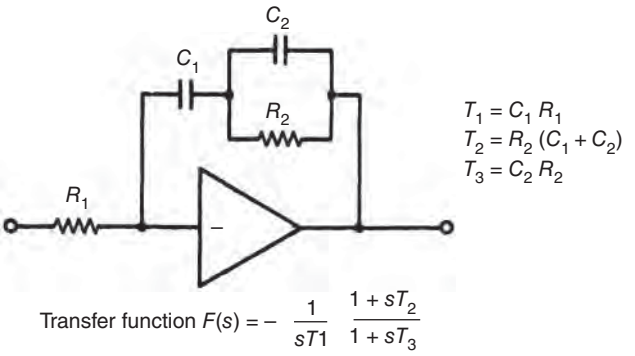


Figure 1-9 Circuit diagram of loop filter for the third-order loop.

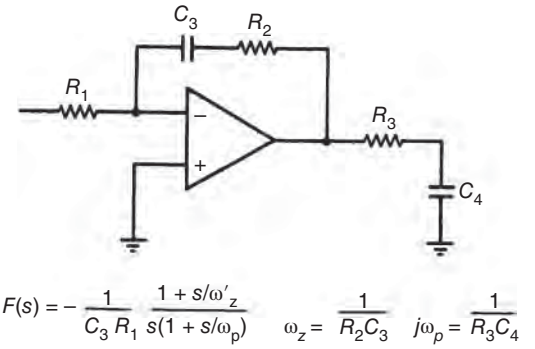


Figure 1-10 Circuit diagram of redrawn Figure 1-9. Note that this is the same type of loop filter as in the type 2 second-order loop with an additional *RC* time constant.

$$\tau_3 = C_2 R_2 \tag{1-114}$$

Let us now determine the transfer function for the type 2 third-order loop.

1-7-1 Transfer Function of Type 2 Third-Order Loop

The forward gain is

$$K = K_\theta F(s) \frac{K_o}{s} \tag{1-115}$$

and for

$$H(s) = \frac{1}{N} \quad N = \text{division ratio} \tag{1-116}$$

the open-loop gain is

$$A(s) = K_\theta F(s) \frac{K_o}{s} \frac{1}{N} \tag{1-117}$$

and the system transfer function is

$$\begin{aligned} B(s) &= \frac{\theta_o(s)}{\theta_i(s)} = \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \\ &= \frac{K_\theta F(s)(K_o/s)}{1 + \frac{K_\theta F(s)(K_o/s)}{N}} \\ &= \frac{K_\theta F(s) K_o}{s + \frac{K_\theta F(s) K_o}{N}} \end{aligned} \tag{1-118}$$

If we insert our time constants τ_1, τ_2, and τ_3, we obtain

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{1 + s\tau_2}{s\tau_1 + s^2\tau_1\tau_3} \frac{K_\theta K_o}{s + \frac{K_\theta K_o}{N} \frac{1+s\tau_2}{s\tau_1 + s^2\tau_1\tau_2}} \tag{1-119}$$

and

$$B(s) = NK_\theta K_o(1 + s\tau_2) \frac{1}{s^3 N\tau_1\tau_3 + s^2 N\tau_1 + sK_\theta K_o\tau_2 + K_\theta K_o} \tag{1-120}$$

$$\text{polynominal } P = s^3 N\tau_1\tau_3 + s^2 N\tau_1 + sK_\theta K_o\tau_2 + K_\theta K_o \tag{1-121}$$

As we have done before, we have to determine the roots:

$$\frac{P}{N\tau_1\tau_3} = s^3 + s^2\frac{1}{\tau_3} sK_\theta K_o \frac{\tau_2}{N\tau_1\tau_3} + K_\theta K_o \frac{1}{n\tau_1\tau_3} = 0 \tag{1-122}$$

Therefore, the coefficients are

$$a_4 = 1 \tag{1-123}$$

$$a_3 = \frac{1}{\tau_3} \tag{1-124}$$

$$a_2 = K_\theta K_o \frac{\tau_2}{N\tau_1\tau_3} \tag{1-125}$$

$$a_1 = K_\theta K_o \frac{1}{N\tau_1\tau_3 = \frac{a_2}{\tau_2}} \tag{1-126}$$

The polynomial is of the order of 3, and we can use a calculator routine to find the roots b_1, b_2, and b_3; finally,

$$s_1 = 0 \tag{1-127}$$

$$s_2 = -b_1 \tag{1-128}$$

$$s_3 = -b_2 \tag{1-129}$$

$$s_4 = -b_3 \tag{1-130}$$

The next step is partial fraction forming:

$$\begin{aligned} \frac{1}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s} &= \frac{1}{a_4 s(s + b_1)(s + b_2)(s + b_3)} \\ &= \left(\frac{c_1}{s + b_1} \frac{c_2}{s + b_2} \frac{c_3}{s + b_3} \frac{c_4}{s} \right) \frac{1}{a_4} \end{aligned} \tag{1-131}$$

Now we have to determine C_i, for $i = 1$–4, and multiply the equation previously,

$$\frac{c_1(s+b_2)(s+b_3)s + c_2(s+b_1)(s+b_3)s + c_3(s+b_1)(s+b_2)s + c_4(s+b_1)(s+b_2)(s+b_3)}{(s+b_1)(s+b_2)(s+b_3)s}$$

which is equal to

$$\frac{1}{(s+b_1)(s+b_2)(s+b_3)s} \quad \text{(numerator = 1)}$$

Rearranging yields

$$\begin{aligned} &s^3(c_1 + c_2 + c_3 + c_4) \\ &+ s^2[c_1(b_2 + b_3) + c_2(b_1 + b_3) + c_3(b_1 + b_2) + c_4(b_1 + b_2 + b_3)] \\ &+ s[c_1b_2b_3 + c_2b_1b_3 + c_3b_1b_2 + c_3b_1b_2 + c_4(b_1b_2 + b_1b_3 + b_2b_3)] \\ &+ c_4b_1b_2b_3 \end{aligned}$$

and since

$$c_1 + c_2 + c_3 = 0 \tag{1-132}$$

$$c_1(b_2 + b_3) + c_2(b_1 + b_3) + c_3(b_1 + b_2) = 0 \tag{1-133}$$

$$c_1b_2b_3 + c_2b_1b_3 + c_3b_1b_2 = \frac{1}{N\tau_1\tau_3} \tag{1-134}$$

our final results are

$$c_3 = -c_1 - c_2 \tag{1-135}$$

$$c_2 = -c_1\frac{b_3 - b_1}{b_3 - b_2} \tag{1-136}$$

$$c_1 = \frac{1}{N\tau_1\tau_3}\frac{1}{(b_3 - b_1)(b_2 - b_1)} \tag{1-137}$$

Let us test this equation with a step function

$$\theta_1(s) = \frac{1}{s} \tag{1-138}$$

We obtain

$$-13\ \text{dBm}$$

$$\begin{aligned} \theta_o(s) &= NK_\theta K_o\frac{1 + s\tau_2}{s}\frac{1/N\tau_1\tau_3}{s^3 + \frac{1}{\tau_3}s^2 + \frac{\tau_2K_\theta K_o}{N\tau_1\tau_3}s + \frac{K_\theta K_o}{N\tau_2\tau_3}} \\ &= NK_\theta K_o\left[\tau_2\left(\frac{c_1}{s+b_1} + \frac{c_2}{s+b_2} + \frac{c_3}{s+b_3}\right) + \frac{c_1}{b_1}\left(\frac{1}{s} - \frac{1}{s+b_1}\right) + \frac{c_2}{b_2}\left(\frac{1}{s} - \frac{1}{s+b_2}\right) + \frac{c_3}{b_3}\left(\frac{1}{s} - \frac{1}{s+b_3}\right)\right] \\ &= NK_\theta K_o\left[\frac{(\tau_2 - 1/b_1)c_1}{s+b_1} + \frac{(\tau_2 - 1/b_2)c_2}{s+b_2} + \frac{(\tau_2 - 1/b_3)c_3}{s+b_3} + \frac{(c_1/b_1) + (c_2/b_2) + (c_3/b_3)}{s}\right] \end{aligned} \tag{1-139}$$

If we perform a Laplace transformation, our final result is

$$\theta_o(t) = NK_\theta K_o\left[\left(\tau_2 - \frac{1}{b_1}\right)c_1e^{-b_1t} + \left(\tau_2 - \frac{1}{b_2}\right)c_2e^{-b_2t} + \left(\tau_2 - \frac{1}{b_3}\right)c_3e^{-b_3t} + \left(\frac{c_1}{b_1} + \frac{c_2}{b_2} + \frac{c_3}{b_3}\right)\right] \tag{1-140}$$

To plot the Bode diagram, the open-loop gain equation for $A(j\omega)$ determined and plotted in magnitude and phase. We obtain

$$\begin{aligned} A(j\omega) &= -\frac{K_\theta K_o}{Nj\omega}\left(\frac{1}{j\omega\tau_1}\right)\frac{1+j\omega\tau_2}{1+j\omega\tau_3} \\ &= \frac{K_\theta K_o}{N\omega^2}\left(\frac{1+j\omega\tau_2}{1+j\omega\tau_3}\right)\frac{1}{\tau_1} \end{aligned} \tag{1-141}$$

We will then abbreviate

$$\frac{K_\theta K_o}{N\omega^2}\tau_9 \tag{1-142}$$

The phase is determined from

$$\frac{(1+j\omega\tau_2)(1-j\omega\tau_3)}{1+\omega^2\tau_3^2} = \frac{1+\omega^2\tau_2\tau_3+j\omega(\tau_2-\tau_3)}{1+\omega^2\tau_3^2} \tag{1-143}$$

and

$$\tan\phi = \frac{\omega\tau_2}{1+\omega^2\tau_2\tau_3} - \frac{\omega\tau_3}{1+\omega^2\tau_2\tau_3} \tag{1-144}$$

The magnitude is

$$|A(j\omega)| = \frac{\tau_9}{\tau_1}\frac{\sqrt{1+\omega^2\tau_2^2}}{\sqrt{1+\omega^2\tau_3^2}} \tag{1-145}$$

with

$$|A(j\omega)| = 1 \quad \text{(crossover point)} \tag{1-146}$$

We finally obtain

$$\tau_1 = \tau_9\sqrt{\frac{1+\omega^2\tau_2^2}{1+\omega^2\tau_3^2}} \tag{1-147}$$

and

$$A_1 = 1+\omega^2\tau_2^2 \tag{1-148}$$

$$A_2 = 1+\omega^2\tau_3^2 \tag{1-149}$$

The phase margin is

$$\phi = \arctan\omega\tau_2 - \arctan\omega\tau_3 + \pi \tag{1-150}$$

assuming that

$$\omega^2\tau_2\tau_3 \ll 1$$

Let us determine the natural loop frequency ω_o from the point of zero slope of the phase response,

$$\frac{d\phi(\omega)}{d\omega} = 0 \tag{1-151}$$

$$\frac{d\phi}{d\omega} = \frac{\tau_2}{1+(\omega\tau_2)^2} - \frac{\tau_3}{1+(\omega\tau_3)^2} = 0 \tag{1-152}$$

and therefore

$$\omega_o = \sqrt{\frac{1}{\tau_2 \tau_3}} \tag{1-153}$$

If we set

$$\alpha = \arctan \omega\tau_2 \tag{1-154}$$

$$\beta = \arctan \omega\tau_3 \tag{1-155}$$

$$\phi = \alpha - \beta + \pi \tag{1-156}$$

and

$$\begin{aligned} \tan\phi &= \tan[(\alpha - \beta) + \pi] \\ &= \frac{\tan(\alpha - \beta) + 0}{1 - 0} = \tan(\alpha - \beta) \end{aligned} \tag{1-157}$$

then

$$\tan(\alpha - \beta) = \frac{\tan\alpha - \tan\beta}{1 + \tan\alpha \tan\beta} = \frac{\omega\tau_2 - \omega\tau_3}{1 + \omega^2\tau_2\tau_3} = \tan\phi \tag{1-158}$$

If we set

$$\omega = \omega_o = \sqrt{\frac{1}{\tau_2 \tau_3}} \tag{1-159}$$

then

$$\tan\phi_o = \frac{(1/\sqrt{\tau_2\tau_3})(\tau_2 - \tau_3)}{1 = 1} = \frac{\tau_2 - \tau_3}{2\sqrt{\tau_2\tau_3}} \tag{1-160}$$

and

$$\sqrt{\tau_2\tau_3} = \frac{1}{\omega_o} \tag{1-161}$$

$$\omega_o^2\tau_2\tau_3 = 1 \tag{1-162}$$

$$\tau_2 = \frac{1}{\omega_o^2\tau_3} \tag{1-163}$$

Using this value, we can determine the time constant τ_3 from

$$\tan\phi_o = \frac{(1/\omega_o^2\tau_3) - \tau_3}{2(1/\omega_o)} = \frac{(1/\omega_o^2\tau_3) - \omega_o\tau_3}{2} \tag{1-164}$$

and

$$2\tan\phi_o\omega_o\tau_3 = 1 - \omega_o^2\tau_3^2 \tag{1-165}$$

$$\omega_o^2\tau_3^2 + 2\tan\phi_o\omega_o\tau_3 - 1 = 0 \tag{1-166}$$

The time constant τ_3 is determined from

$$\begin{aligned}\tau_3 &= \frac{-2\tan\phi_o\omega_o + \sqrt{4\tan^2\phi_o\omega_o^2 + 4\omega_o^2}}{2\omega_o^2} \\ &= \frac{-2\tan\phi_o\omega_o + 2\omega_o\sqrt{\tan^2\phi_o + 1}}{2\omega_o^2} \\ &= \frac{\tan\phi_o + \sqrt{(\cos^2\phi_o + \sin^2\phi_o)/\cos^2\phi_o}}{\omega_o} \\ &= \frac{-\tan\phi_o + 1/\cos\phi_o}{\omega_o}\end{aligned} \tag{1-167}$$

τ_3 is now determined independent of the other parameters, τ_1 and τ_2, by setting the value for ω_o and the phase margin ϕ to begin with. Once τ_3 is determined, the values for τ_1 and τ_2 can be computed by inserting them in the necessary equations.

These equations were somewhat lengthy, but they were spelled out in great detail to show the approach taken. A computer program based on these equations is presented in Section A-3 and can be used for Bode diagram plotting.

It may be useful to compare the normalized output response of the different types of loops. Figure 1-11a shows the step response for a phase margin of 10° and 45° and a type 2 third-order loop. Figure 1-11b shows the result for a type 1 second-order loop similar to the normalized output response for a damping factor of 0.1 and 0.45. Figure 1-11c shows the normalized output response for the same damping factors, 0.1 and 0.45.

These responses can be plotted in the Bode diagram. Figure 1-11d shows the integrated response $F(s)$ of the second- and third-order loops.

The closed-loop response of the type 2, second- and third-order loops is somewhat similar; but as Figure 1-11e shows, we obtain a much better suspension from the type 2 third-order loop than from the type 2 second-order loop.

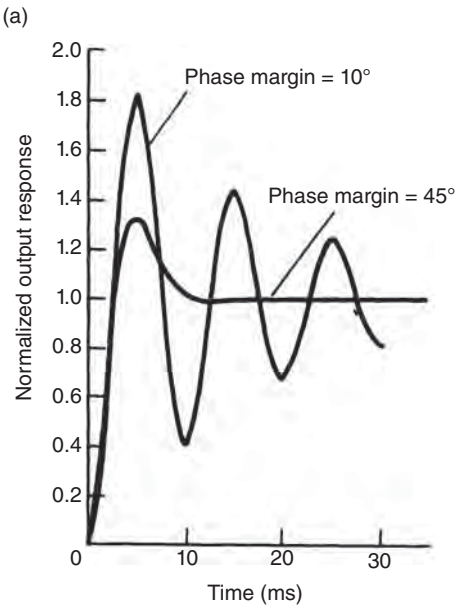


Figure 1-11a Normalized output response of a type 2 third-order loop with a phase margin of 10° and 45°.

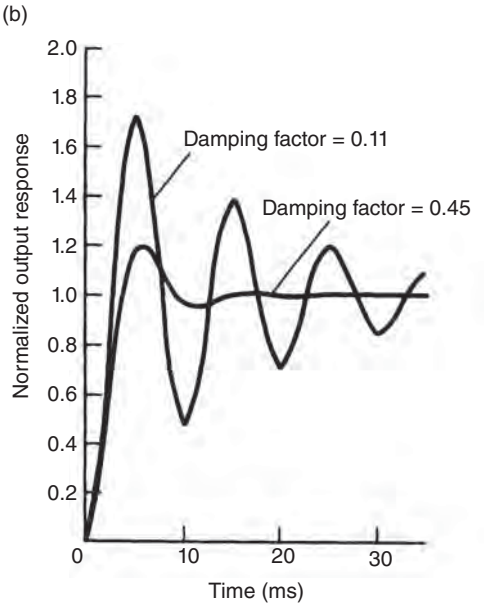


Figure 1-11b Normalized output response of a type 1 second-order loop having a damping factor of 0.1 and 0.45.

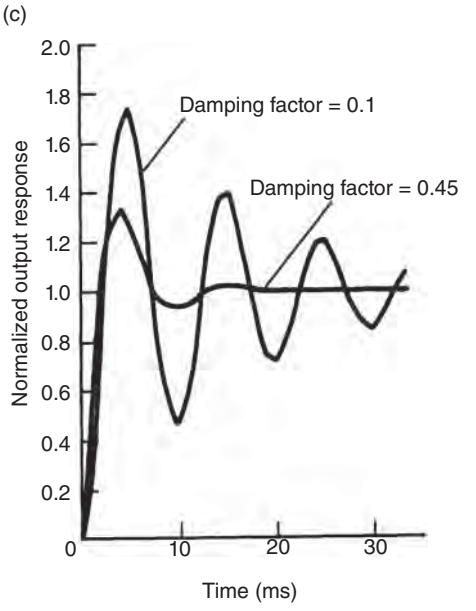


Figure 1-11c Normalized output response of a type 2 second-order loop with a damping factor of 0.1 and 0.05 for $\Omega_n = 0.631$.

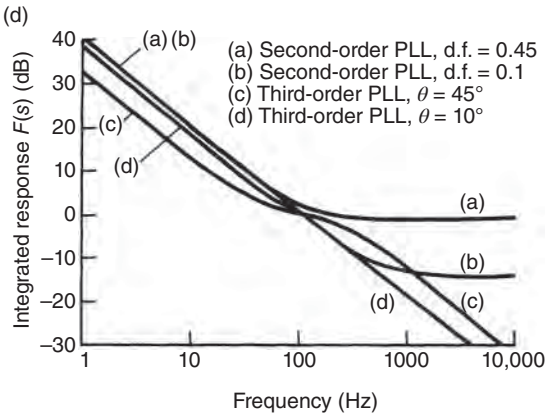


Figure 1-11d Integrated response for various loops as a function of the phase margin.

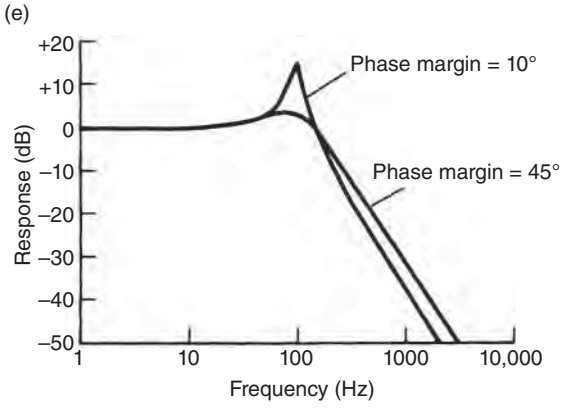


Figure 1-11e Closed-loop response of a type 2 third-order PLL having a phase margin of 10° and 45°.

If the phase margins of the damping factor chosen are inappropriate, we obtain an overshoot that translates into discrete spurious noise at the appropriate offset from the carrier.

1-7-2 FM Noise Suppression

In drawing the Bode plot, it is also convenient to show the suppression of noise of the VCO that is provided by the PLL. Using

$$E_n = \text{VCO noise voltage}$$

and

$$E = \text{noise voltage with loop closed}$$

we can write

$$E(s) = E_n(s)\frac{1}{1 + (\text{open-loop gain})}$$

$$= \frac{1}{1 + G(s)H(s)}$$
$$= \frac{1}{1 + A(s)} \tag{1-168}$$

or

$$\left| \frac{E(\omega)}{E_n(\omega)} \right| = \frac{1}{\frac{K_\theta K_o}{N\omega^2 \tau_1} \left| \frac{1+j\omega\tau_2}{1+j\omega\tau_3} \right| + 1} \tag{1-169}$$

The type 2 third-order loop is really the most important but was not used that often in the past. This may be a lack of understanding or not realizing that, by proper combination of the time constants, the unavoidable feed-through capacitors and some series capacitors can be incorporated to obtain this type of loop. The advantages of the third-order loop over the second-order loop are in the higher reference suppression for a given loop frequency, or if a certain loop frequency has to be chosen because of lockup time, the reference suppression is higher than we would find in the case of a type 2 second-order loop.

Let us take a case where we have the following parameters:

Reference frequency	5000 Hz
K_o	$2\pi \times 1$ MHz
K_θ	2.1
Division ratio N	10,000
ω_n	500 Hz
Phase margin	45°

The resulting values for the loop filter are determined from the computer program:

R_1	5600 Ω
R_2	1105 Ω
C_1	5.7E-7 F
C_2	1.19E-7 F
Reference suppression	32 dB
Lockup time	3 ms

The same loop in a type 2 second-order system would show reference suppression of 20 dB for the same loop bandwidth and 8-ms lockup time. These last two figures clearly indicate the advantage of the type 2 third-order loop.

Many applications require an even higher reference suppression. In the following analysis, we will deal with higher-order loops that are capable of additional suppression. However, the lockup time and the phase stability now may become a trade-off, as we will soon find out.

1-8 HIGHER-ORDER LOOPS

1-8-1 Fifth-Order Loop Transient Response

The fifth-order loop consists of a type 2 third-order loop with a second-order low-pass filter. The integrator is described by

$$F(s) = -\frac{1}{s\tau_1} \frac{1 + s\tau_2}{1 + s\tau_3} \tag{1.111}$$

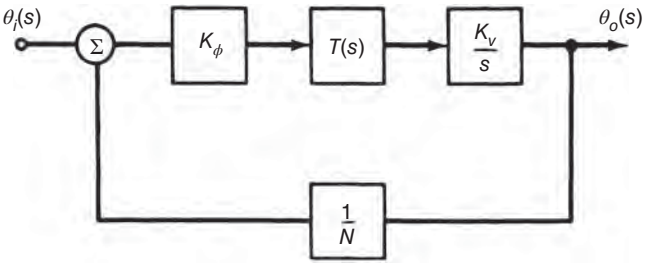


Figure 1-12 Noise contributing block in a type 2 fifth-order loop.

and the second-order low-pass filter is described by

$$K(s) = \frac{1}{s^2(1/\omega_n^2) + s(2d/\omega_n) + 1} \tag{1-170}$$

The transfer function of the filters is

$$\begin{aligned} T(s) &= \frac{-(1+s\tau_2)}{s^2\tau_1\tau_3 + s\tau_1} \frac{1}{s^2(1/\omega_n^2) + s(2d/\omega_n) + 1} \\ &= \frac{1+s\tau_2}{s^4\frac{\tau_1\tau_3}{\omega_n^2} + s^3\frac{\tau_1}{\omega_n}\left(2d\tau_3 + \frac{1}{\omega_n}\right) + s^2\tau_1\left(\tau_3\frac{2d}{\omega_n}\right) + s\tau_1} \end{aligned} \tag{1-171}$$

We use the familiar block diagram, Figure 1-12, which shows the phase detector, the low-pass filter, the active integrator [both condensed in $T(s)$], the VCO, and the divider. The forward gain now becomes $(K_\theta K_o/s)T(s)$, and the open-loop gain is

$$A(s) = \frac{K_\theta K_o}{s}\frac{T(s)}{N} \tag{1-172}$$

The closed-loop transfer function is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \tag{1-173}$$

or

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{(K_\theta K_o/s)\,T(s)}{1 + (K_\theta K_o/Ns)\,T(s)} = \frac{K_\theta K_o T(s)}{s + K_\theta K_o T(s)/N} \tag{1-174}$$

Rearranging yields

$$\theta_o(s) = \theta_i(s) K_\theta K_o \frac{T(s)}{S + K_\theta K_o T(s)/N} \tag{1-175}$$

The output phase, which is the same as the VCO phase, is now assumed to be disturbed by a step of magnitude S_v. The amount S_v would be in the maximum case $N \times 2\pi$, using phase detector operating ranges of $\pm 2\pi$.

If this step is referred to the input of the phase detector, it has to be divided by N, and in Laplace notation, we have

$$\theta_i(s) = \frac{S_v}{Ns} \tag{1-176}$$

from which results

$$\theta_o(s) = \frac{S_v K_\theta K_o}{N} \frac{T(s)}{s^2 + (K_\theta K_o/N)sT(s)} \tag{1-177}$$

with $K_\theta K_o/N = U$. Applying a partial fraction, we obtain

$$\theta_o(s) = \frac{S_v}{s} - \frac{S_v s}{s^2 + UsT(s)} = \frac{S_v}{s} - \frac{S_v}{s + UT(s)} \tag{1-178}$$

After some manipulations, which are deleted, it can be shown that

$$\Delta\theta_o(s) = -S_v \frac{s^4 + s^3\frac{2d\tau_3\omega_n+1}{\tau_3} + s^2\left(\omega_n^2\frac{2d\omega_n}{\tau_3}\right) + s\frac{\omega_n^2}{\tau_3}}{s^5 + s^4\frac{2d\tau_3\omega_n+1}{\tau_3} + s^3\left(\omega_n^2\frac{2d\omega_n}{\tau_3}\right) + s^2\frac{\omega_n^2}{\tau_3} + s\frac{U\tau_2\omega_n^2}{\tau_1\tau_3}\ \frac{U\omega_n^2}{\tau_1\tau_3}} \tag{1-179}$$

We now factorize a denominator polynomial of the form

$$s^5 a_5 + s^4 a_4 + s^3 a_3 + s^2 a_2 + s a_1 + a_o$$

and therefore obtain the following coefficients:

$$a_5 = 1 \tag{1-180}$$

$$a_4 = \frac{2d\tau_3\omega_n + 1}{\tau_3} \tag{1-181}$$

$$a_3 = \omega_n^2 + \frac{2d\omega_n}{\tau_3} \tag{1-182}$$

$$a_2 = \frac{\omega_n^2}{\tau_3} \tag{1-183}$$

$$a_1 = U\tau_2\frac{\omega_n^2}{\tau_1\tau_3} \tag{1-184}$$

$$a_o = U\frac{\omega_n^2}{\tau_1\tau_3} \tag{1-185}$$

The next task is to determine the roots W_i and rewrite the denominator polynomial in the form

$$P_{\text{demoninator}} = (s - W_5)(s - W_4)(s - W_3)(s - W_2)(s - W_1) \tag{1-186}$$

For the Laplace transform, we need the residues

$$K_s = W_i = e^{ts}\frac{\text{numerator}}{\text{demoninator without containing } W_i} \tag{1-187}$$

The next step is to calculate the binomial residues:

$$K_k = e^{tP_k}\frac{A_{k1} + A_{k2} + A_{k3} + A_{k4}}{B_{k1}B_{k2}B_{k3}B_{k4}} \tag{1-188}$$

$$K_1 = e^{tP_1}\frac{A_{16} + A_{15} + A_{14} + A_{13}}{B_{12}B_{13}B_{14}B_{15}} \tag{1-189}$$

$$K_2 = e^{tP_2}\frac{A_{26}+A_{25}+A_{24}+A_{23}}{B_{21}B_{23}B_{24}B_{25}} \tag{1-190}$$

$$K_3 = e^{tP_3}\frac{A_{36}+A_{35}+A_{34}+A_{33}}{B_{31}B_{32}B_{34}B_{35}} \tag{1-191}$$

$$K_4 = e^{tP_4}\frac{A_{46}+A_{45}+A_{44}+A_{43}}{B_{41}B_{42}B_{43}B_{45}} \tag{1-192}$$

$$K_5 = e^{tP_5}\frac{A_{56}+A_{55}+A_{54}+A_{53}}{B_{51}B_{52}B_{53}B_{54}} \tag{1-193}$$

As

$$A_{ij} = P_i \uparrow (j-2)Q\,j \tag{1-194}$$

$$i = 1,\ 2,\ 3,\ N_2 \tag{1-195}$$

$$j = 3,\ 4,5,\ N_2+1 \tag{1-196}$$

and

$$B_{ij} = P_i - P_j \tag{1-197}$$

$$i = 1,2,3,\ \ldots\ ,N_2 \tag{1-198}$$

$$j = 1,2,3,\ \ldots\ ,N_2 \tag{1-199}$$

it is apparent that

$$A_{1ij} \triangleq \text{real}\,A_{ij} \tag{1-200}$$

$$A_{2ij} \triangleq \text{imaginary}\,A_{ij} \tag{1-201}$$

$$B_{1ij} \triangleq \text{real}\,B_{ij} \tag{1-202}$$

$$B_{2ij} \triangleq \text{imaginary}\ \ B_{ij} \tag{1-203}$$

$$K_{1i} \triangleq \text{real}\ \ K_i \tag{1-204}$$

$$K_{2i} \triangleq \text{imaginary}\ \ K_i \tag{1-205}$$

Using the results, we can rewrite

$$\Delta\theta_o(s) = \frac{s^4Q_6 + s^3Q_5 + s^2Q_4 + sQ_3}{s^5Q_6 + s^4Q_5 + s^3Q_4 + s^2Q_3 + sQ_2 + Q_1} \tag{1-206}$$

Finally, we obtain the roots P_1 to P_5 in terms of Q_1 to Q_6; then the partial fraction expansion gives the residues:

$$\underset{s=P_1}{K_1} = e^{tP_1}\frac{P_1^4Q_6 + P_1^3Q_5 + P_1^2Q_4 + P_1Q_3}{(P_1-P_2)(P_1-P_3)(P_1-P_4)(P_1-P_5)} \tag{1-207}$$

$$\underset{s=P_2}{K_2} = e^{tP_2}\frac{P_2^4Q_6 + P_2^3Q_5 + P_2^2Q_4 + P_2Q_3}{(P_2-P_1)\,(P_2-P_3)\,(P_2-P_4)\,(P_2-P_5)} \tag{1-208}$$

$$\underset{s=P_3}{K_3} = e^{tP_3}\frac{P_3^4Q_6 + P_3^3Q_5 + P_3^2Q_4 + P_3Q_3}{(P_3-P_1)(P_3-P_2)(P_3-P_4)(P_3-P_5)} \tag{1-209}$$

$$\underset{s=P_4}{K_4} = e^{tP_4} \frac{P_4^4 Q_6 + P_4^3 Q_5 + P_4^2 Q_4 + P_4 Q_3}{(P_4 - P_1)(P_4 - P_2)(P_4 - P_3)(P_4 - P_5)} \tag{1-210}$$

$$\underset{s=P_5}{K_5} = e^{tP_5} \frac{P_5^4 Q_6 + P_5^3 Q_5 + P_5^2 Q_4 + P_5 Q_3}{(P_5 - P_1)(P_5 - P_2)(P_5 - P_3)(P_5 - P_4)} \tag{1-211}$$

$$\Delta\theta(t) = \left[\sum_{n=1}^{5} K_n \right] \tag{1-212}$$

What is the practical use of higher-order loops? Higher-order loops are really useful only in frequency synthesizers if the reference frequency is substantially higher than the loop frequency. A typical example would be a reference frequency of as high as 5 or 10 MHz down to as low as 25 kHz, which has to be suppressed more than 90 dB. The phase shift introduced by the additional filtering, as can be seen by the computer program in the Appendix B and the example shown here, can be allowed only if the cutoff frequency of the loop is small relative to the additional poles of the filter. What is a typical example? Let us assume that we have a reference frequency of 25 kHz, and our loop frequency is set at 1 or 2 kHz. The resulting reference suppression with the simple loop filter would be approximately 20 times log(25 kHz/2 kHz), or roughly 20 dB. This is totally insufficient, of course.

The third-order loop, because of its deeper filtering, will increase this to roughly 33 dB, but this is still not enough. The insertion of a steep filter, such as an active filter or an inductor-capacitor (*LC*) elliptic filter, with poles at 25 kHz, will have very little phase shift at 2 kHz, the cutoff frequency of the loop filter, and a substantial suppression of the reference becomes possible. However, these high-order systems are useful only if there is enough difference between the reference frequency and the loop frequency. The higher the ratio between the two values, the easier it becomes to design a high-order system.

To get high suppression and not too much phase shift and to be able to work close to the reference frequency, special detectors are generally required. The phase shift introduced by using a sample/hold comparator is fairly small, and it is possible to set the loop filter at about half of the reference. If properly designed, the dual sampler combines good reference suppression with low noise. The phase shift can be adjusted and compensated. The drawback of the sample/hold comparator, as we will see in Chapter 4, is its limits as to what is the highest frequency of operation.

If properly designed, the tri-state phase/frequency comparator, also discussed in Chapter 4, may have 60–70 dB inherent reference suppression without the filter and may ease the requirement on the loop filter. Only techniques that compensate the spikes at the output of the tri-state phase/frequency comparator, as will be described later, will reduce the phase jitter and incidental FM introduced by this somewhat noisy discriminator. As the tri-state comparator is somewhat noisier than the sample/hold, the particular loop with its cutoff frequency and its noise requirements will determine which sample to use.

It may be useful to do some comparison between the different loops based on their performance. Figure 1-13a shows a simple block diagram of a PLL loop with a 15-MHz reference oscillator and 300-MHz output frequency. The division ratio is therefore 20. An active integrator with the time constant $T_1, \ldots, T_4$ and the open-loop gain A_0 is selected.

The plot of Figure 1-13b shows the phase noise of the VCO, the phase noise of the reference oscillator of 15 MHz, and the resulting phase noise when the loop is closed. The overshot is due to the loop bandwidth and the damping factor. In this case, the reduction of the loop and width would have reduced the phase noise as the VCO had better noise properties than the closed loop.

1-9 DIGITAL LOOPS WITH MIXERS

The single-loop synthesizer has a number of restrictions. One immediate restriction is the fact that the step size is the same as the reference frequency, unless special techniques are used, which are described in Chapter 3.

In addition, as we have frequency dividers that work "only" up to about 2 GHz, it becomes difficult, if not impossible, to build a PLL at a much higher frequency unless some mixing techniques are used. These techniques

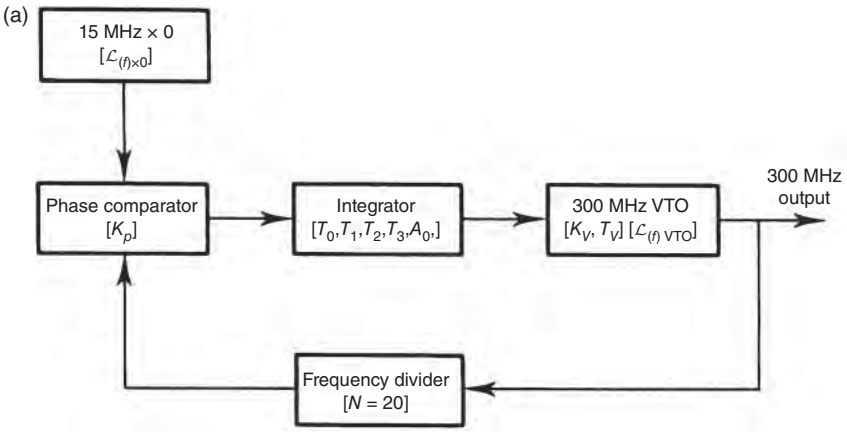


Figure 1-13a Simple block diagram of fifth-order PLL.

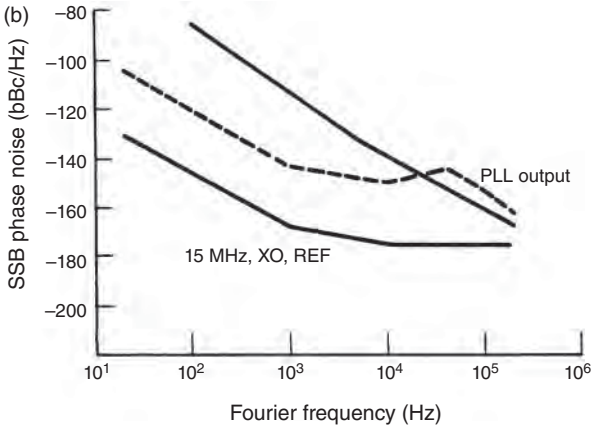


Figure 1-13b Single sideband (SSB) phase noise in dBc/Hz for the 15-MHz crystal oscillator (solid line) 300 MHz L_c VCO (solid line above) and PLL output of total system (curve).

are also sometimes referred to as *heterodyning techniques*. Figure 1-14 shows a single-loop synthesizer that has a mixer incorporated, which heterodynes the VCO frequency down to a lower frequency at which we have dividers available. The auxiliary frequency that is injected in the loop for down-conversion is generated from the reference oscillator and may be a direct-digital synthesis (DDS). Today we can get a DDS system up to 6 GHz, to be driven at 12 GHz or higher. Theoretically we could omit the divide by N stage, but the penalty would be the internal spurious of the DDS, so it is advisable to operate the DDS at less the 1/10 or less of the sampling frequency. For now we are mostly concerned only with the question of loop stability as a function of the introduction of this mixer, and its possible effects as far as unwanted sidebands are concerned.

Let us assume the numerical example shown in Figure 1-15. This synthesizer is intended for use in an amateur transceiver operating from 144 to 148 MHz, a frequency range that is well within the capabilities of current dividers. However, since we want to minimize power consumption, we find that it requires less power to generate an auxiliary frequency of 140 MHz from our 5-MHz standard (synchronizing a 70-MHz crystal and doubling it). The output frequency of this mixer then is 4–8 MHz, and this frequency range can be handled by a programmable divider in CMOS. Between the mixer and the divider, we will insert a bandpass filter of 4-MHz bandwidth. The divider in

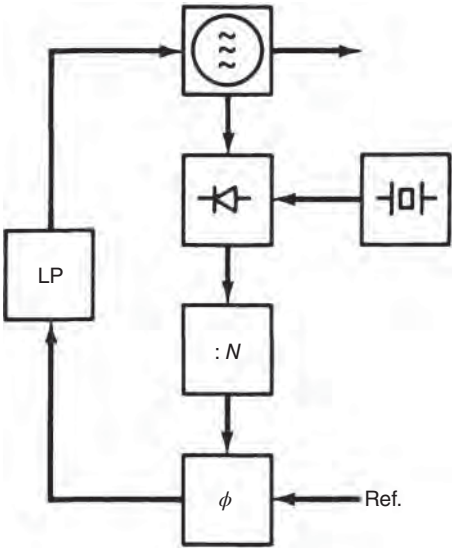


Figure 1-14 Block diagram of a digital PLL using the heterodyne technique.

CMOS now has to operate between 4 and 8 MHz. For such amateur applications it is frequently required that the same synthesizer be used to transmit and receive.

For transmit applications, frequency modulating the synthesizer is required, and the modulation can be inserted in the loop filter, as the loop bandwidth probably is restricted to a few hundred hertz, while the step size will be 5 kHz, in accordance with the channels available. The modulation could also be done if the 140 MHz was generated from a free-running 70-MHz crystal, which is then modulated.

At 70 MHz we will probably have to use a third- or fifth-overtone crystal, which cannot be pulled very well, probably not enough to accommodate a maximum of 3-kHz deviation. More information on pulling of crystals is presented in Chapter 4.

What does the insertion of the mixer do to our system? The division ratio without mixing would have been 28,800–29,600, or a ratio of 1:1.0278. After inserting the mixing stage, the division ratio now is 800–1600, and the absolute ratio is 1:2.

The loop gain, assuming that the VCO gain is constant over the tuning range, is now changing by the amount 1:2. In some loops we will find that the introduction of such a mixer results in a much larger change of division ratios, and if the frequencies are not selected properly, a change of 1:10 will occur. This will cause two difficulties:

(1) If the multiplication changes too much, the sideband of the reference being multiplied at the output will change substantially as a function of frequency setting, while the percentage change of the frequency at the output is very small. Therefore, at the higher frequency, in our case 148 MHz, the noise sideband inside the loop bandwidth will be twice as high as the 144 MHz. In a case where the loop gain changes more dramatically, such as 1:10, the noise will change by this amount.

(2) If the loop gain changes with all other parameters remaining constant, this may cause a stability problem. The net result is that, in the case of a type 2 second-order loop, our damping factor ζ can range from 0.1 to 1, and the transient performance of the loop will vary substantially; therefore, stability will become an issue. We have to find a method to compensate for the change of loop gain, and we will show a method of dealing with this phenomenon in Section 1-10. Right now it is only important to know that it does occur and that it can present a problem.

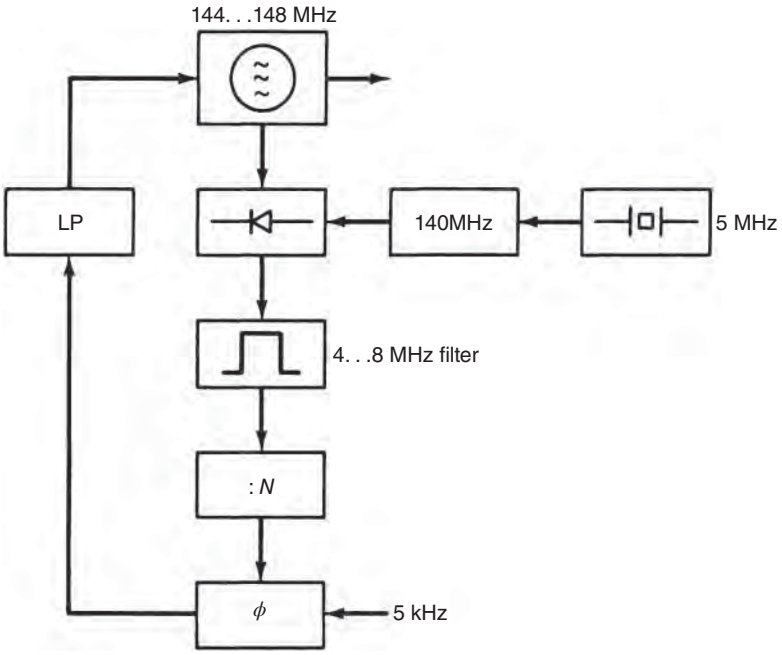


Figure 1-15 Block diagram of a 144- to 148-MHz synthesizer using the heterodyne technique, resulting in an internal IF of 4–8 MHz.

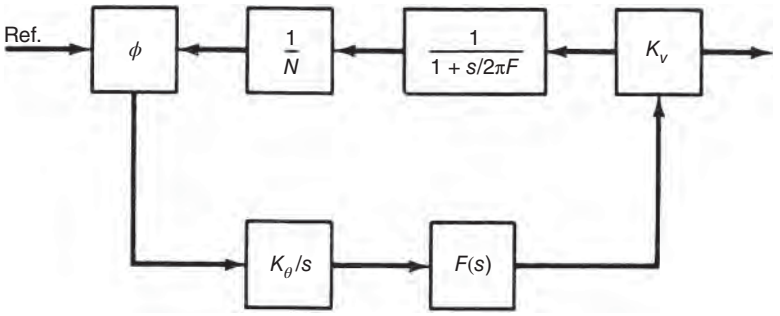


Figure 1-16 Linearized equivalent circuit of a PLL with the heterodyne technique, including delay information introduced by the IF filter.

The next effect the mixer produces is the consequence of phase shift of the IF filter following the mixer, in our case a filter ranging from 4 to 8 MHz. As a result, we have to modify our block diagram of the loop, as shown in Figure 1-16. The additional box represents the low-pass equivalent of the bandpass filter, and the delay of this filter has to be determined. There are a number of good books available that provide the necessary computation aids for these filters and information about the delay. One book, which is by Anatol I. Zverev [2], will be mentioned herein several times and is really an absolute must for the library of any design engineer who handles radio frequency (RF) and filter design.

The phase shift of the equivalent low-pass filter of the IF filter is

$$\theta_{\text{low pass}} = \arctan \frac{G_1(f_m)\sin\theta(f_m) - G_1(-f_m)\sin\theta(-f_m)}{G_1(f_m)\cos\theta(f_m) - G_1(-f_m)\cos\theta(-f_m)} \tag{1-213}$$

In some cases, we will have to use loops with conversions, where the resulting IF filter is very narrow. The use of a crystal filter will introduce a group delay in addition to the phase shift. These delays have to be added to the block diagram and added or subtracted from the actual phase. Since this can be done fairly easily and has a substantial impact on the stability, it is recommended that the interested reader analyze such an example mathematically, where it is assumed that the loop bandwidth is 2 kHz, the IF bandwidth is 100 kHz, and the loop bandwidth is increased to 50 kHz. We also have to take into consideration the effect of the phase shift of the low-pass filter equivalent of the bandpass filter. As the output signal from the mixer is passing the IF filter, which will be assumed to be symmetrical, the amplitude of the carrier G_1 (f_m) will change relative to the input signal. The losses of the filter and the sidebands will be shifted in phase equal to the phase shift generated by the filter. As is known from the literature, it is possible to convert the bandpass performance of this filter into an equivalent low-pass filter and deal with it. These details and examples are beyond the scope of this book and should be studied in the literature, such as in the book by Zverev already mentioned.

There are a number of unpleasant effects in addition to the one mentioned, such as ringing, as a result of non-equalized group delay, and if the IF filter bandpass is not symmetrical relative to the carrier frequency, AM-to-FM conversion occurs and has to be calculated. These special effects are an interesting topic, and the reader not only should be made aware of them but is also encouraged to calculate some numerical examples. In the rest of the book, we will assume that we know how to deal with these effects. The result of the calculations will be that a higher phase margin than the 45° recommended for higher-order loops has to be allowed to compensate for the additional delay. As a result of this higher phase margin, the settling time of the loop will become larger. In analyzing loops and in determining what frequency arrangements to use, one has to be aware of these trade-offs and optimize the loop by calculating a number of examples and finding the best solution by iteration.

The next effect we will analyze is the number of spurious signals introduced by the mixer. The double-balanced mixer, the best for such application, is still a highly nonlinear device that generates harmonics of the two frequencies applied, and those frequencies will mix with each other, resulting in a wide spectrum at the output. To keep the number of unwanted frequencies at the output at an acceptable level, we should observe two design rules:

(1) To obtain an IF, the two input frequencies should be as high and as close together as possible; the lower image is then used. A fairly simple low-pass filter at the output minimizes the possibility of feed-through and unwanted products.

(2) The power ratio between the RF and the LO should meet certain requirements. A design engineer is well advised to have about a 30-dB difference in level. Let us assume that the LO drive is +17 dB, a typical drive level for a medium-level double-balanced mixer; the RF input should then be −13 dBm or less. A further reduction in RF input may have the disadvantage of requiring too many amplifiers following at the output of the mixer and therefore generating additional noise from the post-amplifiers.

In cases such as that of our previous example, where we are mixing a fixed frequency of 140 MHz with a 144- to 148-MHz band, this requirement may be relaxed, and a drive level of 5 or 6 dBm may still be permissible. A decision on this matter depends on the particular case, and the best way of solving it is to take measurements in an actual circuit.

A spectrum analyzer connected at the output of the mixer operating at the range of interest with enough dynamic range should provide the necessary information. If these theoretical guidelines are followed, the design should be fairly trouble-free.

In Chapter 6 you will find several examples where double-balanced mixers are incorporated and IF frequencies inside the synthesizer are being used. In many cases, we have provided level information, and the particular synthesizers shown are spurious-free, at least 90 dB down relative to the carrier.

1-10 ACQUISITION

In order to understand the acquisition performance of the digital PLL, we must first look at the linearized model. As mentioned previously, we have several ranges in which the loop can operate, and Figure 1-17 shows a plot of these

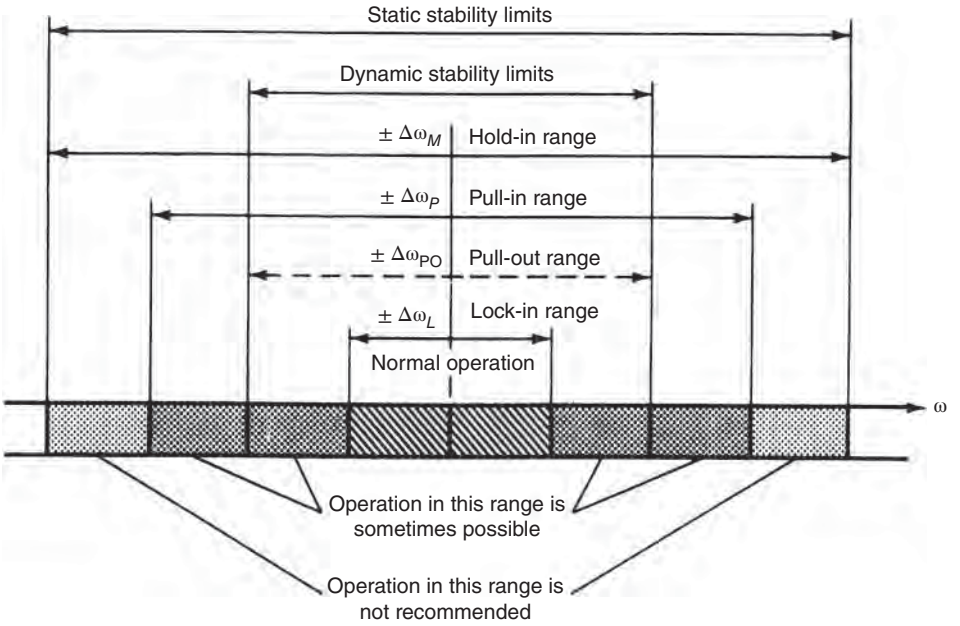


Figure 1-17 Possible operating ranges of a PLL.

ranges. The closest range around the center is the normal operating range and also the capture range, frequently called the *lock-in range*. Once a PLL has acquired lock, it maintains the locked condition within the hold-in range, and the borderline between the hold-in range and instability is fairly narrow. From our previous calculation and Laplace transform, applying

$$\theta_1(s) = \frac{\Delta\omega}{s^2} \tag{1-214}$$

to the input of the PLL, we can determine the maximum error using the final value theorem,

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\,\theta_e(s) = \frac{\Delta\omega}{K_o K_\theta f(o)} \tag{1-215}$$

With the assumption $\theta \approx \sin\theta$, the maximum amount this can be is 1 and therefore

$$\Delta\omega_H = K_o K_\theta F(o) \tag{1-216}$$

For the active filter $F(o)$ is infinite and therefore

$$\Delta\theta_H = \infty \tag{1-217}$$

and for the passive filter $F(o) = 1$ and

$$\Delta\omega_H = K_o K_\theta = \langle\langle \text{loop gain} \rangle\rangle \tag{1-218}$$

We have just calculated the hold-in range of the analog linear PLL. It is apparent that the use of an active loop filter guarantees a wider hold-in range.

Now let us go back and assume that the loop has not yet acquired lock. In the beginning we have two different frequencies applied to the phase detector. It is important to understand that, as the loop will acquire lock, we have

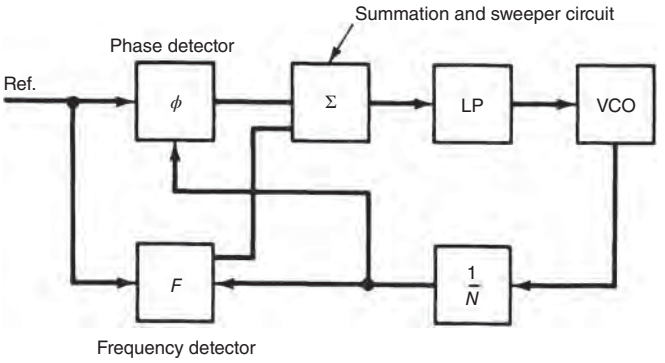


Figure 1-18 Block diagram of a PLL using a phase detector and frequency detector for acquisition aids in addition to the sweeper circuit.

to deal with two different ranges. One is the area in which we acquire frequency lock, and only after frequency lock has been accomplished can phase lock occur. There are several requirements necessary to make frequency lock possible.

(1) The tuning range of the VCO has to be wide enough to cover the desired range of operation.
(2) The VCO itself has to be able to oscillate through this required range without disruption of oscillation, a jump phenomenon frequently called "discontinuities."
(3) The tuning diodes have to be operated in a range where they do not become conductive (see Chapter 4) since leakage current from the diodes into the phase detector causes difficulty.
(4) Depending on the phase detector used, we either have a pull-in phenomenon, which we will discuss later, or sweeping, where the generated beat note at the output will sweep the oscillator from one end of the range to the other as an aid to acquire lock. In some instances, especially with pure phase detectors, an external frequency lock device may be necessary.

Figure 1-18 shows the two popular techniques used to help obtain frequency lock. The first one is the use of an additional frequency comparator, and an electronic device switches over from this to the phase detector. This technique is also used in the Philips HEF4750/51 large-scale integration (LSI) PLL integrated circuits. To obtain frequency lock, we first use a digital tri-state phase/frequency comparator that has a dead zone in the middle of its operating range where it is locked, and the system then switches over to a sample/hold comparator offering low-noise operation.

Another technique used in the past is an external sweeping device. Figure 1-19 shows the schematic of such an arrangement. We find a phase detector that operates into an NPN transistor. The loop filter is at the output of the phase detector, and the gain of the following dc amplifier is defined as the ratio of R_L/R_E.

A unijunction, or double-base transistor, is used to generate a sweeping signal. As the dc output voltage from this circuit reaches a certain level, the unijunction transistor ignites and starts its sweeping action. The frequency of oscillation of this circuit can be determined with the equation

$$f = \frac{1}{R_T C_T \log 2} \tag{1-219}$$

Note that R_T has to be derived from adding $R_{T1} + R_{T2} + R_{T3}$ in the starting condition, whereby we can assume that the amplifier draws no current. For the values taken here, we obtain a frequency of

$$f = \frac{1}{(18\,\text{k}\Omega + 10\,\text{k}\Omega + 220\,\Omega)10^{-6} \log 2} = 118\,\text{Hz}$$

The circuit will be swept with this particular frequency.

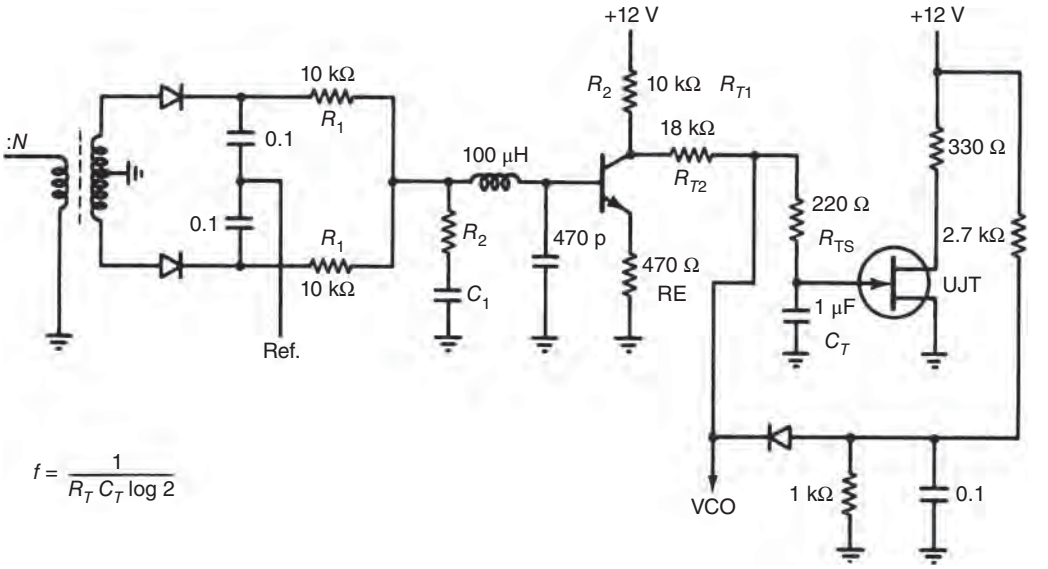


Figure 1-19 Schematic of the phase detector section of a PLL including a dc amplifier and a sweeping circuit.

We must now remember that there is a maximum frequency with which we can sweep the circuit to acquire lock. This is called the *pull-out range*. Pull-out range, defined $\Delta\omega_{PO}$, is determined by the equation

$$\Delta\omega_{PO} = 1.8\,\omega_n(\zeta + 1) \tag{1-220}$$

which is an approximation that can be applied in most cases. In our particular case with the unijunction transistor, the maximum sweep rate for $\zeta = 0.7$ and $\omega_{PO} = 118\,(2\pi)$ results in 38 Hz for the loop frequency ω_n.

However, our system is currently not yet in lock; we still have to calculate the lock-in range. A similar formula can be found as a function of the type of filter. For the simple *RC* filter with no phase compensation, as shown previously, the lock-in range is

$$\Delta\omega_L \approx \omega_n \tag{1-221}$$

and for the filter with phase compensation

$$\Delta\omega_L = 2\zeta\omega_n \tag{1-222}$$

We are interested in determining how long it takes to acquire lock. The following relation gives a good approximation of the lock-in time:

$$T_L \approx \frac{1}{\omega_n} \tag{1-223}$$

This is valid for all type 2 second-order linear PLLs. The calculation that we have just made referred to the phase lock. It becomes apparent from these equations that for $\zeta = 0.7$, the lock-in range is only equal to or slightly larger than the loop bandwidth. To move the VCO frequency within these limits, additional functions are required. This area is called *frequency lock*. We are now dealing with the pull-in range.

The pull-in range is the first range we have to deal with, as the PLL is about to acquire frequency, and later, phase lock. The explanation given here is somewhat backward, but it is easier to understand if one considers the ranges in this sequence, as the equations indicate the limitations. Pull-in is probably best understood by remembering that the system starts off with an offset in frequencies, and therefore a beat note appears at the output of the phase detector and of the loop filter. In the schematic using the sweeping technique shown previously, the loop bandwidth remains

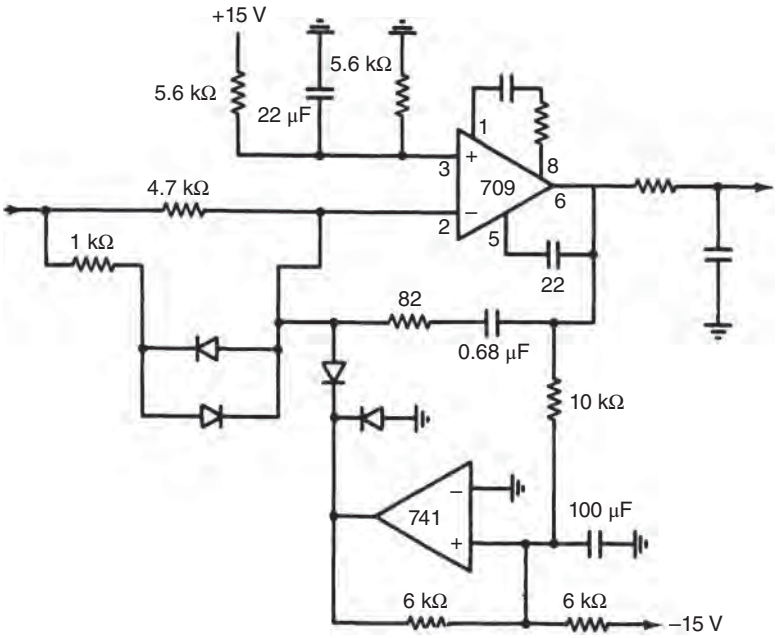


Figure 1-20 Schematic of a loop filter/integrator where the time constant is changed with the help of antiparallel diodes in the loop.

constant. Another way of helping the loop to acquire frequency lock is to widen the bandwidth of the loop filter, enabling phase lock with a larger frequency offset.

Figure 1-20 shows the schematic of a dual-time-constant loop filter, which can be used to explain the pull-in effect. Let us assume that initially we have a difference of several kilohertz between the two frequencies at the phase detector and are currently not considering the effect of a frequency divider.

The beat note generated at the output of the phase detector is an ac voltage together with a dc component. We also have to assume that in the initial condition the beat note is much larger in frequency than the bandwidth of the loop filter. As the output voltage of the loop filter sweeps the oscillator to either a higher or lower frequency, we have to see what the magnitude of the beat note as a function of sweeping is doing. It turns out that the difference in frequency becomes smaller if the VCO is swept toward higher values and becomes larger if the VCO is swept toward smaller frequency values. The output sweep frequency or beat note, therefore, is nonlinear and nonharmonic, and the average frequency at the output is no longer zero. The loop filter acting as an integrator will average the sweep.

The mathematical model for this pull-in is somewhat complicated. The *pull-in time*, defined as the time required for the average frequency error to decay from the initial condition to the locked limit, is

$$T_P = \frac{(\Delta\omega)^2 \tau_2}{K^2} = \frac{(\Delta\omega)^2}{2\zeta\omega_n^3} \tag{1-224}$$

This formula is valid only for the linear type 2 second-order loop. A model for the digital PLL will follow.

Example 1

Let us assume that our initial frequency offset is 1 MHz and that the loop bandwidth ω_n is 10 Hz. The time it requires for the pull-in range is

$$T_P = \frac{(2\pi \times 10^6)^2}{2\zeta(2\pi \times 10)^3} = 113.68 \times 10^6 \text{ s}$$

or 3.6 years. If we use the system that automatically increases the loop bandwidth with the two antiparallel diodes as previously shown, which results in a new loop bandwidth of 10 kHz prior to lock, the formula changes to

$$T_P = \frac{(2\pi \times 10^6)^2}{2\zeta(2\pi \times 10^4)^3} = 0.113 \text{ s}$$

The difference between both is dramatic, and with the simple trick of changing the loop bandwidth, we have speeded up the pull-in substantially.

Immediately after frequency lock has occurred, the switching diodes are no longer conductive. The remaining phase offset is handled by the lock-in function and the time it will now take to phase-lock the loop:

$$T_L = \frac{1}{\omega_n} = \frac{1}{10\,(2\pi)} = 16 \text{ ms}$$

The time required for phase lock, therefore, is much smaller than the time required for frequency lock, and the total lock time would be 0.1296 s.

Lock-in performance of the digital PLL system that uses a tri-state digital phase/frequency comparator as shown in Chapter 4 can no longer be calculated using the linearized model as is frequently done in the literature. The output of the tri-state phase/frequency comparator behaves totally different from the linearized models.

We have to take a look at two different examples. First, we will look at a tri-state phase/frequency comparator where the loop filter is placed after the summation stage, and Motorola CD4046 fits this description. When the system is switched on, first the two pulses that are combined through the CMOS switches will jam the output voltage up to the power supply voltage and the loop filter will delay this action, depending on the integration time constant. The dc voltage to the VCO, therefore, will slowly rise, the VCO will be swept, and pull-in will be accomplished.

It turns out that this particular example practically behaves as the linear analog phase detector version.

Now let us consider a phase/frequency comparator equal to the MC4044, which has two outputs, where pulses are available to charge or discharge a capacitor.

If the loop filter combination shown in Figure 1-21 is used, whereby each output of the phase/frequency comparator is applied to one input of an operational amplifier provided that the amplifier is fast enough to follow the input frequency, we now have to analyze the statistical average and determine from there what the output of the operational amplifier is showing.

The following mathematical mode, to the best of our knowledge, is the only one that ever assessed this effect correctly and was published by Roland Best in his book *Theory and Application of Phase-Locked Loops* [1]. The following discussion is published here with Dr. Best's permission.

1-10-1 Pull-in Performance of the Digital Loop

In the beginning of this chapter, when we were discussing the differences between the analog and digital PLL, we started with the digital phase/frequency comparators. The flip-flop-based digital phase/frequency comparators work on the principle that they analyze the rising edges of the input signals, edge-triggered flip-flops, and are insensitive to the duty cycle.

The output can be used to charge or discharge a capacitor and has to be combined with an active filter to take full advantage of its capabilities. Figure 1-21 showed the typical arrangement using this type of phase/frequency comparator.

Initially, when the loop is not in lock, we can assume that frequencies f_1 and f_2 have a random relation to each other, the phase of one to the other is random, and the next edge of the following signal within the time interval $0 \le t \le T$ can occur with the same probability in any given time. We define $w(t)dt$ as the probability that the next rising edge of the signal f_2 will occur in the time $t \cdot \cdot \cdot t + dt$. Therefore, we can write

$$w(t) = \frac{1}{T^2} \quad (t \le T_2) \tag{1-225}$$

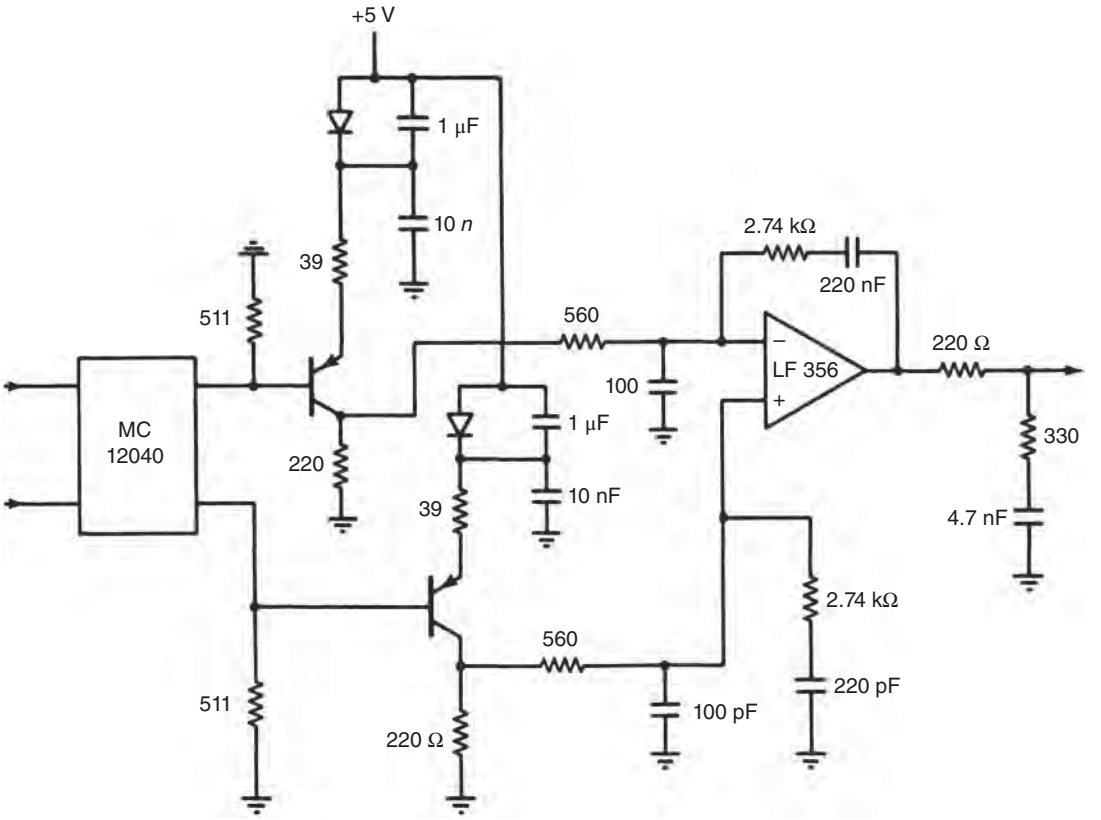


Figure 1-21 Schematic of an ECL phase/frequency comparator driving a high-frequency operational amplifier. The outputs to the inverting and noninverting input of the operational amplifiers are pulses, which are charging and discharging the loop capacitor of 220 nF. Note the additional output filter following the operational amplifier.

$$w(t) = 0 \quad (t > T_2) \tag{1-226}$$

We now may have two principal cases:

(1) f_2 is smaller than f_1 or $T_2 > T_1 = 1/f_1$, and the negative edge will occur: *case 1*, in the time interval $0 \le t \le T_1$; *case* 2, in the time interval $T_1 \le t \le T_2$.
(2) In the case of f_1 being smaller than f_2, these conditions are reversed.

As the output signal of the phase/frequency comparator is a chain of pulses that are combined, the duty cycle $\delta(t)$ will change. The average duty cycle $\bar{\delta}$, according to probability theory, can be determined from

$$\bar{\delta} = \int_0^{T_2} w(t)\delta(t)dt \tag{1-227}$$

The integration of this can be done in two steps:

$$\bar{\delta} = \int_0^{T_1} w(t)\frac{t}{T_1}dt + \int_{T_1}^{T_2} w(t)\frac{t}{2T_1}dt \tag{1-228}$$

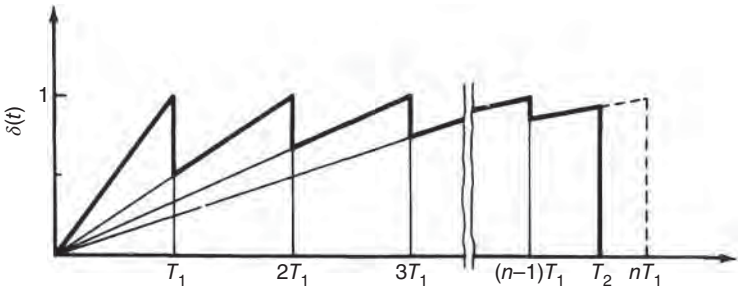


Figure 1-22 Change of duty cycle $\Delta(t)$ as a function of T.

with

$$\delta(t) = \frac{t}{T_1} \quad \text{and} \quad \frac{t}{2T_1}$$

depending on the time area, as discussed previously.

In reality, the time interval is not going to lie between T_1 and $2T_1$ but can be between T_1 and ∞. Therefore, our average duty cycle has to be written in the form of several integrals and

$$\bar{\delta} = \int_0^{T_1} w(t)\frac{1}{T_1}dt + \int_1^{T_1} w(t)\frac{1}{2T_1}dt + \cdots + \int_{T_1}^{T_2} w(t)\frac{1}{nT_1}dt \tag{1-229}$$

This can be converted into the final equation based on $f_1 > f_2$, and we obtain

$$\bar{\delta} = \frac{f_2}{2f_1}n - \sum_{i=1}^{n}\frac{1}{i} + \frac{f_1}{2nf_2} \tag{1-230}$$

with $n = \text{Int}(f_1/f_2) + 1$. Figure 1-22 shows the duty cycle for any combinations of $n\tau_1$, and Figure 1-23 shows the average duty cycle $\bar{\delta}$ as a function of the frequency ratio f_2/f_1. The straight-line approximation in this curve can be used to simplify the formula, as the lock-in will occur for the case $f_1 = f_2$. We will then obtain for the average duty cycle

$$\bar{\delta} = \frac{f_1 - f_2}{f_1} = \frac{\omega_1 - \omega_2}{\omega_1} \tag{1-231}$$

In this case, the average output voltage is

$$\bar{v}_d = \bar{\delta}V_B = \frac{V_B}{\omega_o}(\omega_1 - \omega_2) \tag{1-232}$$

since

$$\bar{v}_d = K_d'(\omega_1 - \omega_2) \tag{1-233}$$

We finally obtain the previously used gain constant of the phase comparator of this particular type in the out-of-lock condition to be

$$K_d' \approx \frac{V_B}{\omega_o} \tag{1-234}$$

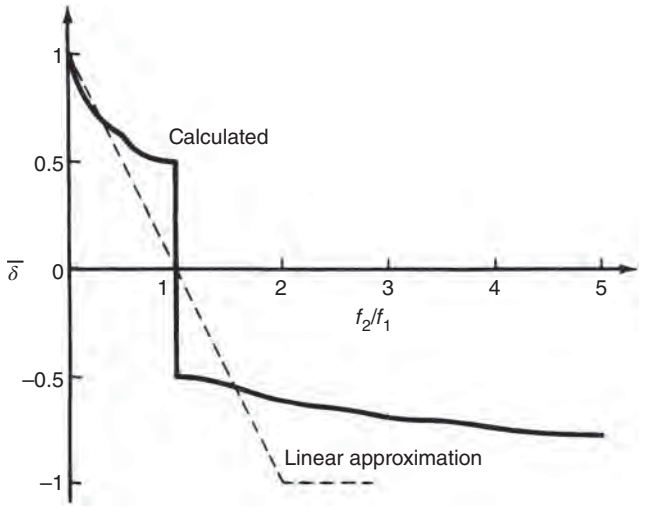


Figure 1-23 Average duty cycle $\bar{\delta}$ as a function of the frequency ratio f_2/f_1.

1-10-2 Coarse Steering of the VCO as an Acquisition Aid

We have learned so far that we can use a frequency detector or a sweep oscillator to steer or sweep the oscillator close to its final frequency.

In the case of sweeping, we have to make sure that the sweeping speed is not too fast, because if it is, the oscillator will never acquire lock or it will skip cycles several times before its acquires lock. The phenomenon of cycle skipping is explained in Gardner's book [5], but generally not enough information is available about the particular loop to take full advantage of the theoretical evaluation.

Once the transfer characteristic of the VCO is known, it is possible to use a read-only memory (ROM) that receives frequency information and, with the help of a digital-to-analog (D/A) converter within very fine resolution, to coarse steer the oscillator toward its desired final frequency. This method avoids the necessity of the additional external frequency comparator and the sweeping technique. The drawback is that if diodes are changed or the characteristic of the tuning diode as a function of age changes, the lookup table will become incorrect. This is true for extremely fine resolution. Let us assume the case where we have an oscillator operating from 70 to 80 MHz, which we want to coarse steer. If we assume for a moment that the tuning diodes do not produce additional noise or that, under certain circumstances, the additional noise contribution of the coarse-steering tuning diodes can be neglected, it is possible to take an 8-bit D/A converter, as shown in Figure 1-24, that is getting its frequency information from the binary-coded decimal (BCD) commands to the frequency divider, and generate within 100-kHz resolution an output that can be used to coarse steer the tuning diodes. Now the tuning diodes responsible for the fine tuning only have to work over a fairly narrow range, and as a result of this, the VCO gain is very small.

The output impedance of the D/A converter can be made very low, and because the coarse-tuning diodes are being driven from a low-impedance point rather than the typical high impedance the dc control line has, there is no pickup on the coarse-steering line from hum of any significant amount. As the fine-control loop now has a voltage gain of 30–100 kHz/V at most, the pickup is reduced by at least 20 dB, if not more. Therefore, the amount of spurious signal because of pickup and hum is reduced by the same amount.

This technique has the advantage also that the loop gain for this narrow window remains fairly constant, regardless of the VCO's curvature, as the transfer characteristic in this narrow window does not change very much.

The D/A converter has to generate a dc voltage that is not only nonlinear but rather is the opposite of the transfer characteristic of the tuning diodes used for the wide tuning range. A larger voltage swing will be needed at the higher frequency, whereas less voltage is required at the low end of the VCO. A practical schematic where this technique is used is given in Chapter 6.

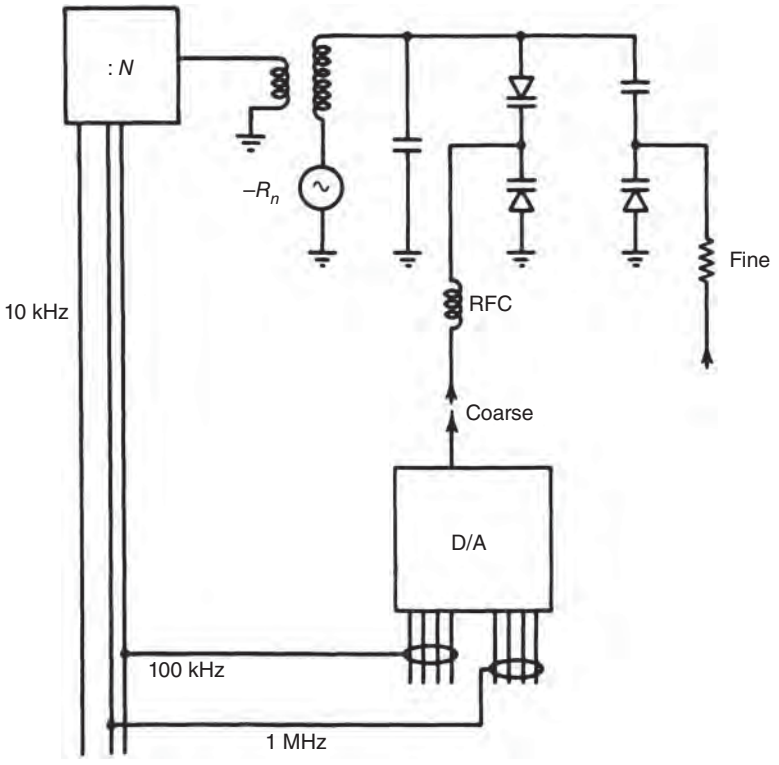


Figure 1-24 VCO coarse steering using a D/A converter.

In dealing with mixers, we have learned that one of the drawbacks of a heterodyne loop is that the open-loop gain changes more dramatically as the division ratio required becomes much larger. A typical loop without a heterodyne technique may have 30% or 40% variation of loop gain due to change of N, and we have seen cases where the division factor N, as a result of heterodyne technique, has changed by 20:1. How do we cope with this problem? The best way of handling this is either to use a coarse-steering technique with either tuning diodes or switching diodes and allow a very narrow window in which the oscillator will operate or change the loop filter dc control gain. Figure 1-25 shows an arrangement where, depending on the frequency setting of the dividers, several CMOS switches change the dc loop gain following the loop filter and, therefore, linearize the loop. The introduction of this amplifier after the loop filter has the drawback that the noise is no longer limited by a following filter, or if such an RC low-pass filter is used after the amplifier, the technique of analyzing high-order loops has to be used, and inside the loop bandwidth, we still find the additional noise contribution.

This approach is typically used in wideband loops where the output oscillator operates from 200 to 300 MHz, as an example, and the reference frequency is between 100 kHz and several megahertz. The loop gain, because of the small division ratio, is fairly high, while the loop gain variation due to some heterodyning may also be very high. In an effort to linearize, either the operational amplifiers are offset with a dc control voltage, or the loop filter is modified with additional capacitors in parallel, or a dc amplifier following the loop filter is used, which changes the dc gain. In some instances, all three techniques are used simultaneously, and it becomes very tricky to avoid additional noise being brought into the loop and to make all systems track without difficulty. Figure 1-26 shows a combination of all these techniques. Table 1-4 shows the most important formulas for digital PLLs. See also [3] and [4].

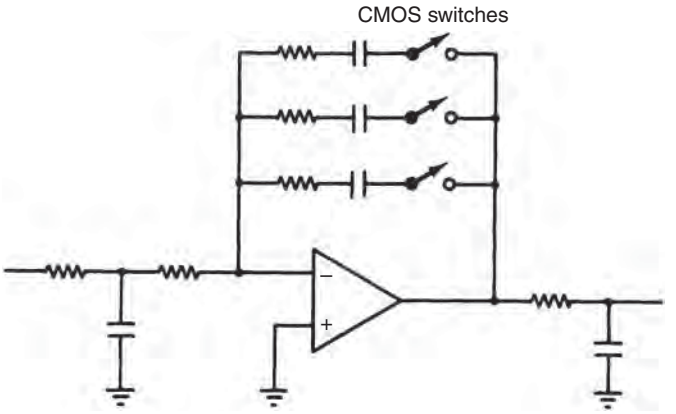


Figure 1-25 Linearizing of loop gain by changing loop components.

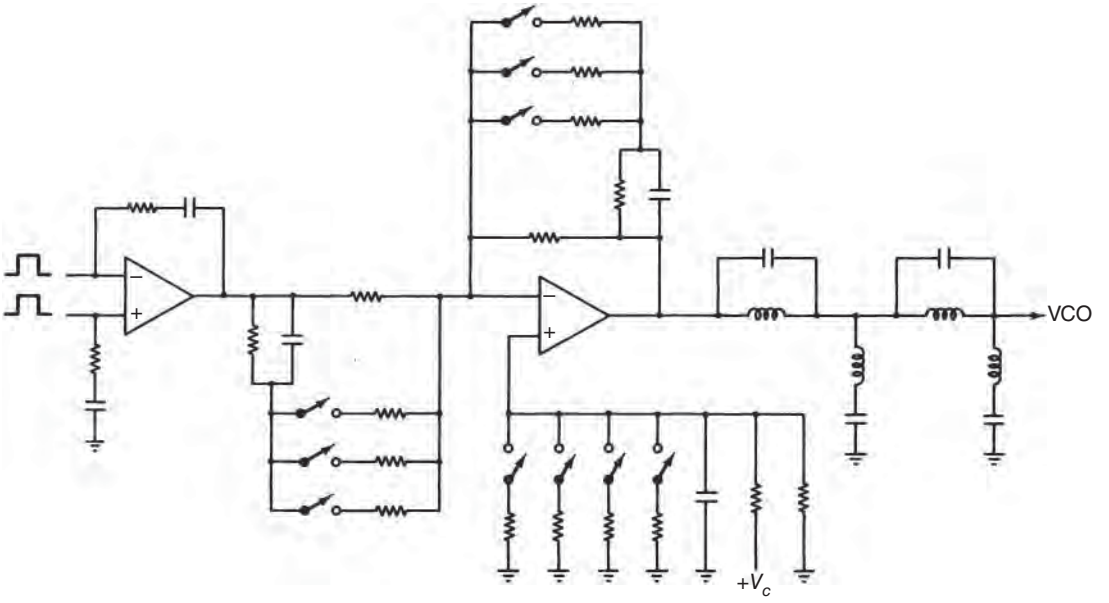


Figure 1-26 Circuit diagram of the loop filter dc amplifier arrangement of a PLL, where the loop gain and dc offset are controlled by CMOS switches to linearize and coarse steer the VCO.

1-10-3 Loop Stability

The easiest way to analyze the loop stability is to plot the magnitude and phase of the open-loop transfer function $K_v F(s)/s$ as a function of frequency. First, consider the case where $F(s)$ is a simple low-pass filter described by Eq. (1-27). For this case the open-loop frequency response is

$$K_v G(j\omega) = \frac{K_v}{j\omega(j\omega\tau + 1)} \tag{1-235}$$

Table 1-4 Most important formulas for digital PLLs (second-order only)

	Exclusive-OR gate		Edge-triggered JK master/slave flip-flop	
Phase/frequency comparator	Active filter	Passive filter	Active filter	Passive filter
Hold-in range	$\Delta\omega_H \to \infty$	$\Delta\omega_H = \frac{\pi}{2}\frac{K_o K_d}{N}$	$\Delta\omega_H \to \infty$	$\Delta\omega_H = \pi\frac{K_o K_d}{N}$
Capture range				
$\tau_2 \neq 0$	$\Delta\omega_L \approx \pi\zeta\omega_n$		$\Delta\omega_L \approx 2\pi\zeta\omega_n$	
$\tau_2 = 0$	$\Delta\omega_L \approx \frac{\pi}{\sqrt{8}}\omega_n$		$\Delta\omega_L \approx \frac{\pi}{\sqrt{3}}\omega_n$	
Pull-in range	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_n K_o K_d}{N}}$	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_n K_o K_d}{N} - \omega_n^2}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_n K_o K_d}{N}}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_n K_o K_d}{N} - \omega_n^2}$
Pull-in time	$T_P \approx \frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$		$T_P \approx \frac{\Delta\omega_o^2}{\pi^2\zeta\omega_n^3}$	
Pull-out range				
$\zeta < 1$	$\Delta\omega_{PO} \approx 1.8\,\omega_n(\zeta + 1)$		$\Delta\omega_{PO} = \pi\,\omega_n \exp\left(\frac{\zeta}{\sqrt{1-\zeta^2}}\arctan\frac{\sqrt{1-\zeta^2}}{\zeta}\right)$	
$\zeta > 1$			$\Delta\omega_{PO} = \pi\,\omega_n \exp\left(\frac{\zeta}{\sqrt{\zeta^2-1}}\arctan\frac{\sqrt{\zeta^2-1}}{\zeta}\right)$	

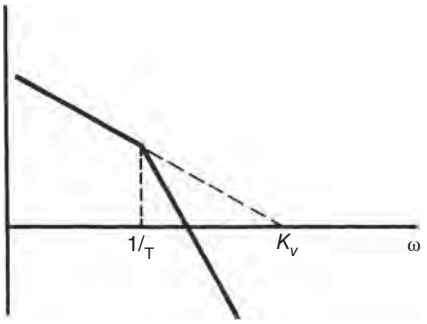


Figure 1-27 Magnitude of the open-loop gain of a PLL system.

The straight-line approximation of the magnitude of this open-loop transfer function is plotted in Figure 1-27. The magnitude of the response decreases at the rate of 6 dB/octave until the frequency is equal to the −3-dB frequency of the low-pass filter (1/2); for higher frequencies the magnitude decreases at a rate of −12 dB/octave.

Several rules of thumb, developed by Bode for feedback amplifiers, are useful in selecting the loop parameters. The first has to do with selecting the filter bandwidth $\omega_L = 1/\tau$. The approximation is: If the open-loop frequency response crosses the 0-dB line with a slope of −6 dB/octave, the system is stable; if the slope is −12 dB/octave or greater, the system is unstable. The second-order system under consideration is inherently stable, but the model is an approximation to a higher-order system. If the open-loop second-order model crosses the 0-dB line at −12 dB/octave, there is little room left for error. Additional phase shift from the VCO or phase detector could cause the loop to go unstable.

To have the open-loop gain cross the 0-dB line at −6 dB/octave, it is necessary that $\omega_L > K_v$. The larger ω_L is, the better will be the loop stability. From the filtering viewpoint, the smaller ω_L, the smaller the loop bandwidth and the less noise that will reach the VCO. K_v should be as small as possible to minimize the bandwidth. The larger the K_v, the smaller the steady-state error and the faster the loop response. Hence, in PLL design, compromises among noise performance, loop stability, steady-state error, and transient performance must be made.

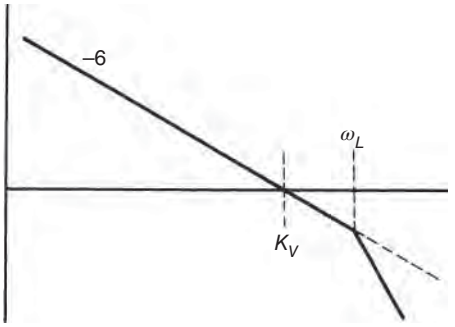


Figure 1-28 Open-loop frequency response in the case $\omega_L = K_v$.

Another rule of thumb that is helpful in PLL design is that the frequency ω_c at which the magnitude of the open-loop transfer function is unity,

$$\frac{K_v F(j\omega)}{j\omega_c} = 1 \tag{1-236}$$

is approximately the closed-loop 3-dB bandwidth. This relation is exact for the case where $F(j\omega) =$ constant.

If $F(s)$ is a simple low-pass filter response and $\omega_L > K_v$, the open-loop frequency response will be as shown in Figure 1-28. In this case, the loop bandwidth is approximately equal to K_v.

If $\omega_L < K_v$, the straight-line approximation will cross the 0-dB line with a slope of -12 dB/octave, which is not good from the standpoint of loop stability. Thus the filter bandwidth should be greater than the open-loop crossover frequency ω_c; ω_c will be approximately equal to the closed-loop bandwidth. Therefore, the filter bandwidth, for good loop stability, should be greater than the loop bandwidth for the simple type 1 system under discussion.

Another parameter that is useful in evaluating the response of second-order and higher systems is the phase margin, which is defined as

$$180^\circ + \arg KG(j\omega_c) \tag{1-237}$$

That is, the phase margin is equal to 180° plus the phase shift of the open-loop gain (a negative number) at the open-loop crossover frequency ω_c. The greater the phase margin, the more stable the system and the more phase lag from parasitic effects that can be tolerated.

Example 2

Consider a PLL that has $K_v = 10$ rad/s and that contains a low-pass filter with a corner frequency of 20 rad/s. The magnitude and phase of the open-loop transfer function are plotted in Figure 1-29. The system crossover frequency is approximately 10 rad/s. At this frequency, the phase shift of the open-loop transfer function is $-112.5°$, so the phase margin is 67.5°.

In this example, the complete phase plot was presented, but once one is familiar with phase plots, they no longer need to be included. One can simply calculate the phase shift after determining the open-loop crossover frequency from the magnitude plot.

Example 3

In Example 2, if the filter corner frequency had been 2 rad/s rather than 20 rad/s, what would have been the system phase margin?

Solution: To determine the phase margin, first plot the magnitude of the open-loop gain and determine the crossover frequency. The straight-line approximation of the magnitude is plotted in Figure 1-30. ω_c is found to be

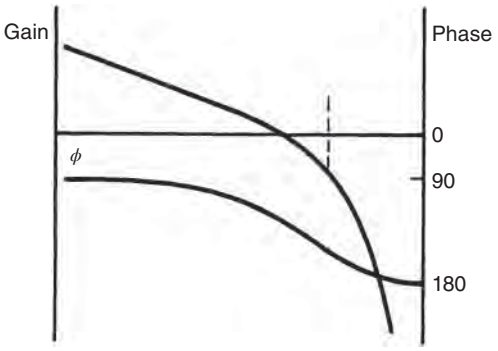


Figure 1-29 Magnitude and phase of the open-loop transfer function for $K_v = 19$ rad/s and $\omega_L = 20$ rad/s.

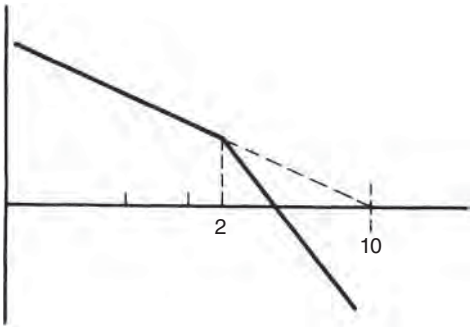


Figure 1-30 Magnitude of the open-loop gain of Example 3.

approximately 4.4 rad/s. Thus, the system phase margin is

$$180^\circ - (90^\circ + \arctan 2.2) = 23.40^\circ$$

which is too small for good loop stability. This is in agreement with the rule of thumb, which states that if the magnitude of the open-loop response described crosses the 0-dB line with a slope of -12 dB/octave, the system is unstable. In this example, the straight-line approximation for the gain decreases at -12 dB/octave, but the actual response crosses the 0-dB line with a slope slightly more positive than -12 dB/octave: hence, the small phase margin.

Although the most important frequency-domain design parameters are the closed-loop bandwidth ω_h and the peak value M_P of the closed-loop frequency response, no design techniques exist that allow easy specification of B and M_P. It is relatively easy to design for specified open-loop parameters ω_c and ϕ_m. There are approximations that relate ω_c and ϕ_m to ω_n, M_P, and ζ, and thus to the system rise time and overshoot. Fortunately, the conditions under which these approximations are valid are satisfied by most PLLs.

For the open-loop system (second-order loop),

$$K_v G(s) = \frac{K_v}{s(s/\omega_L + 1)} \tag{1-238}$$

Used with unity feedback, the closed-loop transfer function is given by Eq. (1-28), with

$$\omega_n^2 = K_v \omega_L \tag{1-239}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_L}{K_v}} \tag{1-240}$$

The open-loop unity gain frequency is easily shown to be

$$\omega_c = \omega_L \left[\frac{\sqrt{1 + 4(K_v/\omega_L)^2} - 1}{2} \right]^{1/2} \tag{1-241}$$

Once ω_c is known, the phase margin

$$\phi_m = 90^\circ - \arctan \frac{\omega_c}{\omega_L} = 90^\circ - \arctan \left[\frac{\sqrt{1 + (1/2\zeta)^2} - 1}{2} \right]^{1/2} \tag{1-242}$$

can be calculated. This equation is plotted in Figure 1-31. The closed-loop system parameters of most importance are adequate stability (which is related to phase margin), system bandwidth (which determines the speed of the transient response), and system transient response (rise time and overshoot). For a low-pass transfer function, the bandwidth ω_n is defined as the frequency at which the gain is equal to 0.707 of its dc value. The bandwidth of the system represented by Eq. (1-28) is

$$\omega_h = \omega_n(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4})^{1/2} \tag{1-243}$$

which can be calculated using Eqs. (1-35), (1-239), and (1-240). For the underdamped second-order system given by Eq. (1-28) ($\zeta < 1$), the peak value of the time response to a unit step input can be shown to be

$$P_o = 1 + e^{-n\,\zeta/\sqrt{1-\zeta^2}} \tag{1-244}$$

The overshoot is determined solely by ζ. P_o as a function of ζ is plotted in Figure 1-32.

For high-order systems, the overshoot and bandwidth are not readily related to the open-loop system parameters, but a good first approximation is that Eq. (1-241) holds for higher-order systems. It is relatively easy to design a system to have a given phase margin. A design can then be evaluated using computer simulation. If the simulation indicates that the overshoot is too high (or too low), the phase margin can be increased (reduced), but the relations among phase margin, damping, and overshoot are amazingly accurate for higher-order systems. This implies that the response of most feedback systems can be described by a second-order model. Also, the closed-loop bandwidth can be related to the open-loop crossover frequency ω_c and the damping ratio, but it usually suffices to use the rule of thumb that the closed-loop bandwidth of underdamped systems is approximately 50% greater than the open-loop crossover frequency ω_c.

If it is desired to design for a peak transient overshoot, Eq. (1-240) can be used to determine the damping and then Eq. (1-241) is used to determine the required phase margin.

Example 4

For the PLL with open-loop transfer function

$$\frac{K_v}{s(s/\omega_L + 1)}$$

($K_v = 1000$), determine the low-pass filter corner frequency ω_L so that the system peak overshoot in response to a step input will be less than 20%.

Solution: Equation (1-242) or Figure 1-32 indicates that for $P_o < 1.2$, the damping ratio ζ must be greater than 0.45. For a ζ of 0.45, the corresponding phase margin is found [using Eq. (1-242)] to be about 50.

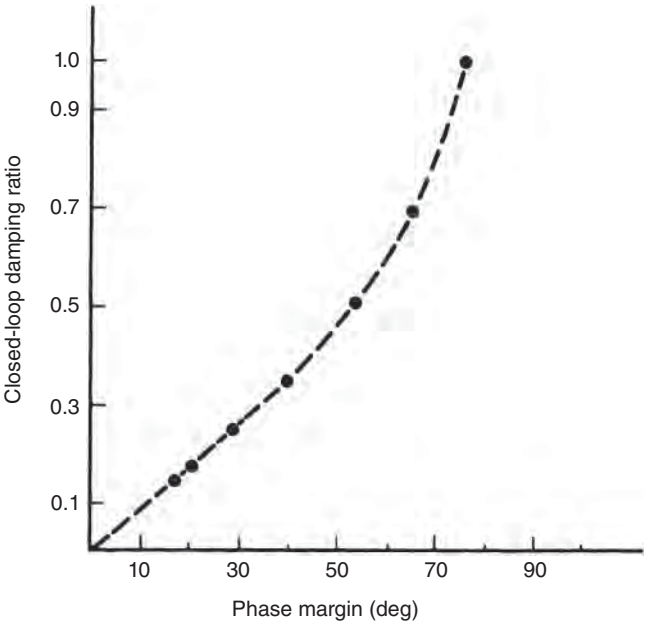


Figure 1-31 Closed-circuit damping ratio and phase margin relationship.

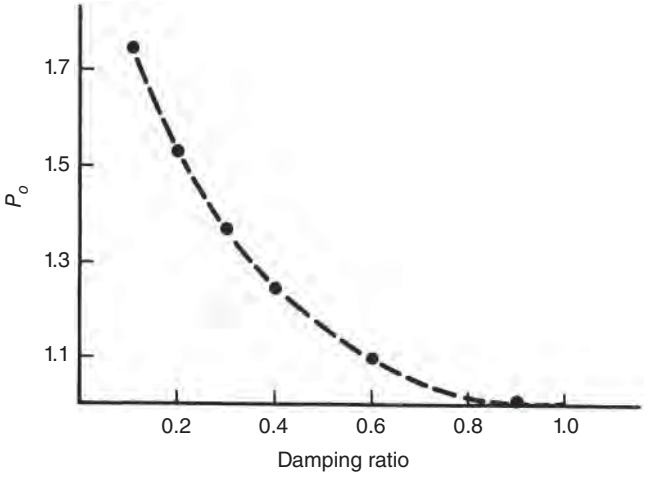


Figure 1-32 Peak overshoot as a function of damping ratio.

The low-pass filter can contribute −40° phase lag 1 and the phase margin will be equal to 50%. Therefore, ω_L must be greater than ω_c (if $\omega_L = \omega_c$, the phase margin would be 45°), so ω_c is approximately 1000 rad/s = K_v. Thus, arctan $1000/\omega_L = 40°$ or $\omega_L = 1192$. (This is somewhat of an approximation, since adding the low-pass filter will slightly reduce the crossover frequency.) The desired open-loop transfer function becomes

$$\frac{1000}{s\left(\frac{s}{1.10\times10^3}+1\right)} = KG(s) \tag{1-245}$$

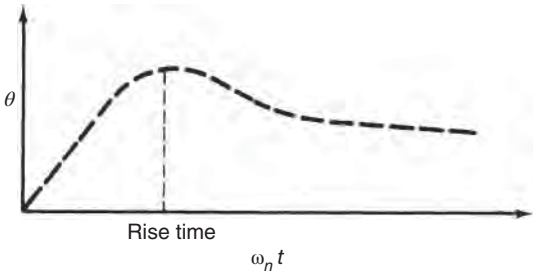


Figure 1-33 Overshoot and rise time of our example.

The step response is plotted in Figure 1-33. The overshoot is 13% and the rise time is 2.1 ms. The overshoot is considerably less than the specified maximum of 20% because of the straight-line approximations used to estimate the gain and crossover frequency. Note that this second-order system is simple enough to be solved analytically since

$$\frac{K_v G}{1 + K_v G} = \frac{1}{(s^2/1000\omega_L) + (s/1000) + 1} = \frac{1}{(s^2/\omega_n^2) + (2\,\zeta s/\omega_n) + 1}$$

where $\omega_n^2 = 1000\omega_L$ and $2\zeta/\omega_n = 1/1000$, or

$$\zeta = \frac{\omega_n}{2000} = \frac{\sqrt{1000\omega_L}}{2000}$$

For $\zeta = 0.45$ (the design value),

$$\omega_L = \frac{(900)^2}{1000} = 810$$

The straight-line approximations resulted in a 32% error in the calculation of the low-pass corner frequency and the overshoot was 13% rather than 20% (for $\omega_L = 810$, the rise time is 2.28 ms). The differences between the two methods could have been reduced by accounting for the fact that the pole of the low-pass filter reduces the crossover frequencies and thus increases the actual phase margin over that estimated with the straight-line approximation.

In some instances it is also necessary to specify the loop bandwidth. In order to control both the loop damping and bandwidth, an amplifier can be added in series with the low-pass filter. If the filter is implemented using active components, the additional gain can be obtained without any additional components.

Example 5

Consider Example 4 with the additional specification that the rise time in response to a unit step input be less than 1 ms. Since the overshoot is to be less than 20%, the phase margin must be approximately 50°. To design for the rise-time specification, it is easiest to use the approximation

$$t_r = \frac{2.2}{B}$$

which is exact only for first-order systems but provides a good design guideline for higher-order systems. Thus, ω_c should be greater than $2.2/t_r = 2.2 \times 10^3$ rad/s.

The previous discussion has shown that

$$\omega_c = K_\theta K_o K = 1000K$$

Thus, for $\omega_c = 2.2 \times 10^3$ rad/s, an additional amplifier with a gain $K = 2.2$ needs to be added. With the increased ω_c, ω_L will have to be increased from Example 4 in order to meet the phase margin specification. For the second-order systems under discussion,

$$\frac{2\zeta}{\omega_n} = \frac{1}{K_v} \tag{1-246}$$

The damping ζ is to be approximately 0.45 to meet the overshoot specification. It suffices to estimate the closed-loop bandwidth by assuming that it is approximately equal to ω_n, which is also approximately equal to the open-loop crossover frequency. Therefore, for $\zeta = 0.45$ and 1 ms rise time,

$$\omega_n = \frac{2.2}{10^{-3}} = 2.2 \times 10^{-3} = 2\,\zeta K_v = \sqrt{K_v \omega_L}$$

Therefore,

$$K_v = \frac{2.2 \times 10^3}{2 \times 0.45} = 2.44 \times 10^3$$

and

$$\omega_L = \frac{(2.2 \times 10^3)^2}{2.44 \times 10^3} = 1.98 \times 10^3$$

An additional gain K required is

$$K = 2.44$$

The complete open transfer function is then

$$K_v G(s) = \frac{2.44 \times 10^3}{s\left(\frac{s}{1.98 \times 10^3} + 1\right)}$$

and the closed-loop transfer function is

$$\frac{K_v G}{1 + K_v G} = \frac{1}{\frac{s^2}{(2.2 \times 10^2)^2} + \frac{s}{2.33 \times 10^3} + 1}$$

A plot of the step response is shown in Figure 1-34. The peak overshoot is 10% and the rise time is 0.7 ms. The two specifications are now met. In general, two adjustable parameters, such as loop gain and filter bandwidth, are needed to independently specify overshoot and rise time.

An operational amplifier circuit to realize the low-pass filter with a gain of 2.4 is shown in Figure 1-35. Since the feedback impedance is

$$Z_f = \frac{R_f}{R_f C_f s + 1} \tag{1-247}$$

the ideal voltage gain is

$$A_v = \frac{-Z_f}{Z_t} = \frac{-R_f / R_i}{R_f C_f s + 1} \tag{1-248}$$

which realizes the desired gain and filter provided that

$$\frac{R_f}{R_t} = 2.44 \quad \text{and} \quad \mathrm{R}_f C_f = \frac{1}{1.98 \times 10^3}$$

If the phase inversion resulting from this circuit is undesirable, phase inverting at the phase/frequency discriminator can be performed.

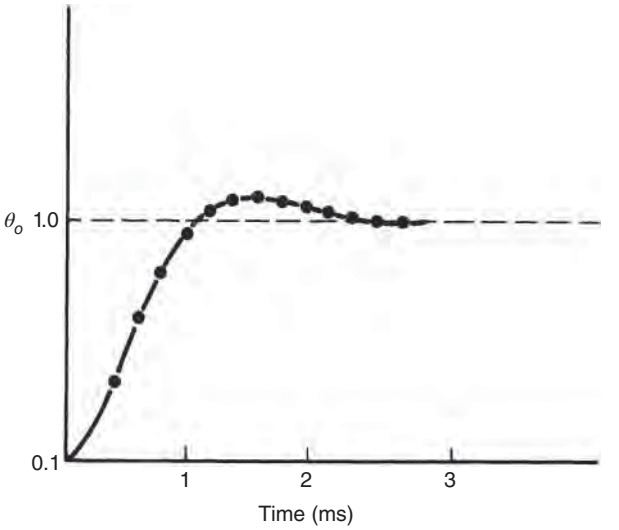


Figure 1-34 Plot of the step response of a 10% overshoot and 0.7-ms rise time.

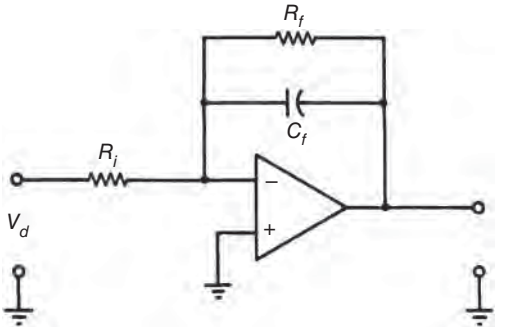


Figure 1-35 Loop filter with a gain of 2.2.

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2

ALMOST ALL ABOUT PHASE NOISE

2-1 INTRODUCTION TO PHASE NOISE

The noise of a synthesizer, an oscillator, or other signal sources is an important parameter, which requires a sophisticated framework to describe it appropriately. If the radio frequency (RF) spectrum is measured at the output of an oscillator, a curve such as that of Figure 2-1 is observed. Rather than all of the power being concentrated at the oscillator frequency, some is distributed in frequency bands on both sides of the oscillator frequency. In principle, such sidebands are originated by phase or frequency fluctuations, and by amplitude fluctuations. A traditional spectrum analyzer cannot divide amplitude modulation (AM) from phase modulation (PM) or frequency modulation (FM), and cannot identify the noise correctly. In this chapter, phase or frequency fluctuations are our main concern.

As noise is a form of stability, it is useful to characterize the frequency stability in the time domain in several areas. Such areas are referred to as short-, medium-, and long-term stability or aging. The interpretation of what is short, medium, or long is a matter of context and jargon of specific communities. We can agree that short-term stability extends between a very small fraction of a second to 1 s, maybe under some considerations up to 1 min, and the value for the stability between 1 s and 1 min will be about the same. For longer time, we talk about long-term stability or aging. The aging is typically expressed in forms of how many parts in 10^{-10} or 10^{-11} per day the frequency changes. This information is in the time domain. In the frequency domain, we find terms like "random walk," "flicker," and "white," which describe the slope of spectral density on a log–log scale. The Fourier frequency, at times labeled f_m or just f when there is no ambiguity, is at times called sideband frequency, offset frequency, or modulation frequency. In this book, we will refer to it as *Fourier frequency* or *offset frequency*, interchangeably, describing the phase fluctuations of an oscillator at a certain frequency off the center frequency. The most common characterization of the phase noise of a source or of a component is the power spectral density (PSD) $L(f)$, or equivalently $S_\theta(f)$, which we will study extensively in the following pages.

2-1-1 The Clock Signal

The clock signal is a highly pure sinusoidal signal that we can write as

$$v(t) = V_0 \left[1 + \alpha(t)\right] \cos\left[2\pi f_0 t + \theta(t)\right] \tag{2-1}$$

where V_0 is the peak amplitude, f_0 is the carrier frequency, $\alpha(t)$ is the random fractional amplitude, and $\theta(t)$ is the random phase. The amplitude noise (AM noise) and phase noise (PM noise) features of such signal are sketched in

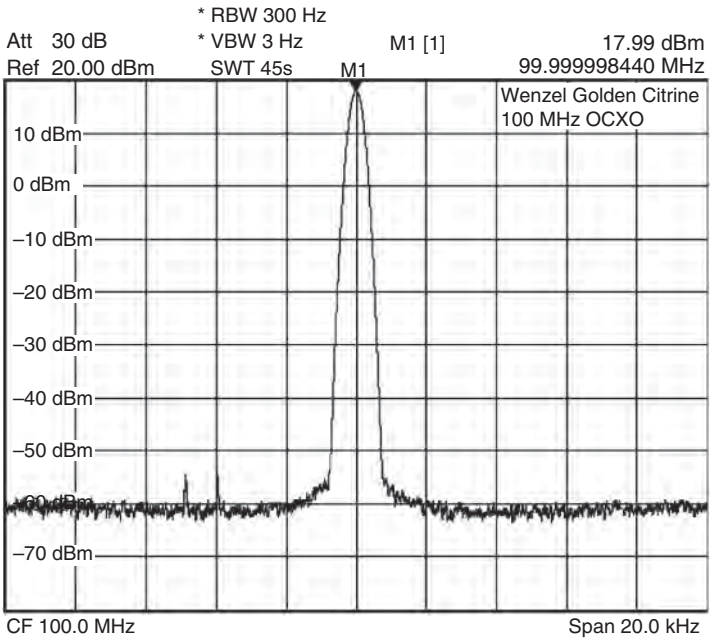


Figure 2-1 Example of the microwave spectrum of an oscillator. Courtesy of © Yannick Gruson, FEMTO-ST Institute, France.

Figure 2-2. In the presence of AM noise only, the peak amplitude changes at random by an amount equal to $V_0\alpha(t)$, while the phase is unperturbed, and consequently the zero crossings occur exactly when expected. Oppositely, a signal affected by PM noise only has peak amplitude exactly equal to V_0, while the phase fluctuates at random, and consequently the zero crossings fluctuate. Both AM and PM are present in all real signals, albeit not in equal amount. The relevant notations and several basic concepts about PM noise and frequency stability presented in this chapter are found in the milestone articles [2, 3]. However, the notation used in this book differs from the standard notation for time and frequency in a small number of details needed to match the common language of phase-locked loops (PLLs) and frequency synthesizers. The most relevant differences in the notation are listed on Table 2-1.

Another, minor, difference is that the normalized quantities $\mathsf{x}(t)$ and $\mathsf{y}(t)$, and some specific parameters, for example, the coefficient b_n, k_n, and h_n found in the polynomial law discussed later, are written in Sans Serif font instead of regular math font. In this way, we let the regular math-font alphabet free, and available for general use.

A well-designed, high-quality oscillator exhibits high amplitude stability. For reference, we found that a short-term stability of 10^{-6} is rather common in high-end RF oscillators, with flicker PSD [4]. The AM noise is generally considered a special topic, discarded in system analysis and design. For our purposes, we assume that V_0 is the best estimation of the amplitude, so that $\alpha(t)$ is very small and has a mean close to zero. In formulas, $|\alpha(t)| \ll 1$ and $\langle\alpha(t)\rangle \approx 0$.

By contrast, we cannot assess a boundary for $\theta(t)$ because real oscillators are subject to aging, drift, and sensitivity to the environment. If we freeze the numerical value of f_0, these phenomena go in $\theta(t)$, which can accumulate a quite large number of cycles (2π rad). Thus, $\theta(t)$ can be a divergent process.

The traditional analog phase detectors work in the range of $\pm\pi$, or $\pm\pi/2$ radians. When these detectors are used for phase-noise measurements, it is often necessary that $|\theta(t)| \ll 1$ for the duration of the test. Conversely, *I*/*Q* detection enables the phase measurement in unbound range, giving a valid result even if $\theta(t)$ accumulates a large number of cycles. The unbound phase is often called *unwrapped phase*.

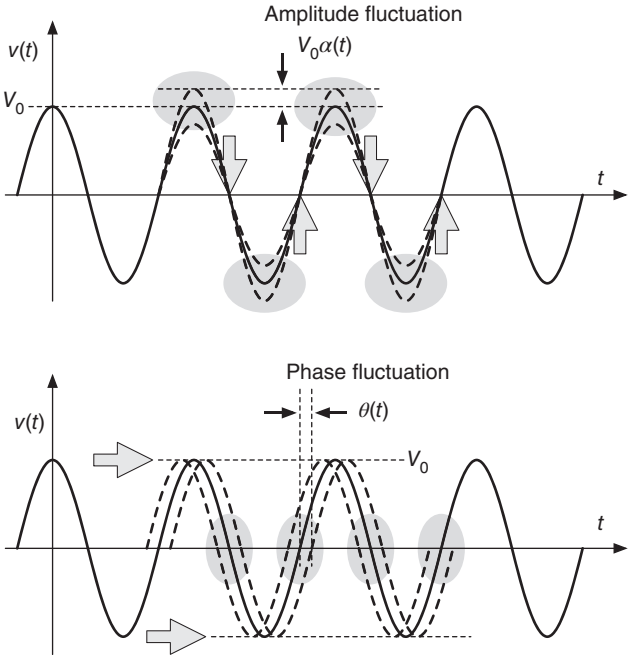


Figure 2-2 Time-domain representation of (A) AM and (B) PM noise. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

Table 2-1 Notation

Quantity	Our notation	General literature	Dimension
Carrier frequency	f_0	ν_0 or f_0	Hz
Fourier frequency	f or f_m	f	Hz
Random phase	$\theta(t)$	$\phi(t)$ or $\varphi(t)$	rad
PM noise PSD	$S_\theta(f)$	$S_\phi(f)$ or $S_\varphi(f)$	rad^2/Hz
	$L(f)$	$\mathcal{L}(f)$	$10\log L(f)$ dBc/Hz
	$L(f) = \frac{1}{2}S_\theta(f)$ by definition	$\mathcal{L}(f) = \frac{1}{2}S_\varphi(f)$ by definition	
Random fractional-amplitude	$\alpha(t)$	$\alpha(t)$, $\epsilon(t)$ or $\varepsilon(t)$	Dimensionless
AM noise PSD	$S_\alpha(f)$	$S_\alpha(f)$, $S_\epsilon(f)$, or $S_\varepsilon(f)$	Hz^{-1}

The quantity $\theta(t)$ is not the one and only option to describe the oscillator fluctuations. Other physical quantities are often preferred, depending on purposes and applications, and sometimes on personal preferences. The clock signal carries a time reference. For this reason, it may be convenient to describe the PM noise as the *time fluctuation*, or *phase time* (fluctuation)

$$\mathrm{x}(t) = \frac{1}{2\pi f_0}\,\theta(t) \tag{2-2}$$

which is $\theta(t)$ converted into time and expressed in seconds. Of course, $\theta(t)$ is allowed to exceed $\pm\pi$ radians, and the number of cycles accumulated is accounted for in $\mathrm{x}(t)$.

For the layman, $\mathrm{x}(t)$ is the time error of a clock driven by our oscillator through an appropriate gearbox. The quantity $\mathrm{x}(t)$ is independent of the carrier frequency, thus it is suitable to compare the timekeeping feature of watches in terms of daily or monthly error.

It is well known in radio engineering that the angular modulation can be formulated in two fully equivalent ways, as PM or as FM. In the same way, we can freeze $\theta(t)$ and move the random fluctuation from $\theta(t)$ to the carrier frequency f_0 by replacing

$$f_0 \rightarrow f_0 + \left(\Delta f_0\right)(t)$$

The quantity Δf_0 is the random frequency fluctuation or error, expressed in Hz. Accordingly, $\theta(t)$ is replaced with $2\pi \int (\Delta f_0)(t)\, dt$. The subscript "0" can be dropped if there is no risk of confusion. The notation $(\Delta f_0)(t)$ emphasizes the fact that Δf is a single variable, function of time. The clock signal becomes

$$v(t) = V_0 \left[1 + \alpha(t)\right] \cos\left[2\pi f_0 t + 2\pi \int (\Delta f)(t)\ dt\right] \tag{2-3}$$

The *fractional frequency fluctuation* or for short *fractional frequency* $\mathrm{y}(t)$ is another quantity often used to describe the oscillator fluctuation, defined as

$$\mathrm{y}(t) = \frac{1}{f_0}\left(\Delta f_0\right)(t) \tag{2-4}$$

Of course, $\mathrm{y}(t)$ is dimensionless. The main reason for $\mathrm{y}(t)$ is that it provides straightforward, fair comparison of oscillators at different frequencies, with no conversion factor. Very common specifications, like "0.1 ppm aging after one year" or "thermal drift of 10^{-9}/°C," refer implicitly to the quantity $\mathrm{y}(t)$. It holds that

$$\mathrm{y}(t) = \frac{d}{dt}\,\mathrm{x}(t) \tag{2-5}$$

2-1-2 The Power Spectral Density (PSD)

The PSD $S(f)$ tells us how the power of a signal is distributed among frequencies, similarly to a prism, which split the light in colors, or to a bank of filter which splits the input signal in bands (Figure 2-3). Taking the power in strict physical sense, the physical dimension of the PSD is W/Hz. The generalized power is often used, which is a squared quantity like a voltage, a current, or a phase. The physical dimension follows in a rather obvious way. For example, the PSD of a voltage $v(t)$, denoted with $S_v(f)$, has the dimension of V^2/Hz. Textbooks often say that there is a 1 Ω resistor implied in order to get a proper unit of power, but this is not necessary because the PSD is a mathematical tool. The PSD of the random phase $\theta(t)$, denoted with $S_\theta(f)$, has the dimension of rad^2/Hz.

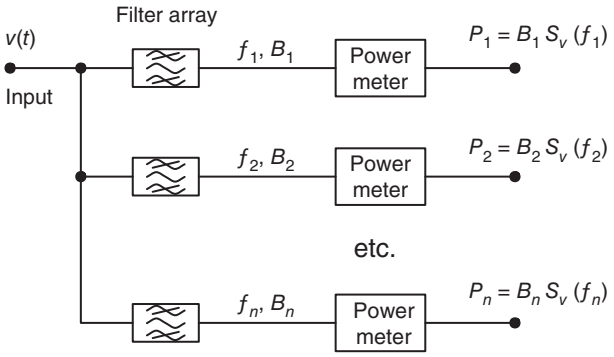


Figure 2-3 Parallel spectrum analyzer. With the appropriate normalization, P_1/B_1, P_2/B_2 … P_n/B_n, the output is the PSD of the input signal. Reprinted from [1], CC BY Rubiola.

Engineers, physicists, and other experimentalists use the single-sided PSD, which is restricted to $f > 0$. There are two important and straightforward properties associated with the PSD. The first is the *Parseval* theorem, which states that the power of a signal $x(t)$ calculated in the time domain and in the frequency domain is the same. In formula

$$P = \lim_{T\to\infty} \frac{1}{T} \int_0^T |x(t)|^2 \, dt = \int_0^\infty S_x(f) \, df \tag{2-6}$$

The second property states that the power of the signal $x(t)$ after bandpass filtering is calculated by integrating the PSD over the filter bandwidth. Denoting the band limits with a and b, the power of the filtered signal is

$$P = \int_a^b S_x(f) \, df$$

A more rigorous version of the aforementioned is formulated with the transfer function $|H(f)|^2$ of the filter as

$$P = \int_0^\infty S_x(f) \, |H(f)|^2 \, df \tag{2-7}$$

General instruments calculate the PSD using the fast Fourier transform (FFT). This implies that the signal is sampled at a given frequency, digitized, and truncated in time. Of course, the input is a stream of real numbers, so the FFT has the usual symmetry properties. Using the uppercase $X(f)$ for the Fourier transform, the subscript T for the truncation over the measurement time of duration T, and f_s for the sampling frequency, the PSD is

$$S_x(f) = \frac{2}{T} \left|X_T(f)\right|^2 \qquad \text{for } 0 < f < f_s/2 \tag{2-8}$$

The factor of 2 is necessary for energy conservation. The energy of $X_T(f)$ is equally split between negative frequencies and positive frequencies, and the energy associated to the negative frequencies of $X_T(f)$ is folded to the positive frequencies in $S_x(f)$. The multiplication by $1/T$ comes from the mathematical development of $S_x(f)$, omitted here. However, the need for such factor is quite evident from physical dimensions. Letting $x(t)$ be a voltage, a valid PSD must have the physical dimension of V^2/Hz. Since the Fourier transform $X(f) = \int_{-\infty}^{\infty} x(t)\, e^{-j2\pi ft} \, dt$ has the dimension of Vs, or equivalently V/Hz, the quantity $|X_T(f)|^2$ has the dimension of V^2/Hz^2. The multiplication by $1/T$ turns the unit into V^2/Hz.

It is a common practice to improve the confidence of the measure, or the readability of the PSD plot, by averaging on a suitable number m of acquisitions. This is written as

$$\left\langle S_x(f) \right\rangle_m = 2\frac{1}{T} \left\langle \left|X_T(f)\right|^2 \right\rangle_m \qquad \text{for } 0 < f < f_s/2 \tag{2-9}$$

In this notation, the angle parentheses $\langle \ldots \rangle$ denote the average, and the subscript m the number of acquisitions.

The PSD has a resolution bandwidth (RBW), which results from the sampling frequency f_s, from the measurement time T, and from the window (tapering) function used in the FFT. The minimum RBW is $1/T$, limited by the time-frequency indetermination theorem. The latter is usually written as $\Delta\omega\Delta t \geq 2\pi$. Wider window functions result in smaller frequency leakage and in better capability to identify correctly a dip between peaks, at the cost of broader RBW. The RBW may change with frequency because the full span is usually obtained by joining pieces sampled at different frequencies. The spectrum of a pure sinusoid of power P and frequency f_1 is a narrow line, ideally a Dirac delta function. However, a real instrument displays a line of bandwidth equal to the RBW, and PSD

$$S(f) = \frac{P}{\text{RBW}} \qquad \text{at} \quad f = f_1, \quad 0 \text{ elsewhere} \tag{2-10}$$

This can be misleading in the case of a smooth PSD affected by spurs. Oppositely, a regular RF and microwave spectrum analyzer displays the *power spectrum* (PS), which is denoted with $G(f)$ and has the physical dimension

of a power (W), or of a generalized power (V^2, A^2, etc.). In the presence of noise of PSD equal to $N(f)$, such instrument displays

$$G(f) = N(f) \times \text{RBW} \tag{2-11}$$

Notice that the term *power spectrum* is sometimes used as an abridged form for *power spectrum density*, leading to a confusion between PSD and PS. Of course, we recommend great attention in all cases where the context may leave a doubt.

Power spectra and PSD are well established concepts. To the reader willing to know more, we recommend the books by Blackman and Tukey, Percival and Walden, and Brigham.

Example 1 Power Spectral Density. Measuring a signal consisting of white noise plus spurs from the power grid, we get the PSD shown on Figure 2-4. We want to know the power and the RMS voltage of all the components of such signal. A straightforward calculation gives the results shown in Table 2-2. ■

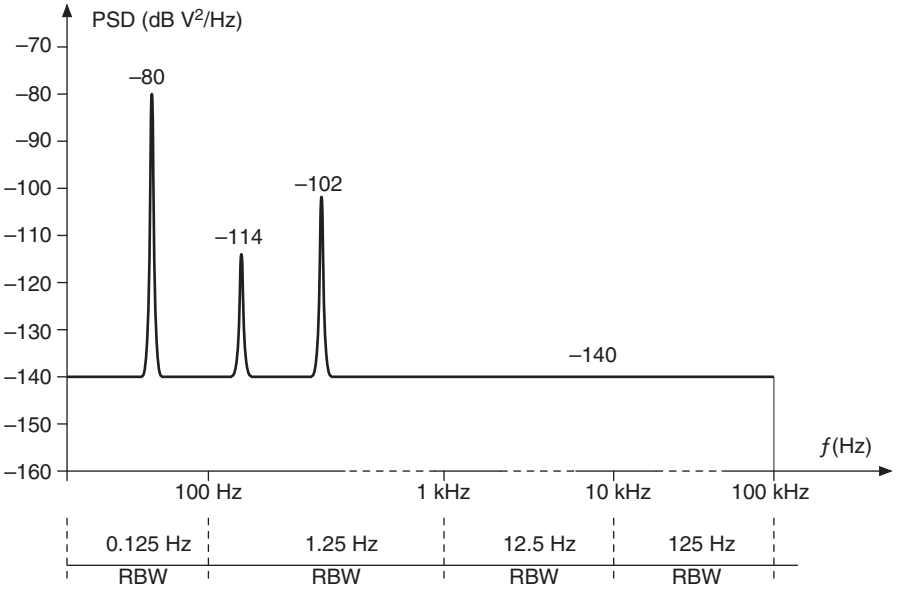


Figure 2-4 Example of PSD constituted of white noise and narrow spectral lines.

Table 2-2 Interpretation of the spectrum of Figure 2-4

Signal component	Power (generalized)	RMS voltage
White noise	$P_n = 10^{-14}\,\frac{\text{V}^2}{\text{Hz}} \times 10^5\ \text{Hz} = 10^{-9}\ \text{V}^2$	$e_n = 31.6\ \mu\text{V}$
60 Hz	$P_1 = 10^{-8}\,\frac{\text{V}^2}{\text{Hz}} \times 0.125\ \text{Hz} = 1.25 \times 10^{-9}\ \text{V}^2$	$e_1 = 35\ \mu\text{V}$
120 Hz	$P_2 = 10^{-11.4}\,\frac{\text{V}^2}{\text{Hz}} \times 1.25\ \text{Hz} = 5 \times 10^{-12}\ \text{V}^2$	$e_2 = 2.2\ \mu\text{V}$
180 Hz	$P_3 = 10^{-10.2}\,\frac{\text{V}^2}{\text{Hz}} \times 1.25\ \text{Hz} = 7.9 \times 10^{-12}\ \text{V}^2$	$e_3 = 8.9\ \mu\text{V}$
Total	$P = P_n + P_1 + P_2 + P_3 = 2.26 \times 10^{-9}\ \text{V}^2$	$e = 47.6\ \mu\text{V}$

2-1-3 Basics of Noise

Thermal (Johnson) Noise

This type of noise is a form of blackbody radiation confined in an electrical line and originates from the thermal agitation of free charges in conductors. It has been observed experimentally by Johnson [5] and explained theoretically by Nyquist [6] in 1928.

The available PSD, that is, the power in 1 Hz bandwidth transferred from the resistor R at the temperature T to the load of equal resistance R and ideally cold ($T = 0$ K), is given by the extended Planck law

$$S(f) = hf + \frac{hf}{e^{hf/kT} - 1} \quad \left[\mathrm{W/Hz}\right] \tag{2-12}$$

where $h = 6.626 \times 10^{-34}$ Js, or equivalently W/Hz, is the Planck constant, and $k = 1.381 \times 10^{-23}$ J/K is the Boltzmann constant. The quantity hf is the photon energy, and kT is the thermal energy of the free electrical charges in thermal equilibrium. The Planck law has a cutoff at the frequency

$$f_{\mathrm{th}} = \ln(2)\,\frac{kT}{h} \tag{2-13}$$

Beyond f_{th}, the blackbody radiation rolls off because the average thermal energy kT is insufficient to produce a photon of energy hf. The exponential shape of the roll off function reflects the statistical nature of the thermal energy. For reference, f_{th} occurs at 4.33 THz at room temperature, and at 60.6 GHz at the liquid helium temperature (4.2 K). So, in almost all practical applications, it holds that $hf \ll \ln(2)\,kT$, thus $e^{hf/kT} \simeq 1 + hf/kT$. The Planck law is approximated with white noise

$$N = kT \quad \left[\mathrm{W/Hz}\right] \tag{2-14}$$

where the $S(f)$ is replaced with the symbol N, as often done with white noise.

The Planck law refers to the available power, in impedance matching conditions. If the conductor is left open, the electromotive force across its ends has PSD

$$S_v(f) = 4kTR \quad \left[\mathrm{V^2/Hz}\right] \tag{2-15}$$

The reference value

$$T_0 = 290\ \mathrm{K} \qquad \left(17.2^{\circ}\mathrm{C\ or\ } 66.3^{\circ}\mathrm{F}\right)$$

is often used in electronics and radio engineering as a convenient approximation of the physical temperature found in most practical cases. The corresponding thermal energy is a round number

$$kT_0 = 4 \times 10^{-21}\ \mathrm{W/Hz} \qquad \text{that is} - 174\ \mathrm{dBm/Hz} \tag{2-16}$$

At that temperature, the equivalent noise voltage kT_0/q is equal to 25 mV. In the jargon of semiconductors, this quantity is often denoted with V_T. The thermal emf in 1 Hz bandwidth is denoted with $e_n = \sqrt{4kT/R}$. Across a $R = 50\ \Omega$ resistor, we find

$$e_n = 0.9\ \mathrm{nV}\big/\sqrt{\mathrm{Hz}}, \qquad \text{or} - 181\ \mathrm{dB\ V}\big/\sqrt{\mathrm{Hz}}$$

The thermal energy contributes to phase noise in two ways. The first and most important effect is the microwave noise added to the carrier. The second, and generally minor, is a PM from the near-dc part of the thermal noise.

Shot (Schottky) Noise

The shot noise in electrical circuits originates from the discrete nature of the electrical charge, which is an integer multiple of the electron charge $q = 1.602 \times 10^{-19}$ C. Its discovery is generally credited to Schottky [7]. Shot noise occurs in junctions, vacuum tubes, and other devices or physical experiments where electrons and holes appear as individual particles. The electrical current in regular conductors, like wires and resistors, is a field, which does

not generate shot noise. The standard picture for the electrical current in vacuum is a stream of Φ electrons per second emitted at random time, with no memory and no space correlation. The average current is $\langle I\rangle = \Phi q$. Unlike thermal noise, shot noise is only present when electrical current flows, and it is independent of temperature and of the resistance of the electrical circuit. This type of noise is a Poisson process, which has uniform (white) PSD

$$S_I(f) = 2q\langle I\rangle \quad [\mathrm{A}^2/\mathrm{Hz}] \tag{2-17}$$

The same formula holds in photodiodes, interpreting $I = \eta P/hf_{\mathrm{opt}}$ as the photocurrent, where f_{opt} is the frequency of the light, and η is the quantum efficiency, that is, the probability that a photon is captured and generates photo-electron or a photo-electron-hole pair.

The bandwidth cannot be infinite. The shot noise rolls off at the cutoff frequency

$$f_{\mathrm{sh}} = \frac{1}{2}\Phi = \frac{\langle I\rangle}{2q} \tag{2-18}$$

The reason is that the generalized power $S_I(f)f_{\mathrm{sh}}$ must be equal to the generalized dc power $\langle I^2\rangle$, which is a consequence of the Parseval theorem. An alternate interpretation relies on the sampling theorem, which states that the maximum frequency is half the sampling frequency. The same holds for random sampling, just with a smooth cutoff. In this picture, the electrons are electrical pulses playing the role of the random samples.

The shot noise equals the thermal noise at the critical current

$$\langle I\rangle = \frac{kT}{2qR} \tag{2-19}$$

determined by $2q\langle I\rangle R = kT$. For reference, this critical current is of 250 µA at 290 K with $R = 50\ \Omega$, and the associated power is of 3.1 µW (−25 dBm).

Like thermal noise, the shot noise contributes to phase noise as it adds to the carrier, and as a near-dc noise that modulates the carrier.

Noise Factor, Noise Figure, and Noise Temperature

The noise factor, or equivalently the noise figure (NF), is likely the most used, if not over-used, parameter to characterize the noise of two-port components or systems, like amplifiers, frequency converters, radio receivers, etc. However, often used interchangeably, one should prefer the term *noise factor* for the dimensionless quantity F, and *noise figure* (NF) for F expressed in dB

$$\mathrm{NF} = 10\log_{10} F \quad [\mathrm{dB}] \tag{2-20}$$

A popular definition of F, given by Friis [8] in 1944, is

$$F = \frac{\mathrm{SNR}_i}{\mathrm{SNR}_o} \quad (\text{Friis, obsolete definition}) \tag{2-21}$$

where SNR is the signal-to-noise ratio, and the subscripts "i" and "o" stand for input and output. A substantially equivalent, and less known definition was given by North [9], as the ratio of (1) the output noise power from the transducer to (2) the output noise power from an equivalent noise-free transducer.

The problem with (2-21), and also with the North's definition, is that the degradation to the SNR depends on the noise of the source that excites the device. This is seen by sending a signal of power P_i and thermal noise kT_i to a device of power gain A^2. Denoting with N_{dev} the available noise contribution of the device in 1 Hz bandwidth, as observed at the output, Eq. (2-21) gives

$$F = \frac{P_i}{kT_i}\,\frac{N_{\mathrm{dev}} + A^2kT_i}{A^2P_i} = 1 + \frac{N_{\mathrm{dev}}/A^2}{kT_i}$$

For the same device at the same temperature, N_{dev} is the same, but F is affected by the temperature T of the input termination.

The ambiguity of (2-21) is solved with the new definition proposed by the IRE [10], and adopted by the NIST (at that time, NBS) [11]:

Definition (IRE):

The **noise factor**, at a specified input frequency, is defined as the ratio of **(1)** the total noise power per unit bandwidth at a corresponding output frequency available at the output port when the noise temperature of the input termination is standard (290 K) to **(2)** that portion of (1) engendered at the input frequency by the input termination.

It is worth mentioning that the IRE definition differs from the Friis definition only in the use of the reference temperature $T_0 = 290$ K. For this reason (2-21) is still found in the literature, with the reference temperature often implied. Both definitions are smart in that the input circuit is taken in its actual configuration, making no assumption on impedance matching and on best noise impedance, if different from the characteristic impedance.

The ***noise temperature***, denoted with T_e, is another widely used parameter to assess the noise, by analogy with the thermal noise.

The case of a source (Figure 2-5A) is quite straightforward. We say that the source has equivalent noise temperature T_e at a specific frequency if the available noise power at its output in 1 Hz bandwidth is $N = kT_e$, the same of a resistor at temperature T_e.

The case of a two-port device is similar, and illustrated on Figure 2-5B. The available output noise N_o is the same for the two cases, (1) when the real device is connected to a noise-free source, and (2) when a noise-free, and otherwise equal device is connected to a source at the temperature T_e.

The noise temperature is related to the noise factor. Assuming impedance matching at the input, the device's noise contribution observed at the output is A^2kT_e. Accordingly, the noise factor (IRE definition) can be written as

$$F = \frac{A^2kT_e + A^2kT_0}{A^2kT_e}$$

thus

$$F = 1 + \frac{T_e}{T_0} \tag{2-22}$$

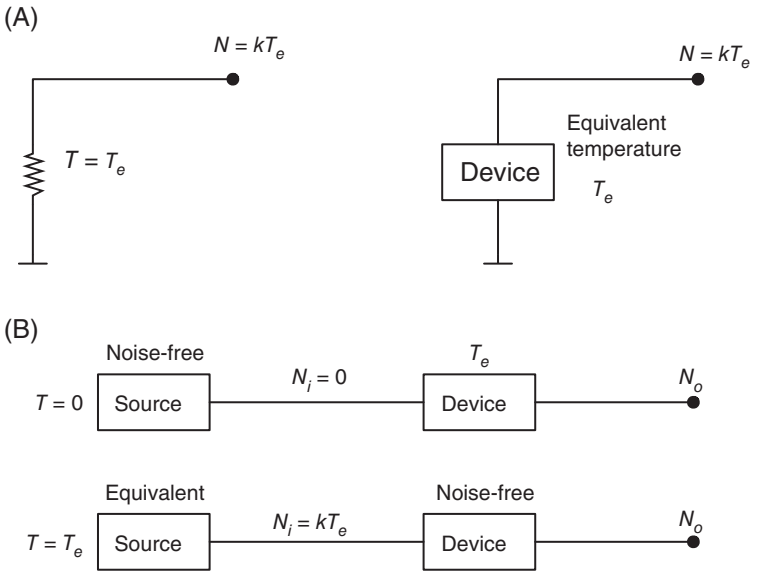


Figure 2-5 Noise temperature. (A) Source and (B) two-port device.

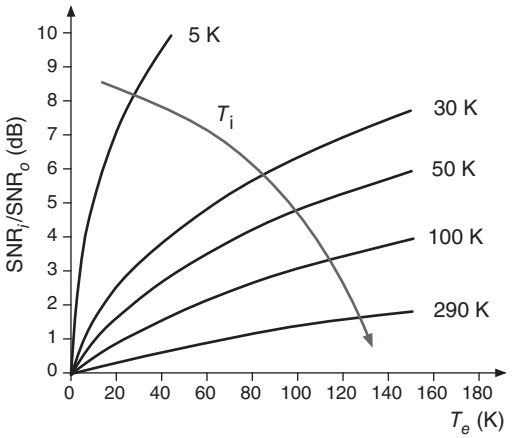


Figure 2-6 SNR degradation due to a two-port device of noise temperature T_e for various values of temperature T_i of the input source. From [12], © 2010–2017 Keysight Technologies. Used with permission, and adapted to the text.

As we mentioned, the SNR degradation produced by a two-port device depends on the input noise, hence on the temperature of the source. Figure 2-6 shows an example. All the plots match Friis' definition $F = \mathrm{SNR}_i/\mathrm{SNR}_o$, but only the plot $T_i = 290$ K matches the IRE definition.

The noise factor of an attenuator is an interesting case because of the physical insight it provides. We first assume that the attenuator impedance-matched at both ends receives the thermal noise kT_i from a resistor. The attenuator "amplifies" the input noise by a factor of $A^2 < 1$, as it does with any signal. The attenuator adds its own contribution, which we will calculate. For this purpose, we set the temperature of both input resistor and attenuator to T_0. The output noise is the sum of (1) the input noise attenuated, that is, $N' = kT_0A^2$, and (2) the noise $N'' = A^2kT_e$ from the attenuator. Because the attenuator output is equivalent to a resistor at the temperature T_0, the total available noise at the output is equal to $N_0 = kT_0$. Thus, $N'' = kT_0 - N'$, and consequently $N'' = kT_0(1 - A^2)$. Referring the attenuator noise to the input, we find $N_e = N''/A^2 = kT_0(1 - A^2)/A^2$. Finally, the equivalent temperature N''/k is $T_e = T_0(1 - A^2)/A^2$. Using $F = 1 + T_e/T_0$, we find $F = 1/A^2$. This proves the thumb rule that the noise factor of an attenuator is equal to the power attenuation.

The noise factor and the noise temperature are simplified representations of the reality. More accurate noise models, generally good enough for virtually all practical purposes, resort to the seminal paper by Rothe and Dahlke [13] on the theory of linear four-poles. Following this approach, the noise is best described by adding a voltage generator e_n and a current generator i_n at the device input, as shown on Figure 2-7. Such generators are described in terms of their PSDs $S_e(f)$, $S_i(f)$, and $S_{ie}(f)$, or equivalently in terms of their variances $\langle | e_n^2 | \rangle$, $\langle | i_n^2 | \rangle$ and the covariance $\langle i_n e_n^2 \rangle$ in 1 Hz bandwidth. The most relevant fact is that e_n and i_n define an impedance that generally differs from the input impedance. Thus, the device has two "optimum" impedances, one for maximum power transfer, which refers to the usual conjugate matching, and one for lowest noise. Consequently, *the impedance of the generator impacts on the noise factor*, and low-noise design requires a tradeoff between gain and noise.

After doing the appropriate math, the noise factor is given by

$$F(\Gamma_g) = F_o + 4\frac{R_n}{Z_0}\frac{\left|\Gamma_o - \Gamma_g\right|^2}{\left|1 + \Gamma_o\right|^2\left(1 - \left|\Gamma_g\right|^2\right)} \tag{2-23}$$

where F_o is the minimum (optimum) noise factor, R_n is the noise resistance (the sensitivity of noise factor to source resistance changes), Z_0 is the nominal input, Γ_g is the reflection coefficient, and Γ_o is the value of Γ_g with which F_o is achieved. The parameters F_o, R_n, and Γ_o describe the noise of the device, and Γ_g is a free design choice. Represented on the Smith chart, the noise factor $F(\Gamma_g)$ looks like a set of equal-noise circles (see Figure 2-8 for an example).

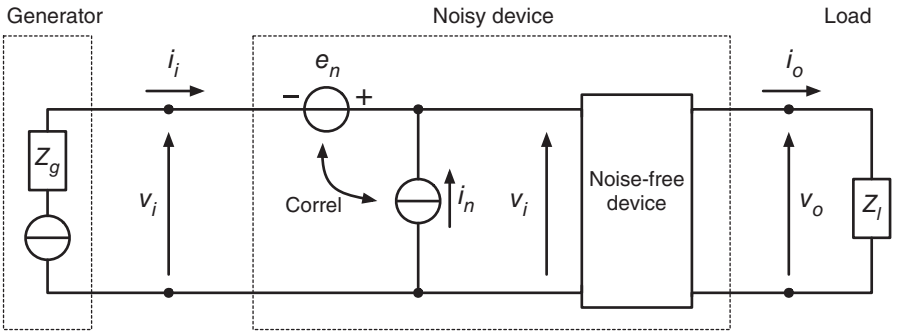


Figure 2-7 Generalized noisy device.

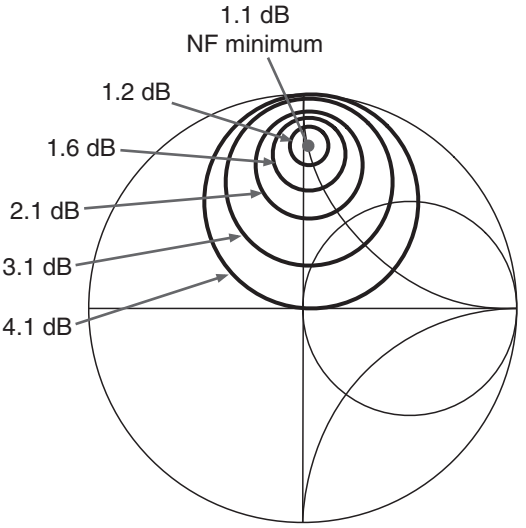


Figure 2-8 Example of equal-noise circles of an amplifier, on the Smith chart. Edited from [12], © 2010–2017 Keysight Technologies. Used with permission, and adapted to the text.

Packaged amplifiers are often impedance-matched in a wide range of frequency, thus the noise factor is degraded because impedance matching is often privileged versus noise matching, and also because of the loss of the input circuit. Values of 1–4 dB are rather common. Conversely, the noise factor of a transistor can be quite low, yet at the cost of uncomfortable impedance matching (see the example on Table 2-3).

When several stages are cascaded, the noise factor of the chain is given by the Friis formula [8]

$$F = F_1 + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \ldots \tag{2-24}$$

Accordingly, the first stage of a chain should have a low noise factor, while the noise factor requirement of subsequent stages is relaxed. The ideas underneath the Friis formula are simple. The overall noise factor F is referred to the input of the chain. The noise contribution of each amplifier is added as square voltage, power, or PSD, as appropriate, because the amplifiers are separate devices, and their fluctuations are statistically independent. The contribution F_1 of the first stage is obvious. The second stage has no resistive load at the input, thus no kT_0. There remains $(F_2 - 1)kT_0$, which becomes $\left(F_2 - 1\right) kT_0/A_1^2$ referred at the input of the chain, after dividing by the power

Table 2-3 Typical noise parameters of the TAV-581+ transistor

f_0 (GHz)	F_o (dB)	$\lvert\Gamma_o\rvert$	$\arg(\Gamma_o)$ (°)	R_n (Ω)	Gain (dB)
0.5	0.09	0.37	16.1	4.0	26.6
0.7	0.12	0.37	28.5	3.5	24.6
0.9	0.16	0.37	40.6	3.0	23.0
1.0	0.18	0.37	46.6	3.0	22.3
1.9	0.34	0.39	97.4	1.5	17.8
2.0	0.35	0.39	102.7	1.5	17.4
2.4	0.42	0.40	123.4	1.5	16.3
3.0	0.53	0.41	152.5	1.5	14.9
3.9	0.69	0.43	−168.1	2.5	13.3
5.0	0.89	0.45	−127.1	5.0	11.8
5.8	1.03	0.46	−102.1	8.0	10.8
6.0	1.06	0.47	−96.5	9.0	10.6

Conditions: $V_{DS} = 4$ V, $I_{DS} = 30$ mA.
Data are taken from the TAV-581+ data sheet (Mini Circuits, NY, USA).

gain A_1^2 of the first stage. Recursively, the noise $(F_3 - 1)kT_0$ of the third stage is divided by the power gain $A_1^2 A_2^2$ of the two preceding stages.

The Friis formula is an approximation based on impedance matching. A more accurate model should account for two main facts. First, impedance mismatch calls for a correction term that lowers the gains A_i^2, based on the reflection coefficients between the i-th and the $(i+1)$-th stage. Second, the noise factor F_1 should account for the source impedance, and likewise all the F_{i+1} should account for the output impedance of the preceding, i-th, stage.

The Measurement of the Noise Temperature

The equivalent temperature of a device is usually measured with the Y method shown on Figure 2-9. The method consists of switching two impedance-matched input sources, one at the temperature T_h (hot) and the other at the temperature T_l (cold). Asymptotically, if one can set $T_h \to \infty$ and $T_l \to 0$, the temperature T_h is the probe signal that enables the measurement of the power gain A^2, and T_l gives the equivalent temperature T_e after taking away the gain A^2. In actual experimental conditions, the output noise power is

$$P_h = A^2 k\left(T_h + T_e\right) B$$

$$P_l = A^2 k\left(T_c + T_e\right) B$$

where B is the bandwidth of a filter at the device output. The solution of the system is

$$T_e = \frac{T_h - YT_l}{Y - 1} \tag{2-25}$$

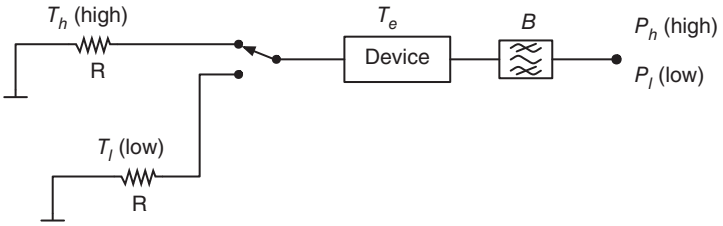


Figure 2-9 The Y method for the measurement of the equivalent noise temperature of a device.

where Y is the power ratio defined as

$$Y = \frac{P_h}{P_l} \tag{2-26}$$

The solution of the system is

$$T_e = \frac{T_h - YT_l}{Y - 1} \qquad \text{with} \qquad Y = \frac{P_h}{P_l} = \frac{T_h + T_e}{T_l + T_e} > 1 \tag{2-27}$$

The main virtue of the Y method is that the factor A^2/B cancels in the evaluation of Y. This simplifies the calibration and results in improved accuracy because A generally suffers from flatness defect, while B is the equivalent noise bandwidth, which results from integrating the transfer function.

It is worth mentioning that the equivalent noise temperature includes thermal noise in strict sense, the shot noise, and any other noise process. For this reason, people with a background in optics may find this concept particularly misleading. In fact, in optical systems there is no temperature and, in high SNR condition, the electrical noise at the detector output is chiefly shot noise.

Flicker Noise

Flicker noise is characterized by the PSD proportional to $1/f$, or close to $1/f$, in a wide range of frequency. The digression about whether flicker noise is fundamental or not, is more academic than pragmatic, and goes far beyond our scopes. The most interesting fact about flicker is its ubiquity [14, 15]. After being discovered in carbon microphones [16], it is found in geophysical phenomena, climatology, mechanics, optics, classical music, Internet traffic, and in a variety of other domains [14], and of course electronics.

Flicker noise originates around dc. Flicker of phase and flicker of frequency are parametric noise types, generated by a near-dc process, which modulates the phase or the frequency of a signal. Flicker is of paramount importance for us because it turns out to be a major limitation in the noise of synthesizers, and of oscillators as well.

Spurs and Other Unwanted Signals

The generation of a clean microwave signal, free from spurs, interferences, and other unwanted signals is a blend of engineering, experience, and art. We all are used to the presence of unwanted signals at 60 Hz (50 Hz in Europe) and multiples, from the power grid. Such signals show up as spectral lines in phase noise, and as a hum sound in audio-frequency. They get in microwave circuits in several different ways, like the ripple of supply lines, unequal potential of different ground points, ground loops, and magnetic fields captured by loops and turned into emf. These signals are added in the low-frequency part of phase lock, and transposed to the carrier as parametric noise. Other interferences have similar behavior, like the ripple from switching power supplies, and the high-voltage raster signals from cathode ray tubes. Unshielded ac magnetic fields affect the magnetic permeability of ferrite cores, which modulate the phase of RF signals. Acoustic noise gets in microwave circuits via the sensitivity to acceleration. Most of such noise comes from fans, from the mechanical vibration of transformers, and again from unshielded magnetic fields via the ac attractive force on iron parts.

Disturbances from 50 to 60 Hz power grid usually extends up to approximately 1 kHz, becoming progressively smaller as the number of harmonic decreases. Odd-order harmonics are generally stronger than even-order harmonics. Acoustic noise is most present between 1 and 2 kHz, while switching power supplies and cathode-ray tubes are typically in the 10–100 kHz region.

Quartz oscillators and other electro-mechanical oscillators are highly sensitive to acoustic noise. Some are also sensitive to magnetic fields, mainly because of the presence of magnetic materials in packaging and springs. YIG materials are highly sensitive to magnetic fields, but packaged YIG oscillators are generally well shielded.

Digital circuits can be an annoying source of spurs and disturbances because of the variety of effects. Radiation occurs at the clock frequency, or at the bus frequency, which occurs from 100 MHz, or less, up to 1 GHz. High

peaks of current on supply lines or ground are driven by software in microprocessors and field programmable gate arrays (FPGAs), which sometimes cause a large number of transistors to switch with random, pseudo-random, or pseudo-periodical appearance. Spurs may be observed in a wide range of frequency from Hz to MHz. Impressively large spurs may be observed in digital phase noise test equipment, if the user removes the post-processing filters that hide the spurs. Digital circuits can also interfere with other parts of a system in another subtle way, via thermal fluctuations. The problem arises from modern very large-scale integration (VLSI) integrated circuits, where high dissipated power per unit of silicon surface is necessary to achieve the computing power. A dissipation of a few watts is usual in FPGAs, direct digital synthesizers (DDSs), etc., in a small chip, and the surface is proportionally hot. If not appropriately shielded, temperature fluctuations show up generally below 10 Hz with a steep spectrum, of slope $1/f^5$ or higher. Every circuit is a special case, and the literature provides little or no help.

To complete the picture, the electromagnetic interference between different part of a system is one of the earliest known forms of spurious signals, and however sometimes difficult to model and predict precisely. The electromagnetic interference impacts on systems as an additive disturbance, or through intermodulation in junctions.

Some classic reference books are available on this topic, by Goedbloed, Ott, Paul, and Perez.

2-1-4 Phase and Frequency Noise

The Quantities $S_\theta(f)$, $S_x(f)$, $L(f)$, and $S_\alpha(f)$

The PSD of the random phase $\theta(t)$, denoted with $S_\theta(f)$ [rad^2/Hz], is the obvious choice to characterize the phase noise in the frequency domain. Its use already appeared as $S_\phi(f)$ in an article [17] presented at an NASA symposium [18] intended to clarify spectral purity and related problems.

Similarly, the phase time fluctuation can be characterized in the frequency domain in terms of $S_x(f)$, which is PSD of $x(t)$. Because it holds that $x(t) = \theta(t)/2\pi f_0$, the quantities $S_\theta(f)$ and $S_x(f)$ are fully equivalent, and related by

$$S_x(f) = \frac{1}{4\pi^2 f_0^2} S_\theta(f) \tag{2-28}$$

The quantity $L(f)$, defined as

$$L(f) = \frac{1}{2} S_\theta(f) \quad \textbf{(definition)} \tag{2-29}$$

is the most widely used measure for phase noise. $L(f)$ is generally given in dBc/Hz using $10 \log_{10} L(f)$. Some authors include $10 \log_{10}$ in the definition of $L(f)$. According to (2-29), $L(f)$ and $S_\theta(f)$ are fully equivalent and differ only in the unit of angle. The unit is the radian for $S_\theta(f)$, and $\sqrt{2}$ rad $= \sqrt{2} \times 180/\pi = 81.03°$ for $L(f)$.

If we started from the scratch now, we would use $S_\theta(f)$, and $L(f)$ would not exist. The reason is that $S_\theta(f)$ is a proper SI quantity, $L(f)$ is not. The problem originates in the early attempts to measure the phase noise with a spectrum analyzer. At that time, the phase noise was measured as

$$L(f) = \frac{\text{Power in 1 Hz bandwidth at a frequency } f \text{ off the carrier frequency } f_0}{\text{Carrier power}} \quad \textbf{(obsolete definition)} \tag{2-30}$$

The true measurement of phase noise became common in the 1970s [19], when the double-balanced mixer (DBM) was available as an off-the-shelf component, suitable to a wide range of carrier frequency.

Notice that the IEEE Standard 1139 replaces (2-30) with (2-29). This was done since the first edition published in 1988 [20] and the second [21] and third edition [22] of this Standard, published in 1999 and 2009, respectively, confirm this choice.

The obsolete definition (2-30) is ***conceptually incorrect*** and ***experimentally incorrect***. Let us discuss why.

First and foremost, the sideband power originates any combination of amplitude noise and phase noise. The obvious consequence is that (2-30) is a conceptually wrong representation of phase noise. For example, there is a

discrepancy of 3 dB in the actual phase fluctuation of two signals having the same spectrum, one affected by equal amount of AM and PM noise, and the other having negligible AM noise.

Second, phase noise is measured with a phase detector. Consequently, "the SSB power in 1 Hz bandwidth" does not match the operation of the instrument.

Third, phase noise is pure angular modulation, thus the total power is the same at any modulation index. The random nature of noise does not change this fundamental property. The definition (2-30) can be used only for small modulation, where most of the power is in the carrier, and the power associated to the sidebands is comparatively small. Slow phenomena, like frequency random walk and drift, yields to large phase swing, exceeding 1 rad^2 in 1 Hz bandwidth. In the presence of such phenomena, (2-30) gives nonsensical results. By contrast, the correct definition (2-29) is perfectly suitable to large phase swing.

Finally, the obsolete definition (2-30) suffers from several pathologies. What happens with an odd signal affected by strong AM noise, and small PM noise? What happens if a spur occurs only in the upper (or lower) sideband, in the PM noise measurement range? In both cases the sideband-to-carrier ratio gives a nonsensical picture of the phase fluctuations.

It is a common belief that $L(f)$, or equivalently $S_\theta(f)$, is a valid measure only for small angles. In reality, there is no reason for such limitation, and $L(f)$ is valid even if $\theta(t)$ accumulates a large number of cycles. In other words, there is no reason to restrict $L(f)$ to values below 0 dBc/Hz. In optics, measuring lasers one may encounter values of +40 or 60 dBc/Hz, which are theoretically and experimentally correct. Of course, the phase detector has to work correctly in this regime.

Heuristic Derivation of L(f) and S_θ(f) in the Simple Case of Additive Noise

It is instructive to derive the quantities $L(f)$ and $S_\theta(f)$ for the simple case of white noise having PSD equal to N [W/Hz] added to a sinusoidal signal of power P_0 [W]. Before proceeding, we have to make clear that the case described does not match the definition of $L(f)$ and $S_\theta(f)$, but approximates it for small N. The catch is that a true random PM keeps the total power constant, while the added noise does not. With this caveat, our heuristic derivation gives useful results.

Let us start with $L(f)$, with the help of Figure 2-10. In the standard notation for microwave circuits, a sinusoidal signal $v(t) = V_0 \cos(\omega_0 t + \theta)$ can be represented as the complex vector

$$V = V_0 e^{j\theta} \tag{2-31}$$

The power of such signal is $P_0 = |V_0|^2/2R$, thus the vector length is $V_0 = \sqrt{2RP_0}$. Similarly, a narrow noise slot of bandwidth B centered at $f_0 + f_m$ can be represented as a vector

$$V = V_n e^{j2\pi f_m t} \tag{2-32}$$

of random amplitude $V_n(t)$ rotating at the frequency f_m and average absolute value $V_n = \sqrt{2RNB}$. Adding carrier and sideband under the approximation of small noise-to-signal ratio, we get

$$\theta(t) = \frac{\sqrt{2RNB}}{\sqrt{2RP_0}} \sin(2\pi f t) = \sqrt{NB/P_0} \sin(2\pi f t) \tag{2-33}$$

The RMS value of $\theta(t)$ for $B = 1$ Hz is $\sqrt{NB/2P_0}$. Accordingly, it holds that

$$L(f) = \frac{1}{2} \frac{N}{P_0} \tag{2-34}$$

The aforementioned formula can be rewritten in terms of equivalent noise temperature T_e or of the noise factor F as

$$L(f) = \frac{1}{2} \frac{k\left(T_e + T_0\right)}{P_0} \quad \text{or} \quad L(f) = \frac{1}{2} \frac{FkT}{P_0} \tag{2-35}$$

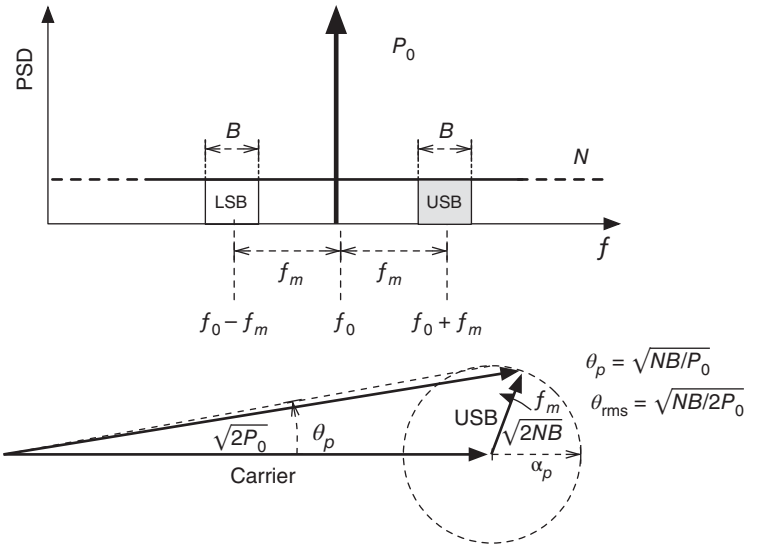


Figure 2-10 Heuristic derivation of $L(f)$ in the case of additive white noise. The resistance R is not shown. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

A similar procedure can be used to derive $S_\theta(f)$, with the help of Figure 2-11. While the carrier is the same as earlier, now we have two symmetric narrow sideband slots of bandwidth B centered at $f_0 - f_m$ and at $f_0 + f_m$

$$V = -V_{\mathrm{LSB}} e^{-j2\pi f_m t} + V_{\mathrm{USB}} e^{+j2\pi f_m t} \tag{2-36}$$

These sidebands have random amplitude $V_{\mathrm{LSB}}(t)$ and $V_{\mathrm{USB}}(t)$. The power associated to each sideband is NB, equally split into AM and PM noise. Thus, the absolute value of the vectors that contribute to PM noise is $V_{\mathrm{USB}} = V_{\mathrm{LSB}} = \sqrt{RNB}$. Combining carrier and sidebands under the approximation of small noise-to-signal ratio, we get

$$\theta(t) = \frac{2\sqrt{RNB}}{\sqrt{2RP_0}} \sin\left(2\pi f_m t\right) \tag{2-37}$$

and

$$\theta(t) = \sqrt{\frac{2NB}{P_0}} \sin\left(2\pi f_m t\right) \tag{2-38}$$

The RMS value of $\theta(t)$ for $B = 1$ Hz is $\sqrt{NB/P_0}$. Thus

$$S_\theta(f) = \frac{N}{P_0} \tag{2-39}$$

Using the equivalent noise temperature T_e or the noise factor F, the aforementioned formula becomes

$$S_\theta(f) = \frac{kT_e}{P_0} \quad \text{or} \quad S_\theta(f) = \frac{FkT}{P_0} \tag{2-40}$$

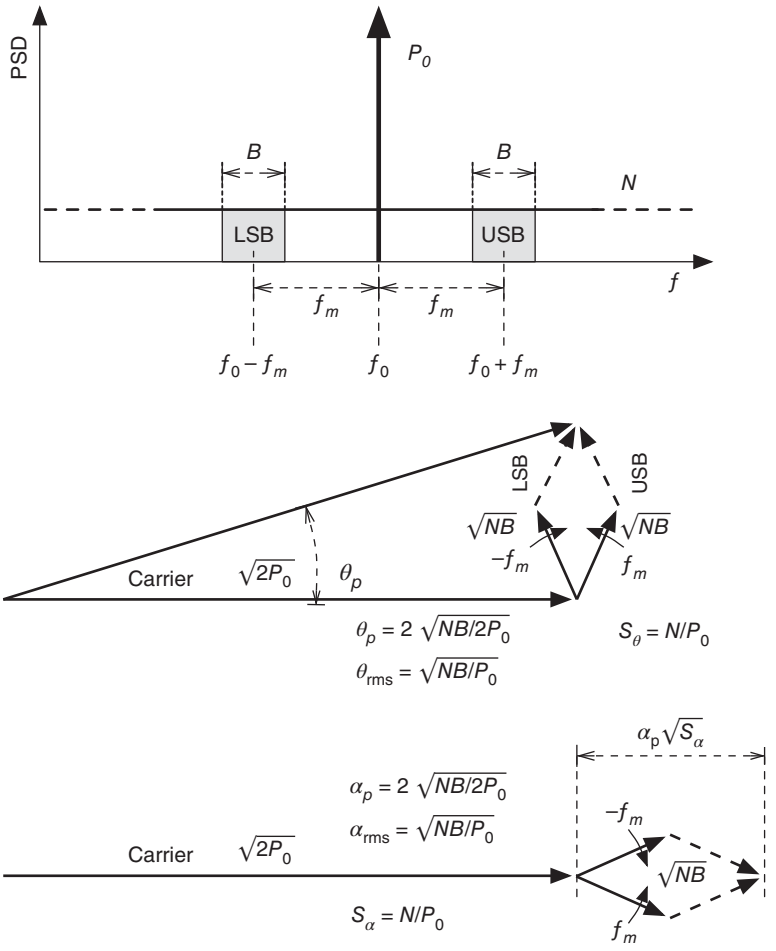


Figure 2-11 Heuristic derivation of $S_\theta(f)$ and of $S_\alpha(f)$ in the case of additive white noise. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

The same development can be used to derive the amplitude noise. In this case, the vector representing the lower side band (LSB) has opposite sign with respect to phase noise; hence the sum of the two sideband vectors is parallel to the carrier. The result is

$$S_\alpha(f) = \frac{N}{P_0} \tag{2-41}$$

Using Figure 2-10 instead, we notice that the old definition of $L(f)$ based on the sideband-to-carrier ratio gives both amplitude fluctuations and phase fluctuations, of equal amount. After our digression on the reason why the definition of $L(f)$ has be changed to $L(f) = \frac{1}{2}S_\theta(f)$, this unpleasant fact does not come as a surprise. Should the reader have to face both PM and AM noise, we recommend the use of $S_\theta(f)$ and $S_\alpha(f)$, or $L_\theta(f)$ and $L_\alpha(f)$ with obvious meaning. The notation $M(f)$ is sometimes encountered as the AM-noise counterpart of $L(f)$.

The smallest amount of white noise for a source characterized by a resistance at a temperature T is

$$S_\theta(f) = S_\alpha(f) = \frac{kT}{P_0} \tag{2-42}$$

Table 2-4 Scaling rules for a noise-free synthesizer delivering $f_{out} = (n/d)f_{in}$

Quantity	Time domain	Spectral domain
Phase	$\theta_{out}(t) = \frac{n}{d}\theta_{in}(t)$	$S_{\theta_{out}}(f) = \left(\frac{n}{d}\right)^2 S_{\theta_{in}}(f)$
Frequency	$(\Delta f_{out})(t) = \left(\frac{n}{d}\right)(\Delta f_{in})(t)$	$S_{\Delta f_{out}}(f) = \left(\frac{n}{d}\right)^2 S_{\Delta f_{in}}(f)$
Phase time	$x_{out}(t) = x_{in}(t)$	$S_{x\,out}(f) = S_{x\,in}(f)$
Fractional frequency	$y_{out}(t) = y_{in}(t)$	$S_{y\,out}(f) = S_{y\,in}(f)$

Scaling the carrier frequency with an ideal noise-free synthesizer, which delivers an output frequency $f_o = (n/d)f_i$, the quantities associated to phase noise scale according to the rules listed in Table 2-4. We want to draw the attention of the reader to the simple fact that the synthesizer scales up or down the input phase noise and the input frequency noise in the same way. By contrast, the amplitude at the output of the ideal synthesizer is determined by the output stage, rather being sensitive to the input amplitude.

Example 2 Noise Factor. A system has a noise factor of 1.8 dB and receives at the input a sinusoid of power $P_0 = 100\ \mu W$ (−10 dBm). The phase noise $L(f)$ is

$$L(f) = \frac{1}{2}\frac{FkT}{P_0} = \frac{1}{2}\ \frac{10^{1.8/10} \times 1.386 \times 10^{-23} \times 290}{10^{-4}} = 3 \times 10^{-17}\ (-165.2\ \text{dBc/Hz})$$

If the reader can think in dB, the aforementioned formula becomes

$$L_{dB} = -3 + 1.8 - 174 - (-10) = -165.2\ \text{dBc/Hz}$$

■

Additive and Parametric Noise

Experience shows that in all oscillators the sideband noise increases greatly as we observe very close to the carrier. Slowly tuning the oscillator to a different frequency, we are faced to the evidence that the noise sidebands are attached to the carrier and follows the carrier frequency. This behavior is incompatible with the noise model we have used in Section 2-1-4 to derive $S_\theta(f)$. How could the additive noise have a sharp peak centered exactly at the carrier frequency, "know" when the oscillator is re-tuned or drifts, and track the carrier by shifting the peak to the new frequency? No way. Our derivation related to Figures 2-10 and 2-11 is correct, but it does not explain this behavior. The answer is that there are two types of phase noise, and of amplitude noise as well, called ***additive noise*** and ***parametric noise***. They already appeared in the seminal article [17], at that time called *additive* and *multiplicative* noise. The basic mechanisms are represented in Figure 2-12. Understanding the difference between these types of noise is of paramount importance to master phase noise. The *additive noise* is exactly what we have explained in Section 2-1-4 when we derived $S_\theta(f)$ by adding carrier and sideband vectors. White, or nearly white, noise is present in a wide radiofrequency and microwave spectrum, and it adds to the carrier. By contrast, the *parametric noise* originates from a near-dc noise, which modulates the carrier phase, frequency or amplitude, or any combination of. The noise spectrum of the near-dc process is transposed to the sidebands around the carrier with the appropriate rules and symmetry. In this way, it is perfectly sound that a noise pattern with spurs in the microwave spectrum is centered at the carrier, and it appears unchanged around the new frequency after tuning or drift.

Notice that the power conservation inherent in the angular modulation of any index or phase swing applies only to parametric phase or frequency noise. By contrast, *adding* a white noise process results in higher total power.

Two-port components show a similar behavior, with the difference that they have no frequency drift because the output frequency is rigidly determined by the input frequency.

The digression about additive and parametric noise and their difference deserves further attention, because the term *added noise* is sometimes encountered in the specs of components and of test equipment. This term denotes the

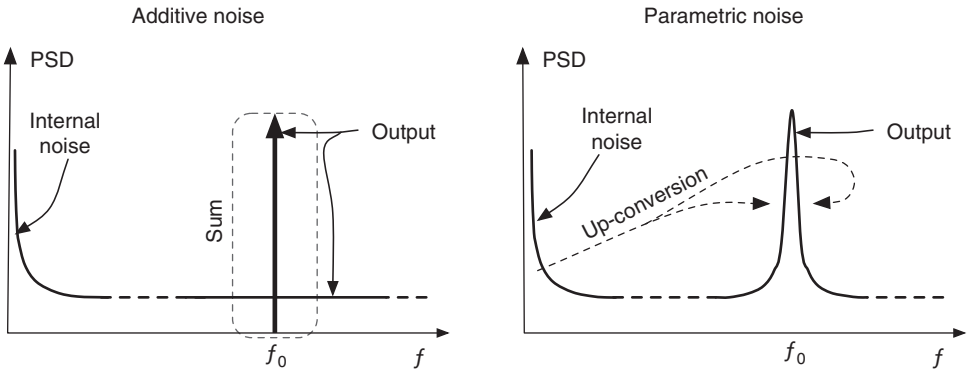


Figure 2-12 Additive and parametric noise. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

phase noise, and sometimes also the amplitude noise, that the component "adds" to the incoming carrier. The choice of the term "added noise" is unfortunate because it is too easily mistaken for "additive noise," while it refers to both the additive noise and the parametric noise that the component "adds" to the incoming carrier.

The Polynomial Law

A model that is found useful to describe the phase noise of oscillators and components is the *polynomial law*, often also called *power law* [2, 23]

$$S_\theta(f) = \sum_{n\le -4}^{0} \mathsf{b}_n f^n \tag{2-43}$$

where the coefficients b_n are the parameters that describe the corresponding noise process. Equivalently,

$$L(f) = \frac{1}{2} \sum_{n\le -4}^{0} \mathsf{b}_n f^n \tag{2-44}$$

The polynomial law for phase noise is shown in Figure 2-13 and Table 2-5. The latter is extended to the phase time and fractional frequency fluctuations, detailed later. For the reader found in mathematics, the polynomial law refers to a Laurent polynomial, which is the extension of the Taylor series to negative-exponent powers of the running variable. In the oscillator phase noise, we find f^0 (constant), $1/f$, $1/f^2$, etc., and each of such processes takes a specific name. Some may be hidden underneath the neighboring terms.

We have studied the additive noise extensively in section "Heuristic Derivation of $L(f)$ and $S_\theta(f)$ in the Simple Case of Additive Noise". The additive noise is chiefly a ***white PM*** process, with at most some smooth irregularities. The reason is that we observe a narrow region $f_0 \pm f_m$ of the microwave spectrum, centered at the carrier frequency f_0.

Surprisingly for some, the white noise is not necessarily all of additive origin. An amount of white noise in a modulation process can be present.

The ***flicker PM*** noise is a parametric noise process originated by near-dc flicker, whose PSD is proportional to $1/f$, which modulates the phase of the microwave signal.

The ***white frequency noise***, or *white FM noise*, is a parametric process originated by white noise that modulates the frequency of an oscillator. This can be due for example to the thermal fluctuations of a resonator, to white noise in the oscillator loop, or to the white noise of the signal at the voltage-controlled oscillator (VCO) input of the oscillator. The phase noise PSD associated to a white FM noise process is proportional to $1/f^2$. The reason is the following. As the phase is the integral of a frequency, its fluctuation $\theta(t)$ can be expressed as the integral of

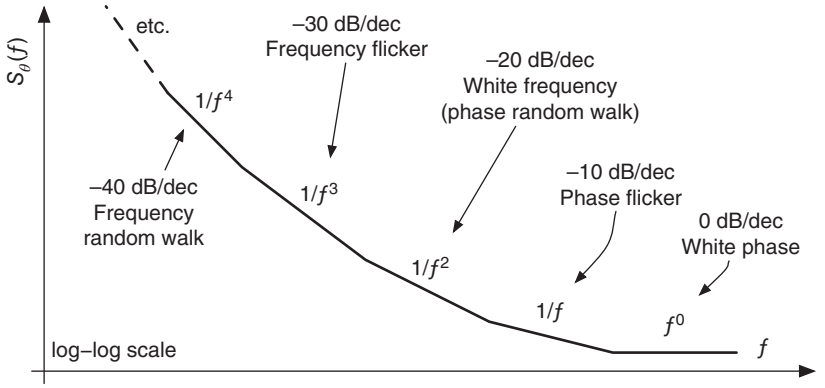


Figure 2-13 The polynomial law for phase noise. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

Table 2-5 Main noise processes of the polynomial law for PM and FM noise

Noise type	Phase noise, $S_\theta(f)$		Phase time, $S_x(f)$		Fractional frequency, $S_y(f)$	
	Law	Unit	Law	Unit	Law	Unit
White PM	b_0	rad^2/Hz	k_0	s^2/Hz (s^3)	$\frac{h_{-2}}{f^2}$	Hz
Flicker PM	$\frac{b_{-1}}{f}$	rad^2	$\frac{k_{-1}}{f}$	s^2	$\frac{h_{-1}}{f}$	Dimensionless
White FM	$\frac{b_{-2}}{f^2}$	rad^2 Hz	$\frac{k_{-2}}{f^2}$	s^2 Hz (s)	h_0	Hz^{-1}
Flicker FM	$\frac{b_{-3}}{f^3}$	rad^2 Hz^2	$\frac{k_{-3}}{f^3}$	s^2 Hz^2 (dimensionless)	$h_1 f$	Hz^{-2}
Frequency RW	$\frac{b_{-4}}{f^4}$	rad^2 Hz^3	$\frac{k_{-4}}{f^4}$	s^2 Hz^3 (s^{-1})	$h_2 f^2$	Hz^{-3}

Source: Reprinted from [1], CC BY Rubiola, and adapted to our notation.

the carrier fluctuation $(\Delta f_0)(t)$ because $\theta(t) = 2\pi \int (\Delta f_0)(t)\, dt$. We exploit the property of the Fourier transform, that the time-domain integral maps into a multiplication by $1/j2\pi f$, that is,

$$\int x(t)\, dt \leftrightarrow \frac{1}{j2\pi f} X(f) \tag{2-45}$$

There follows that

$$S_\theta(f) = \frac{1}{f^2} S_{\Delta f_0}(f) \quad \text{and equivalently} \quad L(f) = \frac{1}{2f^2} S_{\Delta f_0}(f) \tag{2-46}$$

and equivalently

$$S_\theta(f) = \frac{1}{f^2} S_{\Delta f_0}(f) \quad \text{and equivalently} \quad L(f) = \frac{1}{2f^2} S_{\Delta f_0}(f) \tag{2-47}$$

Of course, in the presence of white frequency noise, $S_{\Delta f_0}(f)$ is a constant versus frequency, while $S_\theta(f)$ and $L(f)$ are proportional to $1/f^2$.

The ***flicker frequency noise***, or *flicker FM noise*, is another type of noise very often found in oscillators, and characterized by a phase noise PSD proportional to $1/f^3$. It originates from a flicker noise process, which modulates the frequency of the oscillator. The same reasoning seen for the white PM noise yields the conclusion that $S_\theta(f)$ and $L(f)$ are proportional to $1/f^3$.

Textbooks of statistics teach us that random walk results from integrating a white noise process. But we have seen that the integral operator maps into the multiplication by a factor of $1/f^2$ in the PSD. As a consequence, in the presence of a ***random walk of frequency***, or *frequency RW* for short, $S_\theta(f)$ and $L(f)$ are proportional to $1/f^4$. There are several physical reasons for the presence of frequency RW in oscillators, mainly related to the resonator's natural frequency changing with time, or affected by environmental parameters.

There is no a priori reason for the sum (2-43) to start from $n = -4$, and further negative terms can be added when needed. Oppositely, a "true" $\mathsf{b}_1 f$ term is not allowed because it results in too large power, if not infinite power, after integrating $S_\theta(f)$. A "+1" slope is often found in optical fiber links and other applications involving a control loop. However, this behavior can only be local, that is, the left-hand side of a bump in the spectrum.

The ***frequency drift*** consists in a linear change of the oscillator frequency with time. In the presence of a drift D of the fractional frequency, we can replace the oscillator frequency f_0 as

$$f_0 \to f_{00}(1 + \mathsf{D}t) \tag{2-48}$$

where f_{00} is the oscillator frequency at an appropriate origin of time $t = 0$. The reason for the frequency drift in oscillators is mainly related to the aging of the resonator.

The PSD is not a preferred tool to describe the drift because the curve is too steep for clear visual interpretation, and because the phase $\theta(t)$ grows rapidly and gets too large for the dynamic range of most instruments. Time-domain techniques are more suitable. However, it is instructive to calculate $S_\theta(f)$ in the presence of a frequency drift. We start from a frequency perturbation described by a Dirac $\delta(t)$ distribution. The Laplace transform of $\delta(t)$ is equal to 1. The integral of the $\delta(t)$ distribution is the Heaviside distribution $u(t)$, and its Laplace transform is $1/s$. Further integrating, we get a linear ramp $tu(t)$ starting at $t = 0$, that is, a drift. Its Laplace transform is $1/s^2$. But the phase is the integral of the frequency, thus the Laplace transform is $1/s^3$. We can derive the PSD from the Laplace transform, first by converting the Laplace transform into the Fourier transform (replace $s \to j2\pi f$), and then by taking the absolute square value. In this way, we find $S_\theta \propto 1/f^6$.

We recall that the phase time fluctuation is equivalent to the random phase after converting the unit from radians to seconds, that is, $\mathsf{x}(t) = \theta(t)/2\pi f_0$. As an obvious consequence, the polynomial law applies to $S_\mathsf{x}(f)$

$$S_\mathsf{x}(f) = \sum_{n\le -4}^{0} \mathsf{k}_n f^n \quad \text{with} \quad \mathsf{k}_n = \frac{1}{4\pi^2 f_0^2}\,\mathsf{b}_n \tag{2-49}$$

The classification of noise from white PM to frequency RW applies to oscillators and to frequency sources in general. By contrast, only white and flicker phase noises are possible in two-port components, otherwise the input–output delay would diverge. Steeper terms of the polynomial law, for example, $1/f^4$ or $1/f^5$, are often seen on phase noise plots. However, deeper analysis shows that this behavior is the right-hand side of a large bump in the spectrum due to environmental parameters or to other phenomena, and the full bump does not show up because its left-hand side occurs at too low frequencies, outside the measurement span.

The mean square phase and delay accumulated by a device, in the frequency span from f_1 to f_2, are given by

$$\langle \theta^2 \rangle = \int_{f_1}^{f_2} S_\theta(f)\, df \tag{2-50}$$

and

$$\langle \mathsf{x}^2 \rangle = \int_{f_1}^{f_2} S_\mathsf{x}(f)\, df \tag{2-51}$$

It is clear that, for $1/f^2$, $1/f^3$, and slower processes, the quantities $\theta_{\text{rms}} = \sqrt{\langle\theta^2\rangle}$ and $\mathsf{x}_{\text{rms}} = \sqrt{\langle\mathsf{x}^2\rangle}$ can get quite large as the lower boundary f_1 is small. Conversely, and surprisingly, flicker PM gives rise to small phase and delay, even if the PSD is integrated over a rather extreme frequency span. We will see this in the following example.

Example 3 Flicker Noise. A two-port device used at the carrier frequency $f_0 = 100$ MHz shows a flicker of -80 dBc/Hz extrapolated to 1 Hz (a rather poor value). Let us estimate the phase θ_{rms} and the delay x_{rms}.

For the purpose of convincing the reader that the flicker PM noise does not end in infinitely diverging phase and delay, we make an arbitrary and rather extreme choice of the frequency span. First, we agree that the lifetime of the device will not exceed 10^9 s (30 years), or we do not care about longer time. Accordingly, we take $f_1 = 10^{-9}$ Hz. Second, we agree that the bandwidth of the phase fluctuations is at most equal to the carrier frequency, thus we take $f_2 = 10^8$ Hz. From the statement of the problem, we find $\mathsf{b}_{-1} = 2 \times 10^{-80/10}$, and $\mathsf{k}_{-1} = \frac{\mathsf{b}_{-1}}{4\pi^2 f_0^2} = 5 \times 10^{-26}$. Thus,

$$\left\langle \theta^2 \right\rangle = \int_{f_1}^{f_2} \frac{\mathsf{b}_{-1}}{f}\, df = \mathsf{b}_{-1} \ln \frac{f_2}{f_1} = 2 \times 10^{-8}\ \ln \frac{10^8}{10^{-9}} = 7.8 \times 10^{-7}\ \text{rad}^2$$

hence $\theta_{\text{rms}} = 885$ μrad. Similarly

$$\left\langle \mathsf{x}^2 \right\rangle = \int_{f_1}^{f_2} \frac{\mathsf{k}_{-1}}{f}\, df = \mathsf{k}_{-1} \ln \frac{f_2}{f_1} = 5 \times 10^{-26} \ln \frac{10^8}{10^{-9}} = 2 \times 10^{-24}\ \text{s}^2$$

thus $\mathsf{x}_{\text{rms}} = 1.4$ ps.

The aforementioned results only mean that the internal delay of a device does not diverge in finite time. We encourage the reader to calculate θ_{rms} and x_{rms} in the most extreme conceivable case, where f_1 is the reciprocal of the age of the universe, and f_2 is the reciprocal of the Planck time. The result is surprisingly small. This does not change the fact that flicker is a major concern for oscillators and synthesizers. ■

Frequency Stability PSD

It is well known that the angular modulation can be expressed as a PM or as an FM, and that the two forms are equivalent. The same holds random PM and FM. The phase fluctuation associated to a frequency fluctuation is

$$\left(\Delta f_0\right)(t) = \frac{1}{2\pi} \frac{d\theta(t)}{dt} \tag{2-52}$$

Using the property of the Fourier transform that the time-domain derivative operator maps into a multiplication by $j2\pi f$,

$$dx(t)/dt \rightarrow j2\pi f X(f) \tag{2-53}$$

the PSD of $(\Delta f_0)(t)$ is given by

$$S_{\Delta f_0}(f) = f^2 S_\theta(f) \tag{2-54}$$

Alternatively, we can use the fractional frequency fluctuation $\mathsf{y}(t) = \frac{1}{f_0}\left(\Delta f_0\right)(t)$, and its PSD

$$S_{\mathsf{y}}(f) = \frac{f^2}{f_0^2} S_\theta(f) \tag{2-55}$$

The polynomial laws, rewritten for $S_{\mathsf{y}}(f)$, is (Figure 2-14)

$$S_{\mathsf{y}}(f) = \sum_{n \le -2}^{2} \mathsf{h}_n f^n \quad \text{with} \quad \mathsf{h}_n = \frac{1}{f_0^2} \mathsf{b}_{n-2}$$

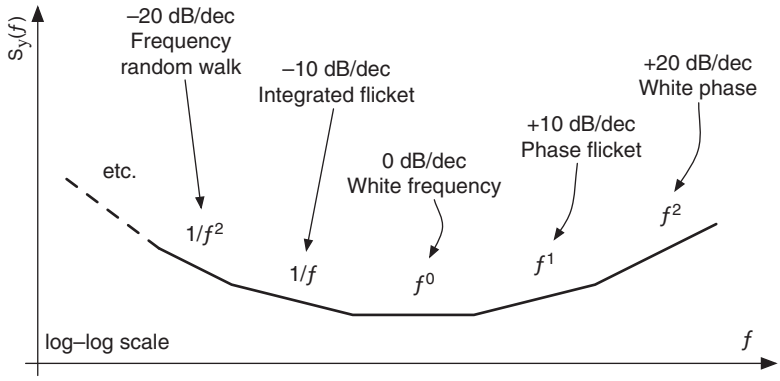


Figure 2-14 Polynomial law for frequency noise. Reprinted from [1], CC BY Rubiola.

The quantities $S_{\Delta f_0}(f)$ and $S_y(f)$ are seldom used in radio engineering. However, $S_y(f)$ is an important step to assess the relationship between phase noise and the time-domain variances Allan variance (AVAR), modified Allan variance (MVAR), parabolic variance (PVAR), etc.

The Low-Fourier-Frequency Part of the Phase Noise PSD

We have seen that the polynomial law fits the phase noise PSD in a large number of cases, that the polynomial law extends to low frequencies, and that the higher negative-power terms, found on the left-hand side of the plot, reveal the slow frequency fluctuations.

A question arises, can $S_\theta(f)$ be used to measure the long-term behavior of oscillators? Of course, $S_\theta(f)$ is a mathematical tool based on the measurement of the physical quantity $\theta(t)$; thus any valid mathematical manipulation yields correct results. However, $S_\theta(f)$ is not to a good tool for describing the long-term behavior, for the following reasons.

First, it is difficult to fit the experimental plot and to extract precisely the coefficients because the terms $\mathsf{b}_i f^i$ associated to drift and other slow phenomena have steep negative slope. The reader can try with the frequency random walk b_{-4}/f^4 or with the frequency drift b_{-6}/f^6.

Second, the measurement of a steep slope requires that the noise test set has a wide dynamic range. For example, the term b_{-4}/f^4 rises by 40 dB over a factor of 10 in frequency.

Third, the measurement time T needed to get $S_\theta(f)$ with a resolution δf is governed by the time-frequency indetermination theorem, which states that $T\,\delta f \geq 1$, where T and δf are the RMS values. The equality holds for Gaussian distributions. The theory underneath is found in many textbooks on the Fourier integral, among which we prefer Papoulis, 1962. Actual instruments work with the acquisition time T_a, which is a finite and well identified quantity. The acquisition time is associated to the window (taper) function used in the FFT analysis, the most popular of which is the Hanning window. In practice, the resolution is governed by $T_a\ \delta f \geq C_1$, with C_1 is in most cases of at least 2–3. The lowest frequency of the FFT is $f_1 = 1/T$. However, the first points may not be plotted, or discarded, because of the poor resolution $\delta f/f$ and because of artifacts related to the window function. The consequence is that the minimum plotted frequency is ruled by $T_a f_{\min} \geq C$, with C of the order of 5–10. For example, the acquisition of a single spectrum down to $f_{\min} = 10$ mHz gives $T_a = 600$ s ($C = 6$). If we decide to average on 12 spectra in order to get a comfortable confidence level, the measurement takes 2 h. By contrast, the AVAR and the other wavelet variances, described later in this chapter, are way more efficient at estimating the long-term behavior of oscillators in a short measurement time. Interestingly, all these variances are easily calculated from a time series of phase data, the same used to calculate the PM noise PSD.

The RF Spectrum of the Oscillator Signal

The oscillator signal, observed with an RF spectrum analyzer, looks like a rather narrow bell-shaped pattern, wobbling, wandering, and drifting. How does it relate to the PM noise PSD, which is seemingly unbounded at low Fourier frequencies?

However naïve the question may seem, the problem underneath is surprisingly complex. All difficulties start from the fact that the variance σ_θ^2 does not exist for flicker ($1/f$) and for steeper processes ($1/f^2$, $1/f^3$, etc.), and from the fact that the variance of the truncated $S_\theta(f)$, high-passed at a frequency f_H, diverges as $f_H \to 0$. Thus, the use of a high-pass filter does not help.

The problem of the line shape is addressed in [24–26]. These references rely on a rather difficult the mathematical framework and provide a separate solution for each PM noise process. Reference [26] is particularly useful for optics, where the line broadening phenomena are amplified by beating two laser beams down to RF. However, the language used in these references may be unusual or difficult to microwave engineer. That said, we try to grab the main physical facts.

First of all, the angular modulation does not affect the total electrical power, and the same happens with phase noise. Consequently, the generalized PM power, given in rad^2, is allowed to be quite large, and even to diverge in the long run, without violating the energy conservation principle. The pattern seen on the display of the spectrum analyzer reveals the average electrical power. The averaging time is set by 1/RBW or by 1/VBW, which is longer (RBW is the resolution bandwidth, and VBW is the video filter bandwidth).

Second, the electrical power is spread in sidebands, governed by the infinite series of Bessel functions $J_n(\beta)$, where β is the modulation index. The sidebands are separate entities at small β, but they collapse in a single line at large β. Something happens in between.

Third, the spectrum analyzer has a limited RBW. In the traditional scanning spectrum analyzer, the transfer function associated to the RBW is a Lorentzian line shape, determined by the intermediate frequency (IF) filter. The displayed shape results from the convolution of the input spectrum and the IF frequency response. The behavior of modern spectrum analyzers based on the FFT of a wide-band IF signal is rather similar, however more difficult to understand in rigorous mathematical terms. For the sake of clarity, let us say that the RBW is associated to a Lorentzian filter.

Now we apply the previous concepts to the oscillator signal.

When the oscillator delivers a pure and stable signal, the RF spectrum is a clean and sharp line, narrower than the instrument RBW. The displayed spectrum is a Lorentzian pattern determined by IF filter. Such pattern wanders and drifts slowly, following the oscillator frequency. The spectrum of white FM noise is a Lorentzian. Thus, if the dominant oscillator noise is white FM, wider than the RBW, the analyzer displays a Lorentzian determined by the oscillator FM noise. When flicker FM or FM random walk is dominant, the numerous random sidebands tend to cluster in Gaussian shape. However, if the width of the Gaussian is still comparable to the Lorentzian RBW, there results a Voigt distribution [27].

Until now, we have implicitly assumed that the frequency reference inside the spectrum analyzer is stable and free from noise. Actually, the displayed pattern results from the PM noise of both the oscillator under test and the analyzer's internal oscillator, and the two contributions are indistinguishable.

2-2 THE ALLAN VARIANCE AND OTHER TWO-SAMPLE VARIANCES

We study the frequency fluctuations of a real oscillator around the nominal value, as a function of the measurement time. Such fluctuations contain true random terms, plus other phenomena like drift and environmental effects. However, the environmental effects are of systematic origin; they can only be described statistically for the part of the environment that escapes from quantitative understanding. This goes under the term *influence quantities* in the formal language of metrology.

Before tackling the analysis of frequency fluctuations, we have to study the basic operation of the *frequency counters*, sometimes called *frequency-to-digital converters*. Other options are possible, chiefly time analyzers and phase meters. These instruments are highly specialized and seldom found in general laboratories.

Modern frequency counters are rather complex, and their statistical properties may be difficult to understand. Reference [28] reviews the high resolution counting techniques, and References [29, 30] provide insight in the statistical processing techniques.

2-2-1 Frequency Counters

The Π Frequency Counter

The Π counter is an instrument that measures frequency or period by counting a number of events occurring during the gate time τ. The classical frequency counter, shown in Figure 2-15, is the simplest example. The instrument counts the integer number N_x of cycles of the input signal in the gate time τ generated by the reference clock. The classical frequency counter is seldom used because of the poor resolution at low input frequency. If $\tau = 1$ s, the number N_x is equal to the frequency expressed in Hz, thus the measurement of the 50 Hz frequency of the European power grid suffers from a quantization of 2%. For this reason, the classical frequency counter is generally replaced with classical reciprocal counter. The roles of the clock signal and of the input signal are interchanged, and the instrument measures the average period by counting the clock cycles in a suitable multiple of the input period that approximates τ. With a clock frequency of 10 MHz, the quantization is 10^{-7} in 1 s measurement time, regardless of the input frequency. More sophisticated instruments can measure a fraction of a clock cycle by interpolating between edges of the clock signal. Combining reciprocal counting and clock interpolation boosts the resolution up to 10 digits and more, but the noise mechanism of the Π counter remains. In this type of instruments, the noise is determined by the fluctuations found at the *start* and at the *stop* event that define the gate time τ, and the fluctuations occurring between start and stop do not contribute to the result. In practice, the time fluctuations originate from the quantization noise, from the interpolator, and from the noise of the input trigger. With sophisticated interpolators, the remaining noise from the input trigger is the dominant noise source. The contribution of the frequency reference is not accounted here, and must be considered separately.

Since the input frequency fluctuates, it is useful to replace f_0 with $f_0 + (\Delta f_0)(t)$. The average frequency is given by

$$\overline{f_0} = \frac{1}{\tau} \int_0^{\tau} f_0 + \left(\Delta f_0\right)(t)\ dt \tag{2-56}$$

Introducing the fractional frequency fluctuation $\mathrm{y}(t) = \left(\Delta f_0\right)(t)/f_0$, we can replace the average (2-56) with the weighted average

$$\bar{\mathrm{y}} = \int_0^{\infty} \mathrm{y}(t)\ w_{\Pi}(t)\ dt \tag{2-57}$$

where

$$w_{\Pi} = \begin{cases} 1/\tau & 0 < t < \tau \\ 0 & \text{elsewhere} \end{cases} \tag{2-58}$$

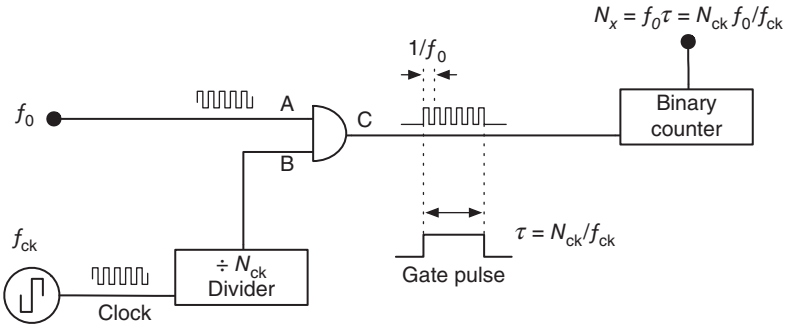


Figure 2-15 Classical frequency counter. Reprinted from [1], CC BY Rubiola.

The name Π counter was chosen because the Greek letter Π recalls shape of $w_\Pi(t)$, which is a rectangular pulse.

The value of our approach is that (2-57) also describes the other counters, just by replacing the weight function $w_\Pi(t)$ with another weight $w(t)$ of our choice. Of course, it is necessary that

$$\int_{-\infty}^{\infty} w(t)\ dt = 1 \tag{2-59}$$

for $w(t)$ to be a valid weight function.

Denoting with σ_x^2 the variance (time fluctuation) associated to each trigger event, the variance of the fractional frequency fluctuation is

$$\sigma_y^2 = \frac{2\sigma_x^2}{\tau^2} \tag{2-60}$$

The factor of 2 comes from the fact that σ_x^2 counts twice, start and stop being statistically independent events. It is to be made clear that (2-60) is the classical variance, as opposite to the two-sample variances that we will introduce later.

Example 4 Frequency Counter. Consider the measurement of a 10 MHz oscillator with a gate time of 100 ms. The instrument has a quantization $\delta t = 5$ ns, and the trigger noise is negligible in this case. The time deviation (TDEV) associated to the quantization noise is $\sigma_x = \delta t/\sqrt{12} = 1.44$ ns. The factor $1/\sqrt{12}$ accounts for the quantization uniformly distributed between $\pm\delta t/2$. Using (2-60) with $\tau = 100$ ms, we find $\sigma_y = \sqrt{2} \times (2 \times 10^{-9}\ \text{s}) / (10^{-1}\ \text{s}) = 2.5 \times 10^{-8}$. The same reasoning applies to the noise in the input trigger, just omitting the $1/\sqrt{12}$ factor, which is characteristic of the quantization. ■

The Λ Frequency Counter

Looking at Figure 2-16, there is a lot of information contained in the fluctuations occurring between the edges of the gate function, which can be exploited to reduce the background noise of the instrument. This requires a different type of hardware, capable of timing more transitions, ideally all the transitions between the two edges. With FPGA technology, such hardware is affordable even in moderate-cost instruments.

The first method to reduce the instrument noise is the Λ counter, whose principle is shown in Figure 2-17. The measurement process consists of averaging n highly overlapped measures of duration τ, spaced by $\tau_0 = \tau/n$. These n measures are the same as in the Π counter. The benefit of the Λ counter derives from the fact that most of the random fluctuations come from the input trigger, which is a wideband stage. Therefore, the white PM noise is dominant, and the samples of such noise, taken at t_0, t_1, t_2, etc., are statistically independent. Thus, the process of averaging on n independent values reduces σ_y^2 by a factor $1/n$. This noise reduction comes at the cost of a longer measurement time, 2τ instead of τ. Ideally, n is maximized by taking a measure at each cycle of the input signal,

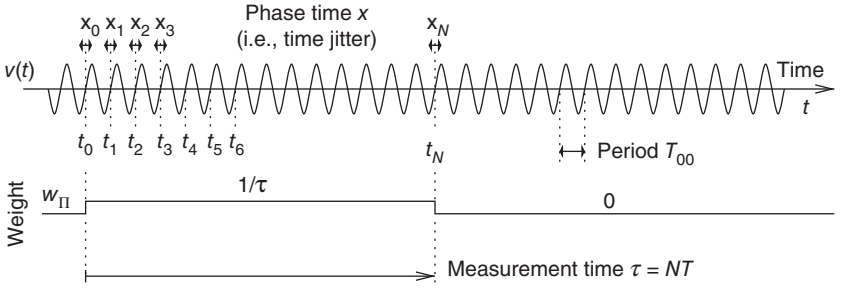


Figure 2-16 Theory of operation of the Π (classic) frequency counter. Reprinted from [29], with the permission of AIP Publishing.

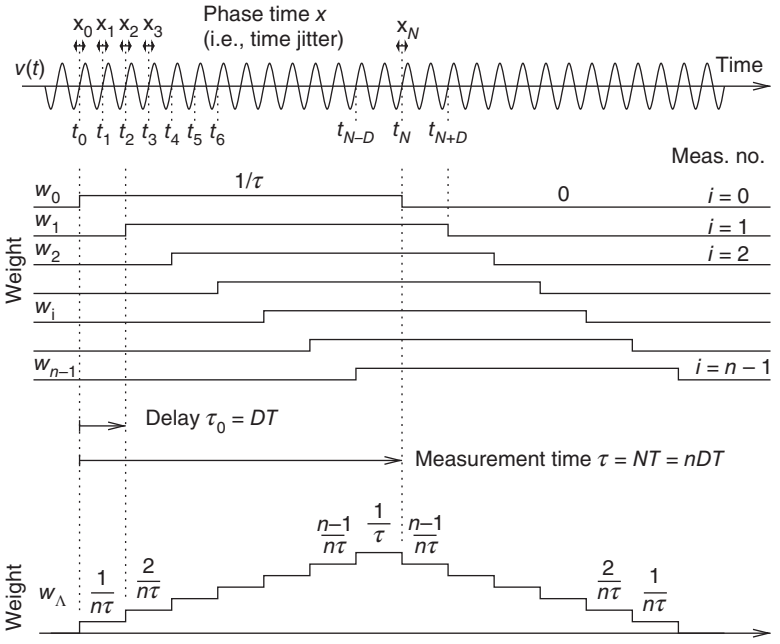


Figure 2-17 Theory of operation of the Λ frequency counter. Reprinted from [29], with the permission of AIP Publishing.

that is, with $\tau_0 = 1/f_0$. However, τ_0 is limited by the data transfer inside the instrument and by the processing rate. In commercial equipment, we find values between a millisecond and a fraction of a microsecond.

In the last example, the standard deviation is reduced from 2.5×10^{-8} to 2.5×10^{-9} if the instrument has a minimum τ_0 of 1 ms ($n = 100$), and to 2.5×10^{-10} if the minimum τ_0 is of 10 µs ($n = 10^4$).

The following points deserve attention before doing statistics with frequency counters:

- Some commercial instruments use the Λ averaging without saying. Of course, the statistical properties are totally different from the Π counter.
- The "gate time" shown on the front panel may be ambiguous. It can be identified either with τ or with the total measurement time, which is 2τ in our notation.
- The gate events can be contiguous, or exactly overlapped by one side of the triangle. The decimation rule is a good reason to choose the overlapped option. Suppose we have a stream of data $f_1, f_2, f_3, \ldots$ overlapped by one side. The rule

$$f_1' = \frac{1}{4}f_1 + \frac{1}{2}f_2 + \frac{1}{4}f_3$$

$$f_2' = \frac{1}{4}f_3 + \frac{1}{2}f_4 + \frac{1}{4}f_5$$

  etc. gives a new data stream with the same type and overlap. The new n is twice the older, and τ is twice longer. By contrast, if the triangles are just contiguous, there is no decimation rule preserving unchanged statistical properties.
- Understanding the internal operation and the meaning of the gate time requires attention and some tests. It is useful to observe the counter readout in the presence of a phase-modulated RF signal. We can get information about the weight function by setting the modulation frequency for the readout to be constant, and for the readout to have the maximum fluctuation.

A more formal description of the Λ counter is the following. We start from a time series of n highly-overlapped measures f_i, of the same type of the Π counter. Each measure is shifted by $\tau_0 \ll \tau$ with respect to the previous one

$$f_i = \frac{1}{\tau} \int_{i\tau_0}^{i\tau_0+\tau} f_0 + (\Delta f)(t)\ dt \qquad i = 0 \ \ldots \ n-1 \tag{2-61}$$

Averaging on these n measures gives

$$\bar{f} = \frac{1}{n} \sum_{i=0}^{n-1} f_i \tag{2-62}$$

Replacing $f_0 + (\Delta f)(t)$ with the fractional frequency $\mathrm{y}(t)$, we write the weighted average

$$\bar{\mathrm{y}} = \int_0^{\tau} \mathrm{y}(t)\ w_\Lambda(t)\ dt \tag{2-63}$$

Taking the limit for large n, thus for $\tau_0/\tau \to 0$, the staircase function shown on Figure 2-17 becomes a triangular function

$$w_\Lambda(t) = \begin{cases} t/\tau^2 & 0 < t < \tau \\ 2/\tau - t/\tau^2 & \tau < t < 2\tau \\ 0 & \text{elsewhere} \end{cases} \tag{2-64}$$

It follows from our reasoning that the variance of the fractional frequency fluctuation is

$$\sigma_{\mathrm{y}}^2 = \frac{1}{n} \frac{2\,\sigma_{\mathrm{x}}^2}{\tau^2} = \tau_0 \frac{2\,\sigma_{\mathrm{x}}^2}{\tau^3} \tag{2-65}$$

This is the same as (2-60), but for a factor $1/n$ that accounts for the average on n measures.

As the reader may expect after our digression, the name Λ counter is due to the graphical analogy of the Greek letter Λ with the triangular step function shown on Figure 2-17.

The Ω Frequency Counter

The total phase $\vartheta(t)$ of the clock signal the ever-growing ramp described as

$$\vartheta(t) = 2\pi \int f_0 + (\Delta f)(t)\ dt = 2\pi f_0 t + \theta(t) \tag{2-66}$$

whose fluctuation is $\theta(t) = 2\pi \int (\Delta f)(t)\ dt$ as the frequency fluctuates. The instantaneous frequency is

$$f(t) = \frac{1}{2\pi} \frac{d\vartheta(t)}{dt} \tag{2-67}$$

The Ω counter measures the average frequency $\bar{f}$ using the *linear regression* on the time series ϑ_0, ϑ_1, ϑ_2 … sampled at regular intervals spaced by τ_0, as shown in Figure 2-18. Denoting with t_i the time when the sample ϑ_i is taken, and with μ_ϑ and $\mu_t$the averages of ϑ and t in the measurement time τ, we find

$$\bar{f} = \frac{1}{2\pi} \frac{\sum_{i=0}^{n-1} \left(\vartheta_i - \mu_\vartheta\right)\left(t_i - \mu_t\right)}{\sum_{i=0}^{n-1} \left(t_i - \mu_t\right)^2} \tag{2-68}$$

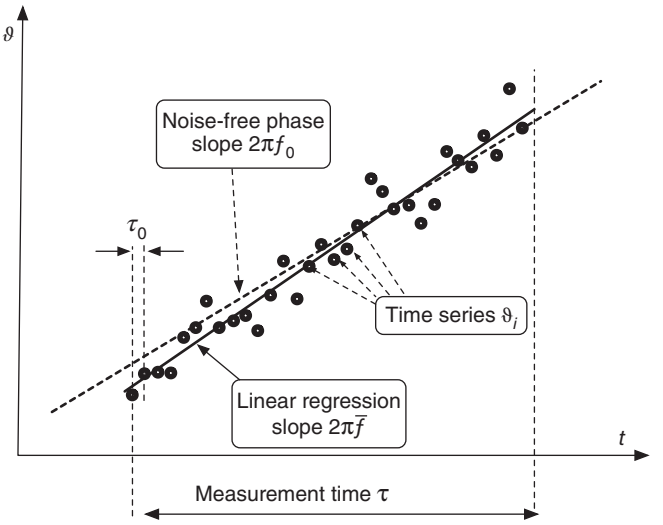


Figure 2-18 Operation of the Ω frequency counter, which measures the average frequency using the linear regression on phase data. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

Replacing $f_0 + (\Delta f)(t)$ with the fractional frequency $\mathrm{y}(t)$, we write the weighted average

$$\bar{\mathrm{y}} = \int_0^\tau \mathrm{y}(t)\ w_\Omega(t)\ dt \tag{2-69}$$

The mathematics underneath is a little more complex than in the case of the Π and Λ counters, and the details are found in Reference [23]. The weight function has the "cap" parabolic shape

$$w_\Omega(t) = \begin{cases} \dfrac{6t}{\tau^2}\left[1 - \dfrac{t}{\tau}\right], & 0 < t < \tau \\ 0, & \text{elsewhere} \end{cases} \tag{2-70}$$

The name Ω has been chosen by the graphical analogy of $w_\Omega(t)$ with the Greek letter Ω, in the continuity of the Π and Λ counters. The theory indicates that the Ω counter exhibits the highest rejection of white PM noise, which is exactly what we want to reduce the effect of the quantization and of the trigger noise.

The variance of the fractional frequency is

$$\sigma_{\mathrm{y}}^2 = \frac{1}{n}\,\frac{12\,\sigma_{\mathrm{x}}^2}{\tau^2} = \tau_0 \frac{12\,\sigma_{\mathrm{x}}^2}{\tau^3} \tag{2-71}$$

Comparison of the Frequency Counters

The performance of the frequency counters is described by the variance σ_{y}^2, that is, (2-60), (2-65), or (2-71). These equations give the background noise of the instrument in the presence of white PM noise (input trigger and quantization). The frequency reference is still not included.

We will learn in Section 2-2-2 that the measurement time τ is a more complex issue, and why the two-sample variances are necessary. That said, the classical variance is perfectly suitable to describe the white phase noise. In the meanwhile, we can draw some conclusions about the time required to test an oscillator, with obvious implications on industrial production. It goes without saying that the instrument background noise must be smaller than the noise of the oscillator under test. This sets a minimum measurement time needed to average out the instrument background.

First, the instrument noise is averaged out proportionally to $1/\tau^2$ in the Π counter, and proportionally to $1/\tau^3$ in the Λ counter and in the Ω counter. Thus, the Π counter is clearly slower in all cases. The two other counters are similar in speed, being governed by the $1/\tau^3$ law.

Second, a comparison between (2-65) and (2-71) gives the false impression that the Ω counter suffers from more noise than the Λ counter, by a factor of six. The catch is that the Λ counter takes a time 2τ to deliver a value, while the Ω counter takes τ. For fair comparison, we have to replace $\tau \to \tau/2$ in (2-65), so that the measurement time is the same. This gives $\sigma_y^2 = 16\,\tau_0\sigma_x^2/\tau^3$ for the Λ counter. The conclusion is that the Ω counter is superior to the Λ counter, to the extent that, for the same measurement time, it exhibits lower noise by a factor of ¾ (1.25 dB). However modest this result may seem, it can be a great choice for large volume tests.

Most old frequency counters work in Π mode.

Major manufacturers sell Λ counters, often without saying. Eventually, Reference [29] originated from the attempt to sort out inconsistent results when we measured some oscillators using an Agilent (now Keysight) counter. We could interpret correctly these results only after setting the formal framework that describes the Π and Λ counters, and after reverse engineering the counter we had. Lange Electronics manufactures a counter specifically intended for the measurement of the two-sample variances, which can be programmed to operate in Π and Λ mode. Pendulum (later acquired by Philips, to the best of our knowledge) was arguably the first company to produce a counter using the linear regression [31]. The statistical properties of the Ω counters were tackled independently in [30, 32, 33]. Recently, Carmel Instruments (formerly Brilliant Instruments) manufactures some time analyzers implemented as PXI Express modules, advertised as capable to operate in Π, Λ, and Ω modes.

2-2-2 The Two-Sample Variances AVAR, MVAR, and PVAR

Until now, we have implicitly used the experimental variance found in many textbooks, defined as

$$\sigma_y^2 = \frac{1}{N-1}\sum_{k=1}^{N}\left(y_k - \mu\right)^2 \tag{2-72}$$

where N is the number of samples f_k, and $\mu = \frac{1}{N}\sum_{k=1}^{N} y_i$ is the average. The problem is that (2-72) is useful only for certain types of fluctuations, and of course it works perfectly with the white PM noise we were really concerned about. In such cases (2-72) converges to the "ideal" value called *mathematical expectation*, and the confidence improves progressively as N increases.

The problem is that real oscillators suffer from frequency flicker, random walk, and drift, and other processes. These processes make (2-72) depend on both N and τ, and the mathematical expectation does not exist. That something goes wrong with N and is clearly seen with linear drift (constant aging). Try yourself to calculate the deviation σ in the case of a 100 MHz oscillator drifting by +1 mHz/s, measured with s gate time of 1 s. After taking $N = 10, 10^2, 10^3$, etc., we agree that the experimental variance is not a good choice in this case.

The problem with τ is a little bit subtler. Let us take the distance from two points on a sheet of sandpaper as a simple example. A human-sized ruler may indicate a distance quite close to 6 in., which we perceive as "correct" at our scale, and that's it. By contrast, a tiny insect experiences a much longer path of consisting of high obstacles it can surmount only thanks to its incredible agility. What happens? The answer is that the distance depends on the size of the ruler used to measure it. Not surprisingly, something similar happens with the oscillator fluctuations $y(t)$ and the measurement time τ. Still on the example of the 100 MHz oscillator drifting at +1 mHz/s, try yourself to calculate σ_y^2 as using (2-72) after switching the gate time to 0.1, 1, and 10 s. The difference between results should convince the reader that (2-72) is to be replaced with a more appropriate tool. Here the family of two-sample (Allan and Allan-like) variances gets on the stage. The key points are as follows:

- The measurement time τ is made explicit
- The variance is calculated using a simple and perfectly defined pattern.

The Allan Variance (AVAR)

Let us first introduce the average fractional frequency $\overline{y}_k(\tau)$, defined as

$$\overline{y}_k(\tau) = \int_{(k-1)\tau}^{k\tau} y(t)\ dt \tag{2-73}$$

This is the fractional frequency y we are familiar with, measured with a Π counter where the gate time has duration τ starting at $t = (k-1)\tau$ and ending at $t = k\tau$. So, $\overline{y}_1(\tau)$ is averaged between 0 and τ, $\overline{y}_2(\tau)$ is averaged between τ and 2τ, etc. It is important that the measures are exactly contiguous, with no dead time in between, otherwise the final result will differ from the AVAR. This requirement is not a real limitation because the speed of nowadays digital hardware is generally sufficient to avoid such dead time. Understanding what happens in the presence of a dead time is a special topic for experts.

Having defined τ, we solve the dependence on N by setting $N = 2$ in (2-72). Notice that $N = 2$ is the smallest value that gives a valid variance. Rewriting (2-72) for $N = 2$

$$\sigma_y^2(\tau) = \left[\overline{y}_2(\tau) - \mu\right]^2 + \left[\overline{y}_1(\tau) - \mu\right]^2 \tag{2-74}$$

and expanding using $\mu = \left(\overline{y}_2 + \overline{y}_1\right)/2$, we find the two-sample variance

$$\sigma_y^2(\tau) = \frac{1}{2}\left[\overline{y}_2(\tau) - \overline{y}_1(\tau)\right]^2 \tag{2-75}$$

This variance is also called the *Allan variance* [2] or AVAR. The obvious notation Allan deviation (ADEV) is often used for $\sigma_y(\tau)$. Equation (2-75) should be intended in the sense of the mathematical expectation, that is, the ideal average on infinite values of $\sigma_y^2(\tau)$. In practice, we use a finite time series of M contiguous values of $\overline{y}_k(\tau)$, $k = 1 \ldots M$. Consequently the average on $M-1$ values of $\left[\overline{y}_{k+1}(\tau) - \overline{y}_k(\tau)\right]^2$ gives

$$\sigma_y^2(\tau) = \frac{1}{2(M-1)} \sum_{k=1}^{M} \left[\overline{y}_{k+1}(\tau) - \overline{y}_k(\tau)\right]^2 \tag{2-76}$$

Equation (2-76) is the usual formula for the AVAR. Figure 2-19 shows the most common noise types, as they appear on the AVAR plot.

It is a common practice to use a counter with a gate time τ_0 and to combine 2^m contiguous measurements to get $\tau = 2^m\tau_0$. In this case, the terms $\left[\overline{y}_{k+1}(\tau) - \overline{y}_k(\tau)\right]$ used in (2-76) can be highly overlapped, and spaced by τ_0. Strictly speaking, this is the *overlapped Allan variance*. For the same noise process, overlapped AVAR and non-overlapped AVAR converge to the same value. The overlapped AVAR is always used because exhibits superior confidence level for finite M.

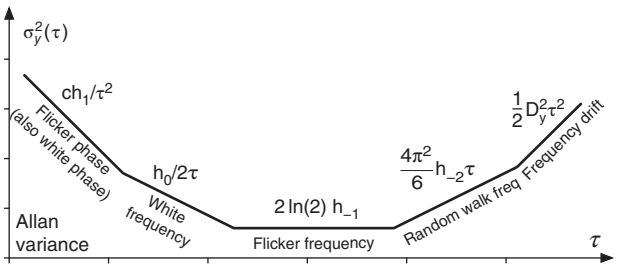


Figure 2-19 Allan variance, plotted for the most common noise terms of the polynomial law. The constant *c* results from a cutoff frequency f_H, necessary to limit the bandwidth of white phase noise. Reprinted from [1], CC BY Rubiola.

Some confusion may arise with the notation $\sigma_y^2(\tau)$ because the number of samples is implied. A more rigorous notation would be $\sigma_y^2(N, \tau)$ for the N-sample variance, and consequently $\sigma_y^2(2, \tau)$ for AVAR, but this notation is seldom used. Notice that the AVAR is always represented as a function of τ, while it is rather uncommon to find τ in the classical variance (our Section 2-2-1 is a necessary exception). Another confusion is around the corner, between AVAR and other similar variances, some of which are described described below.

The Modified Allan Variance (MVAR)

The modified Allan variance [34, 35], denoted with $\mathrm{mod}\,\sigma_y^2(\tau)$ or MVAR, is similar to the AVAR and uses the same formula (2-76), but the weight function used to calculate the average $\overline{y}$ is replaced with $w_\Lambda(t)$. In practice, a Λ counter is used instead of the Π counter, or implement the Λ average in some other ways—the latter option is let to the experts. Using the Λ counter, we should make sure that averaging is done correctly:

- The time τ is interpreted as in Figure 2-17. Accordingly, the measurement of a single $\overline{y}_k(\tau)$ takes a time 2τ.
- Two "contiguous" measures overlap by τ. Thus, the $(k+1)$-th measure starts exactly in the middle of the k-th measure. In other words, the falling side of the k-th measure overlaps exactly to the rising side of the $(k+1)$-th measure. Consequently, the measurement of $\overline{y}_{k+1}(\tau) - \overline{y}_k(\tau)$ takes 3τ.

In the domain of oscillators, frequency synthesis, and telecomm, MVAR should be preferred to AVAR because of its superior capability to divide the fast noise processes, namely, white PM and flicker PM. More details are given in the review article [36].

The Parabolic Variance (PVAR)

The parabolic variance, denoted with "par $\sigma_y^2(\tau)$" or PVAR, relies the same formula (2-76) already used for AVAR and PVAR, but the stream of values $\overline{y}_k(\tau)$ results from Ω averaging (2-69), and the measures are exactly contiguous. Consequently, replacing the Π counter with an Ω counter, we obtain PVAR.

2-2-3 Conversion from Spectra to Two-Sample Variances

We have seen that both the PSD of frequency noise and the two-sample variances are valid measures of the frequency stability. The obvious question arises, about how to convert data between these two worlds. The question is best answered after rewriting the general formula (2-75) for the two-sample variance as

$$\sigma_y^2(\tau) = \left[\int_0^\infty y(t)\ w(t)\ dt \right]^2 \tag{2-77}$$

where the weight function $w(t)$ is either $w_A(t)$, $w_M(t)$, or $w_P(t)$, plotted in Figure 2-20. As one can expect, the subscripts A, M, and P stand for Allan, modified Allan, and parabolic, respectively. Hence, the two-sample variance can be seen as the filter described by

$$\sigma_y^2(\tau) = \int_0^\infty S_y(f)\ |H(f)|^2\, df \tag{2-78}$$

where the transfer function $H(f)$ is the Fourier transform of the impulse response $h(t)$, which is equal to $w(-t)$, and the trivial subscripts A, M, and P apply. After some boring math, it can be proved that

$$\left|H_A(f)\right|^2 = 2\frac{\sin^4(\pi\tau f)}{(\pi\tau f)^2} \tag{2-79}$$

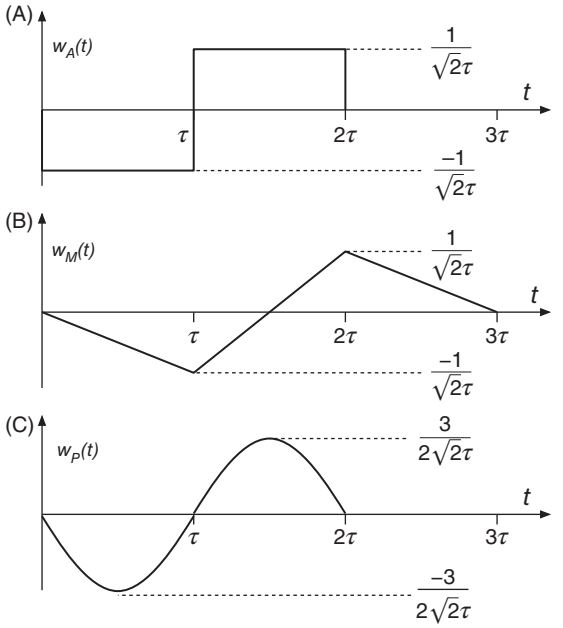


Figure 2-20 Weight function used in (A) AVAR, (B) MVAR, and (C) PVAR. Reprinted from [1], CC BY Rubiola.

$$\left|H_M(f)\right|^2 = 2\frac{\sin^6(\pi\tau f)}{(\pi\tau f)^4} \qquad \text{for } \tau \gg \tau_0 \tag{2-80}$$

$$|H_P(f)|^2 = 9\frac{\left[2\sin^2(\pi\tau f) - \pi\tau f\ \sin(2\pi\tau f)\right]^2}{2(\pi\tau f)^6} \qquad \text{for } \tau \gg \tau_0 \tag{2-81}$$

Should the reader wish to calculate $|H(f)|^2$ by hand, the exercise is simpler if $w(-t)$ is shifted and centered at $t = 0$. Of course, the phase introduced by this time shift has no effect on $|H(f)|^2$.

We can see in Figure 2-21 that $|H_A(f)|^2$, $|H_M(f)|^2$, and $|H_P(f)|^2$ are bandpass filters with a bandwidth of approximately one octave centered at $f \approx 0.4/\tau \ldots 0.45/\tau$. Center frequency and bandwidth are not the same for the three functions. For high frequency, $|H_A(f)|^2$ rolls off as $1/f^2$. For this reason, an additional low-pass filter at a suitable cutoff frequency f_H is necessary if the fluctuations contain white and flicker phase noises. An interesting treatise is given in [37]; however the language may be more difficult because this article is about an application in optical fibers. Such filter is not necessary for MVAR and PVAR because $|H_M(f)|^2$ and $|H_P(f)|^2$ roll off as $1/f^4$. However, a low-pass filter at the cutoff frequency $1/(2\tau_0)$ is implied in MVAR and PVAR because these variances result from sampling $y(t)$ at the rate $1/\tau_0$.

Equations (2-79)–(2-81) enable the conversion from $S_y(f)$ to $\sigma_y^2(\tau)$. The reverse conversion, from $\sigma_y^2(\tau)$ to $S_y(f)$, is not possible in the general case. The reason is that the frequency responses (Figure 2-21) have side lobes at high frequency. Hence, a point on the $\sigma_y(\tau)$ plot represents the FM noise at the center of the bandpass, plus the FM noise captured by these side lobes. The side lobes are smaller for MVAR and PVAR.

Table 2-6 provides all the formulas to convert from PM or FM noise PSD to the three variances described.

Comparison Between AVAR, MVAR, and PVAR

A few more questions arise. First, why are MVAR and PVAR used, after the original AVAR? Second, if these alternate variances are more modern and efficient, why do they not have replaced the AVAR? And third, why do all these variances give different values (Table 2-6) for the same noise process?

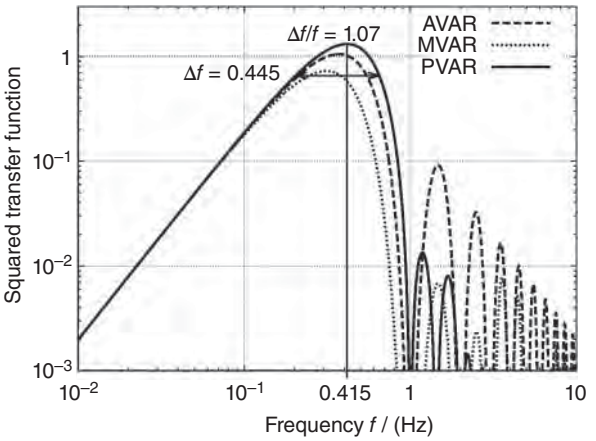


Figure 2-21 Frequency response associated to AVAR, MVAR, and PVAR. Reprinted with permission from [32].

Table 2-6 Noise response of the two-sample variances

Noise type	$S_\theta(f)$	$S_y(f)$	$S_\theta \leftrightarrow S_y$	AVAR $\sigma_y^2(\tau)$	MVAR mod $\sigma_y^2(\tau)$	PVAR $\sigma_y^2(\tau)$
White PM	b_0	$h_2 f^2$	$h_2 = \frac{b_0}{\nu_0^2}$	$\frac{3f_H}{4\pi^2}\frac{h_2}{\tau^2}$ $0.0760 f_H h_2/\tau^2$	$\frac{3}{8\pi^2}\frac{h_2}{\tau^3}$ $0.0380\, h_2/\tau^3$	$\frac{3}{2\pi^2}\frac{h_2}{\tau^3}$ $0.1520\, h_2/\tau^3$
Flicker PM	$b_{-1} f^{-1}$	$h_1 f$	$h_1 = \frac{b_{-1}}{\nu_0^2}$	$\frac{3\gamma - \ln 2 + 3\ln(2\pi f_H \tau)}{4\pi^2}\frac{h_1}{\tau^2}$ $[3\gamma - \ln 2 + 3\ln 2\pi]/4\pi^2 = 0.166$	$\frac{(24\ln 2 - 9\ln 3)}{8\pi^2}\frac{h_1}{\tau^2}$ $0.0855\, h_1/\tau^2$	$\frac{3[\ln(16) - 1]}{2\pi^2}\frac{h_1}{\tau^2}$ $0.2694\, h_1/\tau^2$
White FM	$b_{-2} f^{-2}$	h_0	$h_0 = \frac{b_{-2}}{\nu_0^2}$	$\frac{1}{2}\frac{h_0}{\tau}$	$\frac{1}{4}\frac{h_0}{\tau}$	$\frac{3}{5}\frac{h_0}{\tau}$
Flicker FM	$b_{-3} f^{-3}$	$h_{-1} f^{-1}$	$h_{-1} = \frac{b_{-3}}{\nu_0^2}$	$2\ln(2)\, h_{-1}$ $1.3863\, h_{-1}$	$\frac{27\ln 3 - 32\ln 2}{8} h_{-1}$ $0.9352\, h_{-1}$	$\frac{2[7 - \ln(16)]}{5} h_{-1}$ $1.691\, h_{-1}$
Random walk FM	$b_{-1} f^{-4}$	$h_{-2} f^{-2}$	$h_{-2} = \frac{b_{-4}}{\nu_0^2}$	$\frac{2\pi^2}{3} h_{-2}\tau$ $6.5797\, h_{-2}\tau$	$\frac{11\pi^2}{20} h_{-2}\tau$ $5.4283\, h_{-2}\tau$	$\frac{26\pi^2}{35} h_{-2}\tau$ $7.3317\, h_{-2}\tau$
Linear frequency drift D_y				$\frac{1}{2}D_y^2\tau^2$	$\frac{1}{2}D_y^2\tau^2$	$\frac{1}{2}D_y^2\tau^2$

The formulas for MVAR and PVAR hold for $\tau \gg \tau_0$, being τ_0 the sampling interval.
MVAR and PVAR formular need $\tau > 1/f_H$, where $f_H < 1/2\tau_0$ is the cutoff frequency, and t_0 is the sampling interval.
Source: Reproduced from the 2019 *Enrico's Chart of Phase Noise and Two-Sample Variances*, http://rubiola.org, and adapted to our notation. CC BY Rubiola.

The original AVAR was invented at NBS (the ancient name of NIST) to describe the stability of the atomic clocks used in the time scale. Monitoring the long-term performance of clocks is of paramount importance in this application. When a long data record is available (say, 6 years), we wish to plot $\sigma_y(\tau)$ for τ as large as possible, as close as possible to half of the data record (3 years). AVAR is still the best we have for this purpose, and still the standard tool used by National Laboratories to monitor their primary clocks. Additionally, AVAR has been studied for longer time, and many technical publications are available. It is therefore not a surprise that the engineers and practitioners tend to believe that the Allan deviation is what they should use.

The MVAR came in the 1980s from the field of optics as a better alternative to AVAR for the measurement of fast phenomena. The main features of MVAR are the superior rejection of the instrument noise, related to the Λ counter, and the power to resolve between flicker PM and white PM, which impossible with AVAR. For this reason, MVAR is highly recommended for all applications we are concerned with, like telecom, oscillators, and frequency synthesis. By contrast, MVAR is not a good choice to measure the long-term instability of atomic clocks. The reason is that w_M spans over 3τ, instead of 2τ for w_A. For example, with a data record of 6 years, the maximum τ without averaging is of 3 years for AVAR, and of 2 years for MVAR.

The Parabolic Variance, par $\sigma_y^2(\tau)$, or PVAR, is much less known because it has been proposed only in 2015. Compared with MVAR, PVAR is superior in all cases and for all types of noise, to the extent that it enables the measurement of noise processes with a shorter data record. Compared with AVAR, we notice that PVAR is a better choice in most cases, but it is slightly less suitable to the measurement of the slowest phenomena, like frequency random walk and drift of atomic clocks, where one wants the result with the shortest data record. PVAR is superior to MVAR in all cases for the detection of random processes [32], thus we can expect that it will replace MVAR. However, at the time of writing, PVAR is still not present in standards, in recommendations, and in software packages.

The three tools start from the same formula $\sigma_y^2(\tau) = \left[\overline{y}_2(\tau) - \overline{y}_1(\tau)\right]^2/2$, but the averages $\overline{y}(\tau)$ are different. Thus, it is not a surprise that we end up with different statistical properties. We see in Table 2-6 that the response to the linear drift is the same. This results from a choice of normalization (scale factor), which has historical roots. By contrast, an engineer with a background in signal processing would have probably scaled MVAR E. Rubiola and PVAR for equal response to white FM noise, which is the white noise of the quantity $y(t)$. The different coefficients found in Table 2-6 do not mean that one variance is better than another, no more than inches are a better or worse unit than centimeters.

Example 5 Two-Sample Variances. The phase noise spectrum of a 100 MHz oscillator has the following noise terms, extrapolated to 1 Hz. Calculate the two-sample deviations ADEV, modified (Allan) deviation (MDEV), and parabolic deviation (PDEV). For ADEV, use $f_H = 500$ Hz.

Noise type	RW FM	Flicker FM	White FM	Flicker PM	White PM
Slope	$1/f^4$	$1/f^3$	$1/f^2$	$1/f$	Constant
$L(f)$	−99 dBc/Hz	−134 dBc/Hz	(NA)	−164 dBc/Hz	−180 dBc/Hz
At $f =$	10 Hz	100 Hz	(NA)	1 kHz	10 kHz

Let us start with the FM random walk, which rolls off as $1/f^4$, that is, −40 dB/decade. The value of −99 dBc/Hz at 10 Hz is equivalent to −59 dBc/Hz extrapolated at 1 Hz. The corresponding term of $S_\theta(f)$ is b_{-4}/f^4, with $b_{-4} = 10^{(-59+3)/10} = 2.5 \times 10^{-6}$ rad^2/Hz^3. We convert $S_\theta(f)$ into $S_y(f)$ using $S_y(f) = \left(f/f_0\right)^2 S_\theta(f)$. The FM random walk of $S_y(f)$ is h_{-2}/f^2, with $h_{-2} = b_{-4}/f_0^2 = 2.5 \times 10^{-6}/\left(10^8\right)^2 = 2.5 \times 10^{-22}$ Hz^{-3}.

Then, we follow the same steps with the flicker FM (−30 dB/decade). We calculate the coefficient b_{-3} of $S_\theta(f)$, and in turn the term h_{-1} of $S_y(f)$. And we repeat for all the other noise terms.

Finally, we use the formulas found in Table 2-6 to calculate the two-sample deviations.

Noise type	ADEV	MDEV	PDEV
White PM	$1.52 \times 10^{-15}/\tau$	$2.76 \times 10^{-18}/\tau\sqrt{\tau}$	$5.51 \times 10^{-18}/\tau\sqrt{\tau}$
Flicker PM		$8.25 \times 10^{-16}/\tau$	$1.46 \times 10^{-15}/\tau$
White FM	(NA)	(NA)	(NA)
Flicker FM	3.32×10^{-12}	2.73×10^{-12}	3.70×10^{-12}
RW FM	$4.07 \times 10^{-11}\ \sqrt{\tau}$	$3.70 \times 10^{-11}\ \sqrt{\tau}$	$4.30 \times 10^{-11}\ \sqrt{\tau}$

■

2-3 PHASE NOISE IN COMPONENTS

2-3-1 Amplifiers

Amplifiers are the most ubiquitous element in a synthesizer and serve to different purposes. Amplification is necessary in numerous parts of the circuits, for example, to raise the power after the loss associated to frequency conversion, or after splitting a signal into several branches. Second, it is an absolute necessity to provide isolation between the VCO and the following circuits (e.g., the divider chain or others) to minimize any feedback or noise contribution because of periodic loading. Similarly, high isolation amplifier is necessary at the output of the reference oscillator. Then, power amplification must be provided at the output. Different design rules follow, depending on whether the engineer designs with transistors, or at system level by assembling blocks. The latter approach is privileged here. A wider treatise of phase noise in amplifiers is given in Ref. [38]. We restrict our attention to amplifiers at room temperature, within a reasonable range. High-temperature and cryogenic electronics are highly specialized topics, beyond our scope.

White and Flicker Phase Noise

If we assume that we generate our signal in a noise-free environment, or at least start off with the theoretical minimum of −174 dBm/Hz set by the thermal noise generated by a resistor at room temperature, the signal will be degraded by the amplifier that follows. In virtually all cases, the amplifier can be described in terms of the noise factor F. For reference, the noise factor of most microwave amplifiers is of 1–3 dB. A value of 0.4–0.5 dB is found in some special narrowband amplifiers, while power amplifiers often have a noise factor of 6 dB and more.

The white phase noise of a signal of power P_0 is

$$S_\theta(f) = \frac{FkT_0}{P_0} \tag{2-82}$$

This is the term b_0 of the power law we have seen in Section 2-1-4.

The white noise floor can be observed only beyond a cutoff offset frequency. Various noise sources must be taken into consideration, affecting low offset frequencies. As mentioned previously, flicker noise is the major reason for the noise degradation, and its contribution is device-dependent and can range from a few hundred hertz to 1 MHz. It is caused by internal near-dc noise modulating the phase of the passing signal, and the input and output impedances of the amplifier. References [39–41] provide a more detailed analysis and guidelines for bipolar transistors.

It has already been observed long time ago [42] that the amplifier's flicker of phase, that is, the term b_{-1} of the power law, is rather independent of the carrier power P_0 in a relatively wide power range from very small signals to moderate clipping, and it is also rather independent of carrier frequency in the amplifier bandwidth. Moreover, the spread of values for amplifiers of similar technology and different manufacturers is surprisingly small. Figure 2-22 shows an example of amplifier PM noise, measured at different levels of input power.

The coefficient b_{-1} can be considered a characteristic parameter of the amplifier. We can take as a reference the following values: −100 to −110 dB rad^2/Hz for microwave amplifiers, up to 20 GHz; −120 dB rad^2/Hz for microwave amplifiers in SiGe technology (which unfortunately have a high noise factor, typically 5–8 dB); and −130 to −140 dB rad^2/Hz for bipolar RF amplifiers, up to 1 GHz.

There is very little that one can do to reduce flicker PM noise. Some negative feedback at low frequency proved to be useful, such as an emitter resistor with no bypass capacitor. Useful tips are negative feedback at RF to stabilize the transconductance and a careful design of the amplifier for a low noise factor at low frequency. Kuleshow and Boldyreva [43] suggest that there is a magic bias that reduces the $1/f$ noise in common-emitter amplifiers.

Figure 2-22 also shows what happens combining white and flicker PM noise. An interesting fact is that is that the cutoff frequency f_c, where white PM noise equals flicker PM noise, is proportional to P_0. This happens because flicker PM noise is constant versus power, while white PM noise gets lower at higher power. Computer simulation programs like SPICE may use f_c as the noise parameter. This choice is unfortunate and misleading because the user unaware of the mechanism may not understand the need to update f_c after changing any parameter affecting P_0.

Cascading amplifiers yield a surprising result. The general rule, that the noise of the chain is essentially determined by the noise of the first stage, does not apply to flicker. Since the coefficient b_{-1} is in a first approximation

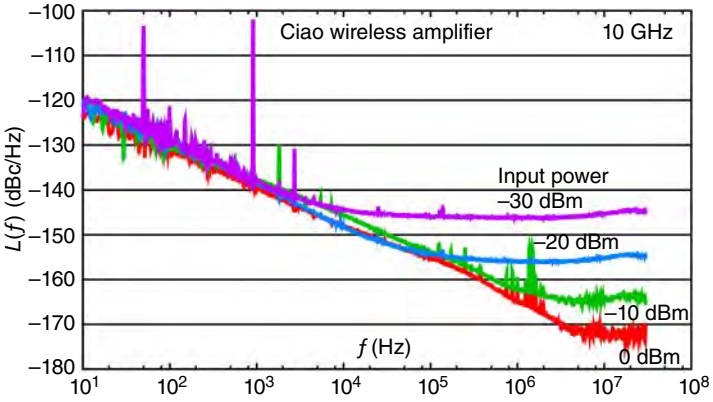


Figure 2-22 Example of amplifier phase noise. Courtesy of © Vincent Giordano, FEMTO-ST Institute.

independent of the carrier power, the flicker PM noise is

$$S_\theta(f) = \frac{\mathsf{b}_{-1}}{f} \qquad \text{with} \quad \mathsf{b}_{-1} = \left[\mathsf{b}_{-1}\right]_1 + \left[\mathsf{b}_{-1}\right]_2 + \cdots \tag{2-83}$$

Most people are surprised to learn that the result is independent of the order of the amplifiers in the chain.

The flicker of two or more amplifier connected in parallel is another amazing consequence of the property that b_{-1} is independent of the carrier power. Splitting the input into two amplifiers gives the same amount of PM noise in each branch, despite of the smaller power. Combining the two outputs, the PM noise is half of the noise of one amplifier because the carrier adds up coherently, and the PM noise adds up statistically. To this extent, push–pull stages, distributed amplifiers, and other configurations where the output power results from adding the contribution of multiple transistors are equivalent to parallel amplifiers. The idea of achieving low flicker by paralleling multiple amplifiers is exploited in some commercial special-purpose amplifiers [38]. By contrast, the white PM noise cannot be improved in this way because the PM noise of each branch scales up as the power is reduced. Actually, the loss associated to power splitting degrades the white noise.

Example 6 Amplifier Noise. A clean noise-free 100 µW signal is amplified by two cascaded amplifiers detailed in the table below. We calculate the phase noise PSD at the output, considering the *A*–*B* order (lower noise amplifier first), and the *B*–*A* order.

Amplifier	Gain A		Noise factor F		Flicker coefficient b_{-1}	
A	3.98	12 dB	1.41	1.5 dB	10^{-13} rad^2/Hz	−130 dB rad^2/Hz
B	3.16	10 dB	2.51	4 dB	1.58×10^{-13} rad^2/Hz	−128 dB rad^2/Hz

Considering the *A*–*B* order first, the noise factor is

$$F_{AB} = F_A + \frac{F_B - 1}{A_A^2} = 1.41 + \frac{2.55 - 1}{3.98^2} = 1.51 \quad (1.8\text{ dB})$$

Thus, the white PM noise is

$$S_\theta(f) = \frac{F_{AB} k T_0}{P_0} = \frac{1.51 \times 1.38 \times 10^{-23} \times 290}{10^{-4}} = 6.06 \times 10^{-17}$$

that is, −162.1 dB rad^2/Hz, or −165.1 dBc/Hz

When the amplifiers are interchanged, we get

$$F_{BA} = F_B + \frac{F_A - 1}{A_B^2} = 2.51 + \frac{1.41 - 1}{3.16^2} = 2.55 \quad (4.1\ \text{dB})$$

and

$$S_\theta(f) = \frac{F_{BA} k T_0}{P_0} = \frac{2.55 \times 1.38 \times 10^{-23} \times 290}{10^{-4}} = 1.03 \times 10^{-16}$$

that is, −159.9 dB rad²/Hz, or −162.9 dBc/Hz. As expected, the noise of the two configurations is different, with ≈2 dB higher PM noise when the noisier amplifier comes first.

The flicker noise is the same for the two configurations (remember that b_{-1} has the physical dimension of rad² because $S_\theta = b_{-1}/f$ must have the dimension of rad²/Hz)

$$b_{-1} = b_{-1}|_A + b_{-1}|_B = 10^{-13} + 1.58 \times 10^{-13} = 2.58 \times 10^{-13}\ \text{rad}^2$$

that is, −125.9 dB rad, or −128.9 dBc/Hz extrapolated to 1 Hz. ■

How to Choose a Low PM Noise Amplifier

The noise factor F is generally well documented and describes the white noise rather precisely. Thus, the amplifier with the lowest F also exhibits the lowest white PM noise according to $S_\theta = FkT/P_0$. By contrast, flicker PM noise is seldom mentioned in the specs, and even when it is present, the documentation is generally poor. Generally, we find a plot, or at most a small number of plots referring to practical cases measured one sample at the company site. No typical/max values are given, and no rule for extrapolation to different conditions. Thus, a discrepancy between actual phase noise and the datasheet is not a surprise.

Figure 2-23 shows the flicker of the Analog Devices HMC-072 amplifier taken from the datasheet. This amplifier was chosen because the phase noise is better documented than we find in similar devices. Designing a complex oscillator intended to provide ultimate low phase noise at that frequency, we were looking for the lowest flicker. We will see later in this chapter that the flicker of the sustaining amplifier impacts on the $1/f^3$ noise (flicker of frequency) of the oscillator. The $1/f$ noise found in the datasheet (Figure 2-23) is equivalent to −132 to −135 dBc/Hz extrapolated to 1 Hz. The flicker we measured is in fair agreement, being −131 dBc/Hz at 1 Hz (Figure 2-24). The measurement was done with a DBM saturated at both inputs, following the classical scheme of Figure 2-72. The mixer is from Marki, and the line stretcher is from Arra.

Having said all that, we can get useful tips by combining physical insight with some other parameters apparently not related to flicker PM noise. This is a good way to avoid numerous blind tests, but measurements are always necessary when flicker PM noise is a critical parameter.

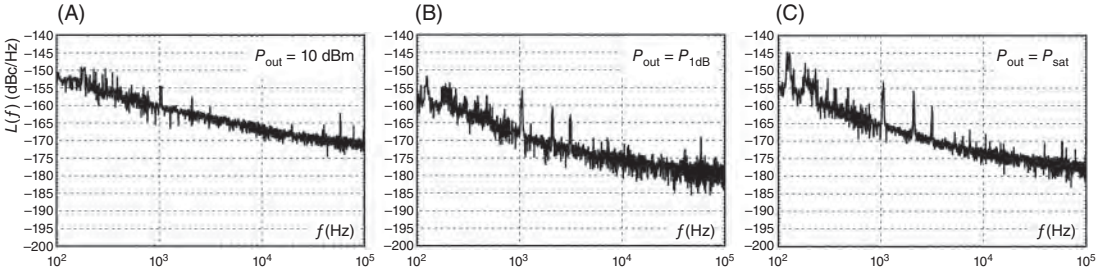


Figure 2-23 Phase noise of the Analog Devices HMC-C072 amplifier at $f_0 = 10$ GHz at different power levels: (A) 10 dBm output, (B) at the 1 dB compression point, and (C) at the maximum output power, in strong saturation regime. The spectra are from the HMC-072 data sheet, © Analog Devices, reproduced with permission. Graphical adaptation is ours.

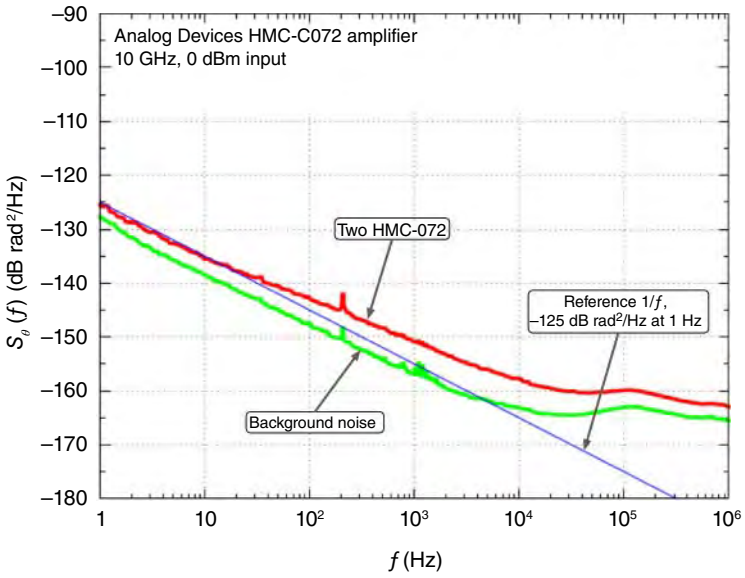


Figure 2-24 Phase noise of two Analog Devices HMC-072 amplifiers at $f_0 = 10$ GHz, measured with a saturated double-balanced mixer. Each amplifier receives 7 V bias and 0 dBm input power. Subtract 3 dB for the noise of one amplifier, and add 3 dB to convert dB rad^2/Hz to dBc/Hz. Courtesy of © Yannick Gruson, FEMTO-ST Institute.

The most important fact about flicker PM noise is that it comes from up conversion of near-dc flicker, that is, the $1/f$ fluctuation of the bias current, internal capacitances, or other parameters. Because up conversion is a nonlinear phenomenon, high linearity is a desired feature. High intercept power IP2 and IP3 and low harmonic distortion are good signs for a potentially good low-flicker amplifier. These parameters must be interpreted together with the amplifier topology. For example, a push–pull configuration cancels the second harmonics, thanks to symmetry, but symmetry does not cancel the PM flicker because the near-dc processes inside the two transistors are independent.

Internal flickering in components is a microscopic phenomenon. The evidence of this is that the probability density distribution of the internal voltage or current, and therefore of random phase, is Gaussian. This distribution can only be originated by large number of small random fluctuation via the central limit theorem. Consequently, we expect lower flicker from devices having larger volume of the gain region and not-too-sharp junctions. If we design at transistor level, these considerations point to transistors with not-too-high gain β (or h_{FE}) and not-too-high transition frequency f_T. Higher V_{CB} max reveals that the collector–base junction is not too thin, thus the C_{BE} capacitance is more stable versus the fluctuations of the bias current. Germanium transistors may exhibit low $1/f$ noise, paradoxically for the same reason why are not as good as silicon transistors in more general terms: the base region is thicker, the current gain is lower, etc. With modern technology, low $1/f$ noise is found in SiGe transistors [44]. Unfortunately, often this comes at the cost of higher noise factor.

Isolation Amplifiers

Isolation amplifiers are special devices optimized for high forward-to-reverse gain ratio, and intended to keep a precision oscillator or a frequency standard free from interferences brought inside from its output. The typical problem is that a resonator accumulates the incoming energy over a time equal to the relaxation time $Q/\pi f_0$, and it is not rare than even a power of picowatts or even femtowatts reaching the core of a precision oscillator impacts on its stability and noise in unpredictable way, or phase lock it. Isolation amplifiers are also needed in frequency distribution systems, where one input signal has to be delivered to multiple destinations. High output-to-input and output-to-output isolation is the main feature, and also isolation from load change.

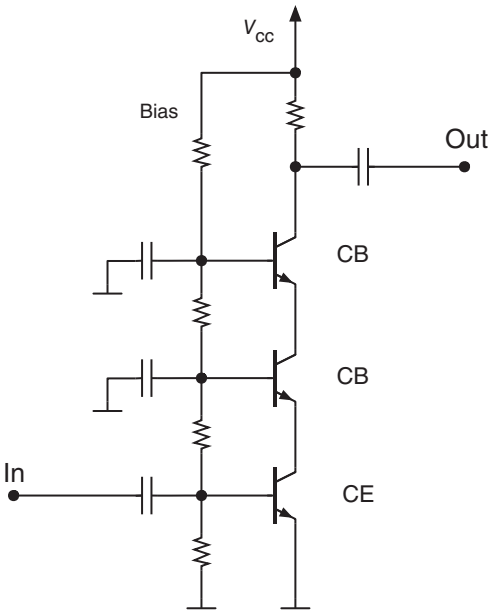


Figure 2-25 Isolation amplifier. The use of two or more common-base transistors results in enhanced output-to-input isolation.

At microwave frequencies, the isolation of regular microwave amplifiers can be increased by using ferrite isolators. One of these devices provides 20 dB typical isolation, and a few can be cascaded. In the radiofrequency region, below some GHz, the isolators are not an option, being the ferrite too large and impractical. At these frequencies, the grounded-base (or common-base) bipolar transistor is the most common choice. The idea is that the base region is a shield, which breaks the capacitive coupling between emitter (input) and collector (output). The grounded-base stage often goes with a common emitter stage to form a cascode amplifier. Increased isolation can be achieved with two or more grounded-base amplifiers stacked on the collector of the first common-emitter stage [45], as shown on Figure 2-25. A problem of this configuration is the higher supply voltage (20–30 V), uncomfortable for regular electronic design. A differential pair is an alternate option, with the input on the base of the first transistor, and the base of the second transistor connected to ground as the shield.

No matter whether the electrical circuit exploits circulators or grounded-base transistors, high isolation, say, 100 dB or more, requires that enclosure and shielding are accounted for. Preventing radiation and blocking the signal propagating on the outer surface of shielded cables and enclosures is of paramount importance. In the high frequency (HF)-very high frequency (VHF) region, a common-mode ferrite filter on the input and output coaxial cables is often necessary.

2-3-2 Frequency Dividers

Digital Frequency Dividers

Frequency division is one of the early applications of digital circuits. The reader can refer to the Egan article [46] for a review based on available data about the classic TTL and emitter-coupled logic (ECL) families. There are two basic types, asynchronous and synchronous dividers (Figure 2-26). The main difference is that in the asynchronous divider the jitter of each flip-flop adds up as the signal propagates along the chain, while in the synchronous dividers all the flip-flops switch simultaneously on the edges of the input clock. The output of an asynchronous divider can be synchronized to the input clock with a D-type flip-flop.

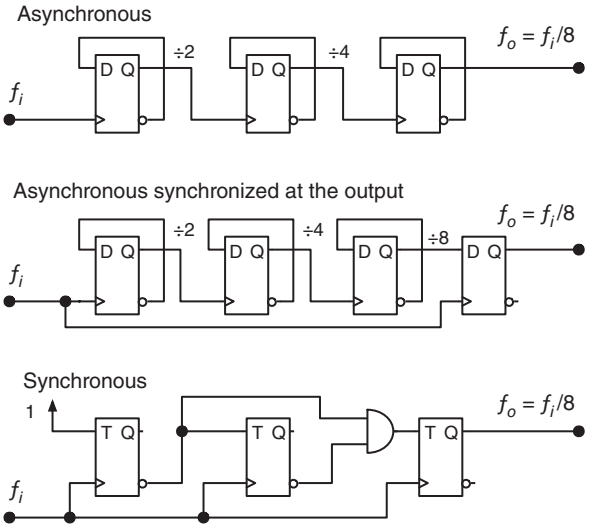


Figure 2-26 Asynchronous and synchronous frequency dividers.

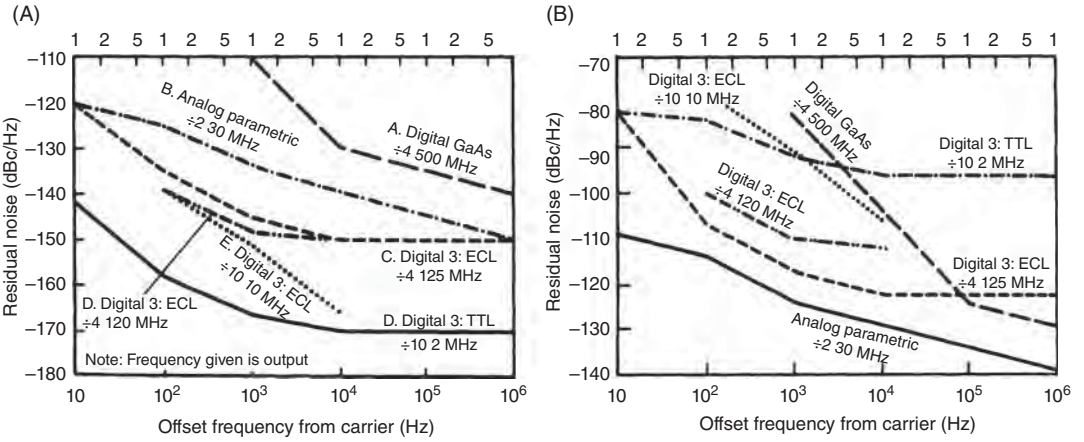


Figure 2-27 Phase noise of some dividers as all data refer to the output frequency (A), and are scaled up to 10 GHz (B). Reprinted with permission from [47].

In accordance with Figure 2-27, the practical noise limit is of the order of −170 dBc/Hz for the old TTL dividers and −155 dBc/Hz for the ECL dividers. Yet, these values are not easy to achieve in practice. Small-scale integration complementary MOS (CMOS) dividers, up to an input frequency of 10 MHz, are similar in phase noise to the TTL devices. However, the close-in noise or noise between 1 and 10 Hz off the carrier is higher than that of TTL devices. TTL devices require higher shielding and better power supply decoupling to prevent external crosstalk between the various stages, which otherwise results in unwanted spurious and sidebands. Programmable logic devices offer new design perspectives, but they are only usable up to 1 GHz. Commercial dividers up to 12–26 GHz input frequency are available from Analog Devices, Hittite (now with Analog Devices), Keysight Technologies, Microsemi, ON Semiconductor, Pasternack, and other manufacturers.

Most of these dividers have another unpleasant effect, in the form of internal crosstalk. Crosstalk is defined as the amount of input signal appearing at the output. In high-performance synthesizers, it is necessary to use a

low-pass filter after the reference or the programmable divider and a pulse shaper to translate the resulting sine wave back into a square wave for appropriate suppression of the crosstalk.

Phase Noise Scaling

In a noise-free divider, the device divides the input phase by N for the same reason it divides by N the input frequency

$$f_o = \frac{f_i}{N} \quad \text{and} \quad \theta_o(t) = \frac{\theta_i(t)}{N} \tag{2-84}$$

Naively, we may be inclined to extend this result to $S_{\theta o}(f) = S_{\theta i}(f)\,/N^2$. Reality is more complex because *aliasing* strikes on some types of signals, but not on others. Some relevant cases will be analyzed in the following text.

Let us start from white noise. In digital circuits, phase noise is sampled at the frequency $2f_0$ for the simple reason that the phase fluctuations exist only during the rising and falling edges of the signal, while the pulse level has no effect on the output. Thus, the *bandwidth* of phase noise is equal to f_0, which is half the sampling frequency. Some circuits switch only on one active edge, either rising or falling. In such case the sampling process takes place at f_0, and the noise bandwidth is equal to $f_0/2$. We take f_0 as the bandwidth, leaving to the reader the extension to $f_0/2$.

The easiest way to understand aliasing is to derive the spectrum from the time fluctuation $\mathsf{x}(t)$ and its mean square value $\langle \mathsf{x}^2 \rangle$. In principle, a noise-free divider transfers the time fluctuation from the input to the output. By virtue of the Parseval identity, it holds that

$$\left\langle \mathsf{x}^2 \right\rangle = S_{\mathsf{x}}(f)\, B \tag{2-85}$$

where the bandwidth B is equal to f_i at the input, and to $f_o = f_i/N$ at the output. The consequence is that

$$S_{\mathsf{x}o}(f) = N S_{\mathsf{x}i}(f) \quad \text{(with aliasing)} \tag{2-86}$$

Thus, the bandwidth reduction by $1/N$ is compensated by increasing the noise PSD by the same factor N. The time fluctuation can be converted into phase fluctuation using $\theta(t) = 2\pi f_0 \mathsf{x}(t)$. This applies to the input frequency f_i and to the output frequency f_o. There results

$$S_{\theta o}(f) = \frac{1}{N}\, S_{\theta i}(f) \quad \text{(with aliasing)} \tag{2-87}$$

By contrast, aliasing produces no detectable effect on flicker noise because the aliases are attenuated by a factor $1/2f_i$, $1/3f_i$, etc. Thus, the output phase noise is described by

$$S_{\mathsf{x}o}(f) = S_{\mathsf{x}i}(f) \quad \text{(no aliasing)} \tag{2-88}$$

and

$$S_{\theta o}(f) = \frac{1}{N^2}\, S_{\theta i}(f) \quad \text{(no aliasing)} \tag{2-89}$$

A further phenomenon occurs when an analog (sinusoidal) is sent to the input, instead of a clean digital signal from the same logic family. The phase noise PSD in the input stage increases because of nonlinearity and other phenomena.

Figure 2-28 shows the interplay of noise levels in a digital divider. The input PM noise increases by a few dB in the first stage, and then it is scaled down by a factor of $1/N$ or $1/N^2$, depending on the noise type. As an unpleasant consequence, a ÷10 divider may scale down the input white PM noise by a mere 5–6 dB instead of the 20 dB of the $1/N^2$ rule.

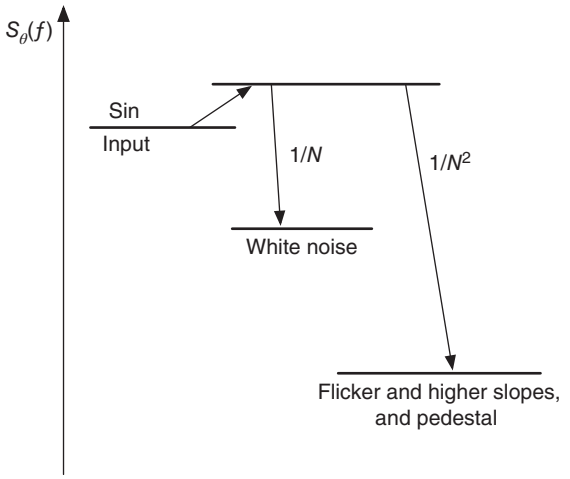


Figure 2-28 Phase noise scaling in a digital frequency divider.

The case of a signal with a pedestal (Figure 2-29) is so common in PLLs and frequency synthesizers, that it deserves special attention. For this purpose, we can divide the input phase fluctuation $\theta(t)$ into pedestal and floor, denoted with the subscripts p and f. Additionally, pedestal and floor have different origins, thus they are statistically independent. The pedestal is rather narrow as compared with the carrier, but it contains most of the mean square fluctuation $\langle\theta^2\rangle$. In most practical cases, N is not large enough to shrink the bandwidth of the pedestal ($N < f_i/f_p$), thus there is no aliasing. This is why $S_\theta(f)$ follows the $1/N^2$ rule. Further dividing, at some point the pedestal shrinks to f_i, aliasing takes place, and the scaling rule changes from $1/N$ to $1/N^2$. By contrast, aliasing strikes on the floor, which is wide and uniform, and $S_\theta(f)$ scales as $1/N$. The latter result is of paramount importance in PLLs.

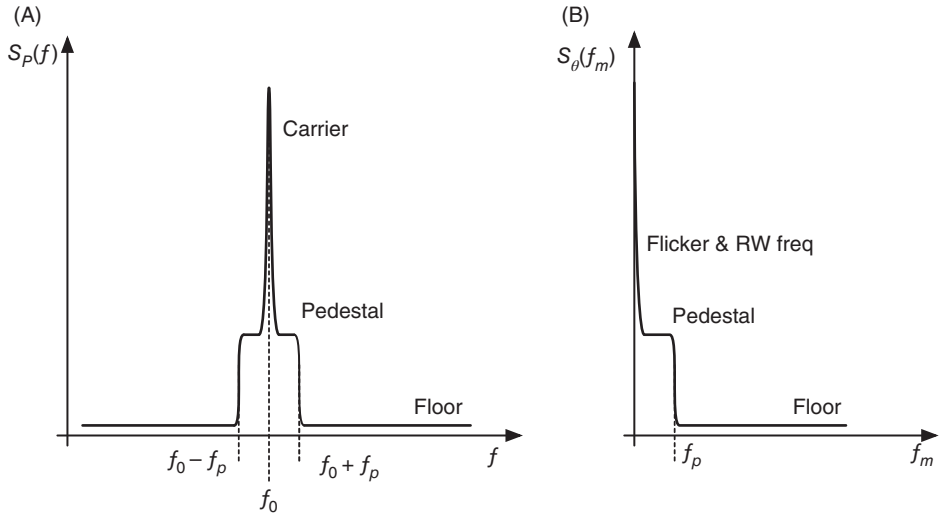


Figure 2-29 Carrier with a noise pedestal, seen with the regular spectrum analyzer (A) and (B) with a phase noise analyzer.

Time-Type and Phase-Type PM Noise

For the purpose of frequency synthesis, we identify two basic types of phase noise, called *phase-type noise*, or φ-type noise for short, and *time-type noise*, or x-type noise. These types of noise, first introduced in [48], differ in how the noise is scaled with the carrier frequency f_0.

The *phase-type noise* is characterized by the statistics of θ independent of f_0. Then, x follows the rule

$$\mathrm{x}(t) = \frac{\theta(t)}{2\pi f_0} \qquad \text{and} \qquad S_{\mathrm{x}}(f) = \frac{1}{4\pi^2 f_0^2} S_\theta(f) \tag{2-90}$$

This is the case of an input signal $v(t)$ crossing a fluctuating threshold $n(t)$. The time fluctuation is $\mathrm{x}(t) = n(t)/\mathrm{SR}$, where SR is the *slew rate*. In the case of a sinusoidal signal of peak amplitude V_0, the slew rate is $\mathrm{SR} = 2\pi V_0 f_0$. Thus $\theta(t) = n(t)/V_0$, and consequently $\langle\theta^2\rangle = \langle n^2\rangle / V_0^2$. The PSD $S_n(f)$ of the threshold fluctuation has a bandwidth B equal to the full analog bandwidth at the device input, while $S_\theta(f)$ has a bandwidth equal to the input frequency f_0. Thus,

$$S_\theta(f) = \frac{\langle n^2 \rangle}{f_0 V_0^2} = \frac{S_n(f)\, B}{f_0 V_0^2} \tag{2-91}$$

Having to guess about a digital circuit with no specific information on hand, one can start from the following values: $\sqrt{S_n(f)} = 10\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ for the analog white noise at the device input, and $B = 4f_{\max}$, four times the maximum switching frequency.

Oppositely, *the time-type noise* is characterized by the statistics of time fluctuation x independent of f_0, and θ given by

$$\theta(t) = 2\pi f_0 \mathrm{x}(t) \qquad \text{and} \qquad S_\theta(f) = 4\pi^2 f_0^2 S_{\mathrm{x}}(f) \tag{2-92}$$

This is the case of the signals propagating inside an integrated circuit. Such signals have full amplitude and SR, thus the delay and its fluctuations result from the sum of the contribution of all the individual gates or cells along the path. Crosstalk is not considered in this simplified description, but it can be a major nuisance in practical cases.

The noise-scaling rule, either $1/N$ or $1/N^2$, is not sufficient to describe the noise in a divider. The phase noise cannot be reduced arbitrarily by dividing a high input frequency by a large N because at some point the scaled-down phase noise hits the phase noise of the output stage. When this happens, the phase noise cannot be reduced by further frequency division.

Figure 2-30 shows an example of a digital circuit when input frequency changes in a wide range. This example is the clock line in an FPGA, including the input and output circuits. Since $f_o = f_i$, there is no $1/N$ or $1/N^2$ scaling. On the right-hand side of the plot, where the phase noise is of the white type, we identify clearly the phase-type with aliasing, ruled by $S_\theta(f) = S_n(f)\, B/f_0 V_0^2$. Changing f_0 in powers of 2, the change in the white PM noise is close to the 3 dB expected. With $V_0 = 1$ V and $B = 2.5$ GHz (four times the maximum input frequency), we infer that the threshold fluctuation is of $11\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, rather independent of f_0. Focusing on flicker noise, we see that at high f_0, 100 MHz and beyond, the noise is clearly of the time type. Converting $S_\theta(f)$ into $S_{\mathrm{x}}(f)$, we find that the $1/f$ coefficient k_{-1} of the polynomial law is rather constant versus f_0. The associated rms time fluctuation is 21 fs. Finally, thermal effects appear at $f < 10$ mHz (not visible on Figure 2-30).

Unfortunately, the data sheets seldom provide more than one example of phase noise, thus it is difficult to extract the noise parameters, and measurements are always necessary for critical applications. Figure 2-31 shows an example of phase noise PSD measured on a microwave divider. A flicker of −110 dBc/Hz extrapolated to 1 Hz, and a floor of −150 dBc/Hz can be expected from similar dividers.

The Λ Divider

The Λ divider [49], shown in Figure 2-32, is a simple trick to circumvent the aliasing phenomenon inherent in digital dividers. The output signal is a triangular wave obtained by adding N square waves shifted by an integer number of half clock periods. In the triangular wave, the power associated n-th harmonics is proportional to $1/n^4$, instead of $1/n^2$ for the square wave. No aliasing takes place because the output signal is sampled at $2f_i$, which is the

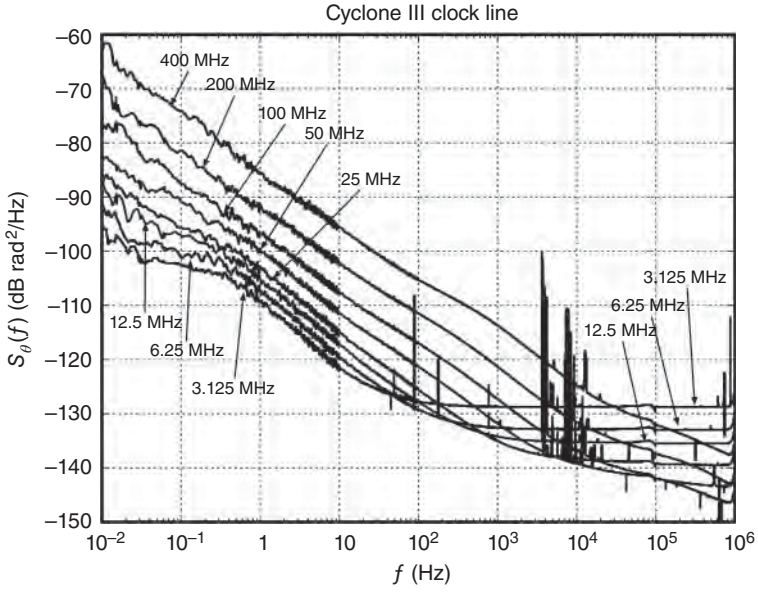


Figure 2-30 Example of noise in a digital circuit (Cyclone III FPGA). For the sake of proving concepts, the FPGA is programmed to replicate the input, so that we observe the input and output stages and the internal clock distribution. Reprinted with permission from [48].

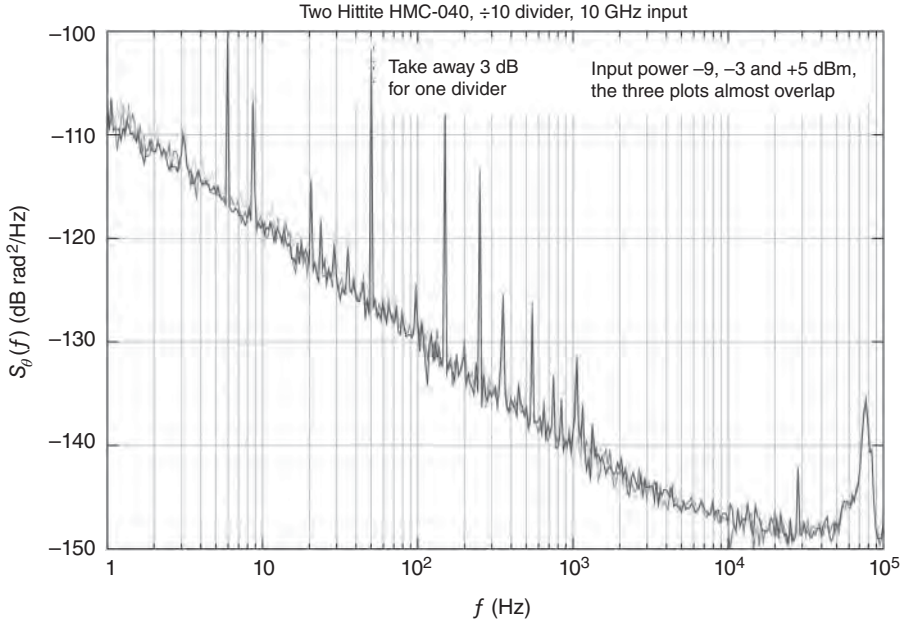


Figure 2-31 Example of phase noise in a microwave divider. Courtesy of © V. Giordano, CNRS FEMTO-ST Institute, Besancon, France.

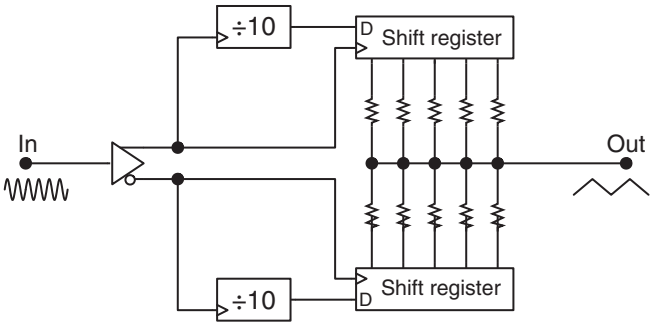


Figure 2-32 The Lambda divider. Reprinted with permission from [49]. © 2013 IEEE.

same sampling frequency of the input. Thus, the phase noise follows the rule $S_{\theta o}(f) = S_{\theta i}(f)\,/N^2$. The triangular wave can be easily cleaned by filtering out the harmonics. The name "Λ divider" derives from the similarity of the Greek letter Λ with a triangle, and for the same reason the regular digital divider is called Π divider for the similarity of the Greek letter Π to the pulse of a square wave. Reference [49] shows an example of ÷10 divider exhibiting a phase noise of −165 dB rad^2/Hz (white) and −130 dB rad^2 (flicker at 1 Hz), measured at the 10 MHz output frequency.

Analog Frequency Dividers

Analog frequency dividers may be a good choice in some special cases, for example, for extremely low noise or when the input frequency is too high and out of reach for digital technology. Unfortunately, these dividers are complex to design, work in a narrow range of input frequency, and a quantitative understanding of phase noise is difficult.

The first of such divider is the *injection locked oscillator*, or ILO [50–52]. Figure 2-33 shows an example of integrated implementation [53]. The idea is quite old and exploits the fact that the nonlinearity in the oscillator loop, naturally, generates harmonics and beats notes. So, a signal injected in the oscillator, having frequency f_i which is sufficiently close to an integer multiple N of the oscillation frequency, pulls the oscillator to lock to $f_o = f_i/N$. This mechanism is effective only in a frequency range, which depends on the amplitude. The ILO is broadly equivalent to a PLL without the integration effect inherent in the VCO.

The second option is the *regenerative frequency divider*, or *Miller divider* [54, 55], shown in Figure 2-34. To start, let us assume that a signal at the frequency f_i/N is present at the mixer output. Such signal crosses the bandpass filter tuned at f_i/N, amplified, frequency-multiplied by $N-1$, and sent back to the mixer. The mixer beats the input f_i with $(N-1)f_o$ and regenerates f_i/N at its output. The feedback equation, as seen at the mixer output, is

$$f_i - (N-1)f_o = f_o \tag{2-93}$$

This gives $f_o = f_i/N$, as expected. Self-starting operation requires that regeneration starts from noise or from the power-up transient. The challenge is to design a frequency multiplier with no threshold, still effective at very low input power. With $N = 2$, self starting is rather easy to achieve because there is no multiplier. The mixer works well at low power at one input (the feedback signal) if the other input (the divider input) is saturated. The phase noise is limited by the amplifier, in the ideal case multiplied by a factor of $1/N^2$ inherent in the phase feedback operation. The full noise theory and some practical examples are found in Ref. [56]. This reference also explains an optimization method, which exploits the third harmonic generated by saturation in the mixer, to reduce the noise of a divider by two.

The regenerative divider is broadly similar to the ILO. The relevant difference appears in the absence of the input signal. The divider delivers no output, while the ILO oscillates at its own free-running frequency.

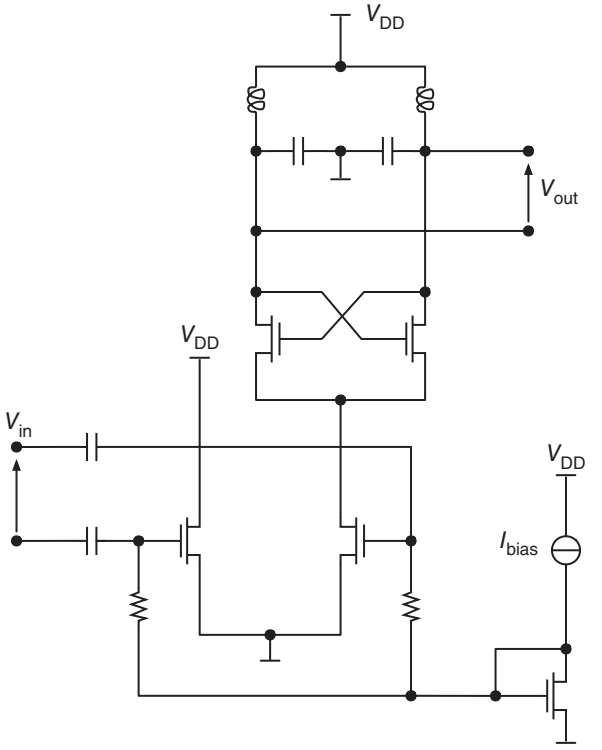


Figure 2-33 Injection locked frequency divider.

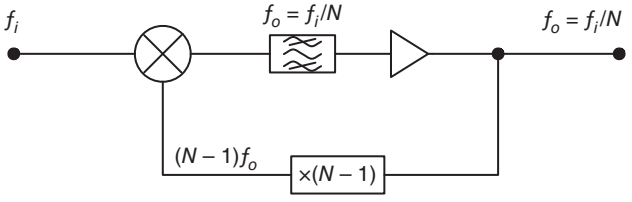


Figure 2-34 Regenerative frequency divider.

The third option is the *parametric frequency divider* [56, 57]. The idea is that the current flowing in the varactor contains two frequencies, f_i and $f_o = f_i/2$. The varactor is a nonlinear capacitance, thus it beats signals with high power efficiency because the capacitance has small energy loss in the charge–discharge cycle. Consider the divider-by-two operation shown in Figure 2-35. The input circuit is an *LC*, which transfers the power to the varactor at the frequency f_i, and has high attenuation at f_o. Similarly, the output circuit extracts the power at the frequency $f_o = f_i/2$, and at f_i it isolates the varactor from the output. Dividers by $N > 2$ make use of a series of idlers (resonators) tuned at the sub-harmonics of the input frequency, so that multiple down-conversions in the varactor result in the output frequency f_i/N. The parametric divider has low phase noise because it can manage relatively high signal level (20 dBm and more) and has low dissipation.

Example 7 PLL Synthesizer. The frequency synthesizer shown in Figure 2-36 is used to generate a 5-GHz signal with 1 kHz resolution. A 1-kHz reference signal is obtained from a 5-MHz reference oscillator ($M = 5000$),

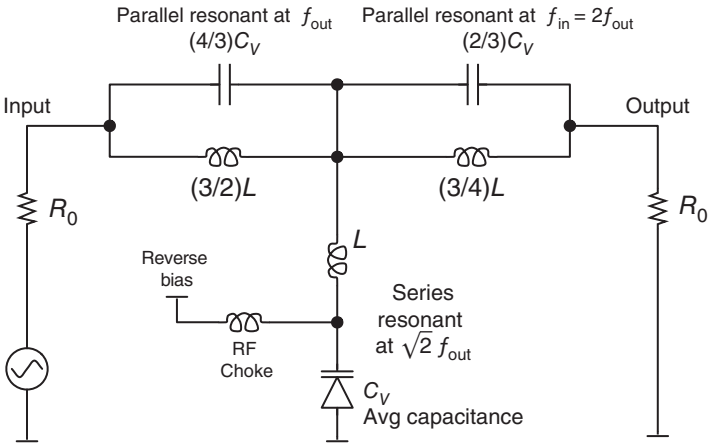


Figure 2-35 Example of parametric frequency divider ÷2.

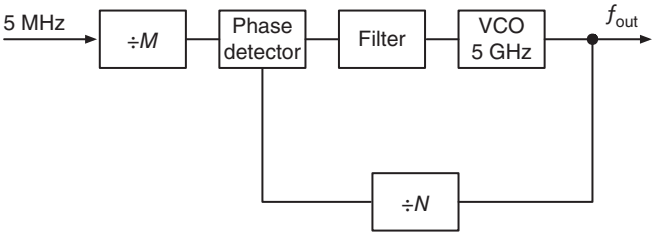


Figure 2-36 A 5-GHz YIG oscillator harmonic stabilized to a 5-MHz reference.

which is specified to have a single-sideband noise power of −140 dBc/Hz at $f = 500$ Hz off the carrier. If the loop bandwidth is assumed to be approximately 1 kHz, the noise from the reference oscillator will not be reduced by the low-pass filtering of the PLL. Although the divider by N will reduce the noise power by the factor $1/N^2$, the approximate loop transfer function is

$$\theta_o(s) = \frac{\theta_r \left[K_v F(s)/s\right]}{1 + \left[K_v F(s)/sN\right]} = N\theta_i(s)$$

for reference frequencies below the loop bandwidth of 1 kHz. The net effect is that the output phase noise is the reference oscillator PM noise multiplied by N^2/M^2. Of course, we need $N = 5 \times 10^6$ to scale the output 5 GHz frequency down to the 1 kHz frequency for the phase detector. The output PM noise due to the reference oscillator, at 500 Hz offset, is

$$L(f) = -140\ \text{dBc/Hz} + 10 \log_{10}\left(\frac{5 \times 10^6}{5 \times 10^3}\right)^2 = -80\ \text{dBc/Hz}$$

This example illustrates a problem inherent in PLL frequency synthesizers used to generate an output frequency much higher than the reference oscillator frequency, with high resolution. Although the reference oscillator noise power may be small, the same noise power appears on the output signal amplified by a large factor. Notice that the phase detector (Section 2-3-5), not accounted here, may introduce even higher the phase noise. ■

2-3-3 Frequency Multipliers

Generally, the long-term frequency stability available in an instrument comes from the internal 10 MHz quartz oscillator, or from an external reference. The external frequency of 100 MHz is sometimes preferred in high-end

instruments, where the lowest phase noise is of paramount importance. In synthesizers there is a frequent requirement for internal signals at higher frequencies, having low phase noise and the stability of the main reference. We have different options for frequency multiplication, which fall in two classes:

- A locked oscillator
  - A PLL with a divider in the feedback, or with harmonic sampling
  - An injection locked oscillator that exploits its internal nonlinearity to generate harmonics of the input frequency and locks to one of it
- A dedicated frequency multiplier
  - Transistor, optionally in push–push or push–pull configuration
  - Step-recovery diodes or snap-off diodes
  - Varactors
  - Nonlinear delay lines (sometimes referred to as nonlinear transmission lines (NLTLs))
  - Diode (rectifier) networks.

The choice is a matter of frequency, target PM noise, electrical power constraints, and complexity. High-order frequency multipliers are very difficult to build. It is often better to use a cascade of multipliers of lower order than a single high-order multiplier. Applications requiring fixed or variable frequency yield different solutions.

The noise-free wide-band frequency multiplier $\times N$ transfers the input time fluctuation to the output, $\mathsf{x}_o(t) = \mathsf{x}_i(t)$, thus it scales up the input PM noise according to

$$\theta_o(t) = N\theta_i(t) \qquad \text{and} \qquad S_{\theta o}(f) = N^2 S_{\theta i}(f) \tag{2-94}$$

This is +20 dB per factor-of-ten. A reduction in the phase noise bandwidth applies in some cases, typically the PLL multiplier and the injection locked oscillator, due to the narrower bandwidth of the loop.

The conversion efficiency is defined as the output-to-input power ratio

$$\eta = \frac{P_o}{P_i} \tag{2-95}$$

This definition is most relevant for passive multipliers, where $\eta < 1$, because the output power may limit the phase noise. By contrast, the conversion efficiency makes little sense in active multipliers, where the power is provided externally, and $\eta > 1$ is allowed. Of course, the conversion efficiency is not a useful parameter to describe PLLs and injection locked oscillators.

Designing a PLL multiplier, harmonic sampling is generally used for upper microwave frequencies, where there are no convenient dividers. However, nowadays commercial microwave prescalers work up to at least 26 GHz. Attempts to use tunnel diodes for this purpose, or parametric effects in tunnel diodes, show up in the literature from time to time but they have failed to show reliable performance, due to complexity and component tolerances in temperature.

A harmonic sampler is typically a balanced modulator that uses hot carrier diodes, driven from a pulse or comb generator with extremely high harmonic contents. A typical application for such a circuit is in spectrum analyzers, where the input frequency and the YIG oscillator can be locked together. A similar application is where a harmonic comb is generated from a 1-MHz reference, and locking can occur every 1 MHz up to several GHz. These circuits require a pre-tuning mechanism to make sure that the desired harmonic is selected, preventing false locking. This type of multiplication is used in systems where the frequency of the VCO is changed frequently and low spurious contents and high SNR are required.

For higher frequency ranges, IMPact ionization Avalanche transit-time (IMPATT) diodes or other exotic devices can generate the necessary frequencies, and some of these multipliers are also built as injection locked oscillators. An injection locked oscillator can be considered as a frequency multiplier within a certain pulling range, where the oscillator locks up with the reference frequency. These are highly nonlinear phenomena, described in the literature

from time to time. Explanations and mathematical models are built primarily around experimental data, not always reliable for extrapolation or new design. Low-frequency injection locking is a very convenient way of combining extremely high stability in certain types of crystal oscillators, which are being used as a reference for extremely low-noise crystal oscillators operating at the same frequency.

For single-frequency applications, we find synthesizer loops using high-frequency crystal oscillators at discrete frequencies between 70 and 150 MHz, locked to a frequency standard with a narrow-band loop, so that the output PM noise depends only on the VHF oscillator, rather than on the input frequency. These loops have bandwidth of a few Hz or less, and therefore compensate only for temperature effects and aging.

The step recovery diode (SRD) generates a comb of sharp pulses at the transition between the on and the off region, and in turn a comb spectrum extending to high harmonics. Such diodes may be useful to generate frequencies up to tens of GHz and generally require a power of +20 dBm or higher. A problem with the SRD is the relatively high phase noise, inherent in abrupt change of capacitance used to generate the sharp pulse. The typical design of a high-order multiplier may include a low-noise pre-multiplier, followed by an SRD.

Example 8 Frequency Multiplication. The frequency multiplier from a stable 5 MHz oscillator to 9.18 GHz for a Cs frequency standard[1] can be implemented with a ×18 low-noise multiplier, followed by a ×102 SRD multiplier. If the floor of the quartz oscillator is −152 dBc/Hz, a noise-free multiplier would rise such floor to −127 dBc/Hz after multiplication ×18 (+25 dB), and to −87 dBc/Hz after further multiplication by 102 (+40 dB). The −127 dBc/Hz at output of the ×18 multiplier sets relaxed specs for the PM noise of the ×102 SRD multiplier at approximately −130 dBc/Hz (3 dB less than the PM noise at its input). Introducing the contribution of a low-noise first stage, the result may differ by +1 … + 2 dB. This reinforces the conclusion that a low-noise pre-multiplier is useful to relax the noise specs of a high-order second stage. ■

For fixed-frequency applications, tuned frequency multipliers with transistors work well up to the order of a GHz. Saturation should be avoided because the charge stored in the forward-biased CB junction slows down the transistor and introduces phase noise. Class-C push–push configurations can be used to improve the efficiency by reinforcing the even harmonics, and canceling the odd harmonics. Likewise, the push–pull configuration reinforces the odd harmonics and cancels the even harmonics. The differential pair is an appealing option of a switch because it generates a square wave with very sharp edges, making efficient use of the transistors bandwidth and keeping the transistors in the linear region. Baugh [58] suggested the use of an inductor to turn the edges into sharp pulses for efficient low-noise multiplication, but this idea is seldom seen in practical applications.

Varactors [57] are a good choice for high power efficiency and low noise because they exploit smooth nonlinear capacitance. The efficiency of an ideal reactive nonlinear reactance, that is, loss-free varactor, is $\eta = 1$, regardless of the order of multiplication. In practice, η is limited by the small series resistance of varactors. A problem with the varactor multiplier is that it works at fixed frequency or in a rather narrow bandwidth. The design can be rather complex because it requires resonant circuits at the input and at the output, and idlers at all intermediate harmonics if $N > 2$. Complexity may limit N to a convenient maximum of 3–5. However, efficiency can be so high (up to −2 … − 1 dB) that the varactor multiplier is an option for the output stage in small radio transmitters, instead of an active multiplier.

The NLTL is another application of varactors suitable to high-order frequency multiplication [59]. It exhibits low phase noise, and relatively wide input bandwidth (one octave). Such device is a ladder *LC* network with series inductors, and the parallel capacitors replaced with varactors. The mechanism derives from studies on soliton waves. The input signal is turned into a pulse comb, and progressively shrunk and sharpened as the signal propagates through the line. Commercial devices are available, delivering multiplication up to ×100 at a maximum output frequency up to tens of GHz. The typical input power is of +20 dBm, and in some cases up to +27 dBm. The loss is of 10–40 dB depending on the order of multiplication, on power, and on other parameters. These components are often difficult to use, and the phase noise is highly dependent on the input power [60]. Figure 2-37 shows the

[1]The clock atomic transition is, by definition, 9.192631770 GHz for the unperturbed ^{133}Cs atom. An offset of the order of 1–2 Hz applies, due to the magnetic C-field needed to align the magnetic momentum of all atoms. Therefore, a high-resolution frequency of ≈12.6 MHz must be added to the 9.18 GHz carrier. More modern schemes start from 9.2 GHz, and subtract a high-resolution 7.4 MHz frequency.

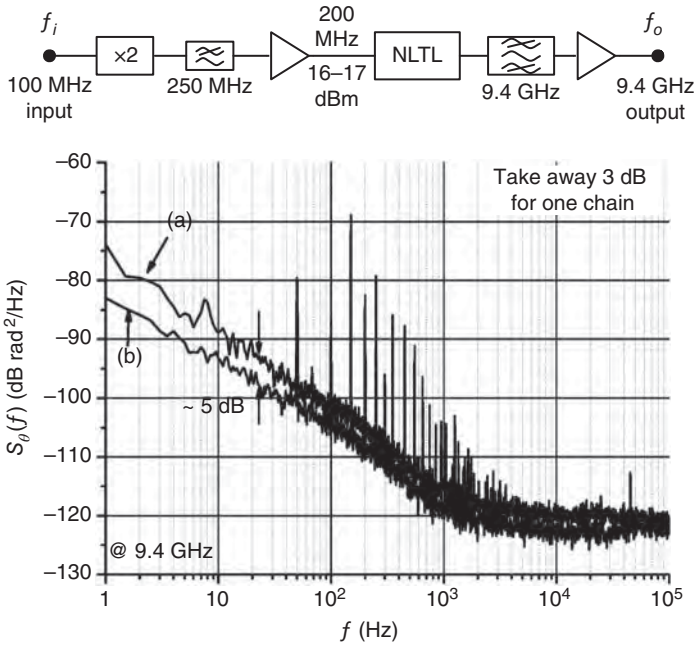


Figure 2-37 Phase noise of a pair of multiplication chains from 100 MHz to 9.4 GHz [61]. The noise is shown for two different values of the input power between +16 and +17 dBm. The phase noise spectrum is © 2009 IEEE, reprinted with permission from [61].

phase noise of a pair of multiplication chains from 100 MHz to 9.4 GHz implemented with nonlinear delay lines. This chain is a part of a miniature atomic clock. The multiplication ×94, inherently, increases the phase noise by 39.5 dB (20 $\log_{10}(94) = 39.5$). So, a floor of approximately −120 dBc/Hz at 9.4 GHz output is equivalent to −160 dBc/Hz at the 100 MHz input. For frequency synthesis, the critical region is beyond about 100 Hz. A flicker PM of −80 dBc/Hz at 1 Hz is extremely low for a 10 GHz signal and exceeds practical needs. For comparison, the PM noise of the best 10 GHz cryogenic oscillators is of the order of −90 dBc/Hz, which gives a frequency stability of 10^{-15} (ADEV at 1 s).

Schottky rectifiers are an appealing option for low-order multiplication (usually 2–3, but up to 7) because low-noise packaged components are available, requiring only an external filter. Figure 2-38 shows some examples of such multiplier. Theoretical efficiency is limited to

$$\eta \propto 1/N^2 \tag{2-96}$$

but practical efficiency is lower. However, the low efficiency is partially compensated by the $\times N^2$ increase in PM noise, inherent in the frequency multiplication. In the end, these multipliers may be a good option as the first stages of high-order multiplication. An example will be provided.

The Schottky diode multiplier deserves attention for special applications, where the thermal and long-term stability of the phase is of paramount importance (timekeeping for space application and for radio navigation). The multiplier can be implemented using only ×2 stages, frequency converters, low-pass filters, and notch filters. The point is that bandpass filters are to be avoided because they suffer from a phase drift determined by the drift of the internal components multiplied by the quality factor Q. Oppositely, low-pass filters and notch filters are immune from this phenomenon if the main signal falls in a region where the frequency response is flat. Accordingly, a multiplier ×4 from 100 MHz can be implemented with two ×2 stages followed by a low-pass at 250 and 500 MHz. These filters are stable because the cutoff frequency of each is far from the carrier frequency. A multiplier ×5 starts from the same ×4, followed by a DBM which adds 100 MHz. Since the mixer delivers 400 ± 100 MHz as the main

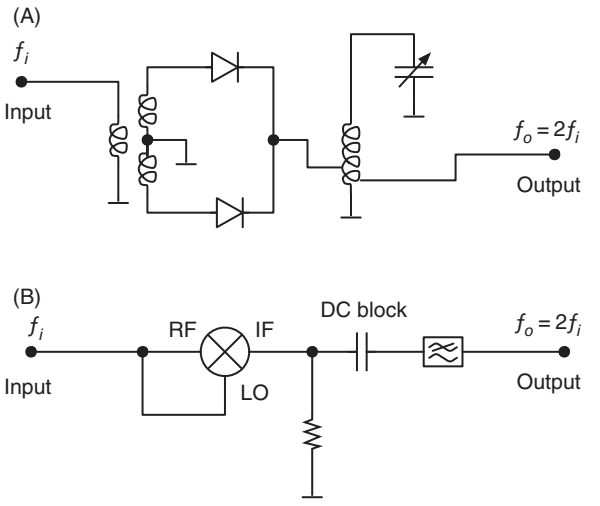


Figure 2-38 Two examples of the Schottky diode multiplier: (A) half bridge, and (B) double balanced mixer. With the scheme (B), frequency doubling ($N = 2$) is preferred.

products, a notch removes the unwanted 300 MHz, and a 550 MHz low-pass cleans the output. The notch filter may suffer from thermal effects at 300 MHz, yielding minor changes in the spur rejection, but the phase of the 500 MHz signal is stable.

Example 9 Frequency Multiplication. We analyze the frequency doubling of a low-noise 100 MHz oven-controlled crystal oscillator (OCXO) using a Mini Circuits LK3000+ frequency doubler. The OCXO has a PM noise floor of −175 dBc/Hz and output power $P = +14$ dBm. The doubler has a loss of 10.5 dB. It is followed by a 250 MHz low-pass filter (0.5 dB loss at 200 MHz) and an amplifier (noise factor $F = 2$ dB). Let's evaluate the phase noise.

First, the thermal noise at the oscillator output is $kT/P = -174 - 14 = -188$ dB rad^2/Hz, thus −191 dBc/Hz. This is 16 dB lower than the oscillator floor, thus guessing 2 dB noise factor for the multiplier will not change the result. *Second*, the power at the amplifier input is +3 dBm ($+14 - 10.5 - 0.5 = 3$). Hence, the PM noise of the amplifier is $FkT/P = +2 - 174 - 3 = -176$ dB rad^2/Hz, thus −179 dBc/Hz. *Third*, the oscillator noise scaled up to 200 MHz is −169 dBc/Hz ($-175 + 6 = -169$), which is 10 dB higher than the amplifier noise. The *conclusion* is that the noise is set by the $S_{\theta o}(f) = N^2 S_{\theta i}(f)$ rule, and that the overall noise of the multiplier is negligible. Should we want *further multiplication*, we start from −169 dBc/Hz instead of −175 dBc/Hz. Therefore, the second stage will be more tolerant to the noise of the components, and it will be easier to keep with the $\times N^2$ law. ■

For extremely high frequencies, hundreds of GHz or some THz, it is necessary to start from a clean microwave oscillator, optionally locked to a stable HF/VHF reference. Conversely, the direct multiplication of a HF oscillator will probably fail because of an intrinsic property of frequency multiplication. PM is ruled by the Bessel $J(\beta)$ functions, where β is the modulation index. Thus, J_0 for the carrier, J_1 for the first-order sidebands, J_2 for the second-order sidebands, etc. The $\times N^2$ scaling rule is an approximation that holds for small angle modulation, where only carrier and first-order sidebands are considered. Since the total RF power is independent of the modulation index, energy conservation requires that the sideband power comes at expenses of the carrier. When the modulation index approaches 2.4, $J_0(\beta)$ nulls, and the carrier sinks abruptly in the noise pedestal. Unlike the simple case of sinusoidal modulation, where the carrier re-appears at higher modulation index following the oscillating behavior of $J_0(\beta)$, the carrier is lost because of the statistical nature of the many spectral component, which constitutes the random PM. This phenomenon, called *carrier* collapse, challenged the early attempts to design high frequency synthesizers starting from the stable 5 or 10 MHz OCXOs [62, 63].

Two technologies are in competition for THz frequency multipliers, the heterostructure barrier varactor, and the Schottky diode [64]. The former is suited for the generation of odd harmonics due to internal symmetry. The latter is the simplest devices, and indeed probably the best for high efficiency. For these reasons it will probably be the preferred option for future applications. Anyway, the THz region is beyond our scope, and the reader should refer to the literature.

2-3-4 Direct Digital Synthesizer (DDS)

The DDS is such an important block in modern frequency synthesis that deserves special attention. This section describes the general principles and the phase noise of commercial components. Most of the material is based on our earlier article [65]. The reader may learn more about the DDS from several references listed in the Suggested Readings at the end of this chapter.

Theory of Operation

The principle of operation follows immediately from the block diagram shown on Figure 2-39. The register is a m-bit D-type flip-flop called *phase accumulator*. The accumulator content at the discrete time k is the integer number x_k, which takes a value from 0 to $2^m - 1$. At each clock cycle, x is incremented by N modulo 2^m. This means that, when x reaches or exceeds 2^m, the overflow is ignored and counting goes on from the reminder. In formula

$$x_{k+1} = \left(x_k + N\right) \mod 2^m \tag{2-97}$$

The modulo-2^m register is the hardware implementation of a finite field, which we find most convenient to represent as a set of 2^m points equally spaced on the circle $z = \exp(j2\pi x/2^m)$ in the complex plane (Figure 2-40). At each point x_k is associated the complex number z_k that has absolute value equal to one and phase $\vartheta_k = \arg(z_k) = 2\pi x_k/2^m$. The accumulator content x describes a discrete sawtooth waveform, which is converted into a sinusoidal signal by the look-up table (LUT) and the digital-to-analog converter (DAC) that follows.

For the layman, the complex-plane representation of the phase accumulator is similar to a watch dial, with the trivial difference that our "dial" has 2^m points instead of 60 s, and the hand jumps forward (counterclockwise) by N points at each tick of the clock signal, starting from the origin at "3 o'clock." Far beyond our concerns, the circular representation of a finite field is a serious branch of number theory, which has roots in the ancient Greek problem of the cyclotomy, that is, dividing the circle into a given number of equal angles and constructing regular polygons.

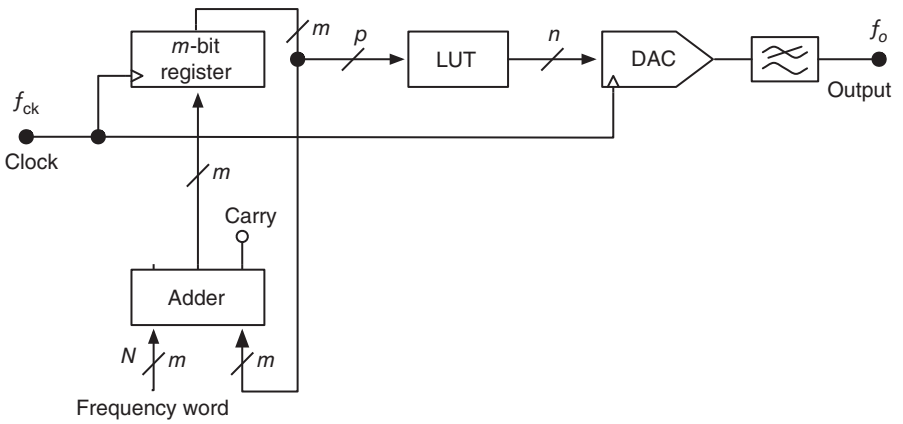


Figure 2-39 Principle of operation of the direct digital synthesizer.

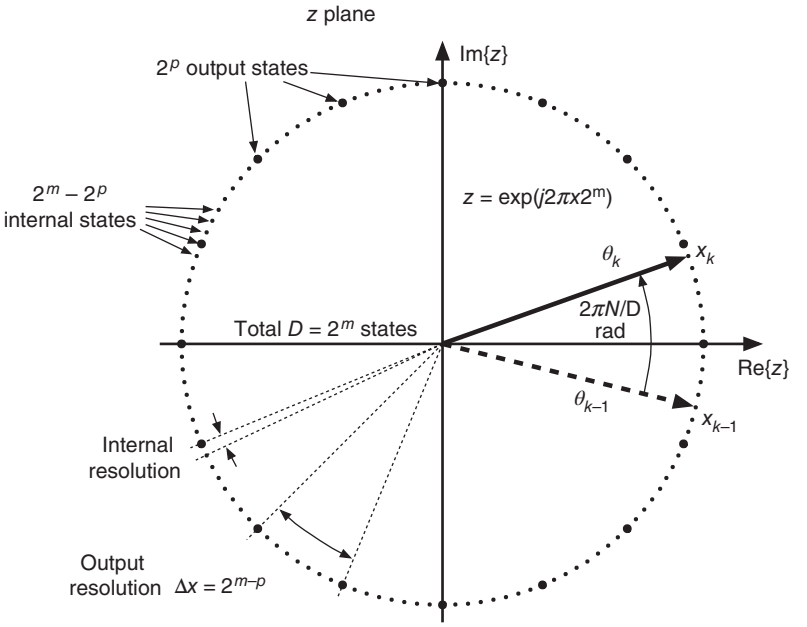


Figure 2-40 Complex-plane representation of the phase accumulator operation.

The output frequency is

$$f_o = \frac{N}{D} f_{\text{ck}}, \quad D = 2^m \tag{2-98}$$

By changing $N \rightarrow N + 1$, we find that the frequency resolution is given by

$$\Delta f_o = \frac{1}{D} f_{\text{ck}} \tag{2-99}$$

The term numerically controlled oscillator (NCO) was originally used instead of DDS. In current jargon, the term NCO refers to the scheme of Figure 2-39, without the output DAC. The NCO is found as a useful building block in FPGAs and in advanced digital components. Oddly, some recent DACs have a built-in NCO. This is the case of the AD9144 (quad DAC, 2.8 GS/s, 16 bit, with internal 48-bit NCO) and of the AD9161/9162 DAC (6 GHz RF synthesis, 16 bit, 11 bit ENOB, internal 48-bit NCO). Modern DDS chips integrate complex functions like modulation, sweep, amplitude, phase control, etc., which may not be implemented in the DACs with embedded NCO.

Our graphical and mathematical introduction describes a DDS free from noise and spurs. Practical DDSs have a phase accumulator with $m = 24$–48 bits, an output DAC with 10–16 bits, and operate at clock frequency up to a few GHz. Noise and spurs are a particularly complex topic. A simplified digression is given in the following text.

Signal to Quantization Ratio (SQR)

The quantization noise is easy to derive using the methods given in the seminal article [66]. A sinusoidal current swinging over the full-scale range I_{FSR} flowing through a resistor R results in a power

$$P = \frac{1}{8} R I_{\text{FSR}}^2 \tag{2-100}$$

The quantization step of a n-bit converter is $I_q = I_{\text{FSR}}/2^n$. Assuming that the quantization results in a random error with rectangular probability function uniformly distributed between $\pm I_q/2$, the associated noise power is

$$\sigma_q^2 = \frac{1}{12} R I_q^2 = \frac{1}{12} \frac{R I_{\text{FSR}}^2}{2^{2n}} \tag{2-101}$$

The signal-to-quantization ratio (SQR) $= P/\sigma_q^2$ is given by

$$\text{SQR} = \frac{3}{2} 2^{2n} \tag{2-102}$$

or

$$\text{SQR} = 1.76 + 6.02\, n \ \text{dBc} \tag{2-103}$$

Using a fraction $a < 1$ of the full-scale range, the SQR decreases by a factor a^2. The hypothesis that the quantization is random in amplitude fits well the observation. However, the SQR relates only to the total power of the quantization error, not to the spectrum. Because the quantization applied to deterministic signals is not random, a fraction of the quantization noise may be organized in harmonic distortion and spurs.

Analog components inside the DAC and at the output contribute a term σ_a^2. Thus, the total noise is $\sigma^2 = \sigma_q^2 + \sigma_a^2$. Interestingly, the noise σ_a^2 of actual components is close to the limits of the technology and also close to fundamental limits. By contrast, the quantization noise σ_q^2 can be reduced by increasing the number of bits, at least within certain limits. Increasing the number of bits has moderate impact on complexity and cost. The critical number n_c of bits, where $\sigma_q^2 = \sigma_a^2$, is of paramount importance in the *design of* converters, and also in *designing with* converters. It is wise to have $n > n_c$, so that the total noise is chiefly limited by σ_a^2. With 2–4 bits in excess, the quantization noise is 12–24 dB smaller than the analog noise. This choice also results in significantly reduced distortion and spurs because these artifacts originate from the non-random nature of the quantization.

The equivalent number of bit (ENOB) results from an attempt of simplification, describing total noise $\sigma^2 = \sigma_q^2 + \sigma_a^2$ with a single parameter. So, the engineer uses the formula

$$\sigma^2 = \frac{1}{12} \frac{R I_{\text{FSR}}^2}{2^{2\,\text{ENOB}}} \tag{2-104}$$

and that's it. The catch is that the ENOB hides the difference between analog noise and quantization noise, and their statistical proprieties. The ENOB is suitable to signals with sufficiently good random characteristics, like audio communication. Conversely, synthesizers deliver highly coherent signals. In this case, the ENOB fails to describe the quality of the output because the quantization noise yields artifacts, harmonics, and spurs, while the analog noise does not.

Truncation Spurs

The output DAC has a finite number n of bits, which in turn determines the number p of address bits that gives distinct values at the LUT output. Higher number of bits results in duplicated codes at the LUT output, and in no improvement. The value $p = n + 2$ or $p = n + 3$ is often found. The full m-bit word of the accumulator represents the exact instantaneous phase, given by $x_{k+1} = x_k + N \bmod 2^m$. However, the voltage delivered to the output is determined only by the higher p bits. In other words, the accumulator defines 2^m possible phases, or states (all the dots on the circle of Figure 2-40), but only 2^p distinct phases (the thick dots on the circle) can be delivered to the output. The resolution $\Delta x = 2^{m-p}$ results in a round off phase error distributed from 0 to $\Delta\vartheta$, where $\Delta\vartheta = 2\pi/2^{m-p}$ rad. Such error is of pseudo-random nature because it results from the fully deterministic operation of the accumulator (the DAC analog noise is not counted here). Pseudo-randomness, as opposite as true randomness, originates spurs. This can be understood by analyzing carefully the Accumulator and the Frequency Control Word (Figure 2-41).

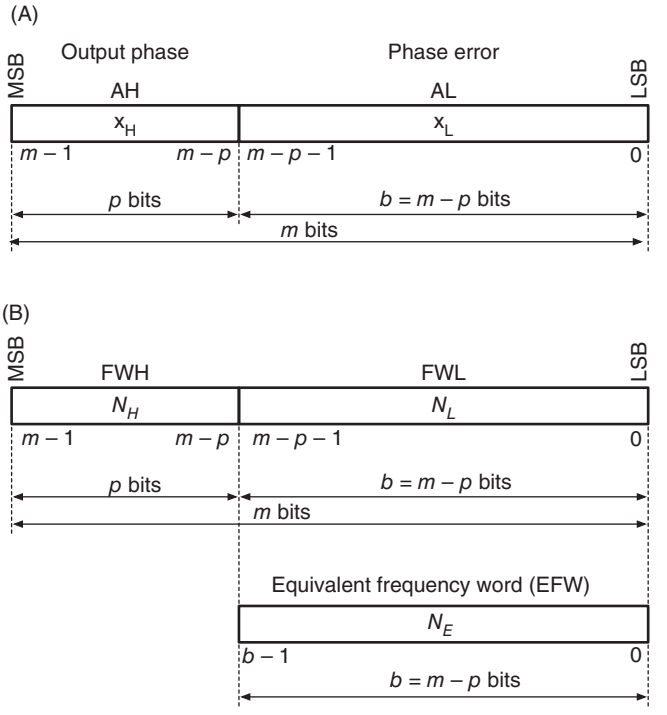


Figure 2-41 (A) Accumulator and (B) frequency word.

For easier interpretation, it is useful to divide the accumulator into two sections, accumulator high (AH) and accumulator low (AL), thus $x = x_H + x_L$. AH has the size of p bits and generates the output phase. AL has the size of $m - p$ bits and generates the truncation spurs. Similarly, we divide the frequency word (FW) in two parts, FWH (the higher p bits), and FWL (the lower $m - p$ bits. Notice that the most significant bit (MSB) of FW must be zero, otherwise f_o exceeds $f_{ck}/2$ and the output frequency results from aliasing.

An important case is FWH containing an odd number, and FWL containing all zeros

FWH	FWL
0xxxxxx**1**	0000000000000000

Accordingly, the value x_k is incremented in steps equal to Δx starting from zero. Thus, at each clock cycle, x_k jumps to the next thick dots on the circle and AL contains all zeros. There is no phase truncation, and no truncation spurs. The case of FWH containing at least one "1," and FWL containing all zeros is an obvious extension. Now x_k walks through the thick dots in steps multiple of Δx, the step being determined by the position of the rightmost "1," and there is no truncation.

Another important case is FWL containing all zeros, but the MSB is equal to one

FWH	FWL
0xxxxxxx	**1**000000000000000

The accumulator content x increments in steps exactly equal to $\Delta x/2$, hence the truncation error is a square wave of peak-to-peak amplitude $\Delta x/2$. This is the condition of maximum spurs. The maximum spur-to-carrier ratio is 2^{-2p}, that is, $-6.02\,p$ dBc/Hz.

The accumulator content x is periodic. It starts from zero and it first returns to zero after a number of clock cycles called Grand Repetition Period[2] (GRP). The maximum GRP is equal to 2^m clock periods, thus $2^m/f_{ck}$ seconds, and occurs when N is an odd number (the FW has the LSB equal one). The GRP can be rather long. For example, with $f_{ck} = 1$ GHz and $m = 48$ bits, the GRP is $2^{48} = 2.81 \times 10^{14}$ clock periods, thus 2.81×10^5 s (3.25 days). If the FW contains r trailing zeros

FWH	FWL
0xxxxxxx	000000000**1000000**
m−1	**r** 0

the GRP is given by

$$\mathrm{GRP} = 2^{m-r} \tag{2-105}$$

This is rather obvious because x is incremented in steps odd multiples of 2^r, thus the lowest r bits of the accumulator will always be zero. We can see this as a smaller DDS, where the accumulator has $m - r$ bits.

The simplest way to understand the truncation spurs is to interpret AL as an accumulator, which behaves in the same way as the full accumulator (Figure 2-41). In fact, the content x_L increments in steps and overflows, exactly as x does. The trivial difference, that the overflow of AL goes to AH while the overflow of AH is discarded, is not relevant here.

Since AL has a number $b = m - p$ of bits, its operation is described by the equation

$$x_{L,k+1} = x_{L,k} + N_E \bmod 2^b \tag{2-106}$$

where the increment

$$N_E = \begin{cases} N_L & \text{for } N_L < 2^{b-1} \\ 2^b - N_L & \text{for } N_L \geq 2^{b-1} \end{cases} \tag{2-107}$$

is the content of the equivalent frequency word (EFW). N_E results from the following reasoning. If the MSB of the FWL is zero ($N_L < 2^{b-1}$), N_L is a valid FW, and $N_E = N_L$. By contrast, if the MSB is equal to one ($N_L \geq 2^{b-1}$), the frequency exceeds half the clock frequency. The frequency observed is in the first Nyquist zone, determined by $N_E = 2^b - N_L$.

The accumulator content x_L is periodic. It starts from zero and it first returns to zero when x falls on one of the thick dots in the circle. This occurs after a number of clock cycles called Truncation Grand Period

$$\mathrm{TGP} = 2^{b-r} \tag{2-108}$$

The value x_L describes a sawtooth (Figure 2-42) whose period is the Sawtooth Repetition Period

$$\mathrm{SRP} = \frac{2^b}{N_E} \tag{2-109}$$

[2]The GRP is a period in a strict sense. However, the term GRR (grand repetition rate) is sometimes used, which is misleading because the word "rate" refers to a frequency.

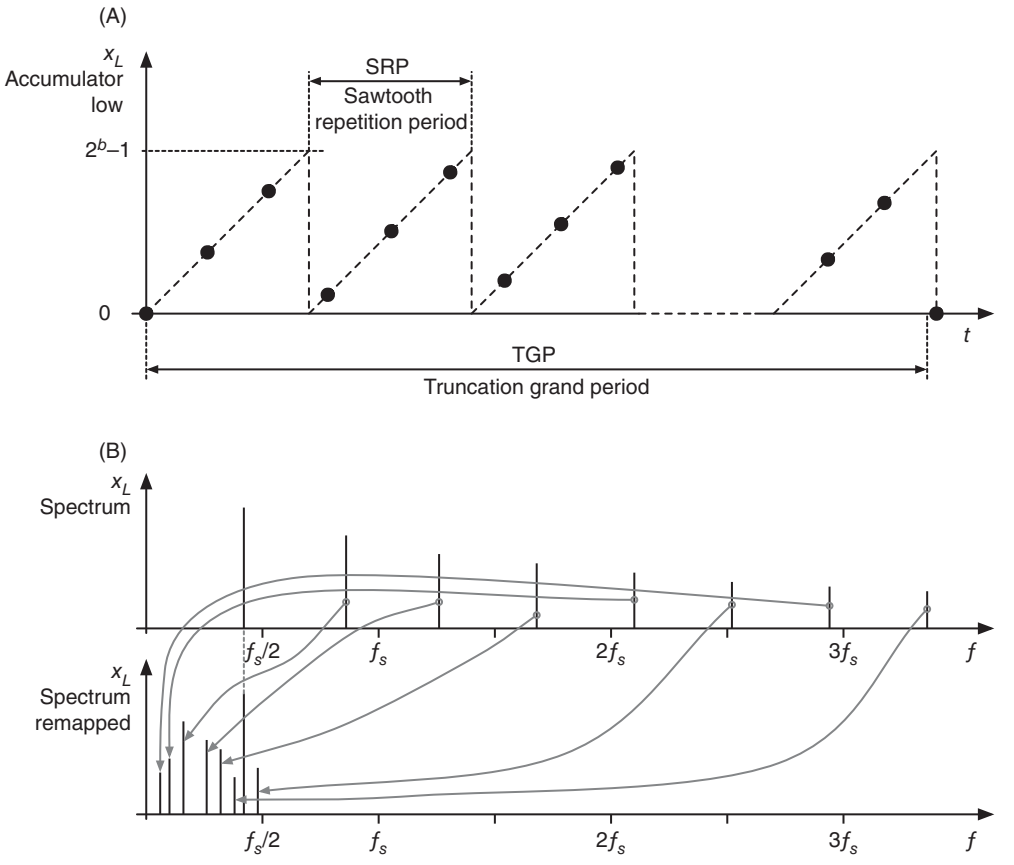


Figure 2-42 (A) Phase error due to the truncation of the accumulator content, and (B) aliasing brings the harmonics of the sawtooth to the first Nyquist zone.

The spectrum of the sawtooth waveform contains all the harmonics multiple of 1/SRP, with amplitude proportional to the reciprocal of the order. The sawtooth is sampled, so all the harmonics exceeding $f_s/2$ are remapped to the first Nyquist zone. The number of samples of x_L in the grand period is equal to TGP. Hence, the discrete transform has TGP/2 = 2^{b-r-1} frequencies. This completely describes the spectrum of the truncation spurs. Unfortunately, the theory is of limited usefulness because the spurs spectrum depends on N_L and changes abruptly changing the FW.

Our approach to the truncation spurs derives from Ref. [67]. Among the suggested readings, we recommend a technical tutorial published by Analog devices, an article by Torosyan, the two seminal articles by Nicholas and Samueli, and a book by Widrow and Kollar, the latter only to the reader willing to tackle an extensive mathematical treatise on the quantization noise.

Other types of spurs arise from harmonic distortion in the output DAC and in the analog electronics that follows. Of course, aliasing is always present, so all the harmonics exceeding $f_s/2$ are remapped to the first Nyquist zone.

Phase Noise

Figure 2-43 shows a simplified noise model of a DDS, and highlights the two basic mechanisms. The noise of the input clock is scaled down according to

$$S_{\theta o}(f) = \left(\frac{N}{D}\right)^2 S_{\theta \mathrm{ck}}(f) \tag{2-110}$$

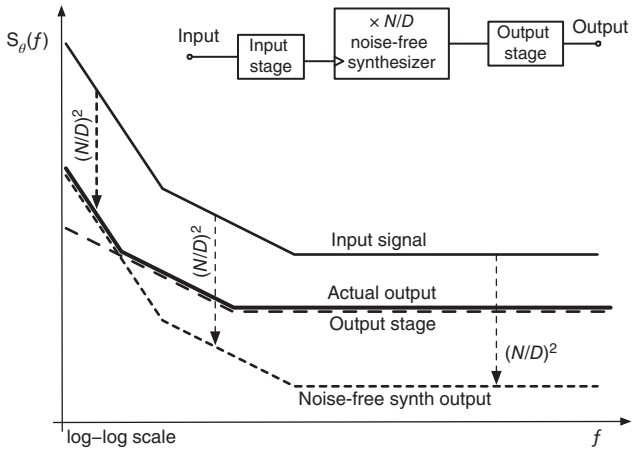


Figure 2-43 Simplified noise model of a synthesizer. Reproduced with permission from [65]. © 2012 IEEE.

because the noise-free synthesizer transfer the time fluctuation $x(t)$ from the input to the output. Unlike in frequency dividers, aliasing has no practical effect on noise scaling because the output DAC samples always at the clock frequency, regardless of the output frequency. The same rule applies to the noise of the input stage, and to the noise of the clock distribution as well, both of the time type. This is rather obvious because the input frequency has a fixed value, thus the time fluctuation at the input and all long the clock distribution does not depend on the output frequency. The output stage adds its own noise. The latter is at first approximation of the phase type, defined by the phase-fluctuation spectrum being independent of frequency. This behavior is similar to that of amplifiers and other analog components. In conclusion, the phase noise follows the $(N/D)^2$ law at high N (high output frequency) and hits the limit set by the output stage at low N. The critical N, where output stage limits, depends on the noise type.

The aforementioned concepts need to be analyzed more in detail. The phase noise of a real DDS includes

- The quantization noise of the output DAC
- The analog noise at the DAC output, and of the stages which follow
- The time fluctuation of the DAC sampling, with respect to the clock input

We have already seen that the signal power is $P = RI_{\mathrm{FSR}}^2/8$, and that the noise power is

$$\sigma_q^2 = (1/12)\, RI_{\mathrm{FSR}}^2/2^{2n} \tag{2-111}$$

The noise bandwidth B is half the sampling frequency, thus $B = f_{\mathrm{ck}}/2$. Starting with the provisional assumption that the spectrum is white, the PSD is equal to σ^2/B. The phase noise PSD results from σ_q^2/P

$$S_{\theta q}(f) = \frac{4}{3}\,\frac{1}{2^{2n} f_{\mathrm{ck}}} \tag{2-112}$$

The hypothesis of white noise is generally untrue in frequency synthesis because of truncation and nonlinearity. In turn, the spurs sink power from noise, or from some portion of, and the noise floor can be lower than in (2-112). Figure 2-44 shows an example.

Flicker noise is a separate issue. It originates from the DAC output and from the analog electronics that follows. This type of noise is generally of the phase type, that is, $S_\theta(f)$ is rather constant versus the output frequency, and described by the experimental parameter b_{-1}

$$S_\theta(f) = \frac{b_{-1}}{f} \quad \text{(flicker)} \tag{2-113}$$

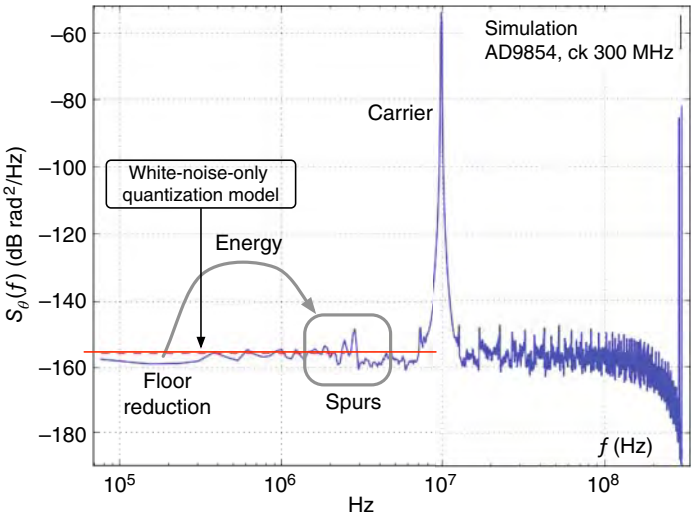


Figure 2-44 A simulation shows the effect of spurs on the noise floor. Adapted version, reproduced with permission from [65]. © 2012 IEEE.

The jitter of the output sampling must be added to the model. It originates in the DAC switching mechanism and in the DDS internal clock distribution from the input to the DAC. This noise is of the time type, thus the time fluctuation $S_x(f)$ is independent of f_0. Such fluctuation appears on the phase noise PSD as

$$S_{\theta\,\mathrm{jit}}(f) = 4\pi^2 f_0^2 S_{x\,\mathrm{jit}}(f) \tag{2-114}$$

Having on hand the phase noise spectrum taken at different values of f_o, we can identify the parameters of the phase-type and of the time-type noise processes, and use them to predict the phase noise in the general case.

Examples

The phase noise measured on commercial DDSs confirms our theoretical models, and also shows some unpredicted facts, inevitable in practical implementations.

Figure 2-45 shows the phase noise of an AD9854 DDS driven with 180 MHz clock frequency, and measured at various output frequencies. The phase noise results from a differential measurement, where the noise of the 180 MHz source cancels because the same source is also used as the reference for the phase meter.

First, we observe that the flicker b_{-1} scales down as $1/f_o^2$, that is, 6 dB per factor of two. This is the signature of the time-type noise, where $S_x(f) = S_\theta(f)/(2\pi f_o)^2$ is independent of f_0, as shown on Table 2-7. The phase noise leaves the $1/f_o$ law only at the lowest values of f_o, where some phase-type noise shows up. The same happens with white noise, yet the phase-type noise starts to be visible at higher f_o.

In the region between 300 Hz and 30 kHz, the phase noise leaves the polynomial law, being higher than the $1/f$ asymptote. Other experiments show that this is due to the residual noise in power-supply lines. So, this behavior may be specific to our measurement rather than a property of the device. At very low Fourier frequencies, below 1 Hz, the phase noise follows an unexpected $1/f^3$ slope (−30 dB/decade). This is due to thermal effects. The evidence is that stabilizing the chip temperature with different heat sinks and thermal masses clamped onto the chip surface shifts the $1/f^3$ corner to lower frequencies. In more recent DDSs, a similar thermal effect appears at lower Fourier frequencies, or has not been detected. This makes us think that the thermal design in the newest components has been significantly improved.

In our measurements, we combined the two outputs of the DAC using a balun (transformer) to get the highest output power, and we used a low-noise RF amplifier at the balun output. Out of experience, we have identified two

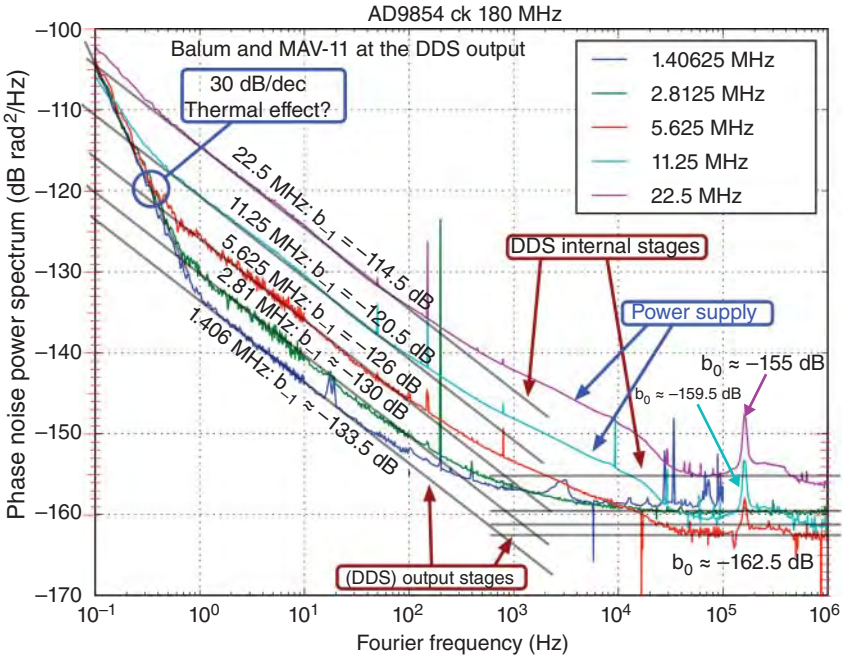


Figure 2-45 Phase noise of the AD9854 DDS measured at different output frequencies. Reproduced with permission from [65]. © 2012 IEEE.

Table 2-7 Flicker noise of the AD9854 DDS

f_0 (MHz)	Scale factor (dB)	b_{-1} (dB rad^2)	$\sqrt{b_{-1}}$ (rad)	k_{-1} (dB s^2)	$\sqrt{k_{-1}}$ (s)
22.5	0 (ref)	−114.5	1.9×10^{-6}	−277.5	1.33×10^{-14}
11.25	−6	−120.5	9.4×10^{-7}	−277.5	1.34×10^{-14}
5.63	−12	−126	5.0×10^{-7}	−277.0	1.42×10^{-14}
2.81	−18	−130	3.2×10^{-7}	−274.9	1.79×10^{-14}
1.41	−24	−133.5	2.1×10^{-7}	−272.4	2.39×10^{-14}
	$(f_o/f_{\text{ref}})^2$	From the plot		$b_{-1}/4\pi^2 f_0^2$	

Values are taken from Figure 2-45.

weak designs that result in unnecessarily higher white PM noise. The first is the use of single output of the DAC, and the second is the use of a high-speed operational amplifier at the DDS output, instead of the RF amplifier. Trite calculations using the noise parameters available in the data sheet give full account.

Most DDSs feature a digital amplitude control. In noise-critical application, the DDS should be operated close to the full-scale range, using this control only for fine tuning. The reason is that the amplitude control generally scales down the values at the LUT output, thus the DAC uses only a fraction of its dynamic range. At half amplitude one bit is lost, and the phase noise gets 6 dB worse. A practical example is seen on Figure 2-46. Of course, amplitude control acting on the reference of the DAC mitigates this problem.

Example 10 Hacking the AD9912 DDS. The phase noise spectrum of the AD9912 is shown in Figure 2-47. We try to understand the noise parameters that describe this device. From this figure, we calculate the flicker coefficients shown on Table 2-8. In this table, we use the coefficients of the polynomial law, b_i for $S_\theta(f)$, and k_i for $S_x(f)$. We take 150 MHz as the reference. From 150 to 50 MHz, $S_\theta(f)$ scales down in exact agreement to the

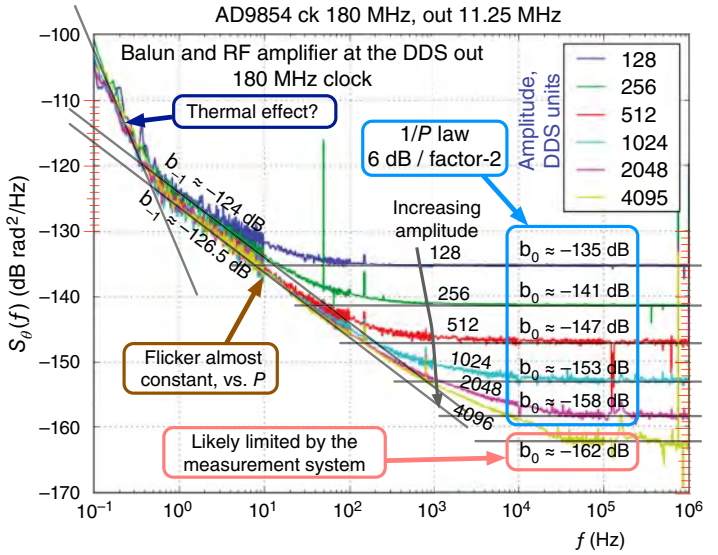


Figure 2-46 Phase noise of the AD9854 DDS measured at different output frequencies. Reproduced with permission from [65]. © 2012 IEEE.

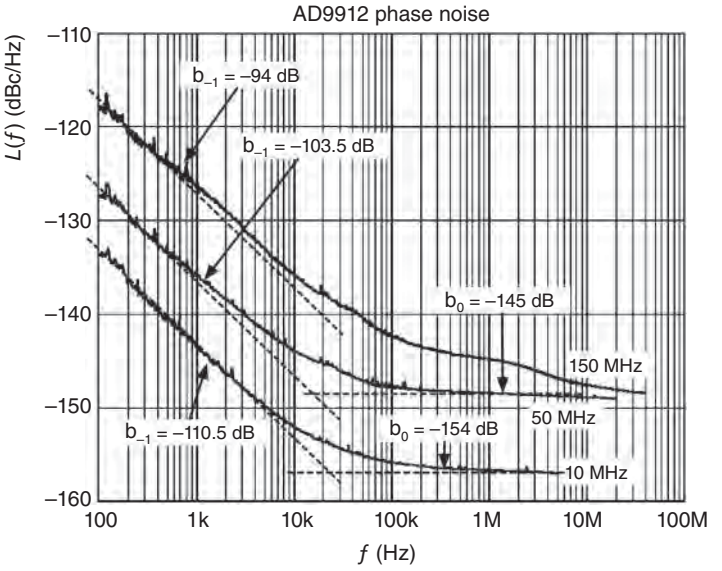


Figure 2-47 Example of phase noise of a DDS (the units rad^2 and rad^2/Hz in the polynomial-law coefficients are omitted). The PM noise spectrum is from the AD9912 data sheet, © Analog Devices, reproduced with permission. Graphical adaptation and comments are ours.

Table 2-8 Flicker noise of the AD9912 DDS

f_0 (MHz)	Scale factor (dB)	b_{-1} (dB rad^2)	$\sqrt{b_{-1}}$ (rad)	k_{-1} (dB s^2)	$\sqrt{k_{-1}}$ (s)
150	0 (ref)	−94	2×10^{-5}	−273.5	2.11×10^{-14}
50	−9.5	−103.5	6.68×10^{-6}	−273.4	2.14×10^{-14}
10	−23.5	−110.5	9.44×10^{-6}	−266.5	4.73×10^{-14}
	$(f_o/f_{\text{ref}})^2$	From the plot		$b_{-1}/4\pi^2 f_0^2$	

Values are taken from Figure 2-47 (data sheet).

$(f_o/f_{\text{ref}})^2$ law, and k_{-1} is the same. This is the signature of the *time-type noise*. Conversely, at 10 MHz the flicker is 7 dB higher than the $(f_o/f_{\text{ref}})^2$ law. This happens because the scaled-down noise hits the noise of the output stage, which is *phase-type noise*. At 10 MHz, we calculate

$$\left[b_{-1}\right]_{\text{phase type}} = \left[b_{-1}\right]_{\text{total}} - \left[b_{-1}\right]_{\text{time type}}$$

The time-type noise scaled down to 10 MHz is $\left[b_{-1}\right]_{\text{time type}} 1.78\times10^{-12}$ rad^2. Thus,

$$\left[b_{-1}\right]_{\text{phase type}} = 8.91\times10^{-12} - 1.78\times10^{-12} = 7.13\times10^{-12}\ \text{rad}^2$$

In conclusion, the flicker of the DDS is given by

$$b_{-1} = 4.5\times10^{-28}\left(2\pi f_o\right)^2 + 7.13\times10^{-12}\ \text{rad}^2$$

The evaluation of white PM noise is not trusted because we have only two values, thus we have no evidence of time-type noise at f_o. With this reservation, we can solve the system

$$\left[b_0\right]_{\text{phase type}} + \left(2\pi f_1\right)^2\left[k_0\right]_{\text{time type}} = 10^{-14.5} \qquad f_1 = 50\ \text{MHz}$$

$$\left[b_0\right]_{\text{phase type}} + \left(2\pi f_2\right)^2\left[k_0\right]_{\text{time type}} = 10^{-15.4} \qquad f_2 = 10\ \text{MHz}$$

which gives $\left[b_0\right]_{\text{phase type}} = 2.83\times10^{-16}$ and $\left[k_0\right]_{\text{time type}} = 2.83\times10^{-16}$, and an overall phase noise $b_0 = 2.92\times10^{-32}\left(2\pi f_o\right)^2 + 2.83\times10^{-16}$ rad^2/Hz. ■

A small number of samples were measured at the Italian Institute of Metrology INRiM. The flicker noise of one of these samples is shown on Table 2-9. The value measured is some 12 dB lower than the spectrum found in the datasheet. Using the data of Table 2-9, the flicker phase noise is

$$b_{-1} = 2.5\times10^{-29}\left(2\pi f_o\right)^2 + 4.4\times10^{-14}\ \text{rad}^2$$

We have little doubt about the measurement made in a laboratory of primary metrology, repeated several times in well controlled conditions, and reproducible over a small number of samples. Conversely, the datasheet says very little about how the spectrum is measured. Whether an unfortunate error was made in the datasheet, or the difference is due to samples from different batches, we cannot know. Nonetheless, the datasheet reports a conservative value, and a lower noise measured on a sample came as a good surprise. The general practitioner relies on data sheets and has seldom the time and equipment for independent measurements.

As we have seen with amplifiers, the documentation about flicker noise is usually rather poor, as compared with our wishes. Occasional difficulties and frustrations, like in this example, are a part of the message we address to the reader.

Table 2-9 Flicker noise of the AD9912 DDS, measured at the Italian Institute of Metrology INRiM

f_0 (MHz)	Scale factor (dB)	b_{-1} (dB rad^2)	$\sqrt{b_{-1}}$ (rad)	k_{-1} (dB s^2)	$\sqrt{k_{-1}}$ (s)
100	0 (ref)	−110	1.9×10^{-6}	−286.0	5.03×10^{-15}
50	−6	−116	9.4×10^{-7}	−285.9	5.04×10^{-15}
25	−12	−122	5.0×10^{-7}	−285.9	5.06×10^{-15}
12.5	−18	−128	3.2×10^{-7}	−285.9	5.07×10^{-15}
6.25	−24	−131.5	2.1×10^{-7}	−283.4	6.78×10^{-15}
3.125	−30	−131.5	2.1×10^{-7}	−277.4	1.36×10^{-14}
	$(f_o/f_{\text{ref}})^2$	From the plot		$b_{-1}/4\pi^2 f_0^2$	

Source: Courtesy of Claudio E. Calosso, INRiM.

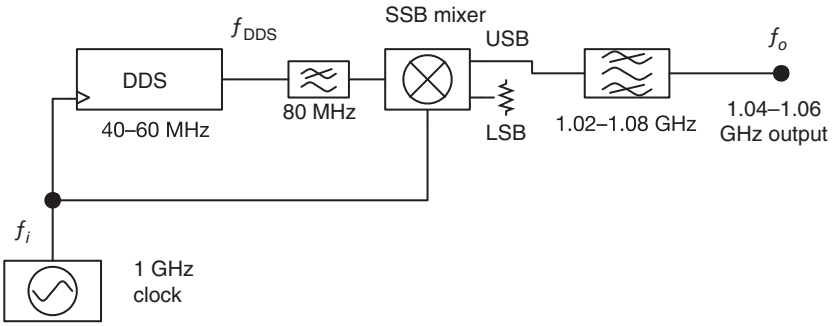


Figure 2-48 Example of application of a DDS in a dedicated synthesizer.

Example 11 An application of the AD9912 DDS. We synthesize a high resolution 1.04–1.06 GHz signal using the scheme of Figure 2-48. The DDS has $m = 48$ bits, thus the resolution is $\Delta f_o = f_{ck}/2^{48} = 7.1$ μHz. Considering the oscillator as an external source, the noise of this synthesizer originates in the mixer and in the DDS. We see on Figure 2-47 that at 50 MHz the phase noise of the DDS is significantly higher than that of a mixer, and from the previous example we expect that the change in the DDS phase noise is a matter of 2 dB in a ±10 MHz region around 50 MHz. The expected phase noise is therefore

$$S_\theta(f) = \frac{4.5\times10^{-11}}{f} + 3.2\times10^{-15}\ \text{rad}^2/\text{Hz}$$

An output frequency in the same range can be obtained multiplying the DDS output by $M = 21$. In this case, the benefit of beating is lost. The resolution is $\Delta f_o = Mf_{ck}/2^{48} = 149$ μHz, and the phase noise by M^2, thus $S_\theta(f) = 2\times10^{-8}/f + 1.4\times10^{-12}$ rad^2/Hz. ■

2-3-5 Phase Detectors

The designer has different options for the phase detector, the DBM, transistor or field-effect transistor (FET) mixers, the XOR gate, the SR flip-flop, and the phase/frequency detector (PFD), to mention the most known types. Relevant parameters are frequency range, residual noise, and noise immunity. The detector noise is the most important parameter for low-noise PLLs because phase comparison generally occurs at a suitable low frequency, and the detector noise is scaled up according to the N^2 law.

The SR flip-flop and the PFD have internal memory that stores the last phase transition. This makes these detectors unsuitable to noisy signals, where multiple bounces occur at the lock point. Conversely, mixers and XOR suffer very little from bouncing because the bounces are averaged out by the loop. The consequence is just a

reduction in the phase-to-voltage gain K_d. This discussion is useful for the detection of small signal in noise, while all signals inside a synthesizer are clean enough for the noise immunity to have little or no importance, as compared with the residual noise of the detector.

The DBM is considered the lowest-noise detector, and for this reason it is widely used in the measurement of phase noise.

The PFD replaces the SR flip-flop in virtually all applications because it provides a valid output signal also in unlock conditions, and because it mitigates the issue of metastable behavior when the S and R signals are nearly simultaneous. The analysis of noise in the DBM is postponed to Section 2-2-6, where we study the measurement of PM noise. Here, we analyze the PFD restricting or attention to phase noise.

Noise in the Phase/Frequency Detector

The PFD is a digital circuit that receives clean digital signals at its inputs, thus we expect that the *time-type* noise is dominant. Related to this, the parameter commonly found in the data sheets is the figure of merit (FOM), which is the noise contribution of the PFD normalized to 1 Hz, and most often expressed in dBc/Hz.

The usual definition of the FOM refers to white PM noise in a PLL with a $\div N$ divider in the feedback path. Denoting with f_c the comparator input frequency and with f_{VCO} the VCO frequency, N results from $N = f_{\text{VCO}}/f_c$. The formula found in application notes is

$$\text{FOM}_{\text{dBc/Hz}^2} = \left[L(f)\right]_{\text{dBc/Hz}} + 10\log_{10}\left(f_c\right) - 20\log_{10}\left(f_{\text{VCO}}\right) \tag{2-115}$$

A value of $-220 \ldots -230$ dBc/Hz^2 can be taken as the order of magnitude, but the direct comparison between components is not easy because the FOM changes with technology and frequency range. Notice that some commercial PFDs include a prescaler, and such prescaler may also work in fractional-N mode.

Removing the dB notation from (2-115), and using $N = f_{\text{VCO}}/f_c$ in different ways, the white phase noise at the output can be written in the following equivalent forms

$$L(f) = \text{FOM}\ \ N^2 f_c \tag{2-116}$$

$$L(f) = \text{FOM}\ \ N f_{\text{VCO}} \tag{2-117}$$

$$L(f) = \text{FOM}\ \frac{f_{\text{VCO}}^2}{f_c} \tag{2-118}$$

The first two forms focus on the two obvious critical points, comparator, and VCO. The third form is subtler because it reveals the aliasing at the input. References [68, 69] provide insight and useful details.

Gao and Klumperink [70] give an alternate definition of the FOM, which differs in that the power is added, expressed in dBm. So, the FOM of a component taking 2 mW is 3 dB worse than that of an otherwise equal component requiring only 1 mW. The Gao definition is not followed by the manufacturers.

Information about flicker noise in commercial PFDs is often absent or difficult to understand, if not confusing. This reflects a quite general lack of documentation on this topic. The following formula is sometimes found in the technical literature

$$\left[L(f)\right]_{\text{dBc/Hz}} = \left[\text{FOM}_{1/f}\right]_{\text{dBc/Hz}^2} + 20\log_{10}\left(f_{\text{VCO}}\right) - 10\log_{10}(f) \tag{2-119}$$

where the term $-10\log_{10}(f)$ expresses the fact that $L(f)$ is proportional to $1/f$. Removing the dB notation, (2-119) becomes

$$L(f) = f_{\text{VCO}}^2\, \text{FOM}_{1/f}\, \frac{1}{f} \tag{2-120}$$

Example 12 Noise of a PLL with a PFD. We lock a 1 GHz VCO to a 100 MHz reference using a PFD, which has an FOM of -220 dBc/Hz for white noise, and of -260 dBc for flicker, including the $\div 10$ internal prescaler.

Accordingly, phase detection takes place at 10 MHz. Let us evaluate the phase noise at the 1 GHz output and also refer it to the 100 MHz input.

We prefer to convert the dBc into SI units. For white noise, we use $\mathsf{b}_0 = \text{FOM}\ \ Nf_{\text{VCO}}$, with $\text{FOM} = 2 \times 10^{-22}$, $N = 10$, and $f_{\text{VCO}} = 10^9$ Hz. Thus $\mathsf{b}_0 = 2 \times 10^{-12}$ rad^2/Hz, that is, -117 dB rad^2/Hz.

Finally, $L(f) = -120$ dBc/Hz at 1 GHz, and -140 dBc/Hz at 100 MHz, after scaling as $1/N^2$.

For flicker noise, we use $\mathsf{b}_{-1} = \text{FOM}_{\text{flicker}} f_{\text{VCO}}^2$ with $\text{FOM}_{\text{flicker}} = 2 \times 10^{-26}$ and $f_{\text{VCO}} = 10^9$ Hz. Thus, $\mathsf{b}_{-1} = 2 \times 10^{-8}$ rad^2, that is, -77 dB rad^2.

Finally, $L(f) = -80$ dBc/Hz referred to 1 Hz at the 1 GHz output, and -100 dBc/Hz referred to 1 Hz at the 100 MHz input. ■

Example 13 Comparison of Some Multiplication Schemes. Let us consider some options to multiply a high stability 10 MHz reference to 640 MHz by combining multiplication and cleanup PLL, which may include a divider. The phase noise of the reference and of two possible auxiliary VCOs are summarized in Table 2-10, and we look at the configurations shown on Figure 2-49. The reference has a stability $\sigma_y = 8.3 \times 10^{-13}$ (flicker floor). This is easily seen with the formula $\sigma_y^2(\tau) = 2\ln(2)\,\mathsf{h}_{-1}$ (holds for flicker of frequency), and $\mathsf{h}_{-1} = \mathsf{b}_{-3}/f_0^2$(converts FM flicker from S_θ into S_y) seen in Section 2-2-2. Thus $\mathsf{b}_{-3} = 10^{-103/10} = 5 \times 10^{-11}$, $\mathsf{h}_{-1} = 5 \times 10^{-11}/\left(10^7\right)^2$, and $\sigma_y^2 = 6.95 \times 10^{-25}$.

Table 2-10 Data for the Example 13

Oscillator type	Frequency	Noise types				
		RW FM	Flicker FM	White FM	Flicker PM	White PM
OCXO (reference)	10 MHz	—	−103	—	−131	−162
OCXO	128 MHz	—	−67	—	—	−172
SAW	640 MHz	−47	−57	—	—	−170
		dB rad^{2}Hz^3	dB rad^{2}Hz^2	dB rad^{2}Hz	dB rad^2	dB rad^2/Hz

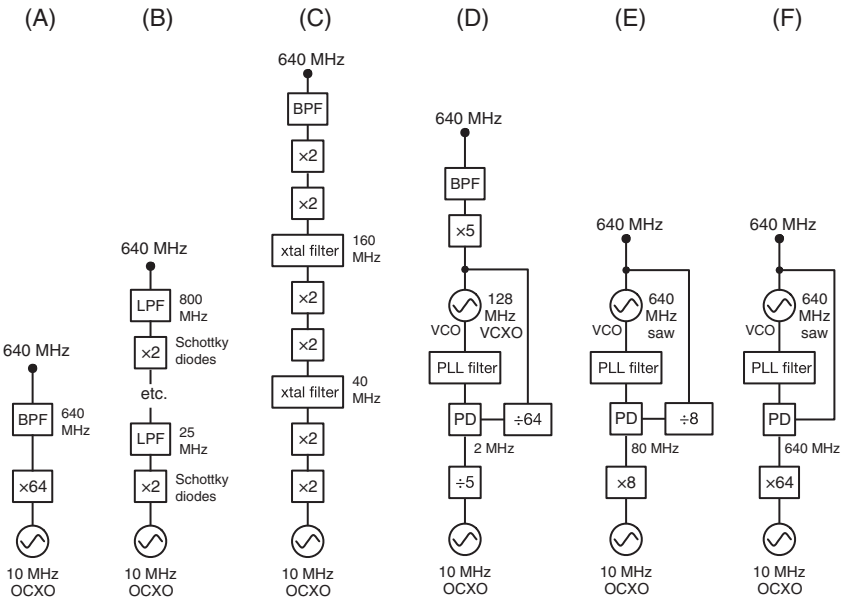


Figure 2-49 Schemes for frequency multiplication from 10 to 640 MHz.

In order to compare the options, we first scale the PM noise of our oscillators to 640, 80, 10, and 2 MHz carrier frequency. These spectra are plotted in Figure 2-50. We start from the schemes A, B, and C, which do not involve phase locking. The scheme A is rather generic, and we expect that the output spectrum is that of the 10 MHz OCXO scaled up to 640 MHz. The output bandpass filter cannot be narrow enough to clean the spectrum, so the phase noise will have a floor of the order of -120 dB rad^2/Hz, which spans over a wide band, hundreds of kHz. The scheme B suffers from the same problem. The scheme C makes use of quartz filters to clean up the phase noise of the 10 MHz OCXO after multiplication. The bandwidth of such filters can be of a few kHz. Besides complexity and cost, the problem is that the filters turn mechanical vibration into PM noise spurs, and temperature drift into phase drift.

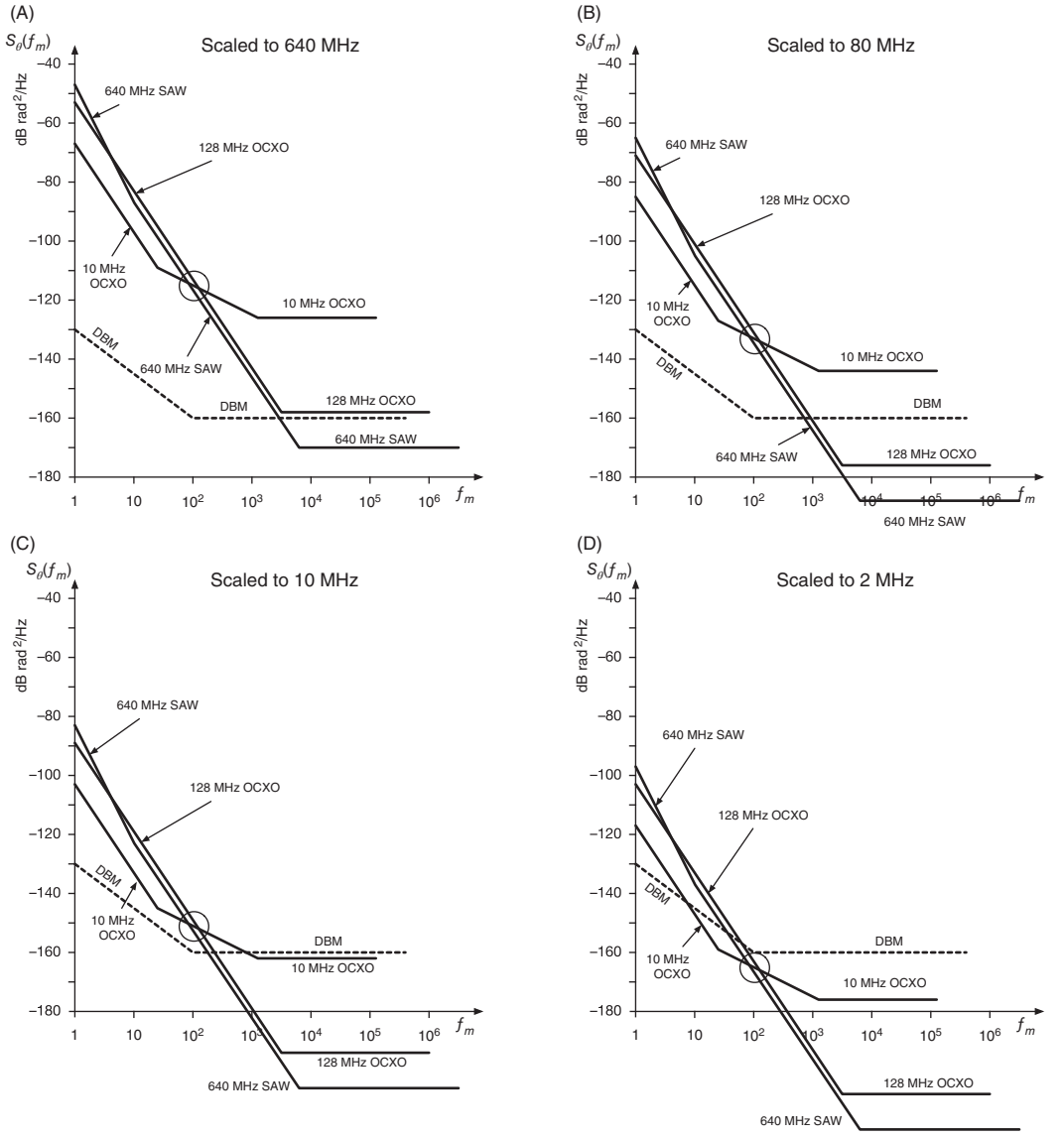


Figure 2-50 Phase noise of the oscillators of Table 2-5. The four spectra (A)–(D) represent the phase noise scaled to different carrier frequencies from 640 to 2 MHz.

In most synthesizer applications, the slow phase drift due to temperature is probably not a problem. However, for special applications and timekeeping, where the phase stability is important, the scheme B probably wins because of its potentially high thermal stability. Unlike the bandpass filter, the phase of the low-pass filters is little affected by the temperature fluctuations.

The schemes D, E, and F make use of phase locking. We see on Figure 2-50 that the preferred cutoff frequency f_c is of approximately 100 Hz, almost the same for the two VHF oscillators. After locking, the frequency flicker and the long-term stability are determined by the reference, and the two VHF oscillators are nearly equivalent. However, the 640 MHz SAW oscillator has lower white noise floor. With appropriate design, the PLL filter can mitigate or reject the noise of the divider in the feedback path, and of the detector, at offset frequencies beyond f_c. This helps in the choice of the divider and phase detector.

The scheme D uses a 128 MHz oscillator phase locked to the 10 MHz reference. The problem is that the highest frequency at the phase detector input (the greatest common divider of 10 and 128) is 2 MHz. After scaling to that low carrier frequency, the PM noise of the 128 MHz oscillator is too low for a frequency divider to preserve it. In conclusion, the output noise will be limited by the divider and by the phase detector.

In the scheme E, the 640 MHz SAW is phase locked at 80 MHz. Phase detector and frequency divider must have a PM noise not greater than -130 dB rad^2/Hz at 130 Hz offset, which is not challenging. Comparing the schemes E and F, E is simpler because it uses a digital divider $\div 8$ and a multiplier $\times 8$, instead of a multiplier $\times 64$. Otherwise, the scheme F relaxes the specs for the phase detector. ■

2-3-6 Noise Contribution from Power Supplies

We have mentioned the effect of line frequency pickup several times so far, the most direct being ripple on the dc supply voltage.

Power supplies can generally be built in one of two ways:

- Using a monolithic regulator
- Using discrete components.

The safe approach is generally to use two cascaded regulator systems, starting with a monolithic regulator, followed by a discrete post-regulation stage.

In traditional synthesizers, it is typical to find the following voltage requirements: +5 V, ±12 V, +9 V, and +24 V. When using a power supply fed from a 117 or 230 V power line, generating these auxiliary voltages is fairly easy. As the 5 V probably has the highest current draw, this will be kept totally separate from the other voltages. The current consumption on the ±12 V is on the order of several hundred mA, and the 9 V is probably an auxiliary voltage that can be generated in a post-regulator from the +12 V.

Modern VLSI digital circuits usually require lower voltages, typically 1.8 and 3.3 V, with rather high current. These voltages can be produced locally by a switching power supply, from a 12 or 24 V line. To prevent spurs, the switching power supply must be carefully shielded, and powered by a separate 12–24 V line, not shared with analog electronics.

The +24 V requirement is generally of low power consumption and is required for the PFD stages and the tuning diodes. If a dc amplifier translation stage is used following the phase/frequency comparators to drive the tuning diode, such a high voltage is necessary.

The dynamic regulation found in a monolithic regulator is typically 60 or sometimes 70 dB, which reduces the input ripple voltage to about 1 mV. This is insufficient for sensitive lines and a post-regulator of at least the same amount must be added. Here, a discrete circuit is the proper choice.

There are numerous regulators on the market, but the one with the lowest noise is probably the old National LM723. The typical output noise of this regulator is in the vicinity of a few microvolts. Figure 2-51 shows a regulator for extremely low noise output. It is based on the fact that the current generating PNP transistor produces much less noise than its emitter-follower equivalent.

In battery-operated synthesizers, especially if they operate from 12 V dc, it is somewhat difficult to generate the higher voltage for the tuning diodes. One of the best approaches is to use a switching dc/dc converter stage that is

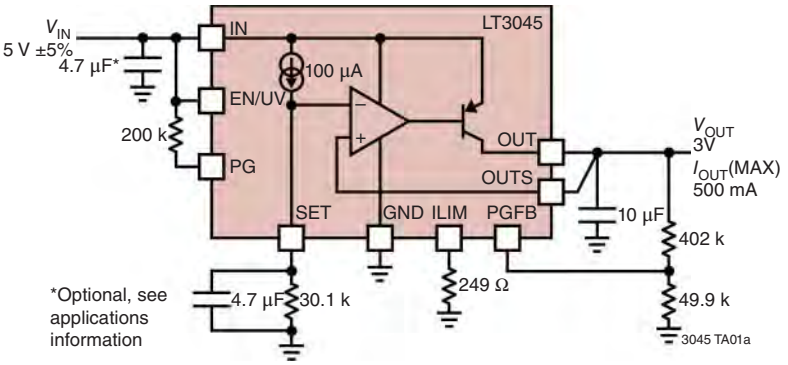


Figure 2-51 Schematic diagram of an extremely low noise output regulator based the Linear Technology LT3045 voltage regulator. Low noise is achieved by using a PNP transistor as the series regulator, with the output taken from on the collector. This solution produces much less noise than its emitter-follower equivalent. Also, this type of circuit has a much smaller voltage drop than the source follower. It operates quite well with voltage differences as low as 0.7 V. Reproduced with permission from the LT3045 data sheet.

being driven from the reference oscillator at a rate of 10 kHz to 1 MHz. As the power consumption on the tuning line is very small, no special power transistors are required, and regulators take care of interference suppression. As these stages are being driven from a square wave generated from a regulated power supply, extremely high values of regulation can be obtained, and the tuning voltage is therefore very clean and noise-free. Attempts to generate the auxiliary voltage from asynchronous dc/dc converters have generally resulted in poor performance, and this approach is not recommended.

Switching circuits are an appealing choice because of high efficiency and potentially low ripple. The reason is the use of LC filters, made simple by the high operating frequency (generally a few hundreds of kHz). Isolation is another unique feature of switching circuits, thanks to ferrite transformers. This makes easy to break ground loops and to block the interferences conducted along power lines. The general performances of commercial modules, in terms of ripple and stability, can be improved by adding an external LC low-pass filter and a linear post regulator. Shielding is the major difficulty for lowest ripple and noise, and also to prevent interferences to other circuits. Low-noise power modules are now available, consisting of a flyback switching circuit followed by a linear regulator. The LTM8068 is an interesting example. It features 2.8–40 V input range, 1.2–18 V output range after the linear regulator, with 300 mA available current and 20 µV rms noise and 2-kV isolation in a 1-cm^2 ball grid array (BGA) package.

2-4 PHASE NOISE IN OSCILLATORS

In electrical engineering, the oscillator is a circuit that delivers a periodic signal, sinusoidal, or square wave, with suitable purity and stability, powered by a source of energy. Different jargon terms may be encountered, like "self-oscillator" or "autonomous oscillator." By contrast, physicists often use the term "oscillator" for the "damped oscillator," which is the resonator in our terminology.

The simplest form of oscillator consists of a resonator and a sustaining amplifier in closed loop, so that the resonator sets the oscillation frequency f_0, and the sustaining amplifier compensates for the loss of the resonator. A buffer is generally necessary, to amplify the output power and to isolate the oscillator from load perturbations. Denoting the amplifier gain with A, and the resonator transfer function with B, stationary oscillation requires that

$$AB = 1 \tag{2-121}$$

that is, $|AB| = 1$ and $\arg(AB) = 0$. This is known as the Barkhausen condition. A gain compression mechanism is necessary, which stabilizes the oscillation amplitude to a given level. Otherwise, even the smallest discrepancy

from unity gain results in exponentially increasing oscillation ($AB > 1$) or in exponentially decaying oscillation ($AB < 1$).

The oscillator's internal components introduce noise and fluctuations. Other types of fluctuation originate from power supply, temperature, and other quantities. Understanding and modeling the oscillator is a complex issue because of the multi-scale time range, from the period to the long time related to aging.

We focus on the Leeson model analyzed from the modern standpoint. The original article [71] proposed a quasi-linear analysis, inherently limited to additive white noise. Adding very little complexity, we introduce the perturbation and modulation analysis, which is perfectly suitable to parametric noise [72]. An extension to AM noise is available in [73]. Our approach is probably the simplest and the most suitable to understand real oscillators because we analyze the oscillator as a system, as opposed to a detailed schematic. Of course, simplicity and generality come at expenses of accuracy. A few alternate models are available in the literature. These models are either specialized (e.g., the ring oscillator), or extremely complex (e.g., the Fokker–Planck equation). We provide a list in the Suggested Readings, at the end of this chapter. For a perspective on different approaches and oscillator models, we suggest starting from [74, 75].

2-4-1 Modern View of the Leeson Model

The oscillator is seen as a system consisting of an amplifier and a resonator in closed loop, shown on Figure 2-52A. The amplifier is operated at the compression point, where it stabilizes the amplitude. The phase noise is modeled as a phase modulator at the amplifier input, driven by a generator which introduces white noise, flicker noise, spurs, etc. The resonator is a bandpass filter exhibiting a sharp response which sets the oscillation frequency. The loop has an input for the virtual signal that starts the oscillation. Actual oscillation starts from noise or from the switch-on transient.

It is convenient to write the equations in terms of angular frequency ω, and to use the regular frequency f to represent the results. So, ω and f are used interchangeably implying that $\omega = 2\pi f$, and a quantity is uniquely identified by a subscript. For example, the natural frequency of an LC oscillator can be written as $\omega_n = 1/\sqrt{LC}$ or as $f_n = 1/2\pi\sqrt{LC}$, interchangeably. Without subscript, ω and f refer to the running variable in spectral analysis, denoted with f_m in other parts of this book.

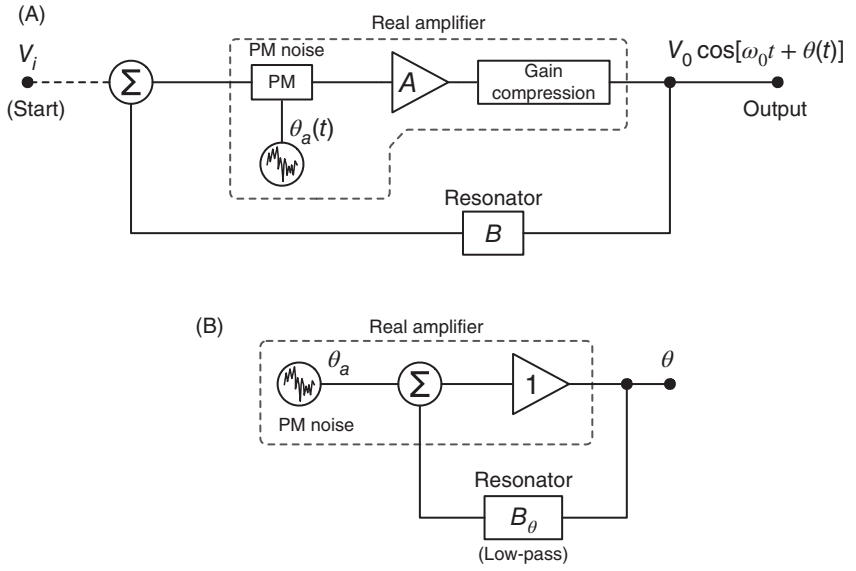


Figure 2-52 General scheme of the oscillator loop (A) and its companion circuit (B) for phase noise. Reprinted/adapted from [1], CC BY Rubiola.

For the sake of simplicity, we assume that the gain A is constant versus frequency, at least in the region around the oscillation frequency. If the gain flatness defect is not negligible, we move it from A to B, so that A is constant. Second, we assume that the resonator transfer function B is linear. Some resonators are nonlinear, and the resonant frequency depends on the amplitude. In quartz resonators, this is called "isochronism defect." Frequency may depend on amplitude, and bi-stability is observed at high amplitudes [76, 77]. However, for the small amplitude fluctuations found in real oscillators, B is sufficiently linear at the operating point.

Modeling parametric noise and spurs requires that a phase modulator is introduced in the loop, as shown in Figure 2-52A because these types of noise cannot be represented as additive processes. The presence of such phase modulator breaks the simplicity of the original Leeson model. We solve this difficulty by using the companion circuit for phase noise shown on Figure 2-52B. The companion circuit relies on the following ideas and simplifications:

- The startup transient is ended, and the oscillator is in its stationary condition.
- The gain compression, needed to stabilize the amplitude, has no effect on the phase.
- The *phase amplifier* has a gain equal to one, exact. This is consistent with the fact that time cannot be stretched or compressed, thus the noise-free amplifier delivers an exact copy of the input phase with no error.
- The amplifier's random phase is an additive process in this representation.
- The transfer function B_θ of the resonator is linear, and independent of the small fluctuations of amplitude.

The most important virtue of this companion scheme is that it is *inherently linear* because all the elements in the loop are linear.

Our approach differs from the original Leeson model in that we use a modulation method or a perturbation method, interchangeably and equivalently. More precisely, we introduce a phase perturbation θ_a in the companion loop. The quantity θ_a is the phase fluctuation of either the amplifier or the resonator. Thus, the phase noise transfer function is

$$H_\theta(s) = \frac{\Theta(s)}{\Theta_a(s)} \tag{2-122}$$

The uppercase stands for the Laplace transform (notice the difference between Θ and θ), and the quantity $s = \sigma + j\omega$ is the complex frequency. Replacing $s \to 2\pi f$ and taking the square absolute value, we get

$$S_\theta(f) = |H_\theta(f)|^2 \, S_{\theta a}(f) \tag{2-123}$$

This approach is surprisingly similar to the analysis of the response of a PLL, already familiar to the reader.

The Resonator and Its Impulse Response

Close to the resonance, the resonator can be approximated with a second-order linear differential equation

$$\ddot{v}_o + \frac{\omega_n}{Q}\dot{v}_o + \omega_n^2 v_o = \frac{\omega_n}{Q}\dot{v}_i \tag{2-124}$$

where ω_n is the natural angular frequency, Q is the quality factor in actual load conditions, and the term $\left(\omega_n/Q\right)\dot{v}_i$ is the driving force. We have chosen this type of driving force because it is homogeneous with the dissipative term $\left(\omega_n/Q\right)\dot{v}_o$, as it occurs in relevant cases like the series (parallel) RLC resonator driven by a voltage (current) source. Using the Laplace transforms, we find the resonator response $B(s) = V_o(s)/V_i(s)$

$$B(s) = \frac{\omega_n}{Q}\,\frac{s}{s^2 + \left(\omega_n/Q\right)s + \omega_n^2} \tag{2-125}$$

The square modulus $|B(f)|^2$, for $Q \gg 1$, describes a Lorentzian line shape of width f_n/Q centered at f_n.

The homogeneous equation, which is (2-124) with the force $\dot{v}_i$ set to zero, describes the free decaying oscillation

$$v(t) = \cos\left(\omega_p t + \phi\right)\ e^{-t/\tau} \tag{2-126}$$

where ϕ is an arbitrary phase which results from the initial conditions,

$$\omega_p = \omega_n \sqrt{1 - \frac{1}{4Q^2}} \tag{2-127}$$

is the free decay angular pseudo frequency,[3] and

$$\tau = \frac{2Q}{\omega_n} \tag{2-128}$$

is the relaxation time.

In virtually all cases of interest for us, the resonator has large Q, and the oscillator oscillates close to the exact peak of resonance. Therefore, the following approximation holds

$$\omega_0 = \omega_n = \omega_p \tag{2-129}$$

Our phase-noise equivalent circuit relies on the knowledge of the resonator's response to the Dirac $\delta(t)$ impulse of phase, when the resonator is driven by a sinusoidal signal. This concept is illustrated in Figure 2-53. When the resonator is driven with the input signal $\cos[\omega_0 t + \delta(t)]$, it responds with $\cos[\omega_0 t + b_\theta(t)]$. The function $b_\theta(t)$ is the impulse response we need.

For most people, it is hard to figure out the meaning of a Dirac $\delta(t)$ in the argument of a sinusoid. However, the difficulty can be solved using a simple property of linear systems. The impulse response $b_\theta(t)$ is related to the response $k_\theta(t)$ to the Heaviside (step) function $u(t)$ by

$$k_\theta(t) = \int b_\theta(t)\ dt \tag{2-130}$$

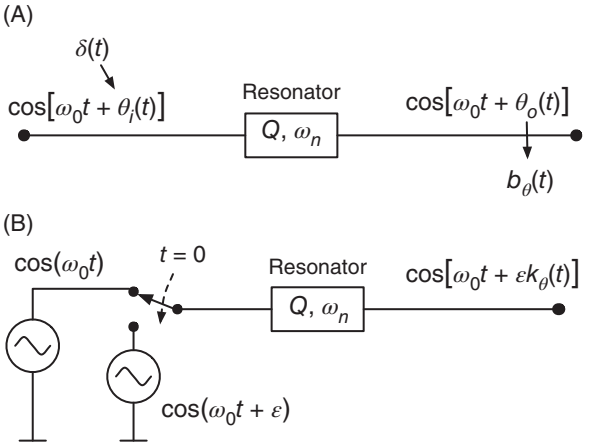


Figure 2-53 The concept of phase-impulse response of a resonator (A) and its derivation (B) from the response to a small Heaviside (step) of phase. Simulation is also straightforward. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

[3]The quantity ω_p is not a valid angular frequency because $v(t)$ is not periodic in a strict sense, being progressively attenuated by the term $e^{-t/\tau}$.

because

$$u(t) = \int \delta(t)\ dt \tag{2-131}$$

Let us apply to the resonator a small phase step $\varepsilon u(t)$, $\varepsilon \ll 1$, at the time $t = 0$ (Figure 2-53). The small value makes the derivation of $k_\theta(t)$ simpler, but the result is general. The complete input signal is

$$v_i(t) = \cos\left(\omega_0 t\right)\ u(-t) + \cos\left(\omega_0 t + \varepsilon\right)\ u(t) \tag{2-132}$$

where $u(t)$ is the Heaviside function

$$u(t) = \begin{cases} 0 & t < 0 \\ 1 & t > 0 \end{cases} \tag{2-133}$$

Thus, at $t = 0$ the signal $\cos(\omega_0 t)$ is switched off by $u(-t)$, and the signal $\cos(\omega_0 t + \varepsilon)$ is switched on by $u(t)$. The resonator response results from

$$v_o(t) = v_{\text{off}}(t) + v_{\text{on}}(t)$$

where

$$v_{\text{off}}(t) = \cos\left(\omega_0 t\right) e^{-t/\tau} \tag{2-134}$$

is the exponentially decaying response to $\cos(\omega_0 t)$, switched off at $t = 0$; and $v_{\text{on}}(t)$ is the growing response to the phase-shifted signal $\cos(\omega_0 t + \varepsilon)u(t)$, switched on at $t = 0$. Calculating the term $v_{\text{on}}(t)$ requires some manipulations

$$\begin{aligned} v_{\text{on}}(t) &= \cos\left(\omega_0 t + \varepsilon\right)\left[1 - e^{-t/\tau}\right] && t > 0 \\ &= \left[\cos\left(\omega_0 t\right)\cos(\varepsilon) - \sin\left(\omega_0 t\right)\sin(\varepsilon)\right]\left[1 - e^{-t/\tau}\right] \\ &\simeq \left[\cos\left(\omega_0 t\right) - \varepsilon \sin\left(\omega_0 t\right)\right]\left[1 - e^{-t/\tau}\right] && \varepsilon \ll 1 \end{aligned}$$

Combining $v_{\text{off}}(t)$ and $v_{\text{on}}(t)$, we get

$$v_o(t) = \cos\left(\omega_0 t\right) - \varepsilon \sin\left(\omega_0 t\right)\left[1 - e^{-t/\tau}\right] \qquad \varepsilon \ll 1 \tag{2-135}$$

This is a sinusoid of phase $\theta_o(t) = \varepsilon[1 - e^{-t/\tau}]$. The step response is obtained by deleting ε

$$k_\theta(t) = \left[1 - e^{-t/\tau}\right] \tag{2-136}$$

Finally, the impulse response is obtained by differentiating the Heaviside response

$$b_\theta(t) = \frac{1}{\tau} e^{-t/\tau} \tag{2-137}$$

The result is plotted in Figure 2-54. The Laplace transform of $b_\theta(t)$ is

$$B_\theta(s) = \frac{1/\tau}{s + 1/\tau} \tag{2-138}$$

This is a single-pole low-pass filter, like the *RC* low-pass filter. The cutoff frequency $f_L = 1/2\pi\tau = f_0/2Q$ is called Leeson frequency and is equal to the half the resonator bandwidth.

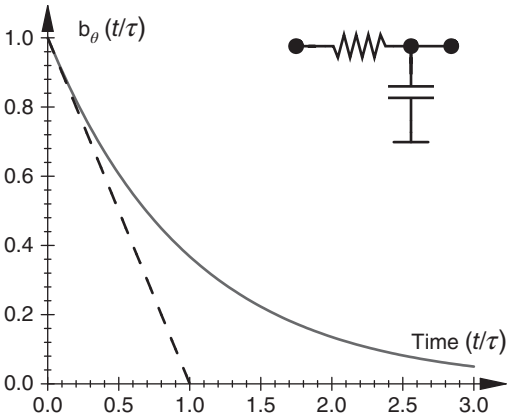


Figure 2-54 Impulse-of-phase response of a resonator at the exact resonant frequency. The response is equivalent to that of a first-order low-pass filter, like the *RC* network shown. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

The Oscillator's Phase-Noise Transfer Function

We have all the pieces we need to calculate the phase-noise transfer function $H_\theta(s)$ of the complete oscillator

$$H_\theta(s) = \frac{\Theta(s)}{\Theta_a(s)} \tag{2-139}$$

The oscillator is described in Figure 2-52B as a classical feedback system, where

$$H_\theta(s) = \frac{1}{1 + B(s)} \tag{2-140}$$

Using (2-138) in earlier, we get immediately

$$H_\theta(s) = \frac{s + 1/\tau}{s} \tag{2-141}$$

Using $f_L = 1/2\pi\tau$, we get

$$\left|H_\theta(f)\right|^2 = \frac{f^2 + f_L^2}{f^2} = 1 + \frac{f_L^2}{f^2} \tag{2-142}$$

and finally

$$\left|H_\theta(f)\right|^2 = 1 + \frac{f_0^2}{4Q^2}\,\frac{1}{f^2} \tag{2-143}$$

This is the simple function plotted in Figure 2-55. The physical meaning, related to the phase-noise scheme of Figure 2-52B, is surprisingly simple. At low offset frequency, $f \ll f_L$, the phase fluctuations are fed back to the input of the phase amplifier, and integrated. Because time cannot be compressed or stretched, the phase amplifier has a gain exactly equal to one. Thus, the loop is a perfect loss-free integrator, and $H_\theta(s)$ has a pole in the origin. By contrast, at high offset frequencies, $f \gg f_L$, the resonator filters out the phase noise, preventing the fluctuations to be fed back to the input. Thus, the random phase θ at the output is equal to the random phase θ_a introduced in the loop, and asymptotically $|H_\theta(f)|^2 = 1$.

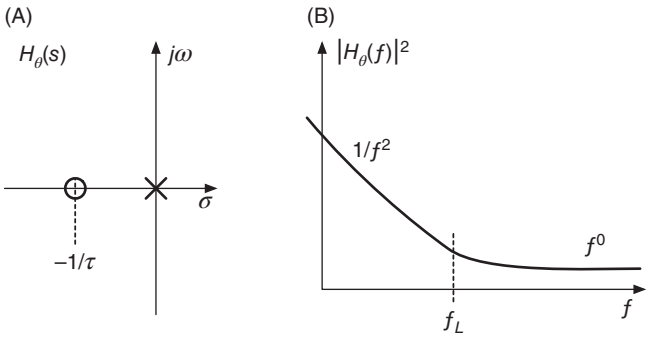


Figure 2-55 Phase-noise transfer function of the complete oscillator: (A) complex plane, and (B) frequency response. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

The Phase Noise of the Complete Oscillator

We have seen in Section 2-2-3 that the amplifier phase noise is described by the polynomial law restricted to two terms, white and flicker

$$S_\theta(f) = \mathsf{b}_0 + \frac{\mathsf{b}_{-1}}{f} \qquad \text{amplifier} \tag{2-144}$$

In turn, b_0 is usually expressed as $\mathsf{b}_0 = FkT_0/P_0$, where F is the noise factor of the sustaining amplifier, kT_0 is the thermal energy, and P_o is the power at the amplifier input; and b_{-1} is a parameter of the amplifier. Combining the amplifier noise with $|H(f)|^2$, we get

$$S_\theta(f) = \left[\frac{FkT_0}{P_0} + \frac{\mathsf{b}_{-1}}{f}\right]\left[1 + \frac{f_0^2}{4Q^2}\frac{1}{f^2}\right] \tag{2-145}$$

Additional noise contributions are still to be included, namely, the frequency fluctuations of the resonator's natural frequency, the FM noise brought in by the tuning diode, and the phase noise of the output buffer. These noise perturbations are shown in Figure 2-56.

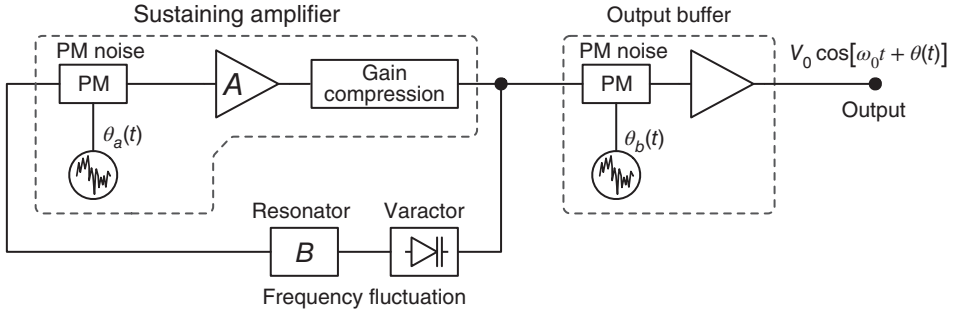


Figure 2-56 The complete oscillator, including the frequency fluctuations of the resonator, and the phase noise of the output buffer. The tuning diode can be in series, in parallel, or take other configurations, depending on the type of oscillator and resonator. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

The resonator introduces flicker-of-frequency noise, originating a term

$$S_\theta(f) = \frac{\mathsf{b}_{-3}}{f^3} \qquad \text{resonator} \tag{2-146}$$

in the phase noise plot. The coefficient b_{-3} can be derived from the floor of the resonator's AVAR $\sigma_y^2(\tau)$, or from the floor of the MVAR $\mathrm{mod}\,\sigma_y^2(\tau)$, if known,

$$\mathsf{b}_{-3} = \frac{f_0^2}{2\ln(2)}\sigma_y^2(\tau) \qquad \text{AVAR floor} \tag{2-147}$$

$$\mathsf{b}_{-3} = f_0^2 \frac{8}{27\ln(3) - 32\ln(2)}\ \mathrm{mod}\,\sigma_y^2(\tau) \qquad \text{MVAR floor} \tag{2-148}$$

The MVAR is preferred to the AVAR because its superior capability to identify the fast noise processes, white and flicker PM, as we have seen in section "Comparison Between AVAR, MVAR, and PVAR". However, the (regular) AVAR is most often found in the technical documentation of oscillators. In practical cases, the b_{-3}/f^3 term due to the resonator fluctuations can be higher than the similar term from the sustaining amplifier (2-145). This is the case, for example, of the high-stability 10 MHz OCXOs used as the frequency reference in electronic instruments.

Higher-order fluctuations of the resonator, like the frequency random walk b_{-4}/f^4, and the drift are more difficult to model in the phase noise spectrum, mainly because of the lack of data. Moreover, these perturbations depend on the environment, on the temperature control, etc.

If the oscillator is electrically tunable, it turns the voltage noise at the VCO input into FM noise. In the case of white noise across the tuning diode, the oscillator phase noise is

$$S_\theta(f) = \frac{\mathsf{b}_{-2}}{f^2} \tag{2-149}$$

with

$$\mathsf{b}_{-2} = e_n^2 K_o^2 \tag{2-150}$$

where e_n is the RMS voltage noise in 1 Hz bandwidth, and K_o is the VCO gain in (rad/s)/V. When the VCO input is connected to a resistor R, the noise cannot be lower than the thermal noise $\sqrt{4kT_0R}$. In this condition, the oscillator PM noise is

$$S_\theta(f) = \frac{4kT_0RK_o^2}{f^2} \tag{2-151}$$

as explained in [78].

The contribution of the output buffer is an additional term like (2-144), yet with different noise factor, power, and flicker parameter b_{-1}. In most practical cases, the white phase noise of the buffer is lower than that of the sustaining amplifier because the carrier power is higher. By contrast, the phase flicker of the buffer is generally higher than that of the sustaining amplifier. This happens for two reasons. First, the sustaining amplifier is in the loop, where the $1/f$ noise is turned into $1/f^3$ noise below f_L, thus a wise engineer spends a larger budget in a low-noise sustaining amplifier. Second, for proper isolation, the buffer consists of 2–3 cascaded stages, each of which contributes its own flicker.

In synthesis, the oscillator phase noise is given by

$$S_\theta(f) = \left[\frac{FkT_0}{P_0} + \frac{\mathsf{b}_{-1}}{f}\right]\left[1 + \frac{f_0^2}{4Q^2}\frac{1}{f^2}\right] \qquad \text{sustaining amplifier}$$

$$+ \frac{f_0^2}{2\ln(2)}\sigma_y^2(\tau)\frac{1}{f^3} \qquad \text{resonator flicker}$$

$$+\frac{4kT_0RK_o^2}{f^2} \qquad \text{tuning diode white}$$

$$+\frac{FkT_0}{P_{\text{buf}}}+\frac{\mathsf{b}_{-1}}{f} \qquad \text{output buffer}$$

$$+\ \text{FM, RW and higher-order terms, and spurs}$$

It is understood that symbols take their meaning from the context indicated on the right hand of the equation. For example, F in the first line refers to the sustaining amplifier, while the same symbol F in the fourth line refers to the output buffer.

Example 14 10.24 GHz DRO. We consider a 10.24 GHz dielectric resonator oscillator (DRO) where the resonator has a loaded quality factor $Q = 1000$. The sustaining amplifier has a noise factor of 4 dB, and a flicker noise of −106 dBc/Hz extrapolated to 1 Hz. The power at the input of the sustaining amplifier is of −20 dBm. Let us calculate the phase noise spectrum, accounting only for the oscillator loop.

From the statement of the problem, we calculate the Leeson frequency

$$f_L=\frac{f_0}{2Q}=\frac{1.024\times10^{10}}{2\times1000}=5.12\,\text{MHz}$$

and the amplifier noise parameters

$$\mathsf{b}_0=\frac{FkT_0}{P_0}=\frac{10^{4/10}\ \times\ 1.38\times10^{-23}\ \times290}{10^{-20/10}\times10^{-3}}=10^{-15}$$

$$\mathsf{b}_{-1}=2\times10^{-106/10}=5\times10^{-11}$$

Using (2-145), we calculate the oscillator phase noise PSD shown on Figure 2-57. The phase-noise coefficients are

$$\mathsf{b}_0=10^{-15}\quad(-153\,\text{dBc/Hz})$$

$$\mathsf{b}_{-1}=5\times10^{-11}\quad(-106\,\text{dBc/Hz at 1 Hz})$$

$$\mathsf{b}_{-2}=\frac{f_0^2}{4Q^2}\mathsf{b}_0=\frac{\left(1.024\times10^{10}\right)^2}{4\times1000^2}\times10^{-15}=2.62\times10^{-2}\quad(-18.8\,\text{dBc/Hz at 1 Hz})$$

$$\mathsf{b}_{-3}=\frac{f_0^2}{4Q^2}\mathsf{b}_{-1}=\frac{\left(1.024\times10^{10}\right)^2}{4\times1000^2}\times5\times10^{-11}=1.25\times10^{3}\quad(+31.2\,\text{dBc/Hz at 1 Hz})$$

■

Example 15 10 MHz OCXO. We consider a 10 MHz OCXO where the resonator has a loaded quality factor $Q = 10^6$. The sustaining amplifier has a noise factor of 1 dB, and a flicker noise of −140 dBc/Hz extrapolated to 1 Hz. The power at the input of the sustaining amplifier is −16 dBm. The buffer has a noise factor of 1 dB, and a flicker noise of −135.2 dBc/Hz extrapolated to 1 Hz. The power at the input of the buffer is of −7 dBm. The resonator has a stability of 3.2×10^{-13} (flicker term in the Allan deviation). Let us calculate the phase noise spectrum.

We calculate the oscillator loop, the buffer, and the fluctuation of the resonator separately, and we add the results. The single contributions and the full spectrum are shown in Figure 2-58.

From the statement of the problem, we calculate the Leeson frequency

$$f_L=\frac{f_0}{2Q}=\frac{10^7}{2\times10^6}=5\,\text{Hz}$$

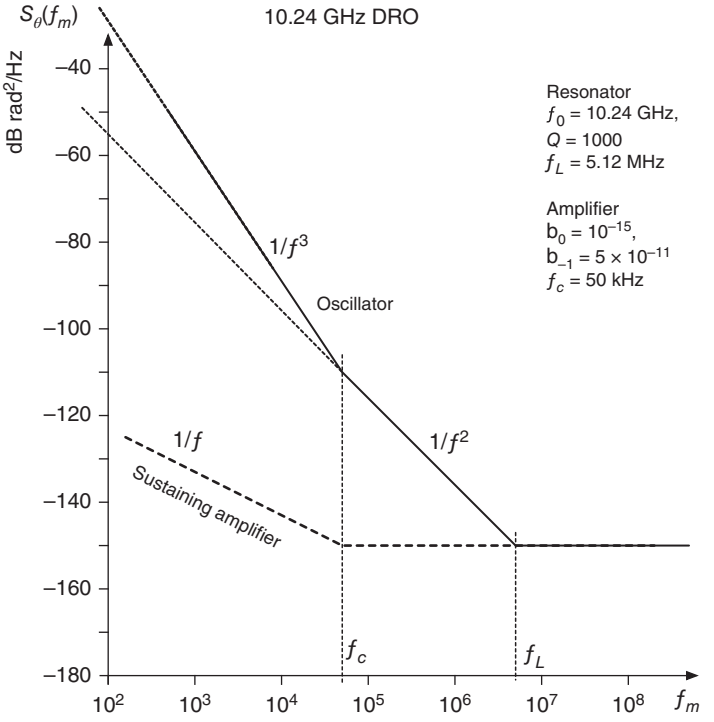


Figure 2-57 Phase noise PSD of the 10.24 GHz DRO discussed in the example.

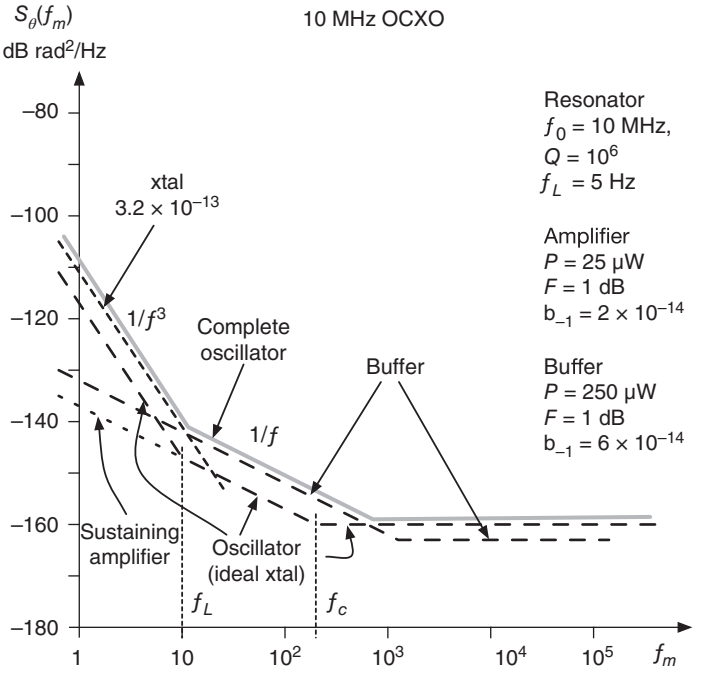


Figure 2-58 Phase noise PSD of the 10 MHz OCXO discussed in the example.

and the noise parameters of the sustaining amplifier

$$\mathsf{b}_0 = \frac{FkT_0}{P_0} = \frac{10^{1/10} \times 1.38 \times 10^{-23} \times 290}{10^{-16/10} \times 10^{-3}} = 2 \times 10^{-16}$$
$$\mathsf{b}_{-1} = 2 \times 10^{-140/10} = 2 \times 10^{-14}$$

Using (2-145), we calculate the phase noise coefficients of the oscillator loop

$$\mathsf{b}_0 = 2 \times 10^{-16}$$
$$\mathsf{b}_{-1} = 2 \times 10^{-14}$$
$$\mathsf{b}_{-2} = \frac{f_0^2}{4Q^2}\mathsf{b}_0 = \left[\frac{10^7}{2 \times 10^6}\right]^2 \times 2 \times 10^{-16} = 5 \times 10^{-15}$$
$$\mathsf{b}_{-3} = \frac{f_0^2}{4Q^2}\mathsf{b}_{-1} = \left[\frac{10^7}{2 \times 10^6}\right]^2 \times 2 \times 10^{-14} = 5 \times 10^{-13}$$

The contribution of the output buffer is

$$\mathsf{b}_0 = \frac{FkT_0}{P_0} = \frac{10^{1/10} \times 1.38 \times 10^{-23} \times 290}{10^{-7/10} \times 10^{-3}} = 2.5 \times 10^{-17}$$
$$\mathsf{b}_{-1} = 2 \times 10^{-135.2/10} = 6 \times 10^{-14}$$

The phase noise due to the fluctuation of the resonator's natural frequency is

$$\mathsf{b}_{-3} = \frac{f_0^2}{2\ln(2)}\sigma_y^2(\tau) = \frac{\left(10^7\right)^2}{1.386} \times \left(3.2 \times 10^{-13}\right)^2 = 7.4 \times 10^{-12}$$

Adding all these terms, the phase noise PSD of the complete oscillator is

$$S_\theta(f) = 2.3 \times 10^{-16} + \frac{8 \times 10^{-14}}{f} + \frac{5 \times 10^{-15}}{f^2} + \frac{7.9 \times 10^{-12}}{f^3}$$

■

Some Lessons from the Examples

We discuss the phase noise spectra of the two aforementioned examples with respect to the scheme of Figure 2-56, extending some consideration to other types of oscillator.

First, we notice that in Figures 2-57 and 2-58 there is either $1/f$ or $1/f^2$ noise, not both. This relates to the fact that we have two distinct corners, where the exponent of f changes by 1 crossing f_c, and by 2 crossing f_L.

If $f_c < f_L$, we get the $1/f^2$ slope term in the region between f_c and f_L, as in the DRO. This type of behavior is typical of microwave oscillators, where f_0 is of tens of GHz and Q generally not higher than a few thousands, thus we expect f_L of the order of a few MHz. With microwave oscillators, we often find f_c between 10 and 100 kHz. A similar behavior is found in the internal VCOs of integrated circuits like FPGAs and DDSs. Such oscillators have an integrated LC tank having $Q \approx 10$ at f_0 of a few hundred of MHz, thus f_L of a few tens of MHz.

Oppositely, if $f_c > f_L$, we get the $1/f$ term in the region between f_L and f_c, as in the OCXO. This is typical of high-stability HF quartz oscillators, where technology suggests that $Qf_0 \approx 10^{13}$. Accordingly, we encounter typical $Q \approx 10^6$ at 10 MHz, thus $f_L \approx 5$ Hz. The flicker noise of HF amplifiers is rather low, in some cases even lower than −140 dBc/Hz extrapolated at 1 Hz. With a typical power of 10 … 100 μW, f_c is of a few hundreds of Hz.

The noise pattern of VHF quartz oscillators is different. For example, using the thumb rule $Qf_0 \approx 10^{13}$, we expect $Q \approx 10^5$ at 100 MHz, thus $f_L \approx 500$ Hz. Since these resonators can work at higher power than the HF resonators, f_c is proportionally lower. So, f_L and f_c may more or less overlap, or even give $f_L > f_c$.

With a good design, the white noise of the buffer should not degrade the oscillator noise. We expect this because the Friis formula applies to white noise, and the power level is generally higher at the input of the buffer than at the input of the sustaining amplifier.

By contrast, cascading several amplifiers, the b_{-1} coefficients add up in a way that is independent, or almost independent of the carrier power. When $f_L < f_c$, the oscillator loop has a $1/f$ region clearly visible, due to the sustaining amplifier (Figure 2-58). We expect that the $1/f$ noise at the oscillator output results from the contribution of the sustaining amplifier and of the buffer, and that the latter is generally dominant. A first reason is that the loop turns the $1/f$ noise of the sustaining amplifier into $1/f^3$ noise, while the $1/f$ noise of the buffer remains of the $1/f$ type at the output. In this respect, it is wise to put larger budget and design care in the sustaining amplifier. The second reason is that the output buffer has larger number of stages, because it has to isolate the loop from the output. Observing a $1/f$ region in an oscillator, in the absence of specific information, we may guess that 1/4 comes from the sustaining amplifier, and 3/4 from the buffer.

A further consequence of the buffer $1/f$ noise is that the corner between $1/f$ and $1/f^3$ noise is no longer at f_L. Interpreting the spectra gets more challenging.

The $1/f^3$ region results from the two contributions, the phase feedback in the oscillator (2-145) and the fluctuation of the resonator's natural frequency (2-147). These contributions are equal when

$$\left[\mathsf{b}_{-1}\right]_{\text{sustaining amplifier}} = \frac{4Q^2}{2\ln(2)} \left[\sigma_y^2\right]_{\text{resonator FM flicker}} \tag{2-152}$$

or

$$\left[\mathsf{b}_{-1}\right]_{\text{sustaining amplifier}} = 4Q^2 \frac{8}{27\ln(3) - 32\ln(2)} \left[\text{mod}\,\sigma_y^2\right]_{\text{resonator FM flicker}} \tag{2-153}$$

The phase feedback is usually dominant in microwaves and in *LC* oscillators, which have moderate Q. Oppositely, the fluctuation of the resonator's natural frequency in the case quartz resonators (Figure 2-58) and other extremely high Q resonators.

2-4-2 Circumventing the Resonator's Thermal Noise

The noise factor F and the Friis formula describe the noise of an amplifier impedance-matched to the resistive input load at temperature T_0. The equivalent noise PSD at the amplifier input is FkT_0. This quantity is the sum of the available thermal energy kT_0 of the resistor, plus the contribution $(F-1)kT_0$ of the amplifier. If the amplifier input is left open, is shorted to ground, or is connected to a noise-free load, the equivalent input noise is $(F-1)kT_0$.

The Rohde oscillator (Figure 2-59B) provides a means to circumvent the thermal noise of the resonator and of the sustaining amplifier by using the resonator also as an output filter. The series resonator consists of an inductance L, a capacitance C, and a resistance R_s. The latter represents the mechanical loss of the quartz resonator. At the resonance, the reactance ωL and $1/\omega C$ cancel one another, and the resonator is equivalent to the resistance R_s. Out of the resonator bandwidth the reactance is dominant, either $1/\omega C \gg R_s$ or $\omega L \gg R_s$, and the thermal noise is no longer coupled to the surrounding electrical circuit. Likewise, the noise of the sustaining amplifier falls in the stopband.

The original scheme [79] derives from the Colpitts circuit, as shown in Figure 2-59. In the Colpitts oscillator, the white noise floor is determined by the transistor. In the Colpitts–Rohde oscillator, the resonator has the double role of the frequency reference and of the output filter. At the resonant frequency, the white phase noise is determined by R_s, by R, and by the noise of the transistor. Out of the resonator bandwidth, asymptotically, the resonator is open circuit, and the output noise is the thermal noise of the resistor R. Thus, the oscillator white phase noise PSD is given by

$$S_\theta(f) = kT_0/P_0 \tag{2-154}$$

where P_0 is the carrier power dissipated by the resistor R.

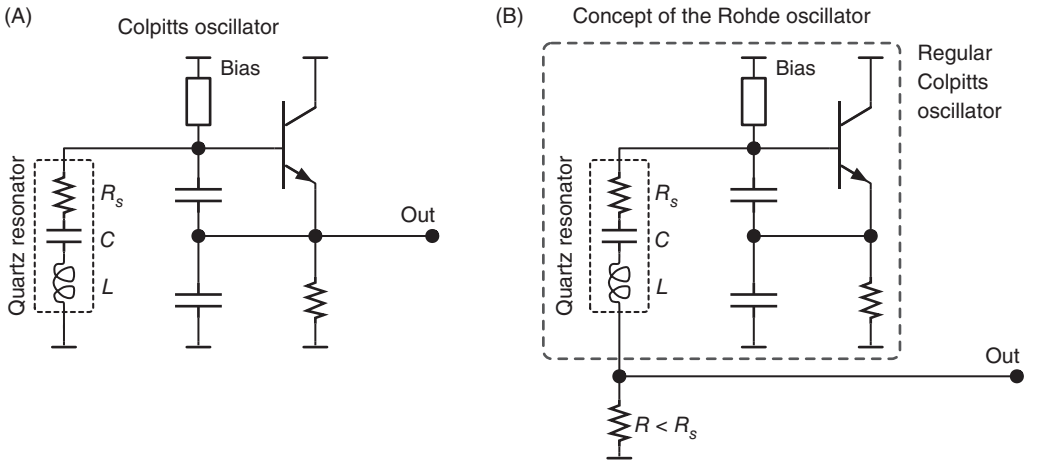


Figure 2-59 (A) The Colpitts oscillator and (B) the concept of the Rohde oscillator. The latter circumvents the thermal noise of the quartz resonator by using the resonator as the output filter.

The scheme of Figure 2-59 should be regarded as a concept, rather than a working oscillator. A problem is that R is in series to the resonator and reduces the resonator's Q. Another problem is that any perturbation to the load impacts on the frequency stability. Porting this idea to the complete circuit, we get the Rohde oscillator, shown in Figure 2-60. The entire circuit works in current mode. The sustaining amplifier is a feedback circuit implementing a negative resistance equal to $-(R_s + R_E)$. It could be the Colpitts scheme or any other configuration suitable to oscillate with the resonator connected to ground. Instead of being grounded, the quartz resonator is connected to a grounded-base amplifier, which has low input impedance R_E, thanks to local negative feedback. Neglecting the base current, the collector current I_C is equal to the current I_R flowing in the resonator. The conclusion is that the white phase noise is determined by the thermal noise of the collector resistance referred to the output carrier power

$$S_\theta(f) = kT_0/P_{\text{out}} \tag{2-155}$$

From the ideal scheme to practical implementation, we notice that the condition $R_E \ll R_s$, necessary to preserve the resonator Q, can be obtained rather easily because R_E can be of the order of 1 Ω. The buffer contributes some white and flicker phase noise.

The main feature of the Rohde scheme is that it circumvents the thermal noise associated to the quartz internal dissipation, represented as the resistance R_s. However, it cannot remove the phase-to-frequency noise conversion

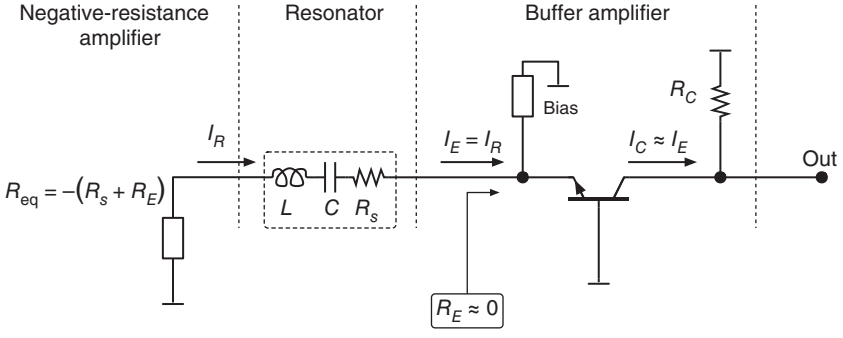


Figure 2-60 Principle of the Rohde oscillator.

mechanism inherent in the oscillator loop. Thus, the Rohde oscillator is an excellent solution for VHF quartz oscillators, typically 100 or 125 MHz, where the lowest phase noise floor is the most desirable feature, and the frequency stability is comparatively less important. When the highest frequency stability is of paramount importance, the Rohde oscillator may not be the best choice. The problem is that fluctuation of the buffer input impedance, however small, is converted into frequency noise.

2-4-3 Oscillator Hacking

Inspecting on phase noise spectra provides information on the oscillator inside. Of course, our conclusions are only approximate, and mistakes are around the corner. Nonetheless, hacking oscillators from the phase noise spectra turns out to be surprisingly useful.

We provide guidelines based on the Leeson model, mainly addressed to the readers already familiar with the technology of oscillators and resonators.

The interplay between the Leeson frequency f_L and the corner frequency f_c of the sustaining amplifier defines the two main types of PM noise, shown on Figure 2-61A and B. The type A, defined by $f_L < f_c$, is found with high Q resonators at low carrier frequency (HF). The type B, defined by $f_L > f_c$, is generally found in microwave oscillators and in low Q VHF and ultrahigh frequency (UHF) oscillators. As we have seen, the spectrum contains either $1/f$ or $1/f^2$ phase noise types, not both. The Rohde oscillator (Section 2-4-2) presents additional difficulty in the interpretation, and for this reason it is not included in this analysis. The resonator is considered ideally stable in Figure 2-61A and B, while Figure 2-61C and D shows the same spectra with the resonator's $1/f$ frequency fluctuation added, which is of the $1/f^3$ type in the phase noise plot.

The analysis starts from the identification of the coefficients b_i of the polynomial law. This is best done *by hand* sliding old-fashion *set squares* on the usual log–log plot of $L(f)$, or on a comfortably large computer display by shifting a line. Don't forget the factor of two to convert $L(f)$ into $S_\theta(f)$. One of us (ER) is often seen at conferences doing this exercise on the data sheets found at the exhibitor boots, sliding two credit cards on the $L(f)$ plots. With little training, the human eye does a good approximation close to the least square fit, which is exactly what we need. Rather than searching for the exact slope for the specific oscillator, we fit the spectrum with the canonical slopes f^0, $1/f$, $1/f^2$, etc. Frequency random walk, of the $1/f^4$ type and not shown in Figure 2-61, is almost always found at low f.

We proceed from the right-hand side of the spectrum to the left, thus from high f to low f.

Moderate/Low-Q (Type A/C) Oscillators

The spectrum of the type A/C is identified by the presence of $1/f^2$ PM noise, and the absence of $1/f$.

First, the white phase noise tells us about the power P_0 at the input of the sustaining amplifier because the white noise of the buffer is negligible. This approximation makes sense because the power at the buffer input is generally higher than at the input of the sustaining amplifier. For the sake of simplification, we discard the effect of impedance mismatching out of the resonator bandwidth, which would give a white RF noise between $(F-1)kT_0$ and FkT_0, and we take $F = 1$ dB as an approximation. Using the formula $\mathsf{b}_0 = FkT_0/P_0$, we calculate

$$P_0 = \frac{FkT_0}{\mathsf{b}_0} \tag{2-156}$$

The power dissipated by the resonator is probably a little higher, yet of the same order of magnitude.

Second, we evaluate the Leeson frequency f_L as the intersection between the oscillator white phase noise b_0, and the oscillator white frequency noise b_{-2}/f^2. There is no need to account for the buffer because both white and $1/f$ noise types are negligible. Thus

$$f_L^2 = \frac{\mathsf{b}_0}{\mathsf{b}_{-2}} \tag{2-157}$$

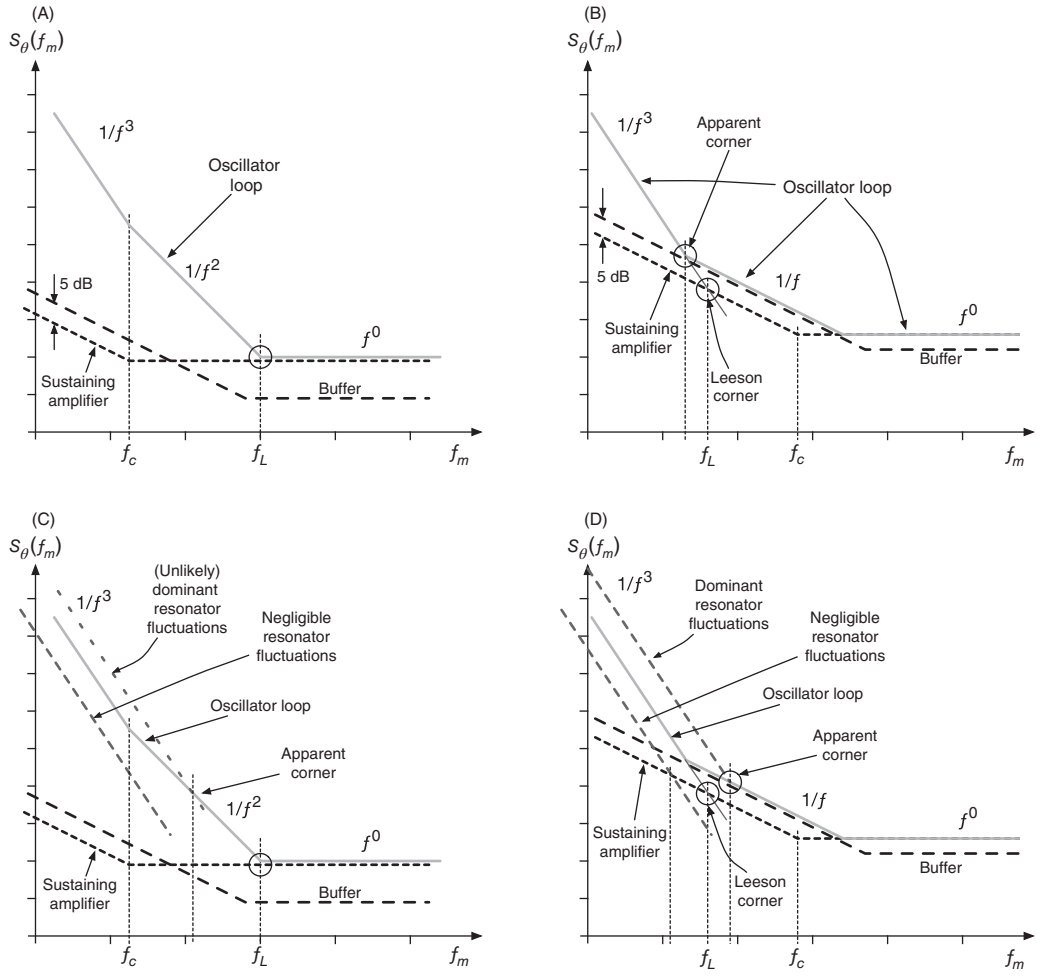


Figure 2-61 Basic types of oscillator PM noise spectra. (A) Low-*Q* fluctuation-free resonator, (B) high-*Q* fluctuation-free resonator, (C) low-*Q* real resonator, and (D) high-*Q* real resonator.

and consequently

$$Q = \frac{f_0}{2f_L} \tag{2-158}$$

Third, we estimate the corner frequency $[f_c]_{\mathrm{SA}}$ of the sustaining amplifier, which occurs when b_{-3}/f^3 equals b_{-2}/f^2

$$[f_c]_{\mathrm{SA}} = \frac{\mathsf{b}_{-3}}{\mathsf{b}_{-2}} \tag{2-159}$$

These oscillators are rather simple to understand because the high value of f_L ends up in high value of b_{-3} (frequency flicker), which in practice exceeds the fluctuations of the resonator. Additionally, with this type of oscillator we spend comparatively little attention to low Fourier frequencies, say 100 Hz and below, where higher-slope phenomena show up.

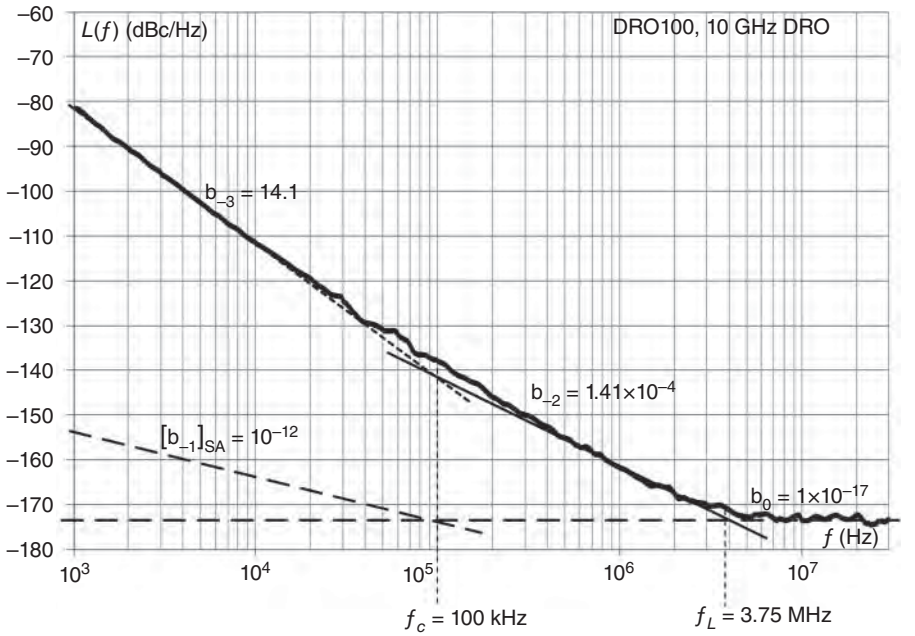


Figure 2-62 Phase noise of the DRO100, 10 GHz DRO. The spectrum is from the DRO100 data sheet, © Synergy Microwave Corp., reproduced with permission. Graphical adaptation and comments are ours.

Example 16 Synergy Microwave DRO100, 10 GHz DRO. By inspection on the phase noise plot shown in Figure 2-62, we estimate

$$\begin{aligned} \mathsf{b}_0 &= 10^{-17}\ \text{rad}^2/\text{Hz}, \\ \mathsf{b}_{-1} &\approx 0\ \text{(hidden below other noise processes)}, \\ \mathsf{b}_{-2} &= 1.41 \times 10^{-4}\ \text{rad}^2\ \text{Hz}, \text{ and} \\ \mathsf{b}_{-3} &= 14.1\ \text{rad}^2\ \text{Hz}^2. \end{aligned}$$

First, we calculate P_0 using $F = 1$ dB, thus $FkT = 6.2 \times 10^{-21}$ W/Hz at room temperature (300 K)

$$P_0 = \frac{FkT}{\mathsf{b}_0} = \frac{5.2 \times 10^{-21}}{10^{-17}} = 520\,\mu\text{W} \quad (-2.8\,\text{dBm})$$

This is a reasonable value for a microwave DRO, optimized for low phase noise floor. The oscillator inside is not known, and we cannot know if the trick of Section 2-4-2 is implemented or not. In the absence of insider information, we are inclined to believe that the answer is "not" because the design of a low-impedance common-base amplifier is rather difficult at these frequencies.

Assuming that the floor gives the power at the amplifier input, the corner at 3.75 MHz is the Leeson frequency. Thus, we calculate

$$Q = \frac{f_0}{2f_L} = \frac{10^{10}}{2 \times\ 3.75 \times 10^6} = 1330$$

This is rather a typical value for a microwave dielectric resonator.

The frequency flicker b_{-3}/f^3 crosses the white frequency b_{-2}/f^2 at the corner frequency

$$f_c = \frac{\mathsf{b}_{-3}}{\mathsf{b}_{-2}}$$

This enables to calculate the flicker of phase of the sustaining amplifier

$$\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}} = \mathsf{b}_0 f_c = 10^{-17} \times 10^5 = 10^{-12}\ \mathrm{rad} \quad \left(-120\ \mathrm{dB\ rad^2}\right)$$

This is quite a good value for a microwave amplifier, indeed well in the range of high-tech devices.

Using the formulas of Table 2-6, the modified Allan deviation is

$$\mathrm{mod}\ \sigma_{\mathrm{y}}(\tau) = \frac{5.94 \times 10^{-13}}{\sqrt{\tau}} + 3.63 \times 10^{-10}$$

It is important to interpret correctly this result. First, the $1/\sqrt{\tau}$ term equals the flicker floor at $\tau = 2.7$ µs. This short time is probably shorter than the sampling interval τ_0 of actual instruments (section "The Allan Variance (AVAR)"). The consequence is that the $1/\sqrt{\tau}$ term cannot be measured directly. Second, the estimation of mod $\sigma_{\mathrm{y}}(\tau)$ from $S_\theta(f)$ makes sense only for very short measurement time, more or less up to $\tau = 1$ ms, which is the reciprocal of the lowest frequency (1 kHz) on the left-hand side of Figure 2-62. Beyond, other terms may show up, like frequency random walk, temperature fluctuations, and aging.

After this digression, it is clear that the white PM and the flicker PM terms are too low and out of range for any practical measurement of mod $\sigma_{\mathrm{y}}(\tau)$, thus it have been discarded. For the sake of exercise, let us do the math. The white PM noise gives $\mathrm{mod}\ \sigma_{\mathrm{y}}(\tau) = 6.16 \times 10^{-20}/\left(\tau\sqrt{\tau}\right)$. The flicker PM is not directly accessible, but it can be guessed by adding the noise of three buffer stages similar to the sustaining amplifier, thus $\mathsf{b}_{-1} = 4\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}} = 4 \times 10^{-12}\ \mathrm{rad}^2$, and finally $\mathrm{mod}\ \sigma_{\mathrm{y}}(\tau) = 5.94 \times 10^{-13}/\tau$. The corner where the flicker PM noise equals the white FM noise occurs at $\tau = 9.7$ ns.

What happens if our guess is wrong, and the resonator is used to reduce the white noise as in Section 2-4-2? Let us say that the unfiltered white noise is

$$S_\theta(f) = \mathsf{b}_0' = \lambda \mathsf{b}_0$$

and take $\lambda = 4$ (6 dB) as an example. Equivalently, we allow that the unfiltered phase noise is a floor a factor of λ higher than the floor shown in Figure 2-62. Under this new hypothesis, the power at the amplifier input is

$$P_0 = \frac{fkT}{\lambda \mathsf{b}_0} = 260\ \mu\mathrm{W} \qquad (-5.8\ \mathrm{dBm})$$

the "true" Leeson frequency is

$$f_L' = \lambda f_L = 1.88\ \mathrm{MHz}$$

and the resonator quality factor is

$$Q = \frac{f_0}{2f_L'} = \frac{f_0}{2\lambda f_L} = 665$$

However unsatisfied with this spread of values, we observe that the hacking process still provides useful information on the oscillator inside. We hope that the reader will dig in the literature and find his/her own way to improve on our estimates. ■

Example 17 Synergy Microwave DCMO 1027, 100–270 MHz VCO. We proceed exactly as before, from the right-hand side of Figure 2-63 to the left-hand side, thus

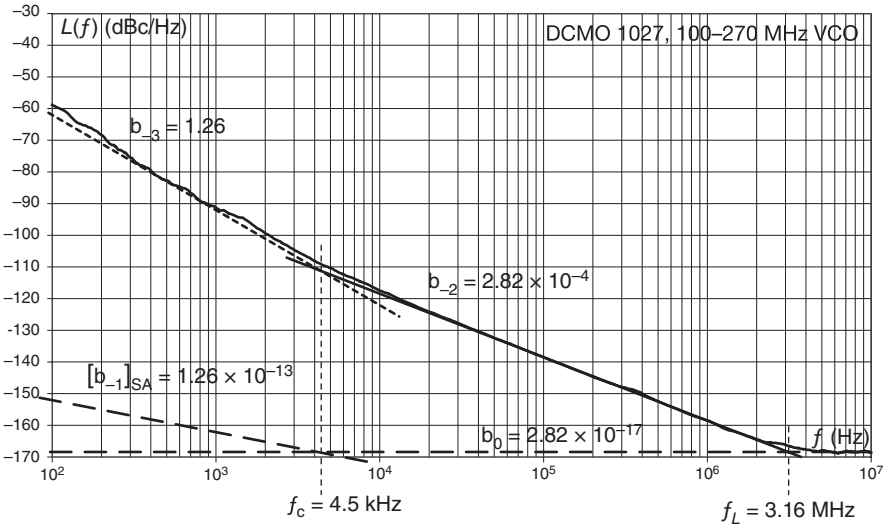


Figure 2-63 Phase noise of the Synergy Microwave DCMO 1027, 100–270 MHz VCO. The spectrum is from the DCMO 1027 data sheet, © Synergy Microwave Corp., reproduced with permission. Graphical adaptation and comments are ours.

$$\begin{aligned} \mathsf{b}_0 &= 2.82 \times 10^{-17}\ \text{rad}^2/\text{Hz}, \\ \mathsf{b}_{-1} &\approx 0 \text{ (actually, hidden below other noise processes)}, \\ \mathsf{b}_{-2} &= 2.82 \times 10^{-4}\ \text{rad}^2\text{Hz}, \text{ and} \\ \mathsf{b}_{-3} &= 1.42\ \text{rad}^2\text{Hz}^2. \end{aligned}$$

We calculate P_0 using $F = 1$ dB, at room temperature (300 K)

$$P_0 = \frac{FkT}{\mathsf{b}_0} = \frac{5.2 \times 10^{-21}}{2.82 \times 10^{-17}} = 185\ \mu\text{W} \quad (-7.3\ \text{dBm})$$

With the same reservations, we assume that the floor indicates the power at the amplifier input, hence the corner at 3.16 MHz is the Leeson frequency. The phase noise is measured at $f_0 = 136.9$ MHz. Thus, we calculate

$$Q = \frac{f_0}{2f_L} = \frac{1.369 \times 10^8}{2 \times\ 3.16 \times 10^6} = 21.6$$

This is more or less what we expect in a *LC* oscillator with a wide tuning range.

The frequency flicker b_{-3}/f^3 crosses the white frequency b_{-2}/f^2 at the corner frequency $f_c = \mathsf{b}_{-3}/\mathsf{b}_{-2} =$ 4.5 kHz. This enables to calculate the flicker of phase of the sustaining amplifier

$$\left[\mathsf{b}_{-1}\right]_{\text{SA}} = \mathsf{b}_0 f_c = 2.82 \times 10^{-17} \times\ 4.5 \times 10^3 = 1.26 \times 10^{-13}\ \text{rad}^2 \quad \left(-129\ \text{dB rad}^2\right)$$

The flicker of a good VHF amplifier should be lower, but this value probably includes the flicker of the tuning diodes. Notice that a tuning range of a factor of 2.7 requires a capacitance range of a factor of $2.7^2 = 7.3$. The burden of the tuning varactors is certainly higher because of the residual capacitance in the circuit.

Using the phase noise data we have, the modified Allan deviation is

$$\text{mod}\,\sigma_{\text{y}}(\tau) = \frac{6.1 \times 10^{-11}}{\sqrt{\tau}} + 7.9 \times 10^{-10}$$

We have discarded white and flicker PM for the same reasons of the previous example, and the same consideration about the meaning of the low value of mod $\sigma_y(\tau)$ applies here. ■

High-Q (Type B/D) Oscillators

With reference to Figure 2-61, the PM noise spectrum of the type B/D is identified by the presence of $1/f$ noise, and by the absence of $1/f^2$ noise.

First, we use the white phase noise to infer the power P_0 at the input of the sustaining amplifier. As with the A/C-type spectra, we assume that the white noise of the buffer is negligible because the power at the buffer input is generally higher than at the input of the sustaining amplifier. Likewise, we discard the effect of impedance mismatching out of the resonator bandwidth, and we take $F = 1$ dB as an approximation. Using the formula $\mathsf{b}_0 = FkT_0/P_0$, we calculate

$$P_0 = \frac{FkT_0}{\mathsf{b}_0} \tag{2-160}$$

We expect that the power dissipated by the resonator is close to this value, maybe a little higher.

Let provisionally neglect the resonator's frequency fluctuations, as in Figure 2-61B. Highlighted with a circle, we see the "apparent corner" where the spectrum changes from $1/f$ to $1/f^3$. However related, this is not the Leeson frequency. The reason is that the oscillator $1/f$ phase noise is due to both the sustaining amplifier and the output buffer. We guess that 1/4 of such flicker is due to the sustaining amplifier, and 3/4 is due to the buffer

$$\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}} = \frac{1}{4}\left[\mathsf{b}_{-1}\right]_{\mathrm{osc}} \qquad (-6\ \mathrm{dB}) \tag{2-161}$$

This formula is used to estimate the $1/f$ noise of the sustaining amplifier. In terms of electrical circuit, we guess that the buffer consists of three stages similar in noise to the sustaining amplifier. This is sound because the buffer has to provide high isolation from the load circuit.

Next, still assuming that the resonator is free from fluctuations, the $1/f^3$ noise is given by $\left[\mathsf{b}_{-3}\right]_{\mathrm{osc}} = \left[\mathsf{b}_{-1}\right]_{\mathrm{SA}} f_L^2/f^3$. Hence, we estimate the Leeson frequency f_L as the intersection between the sustaining amplifier $\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}}/f$ and the oscillator frequency flicker $\left[\mathsf{b}_{-3}\right]_{\mathrm{osc}}/f^3$

$$f_L^2 = \frac{\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}}}{\left[\mathsf{b}_{-3}\right]_{\mathrm{osc}}} \tag{2-162}$$

The result is marked as f_L on Figure 2-61A. The corner, highlighted with a circle, occurs *below* the oscillator noise, thus it is not visible. Accordingly, we find a first estimate of resonator's quality factor using $f_L = f_0/2Q$

$$Q = \frac{f_0}{2f_L} \qquad \text{(First estimate)} \tag{2-163}$$

At this point, we have to introduce the frequency flicker of the resonator, $\left[\mathsf{b}_{-3}\right]_{\mathrm{res}}/f^3$ on the phase noise plot. This is shown as the thick dashed lines on Figure 2-61D. Understanding whether $\left[\mathsf{b}_{-3}\right]_{\mathrm{res}}$ is the dominant noise, or $\left[\mathsf{b}_{-1}\right]_{\mathrm{SA}} f_L^2/f^3$ prevails, requires experience and skill. We may start to collect information from the datasheet and from the literature, figuring out the stability (flicker of frequency floor on the Allan deviation plot) and the possible Q.

If the oscillator stability is limited by the Leeson effect, (2-163) is consistent with the technology, and the oscillator is fully described by Figure 2-61B.

Oppositely, HF oscillators (5–10 MHz) exhibiting ultimate stability are generally limited by the fluctuations of the resonator. In this case, the Leeson effect is completely hidden. We can only do the academic exercise of guessing Q from the technology, or from other sources of information, calculating f_L, and identifying the $1/f^3$ part of the "oscillator loop" plot of Figure 2-61D.

Example 18 Rakon HSO 14 OCXO, 5 MHz. This oscillator is intended for space and scientific applications that require ultimate stability, for example, the VCO to be locked to the 1.42 GHz atomic transition in a Hydrogen maser. The phase noise spectrum is shown on Figure 2-64. By inspection on the plot, we estimate

$$\begin{aligned}
\mathsf{b}_0 &= 1.6 \times 10^{-16}\ \text{rad}^2/\text{Hz},\\
\mathsf{b}_{-1} &= 8 \times 10^{-15}\ \text{rad}^2 \text{ upper bound},\\
\mathsf{b}_{-2} &\approx 0 \text{ (actually, hidden below other noise processes), and}\\
\mathsf{b}_{-3} &= 6.3 \times 10^{-13}\ \text{rad}^2\ \text{Hz}^2.
\end{aligned}$$

The thick and irregular spectrum between 3 and 10 Hz may indicate that the correlation instrument has still not reached the final value, thus the true b_{-1} may be lower than indicated.

First, we calculate P_0 using $F = 1$ dB, thus $FkT = 6.2 \times 10^{-21}$ W/Hz at the oven temperature of 350 K (75–80 °C). Thus

$$P_0 = \frac{FkT}{\mathsf{b}_0} = \frac{6.2 \times 10^{-21}}{16 \times 10^{-16}} = 33\ \mu\text{W}$$

This is quite a plausible value for this type of oscillator, which is optimized for stability rather than for low phase noise floor. The oscillator inside is not known. However, we believe that the trick of the Rohde oscillator is not implemented, first because it is not necessary for the target applications of this oscillator, and second because even the lowest instability introduced by the virtual ground would be detrimental to the stability at the ultimate level required.

Assuming that the sustaining amplifier contributes 1/4 of the oscillator flicker $\mathsf{b}_{-1} = 8 \times 10^{-15}$ rad^2, we get $\left[\mathsf{b}_{-1}\right]_{\text{SA}} = 2 \times 10^{-15}$ rad^2.

By inspection on the plot, the flicker of frequency b_{-3}/f^3 crosses the sustaining amplifier flicker $\left[\mathsf{b}_{-1}\right]_{\text{SA}}/f$ at $f' = 6$ Hz. If we interpret this as the Leeson frequency, we find a quality factor $Q' = f_0/2f' = 8.9 \times 10^5$. This seems too low for this class of oscillator. So, let us stick on the thumb rule $f_0 Q \simeq 10^{13}$, thus $Q = 2 \times 10^6$.

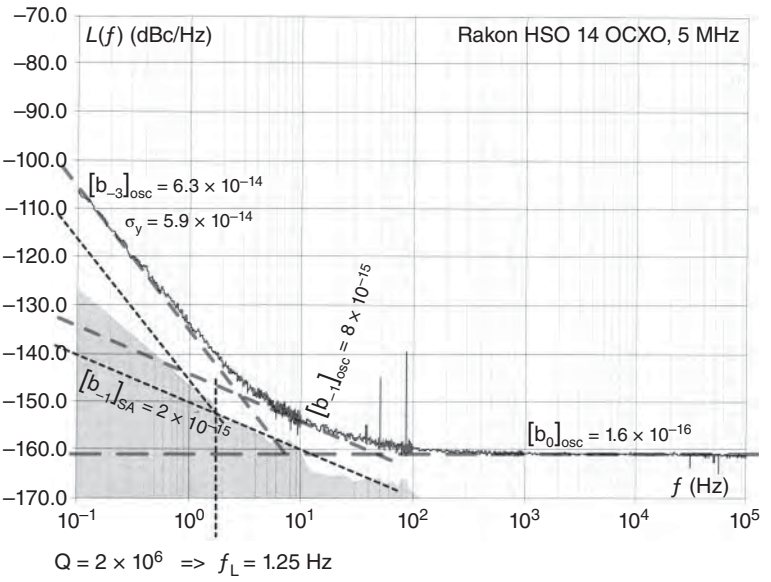


Figure 2-64 Phase noise spectrum of the Rakon HSO 14 OCXO measured with a Microsemi 5120A test set. The spectrum is © 2019 Rakon France SAS, courtesy of Patrice Canzian and Vincent Candelier. Graphical adaptation and comments are ours.

Using the formulas of Table 2-6, the modified Allan deviation is

$$\mathrm{mod}\,\sigma_y(\tau) = \frac{4.9\times10^{-16}}{\tau\sqrt{\tau}} + \frac{5.2\times10^{-15}}{\tau} + 4.9\times10^{-14}$$

Unlike in the previous examples, white and flicker PM (the $1/\tau\sqrt{\tau}$ and $1/\tau$ terms) provide useful information because the corners where white PM crosses flicker PM and where flicker PM crosses flicker FM, are of 8.9 and 106 ms, respectively, which is still in the range of practical measurements. Random walk, temperature fluctuations, and frequency drift are not visible on Figure 2-64. Such phenomena will inevitably show up, however, only for $\tau > 10$ s, which is the reciprocal of the lowest frequency (0.1 Hz) available on the phase noise plot.

Given the applications this oscillator is intended for, rather specialized in the long-term performances, the Allan deviation is preferred to the modified Allan deviation. Setting $f_H = 5$ Hz, we find

$$\sigma_y(\tau) = \frac{9.6\times10^{-15}}{\tau} + 5.9\times10^{-14}$$

with a corner at $\tau = 162$ ms.

It is interesting to compare $\mathrm{mod}\,\sigma_y(\tau)$ to $\sigma_y(\tau)$. As we have seen, $\mathrm{mod}\,\sigma_y(\tau)$ provides separate values for white PM and flicker PM, with no need of a low-pass filter. The low-pass, however, is implied in the sampling interval τ_0. By contrast, $\sigma_y(\tau)$ provides a single value for both, proportional to $1/\tau$, with a strong effect of the low-pass filter on the contribution of white PM noise. Additionally, $\mathrm{mod}\,\sigma_y(\tau)$ always gives values lower than those of $\sigma_y(\tau)$. ■

2-5 THE MEASUREMENT OF PHASE NOISE

We have already seen that the measurement of SSB noise referred to the carrier power has been abandoned long time ago, replaced with the direct measurement of the phase fluctuations versus an appropriate reference. Some general-purpose spectrum analyzers include the dedicated hardware that enables the measurement of the phase noise associated to an input signal. However, these instruments are limited by the stability and by the noise of their internal oscillator and synthesizer, and they are usable only for the measurement of some rather noisy oscillators. Instead, dedicated instruments are the right choice.

Three basic ingredients are needed for the measurement of phase noise:

- Phase reference
- Phase detector
- Signal processing unit based on FFT and averaging.

The phase reference is an oscillator or a synthesizer, which provides a suitably pure signal. The phase detector converts the phase difference, input versus reference, into a voltage or other signal. The DBM—or diode ring—saturated at both inputs is in most cases the preferred phase detector because of its low background noise. Digital detectors, like the XOR gate and the PFD, are not suitable to general test equipment, mainly because of their background noise. All these detectors require that the phase reference is at the same frequency of the input signal. The DBM is not the only option for the phase detector. Other types of instruments are found, based on direct digitization of the input signal, and on software defined radio (SDR) techniques. These digital techniques are more flexible, overcome some of the problems of the saturated mixer, and enable to compare the phase of two signals that are not at the same frequency. However, the noise of the ADCs is the major problem of such instruments.

Most modern instruments make use of two separate and equal channels that measure simultaneously the input signal. The background noise is rejected thanks to an appropriate correlation-and-averaging algorithm which relies on the hypothesis that the two channels are statistically independent. The use of correlation relaxes the noise specifications for the reference oscillator and for the phase detector, at the cost of longer measurement time. The measurement of noise below the background noise of a single channel is possible. As a consequence, correlation

and averaging allow the use of a synthesizer as the reference in each channel, which is generally noisier than a dedicated low-noise oscillator. Without synthesizers, a specific low-noise reference oscillator is necessary for each frequency of interest.

In this section, we will learn about this type of equipment, principles, background noise and other limitations, and some tricks useful to extend the range of application.

2-5-1 Double-Balanced Mixer Instruments

The basic measurement scheme, shown on Figure 2-65, is straightforward. Unlike the regular use of the mixer, the local oscillator (LO) and RF signals are synchronous ($f_{LO} = f_{RF} = f_0$), close to the quadrature, and large enough to saturate the input. In this condition, the difference $f_{LO} - f_{RF}$ degenerates to a dc signal sensitive to the phase θ

$$V = K_\theta \theta \tag{2-164}$$

The sum $f_{LO} + f_{RF}$ falls at $2f_0$, which is filtered out. The value of K_θ can be up to 0.3–0.7 V/rad in favorable conditions (Figure 2-66). A low-noise amplifier (LNA) is needed at the mixer output to raise the small signal to a level suitable to the FFT analyzer.

For an introduction the DBM, the reader can refer to the author's earlier work [80], to an old but good white paper from Watkins Johnson [81], and to the classic Maas book [82].

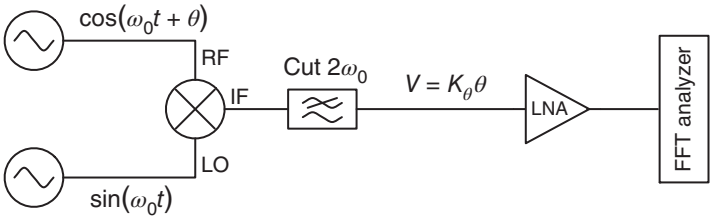


Figure 2-65 Basic phase noise measurement. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

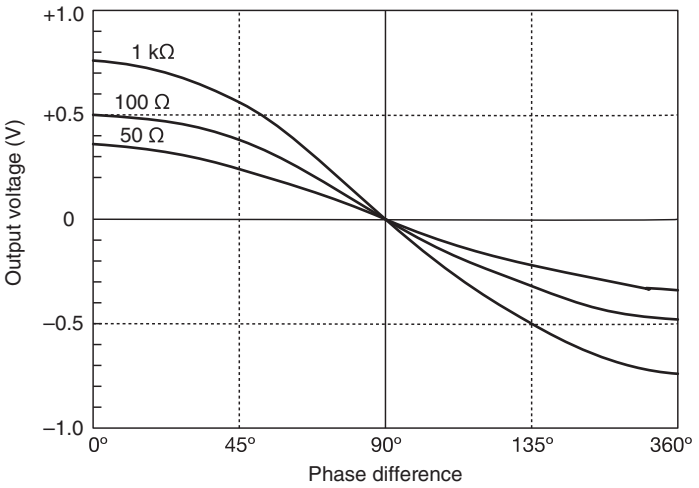


Figure 2-66 Phase-to-voltage conversion of a double-balanced mixer saturated at 15–20 dBm power at each input, plotted for different values of the load resistance. Reproduced with permission from [80].

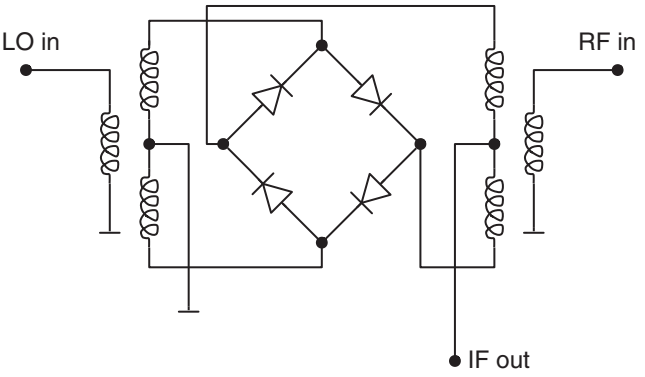


Figure 2-67 Double-balanced mixer. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

The mixer is implemented with a diode ring and baluns, similar to the circuit shown on Figure 2-67. However, the actual implementation may be more complex. Baluns are present at both RF and LO input to match the unbalanced-mode input to the diode ring, which is balanced. Two types of balun are often found. At microwaves frequencies, multi-section microstrip lines are preferred, providing a typical bandwidth is of 1–3 octaves. Wider bandwidth comes at the cost of larger physical size and higher loss. The HF-UHF implementation is based on iron powder transformers that exhibit a bandwidth of up to three decades. A wider bandwidth, up to four decades, is achieved with a smart transformer, where twisted pairs are wound on an iron powder core shaped in toroidal form or in binocular form. Primary and secondary windings are coupled magnetically lower frequencies, while capacitive or electromagnetic-line coupling takes over at high frequencies. The boundary between RF-type and microwave-type implementation is in the region of 3 GHz, depending on design and manufacturing choices.

The Schottky diodes are preferred because of low threshold and fast switching time. High-level mixers, up to 200 mW (+23 dBm) or more input power, are convenient because of the higher value of K_θ, and in turn the lower background noise. These mixers differ from Figure 2-67 in the use of 2–3 diodes in series in each arm of the ring. In each arm, an appropriate network distributes power and reverse bias equally between the diodes. By contrast, the double-DBM (sometimes called triple balanced mixer) cannot be used as a phase detector because the IF output cannot be dc coupled. Special mixers intended as phase detectors achieve higher gain by increasing the IF impedance to 500 Ω typical.

Proper switching operation requires that the IF output current can circulate at both dc and $2f_0$. The problem arises in wideband mixers, where the circulation of the $2f_0$ current has to be ensured by the load at the IF output, the reason being that the upper IF frequency falls in the LO/RF frequency range. In such cases, the low-pass filter must have resistive or capacitive input impedance, not inductive impedance.

It has been reported that a series resonator at the IF output, tuned at $2f_0$, is useful in that it maximizes the IF current at $2f_0$, and increases K_θ. Of course, this trick is reserved to special cases, where the experimentalist is interested in a single value of f_0, or at most in a small set of frequencies, and has full access to the system inside.

The DBM is an appealing choice for a phase detector because of the low background noise, the wide range of operating frequency, and the overall simplicity of the system. Most general-purpose DBMs are suitable as phase detectors. In the absence of specific information, one can assume that best power is 3 dB above the nominal LO power, and that the same power should be used for the LO input and for the RF input. One can also assume that phase-detector bandwidth is ¾ of the nominal bandwidth.

The narrow power range, typical of the DBM, can be annoying. The problem is that the input power must be sufficient to saturate the mixer, but smaller than the absolute maximum rating level, with a safe margin. Unfortunately, the gap between nominal and maximum power is not comfortable and leaves approximately ±5 dB around a nominal power of 10–15 dBm. At lower power, the background noise increases. Further decreasing the power, K_θ drops abruptly and the mixer is no longer usable.

The mixer inputs, strongly saturated, have highly nonlinear behavior and the input impedance changes with frequency. Strong odd harmonics of the carrier frequency are reflected back, combining in rather unpredictable

way depending on cable length. For this reason, it is a good practice to introduce a 3-dB attenuator as close as possible to the mixer inputs.

The Measurement of Oscillators

The basic scheme for the measurement of the PM noise of oscillators is shown on Figure 2-68. Taking the error voltage V as the output of the mixer, the PLL is used as a high-pass filter. So, beyond a cutoff frequency f_{HP}, the error signal is asymptotically equal to $V = K_\theta(\theta_{DUT} - \theta_{REF})$. Below the cutoff, the error signal is small, but the phase noise can still be calculated using the equation of the PLL. It is useful to bring the reference oscillator as close as possible to the device under test (DUT) frequency by adjusting the dc offset, so that the detector and the control work close to 0 V. In this condition K_θ is the highest, and the measurement starts with the instrument in the middle of the dynamic range.

In production and in industrial applications, it is generally possible to rely on a reference oscillator whose PM noise can be neglected, being $L_{REF}(f) \ll L_{DUT}(f)$ with a sufficient margin.

In rare cases, we may have to test special low-noise oscillators, where no lower-noise reference is available. As a first approximation, we can measure two equal oscillators, so that the noise of each is half (−3 dB) of the result displayed by the test set. Dropping the hypothesis that the two oscillators are equal, the reliable measurement of a single oscillator with the scheme of Figure 2-68 is a complex and time-consuming task because we need to compare all the possible pairs in a set of at least three similar oscillators and to solve for the noise of each. However, the cross-spectrum method provides a simple and practical solution, discussed later in this chapter.

Notice that in Figure 2-68 we have kept the reference oscillator outside the test set. This is often necessary in a general-purpose instrument because a low-noise reference is needed, at the same frequency of the oscillator under test. Neither a wideband VCO nor a synthesizer would feature the low noise needed to measure high purity oscillators. Introducing a synthesizer for flexible operation requires the dual-channel scheme, which we will study later.

The PLL error function $E(s) = \theta_e(s)/\theta_i(s)$ is given by

$$E(s) = 1 - B(s) = \frac{1}{1 + G(s)H(s)} \tag{2-165}$$

Including the gain of the LNA in K_θ, the closed-loop error voltage $K_\theta E(s)$ is described by the transfer function

$$T(s) = \frac{V(s)}{\theta(s)} = K_\theta\,[1 - B(s)] \tag{2-166}$$

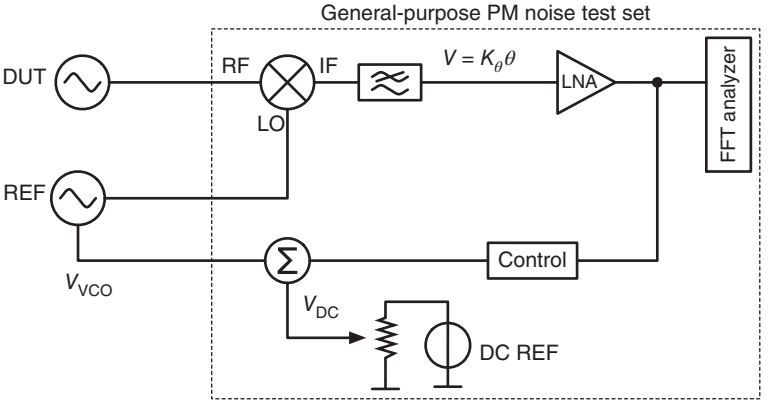


Figure 2-68 Phase noise measurement of an oscillator using the error signal of a PLL.

For the simplest loop, where $G(s)H(s) = K_\theta K_o/s$, the function $T(s)$ is a first order (single pole) high pass filter

$$T(s) = \frac{K_\theta s}{s + K_\theta K_o} \tag{2-167}$$

or equivalently

$$|T(f)|^2 = K_\theta^2 \frac{f^2}{f^2 + f_{\text{HP}}^2} \tag{2-168}$$

where f_{HP} is the cutoff frequency

$$f_{\text{HP}} = \frac{1}{2\pi} K_\theta K_o \tag{2-169}$$

In commercial test sets, f_{HP} is generally chosen by an internal algorithm, and only advanced users can take control on it. However, the implications of f_{HP} deserve attention. Naively, one may be inclined to set f_{HP} at a value lower than the lowest analysis frequency. For example, being interested in $L(f)$ from 10 Hz to 100 kHz, we would choose $f_{\text{HP}} = 1 \ldots 2$ Hz, so that $|T(f)|^2 = K_\theta^2$ (constant) in the full span. However, a tighter loop is a better choice, with f_{HP} set approximately at the corner between the $1/f^2$ noise, or the $1/f^3$ noise, and the white region (Figure 2-69). The instrument measures $S_v(f)$, that is, the PSD of v, and calculates $L(f)$ as

$$L(f) = \frac{1}{2} \frac{S_v(f)}{|T(f)|^2}$$

Of course, this relies on the accurate measurement of $|T(f)|^2$ in actual conditions, which can be accomplished by modulating the VCO signal. A first advantage of this approach is the reduced burden for the FFT's dynamic range. This is quite obvious from Figure 2-69. The oscillator $S_\theta(f)$ has a wide dynamic range (plot A) because of the $1/f^3$ and $1/f^4$ behavior. By contrast, V requires a comparatively smaller dynamic range because its spectrum (plot B)

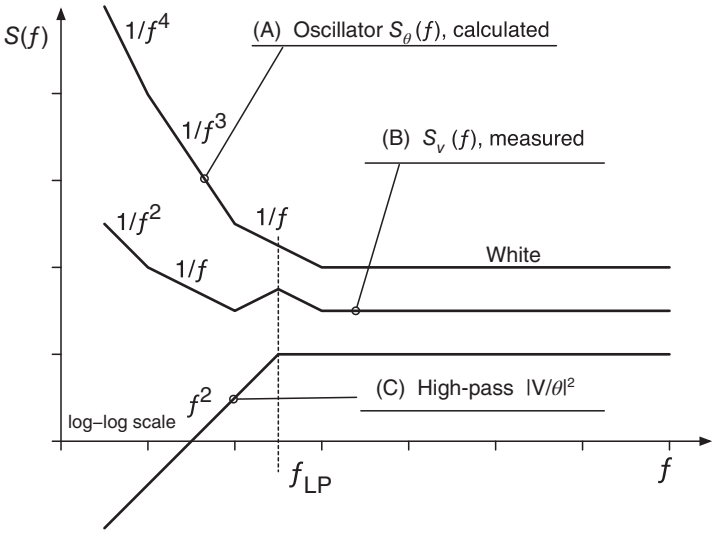


Figure 2-69 Tight PLL for the phase noise measurement of oscillators. An arbitrary constant is added to the plots for better readability of the plot.

contains at most $1/f^2$ components at low frequency. A second and more subtle advantage is that the tighter lock overrides some uncontrolled effects of electromagnetic interferences and in turn provides more reliable results.

Electromagnetic interference is sometimes a source of erratic or wrong results, difficult to identify and fix. RF/microwave leakage is to some extent inevitable, due to connectors, coaxial cables, power lines, grounding, insufficient shielding, etc. The problem arises from the fact that the reference oscillator and the oscillator under test are at the same frequency. The power leaking from one oscillator builds up as a significant energy in the second oscillator, after integration over the relaxation time of the internal resonator. The resonator's relaxation time may be unexpectedly long, up to hundreds of milliseconds in the case of high stability 5–10 MHz OCXOs. Of course, reciprocity makes the stray coupling bidirectional. Leakage may injection-lock the two oscillators to one another or corrupt the transfer function $T(s)$ if coupling is insufficient for locking. Interestingly, injection locking is a phase sensitive phenomenon. With the same amount of power leakage, the oscillator may lock or not, depending on the electrical length of the path. Should a phase noise spectrum be suspected of being corrupted by leakage, the following tests are recommended:

- Opening the loop when the two oscillators are set as close as possible to the same frequency, they phase lock to one another.
- In open loop condition as earlier, the beat note is not sinusoidal. Instead, it slows down or almost stops when certain phase relationships are met. In this case, it is likely that the two oscillators *try* periodically *to lock* to one another when the phase relationships are favorable, but coupling is insufficient and injection locking fails.
- In the $1/f^3$ or $1/f^4$ region of $S_\theta(f)$, the slope tends to decrease or get flat toward low frequencies instead of getting steeper.
- Changing the length of critical cables affects the low-frequency region $S_\theta(f)$. The critical cables are those connecting the oscillator under test to the mixer, or the reference oscillator to the mixer.
- The shape of $S_\theta(f)$ changes after introducing a common mode filter—a ferrite ring or clamp—along a cable, RF output, VCO input, or power supply.

If any of the previous symptoms show up, the experimentalist should be aware that the phase noise measurement is unreliable. Investigate on the transfer function $T(s)$ is recommended.

Background Noise, Spurs, and Other Experimental Issues

Recalling the scheme of Figure 2-68, we identify the following contributions to the instrument background noise:

- Mixer
- LNA between mixer and FFT analyzer
- Reference oscillator
- The dc reference, providing the tuning voltage
- Pollution from AM noise (CF section "The Effect of AM Noise")

Let us start with the mixer and the LNA. They must be analyzed together. The typical background noise is shown on Figure 2-70 and discussed in the following text. Lowest noise operation requires high driving power, at least +10 dBm. The mixer adds little white PM noise because its noise factor is of some dB [83], but it has a low gain K_θ. The consequence is that the white noise floor is set by the LNA after the mixer. The reader can refer to [84] for the design of LNAs specifically intended for the lowest background noise in this type of applications. Unfortunately, we do not have analytical expressions for K_θ and for the mixer noise factor. The flicker noise is an experimental parameter, for both the mixer and the amplifier. We see on Figure 2-70 that the total noise is significantly higher than the noise of a good amplifier divided by the mixer gain. The following examples show typical values of white and flicker PM noise, and their origin.

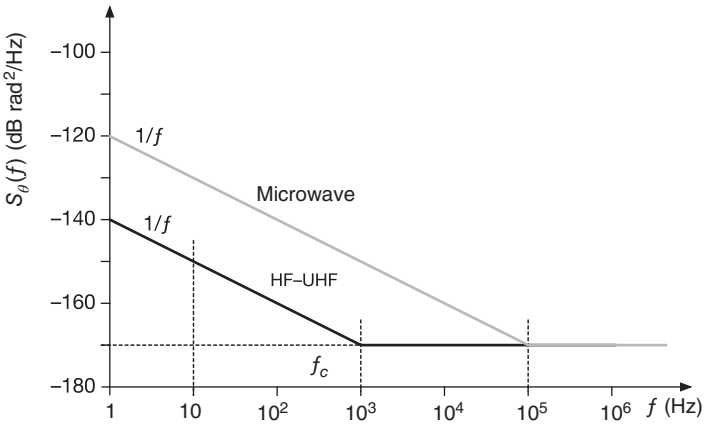


Figure 2-70 Typical background noise of a mixer, including the low-noise amplifier that follows. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

Example 19 Mixer and LNA white noise. Let us calculate the white PM noise background assuming that the mixer has $K_\theta = 500$ mV/rad driven at 40 mW (+16 dBm), and that the white noise of the LNA is $e_n = 1.25\ \text{nV}/\sqrt{\text{Hz}}$, including the 50 Ω input load.

We first convert e_n into $S_v(f) = e_n^2 = 1.56 \times 10^{-18}$ V^2/Hz, that is, −178 dB V^2/Hz. Going backward to the input, the background noise is

$$S_\theta(f) = S_v(f)\,/K_\theta^2 = 6.25 \times 10^{-18}\ \text{rad}^2/\text{Hz} \qquad \left(-172\ \text{dB rad}^2/\text{Hz}\right)$$

For comparison, the thermal noise at the mixer input is

$$S_\theta(f) = kT/P = 4 \times 10^{-21}/4 \times 10^{-2} = 10^{-19}\ \text{rad}^2/\text{Hz} \qquad \left(-190\ \text{dB rad}^2/\text{Hz}\right)$$

In this example, it takes a noise factor of 18 dB for the mixer noise to match the noise of the amplifier. Choosing different components and parameters, the result does not change significantly. For example, the highest K_θ found in a commercial instrument is of 1 V/rad, which requires +20 dBm input power.

Notice that the value of e_n of this example is quite optimistic because it includes the thermal noise $\sqrt{4kTR}$ of the input resistor, $0.9\ \text{nV}/\sqrt{\text{Hz}}$ with $R = 50\ \Omega$ at room temperature. ■

Example 20 Mixer and LNA flicker noise. We use the mixer of the previous example, $K_\theta = 500$ mV/rad, and the LNA designed for PM noise applications [84], which exhibits 1.6 nV flicker (−176 dB V^2). Referring this value to the input, we find

$$S_\theta(f) = S_v(f)\,/K_\theta^2 = \left(2.5 \times 10^{-18}/f\right)/0.5^2 = 10^{-17}/f\ \text{rad}^2 \quad \left(-170\ \text{dB rad}^2\right)$$

This is 30 dB lower than the overall noise shown on Figure 2-70, which refers to the HF-UHF mixers. Such margin may be reduced by 10 dB with better mixers, if any, and with a not-as-good amplifier. Anyway, the result yields safely to the conclusion that the background noise is chiefly originated in the mixer. ■

At low frequencies, the dominant phase noise in oscillators is $1/f^2$, $1/f^3$, and higher slope types, while mixer and low-noise dc amplifier have only white and $1/f$ noise. In this region, the phase noise of the reference oscillator is generally the most severe limitation to the measurement.

It is often necessary to provide a dc voltage at the VCO input to bring the oscillator at the nominal frequency, as in Figure 2-68. The voltage noise of this source turns into FM noise at the oscillator output. Thus, white and flicker noise show up as white and flicker FM noise, whose slope is $1/f^2$ and $1/f^3$ on the phase noise spectrum. In principle, the contribution of the dc source should be made smaller than the oscillator noise. This is not always possible, chiefly in the case of oscillators having low phase noise and high voltage-to-frequency gain. By contrast, the control provides only the small correction needed to keep the oscillator locked during the measurement. For this reason, in a good design the fluctuations coming from the control fall below other noise contributions. Having seen unexpected experimental mistakes, we strongly recommend at least a quick check on the noise sent to the VCO input.

The FFT analyzer is preceded by an LNA. Thus, an appropriate choice of the amplifier and of its gain makes the noise of the analyzer negligible. That said, the noise of the analyzer deserves more attention in earlier FFT analyzers, where the low-frequency decades were obtained by reducing the sampling frequency of the converter. The problem comes from the quantization noise, whose variance is $\sigma^2 = V_{\mathrm{LSB}}^2/12$. The Parseval identity states that $\sigma^2 = S_v(f)f_s/2$, where $S_v(f)$ is the white noise floor, and $f_s/2$ is the bandwidth of the quantization noise, equal to half the sampling frequency f_s. Thus, the quantization noise is $S_v(f) = V_{\mathrm{LSB}}^2/6f_s$. On the FFT analyzer, this is seen as a staircase-shaped noise floor, increasing steadily toward the low-frequency decades, where the sampling frequency is progressively lower. The problem is solved in modern analyzers. The input ADC runs always at full speed, and the lower sampling rate is obtained by data decimation after digital low-pass filtering.

Asymmetric Driving for Low-Power Signals

The mixer is unsuitable to low power signals because K_θ decreases. This impacts strongly on the white noise floor, and flicker PM noise tends to increase at low power. Below a threshold power, K_θ drops suddenly, and the mixer is no longer usable. However, asymmetric power driving is possible, with the LO input saturated, and the RF input in the linear regime, say, at a power 10 dB lower than the LO nominal power, or even less. This may be convenient for the measurement of oscillators and of two-port components, when only the reference signal has a power sufficient to saturate the mixer.

In the asymmetric power driving, the mixer works as a synchronous detector. This mode is broadly similar to the regular "superheterodyne receiver," differing in that LO and RF frequency is the same, thus $|f_{\mathrm{LO}} - f_{\mathrm{RF}}|$ degenerates to dc. The LO signal is

$$V_{\mathrm{LO}}(t) = V_{\mathrm{sat}} \sin\left(\omega_0 t\right) \tag{2-170}$$

where the peak voltage V_{sat} results from saturation. Using the approximation $\cos\theta \simeq 1$ and $\sin\theta \simeq \theta$ for small θ, the RF signal $V_{\mathrm{RF}}(t) = V_0 \cos(\omega_0 t + \theta)$ becomes

$$V_{\mathrm{RF}}(t) = V_0 \cos\left(\omega_0 t\right) - \theta V_0 \sin\left(\omega_0 t\right) \tag{2-171}$$

Dropping the $2\omega_0$ term, the detected signal at the IF port is

$$V = V_0 A \theta \tag{2-172}$$

where A is the mixer loss written as a "gain." For example, a loss of 6 dB translates into $A = 0.5$ because $10^{-6/20} = 0.5$. From the definition of the phase-to-voltage gain $K_\theta = V/\theta$, we find

$$K_\theta = V_0 A \tag{2-173}$$

Example 21 We use a mixer that has a loss of 8 dB ($A = 0.4$) when the LO port is saturated at +18 dBm ($V_{\mathrm{sat}} = 2.5$ V across 50 Ω load). Sending a −12 dBm signal ($V_0 = 80$ mV across 50 Ω load) to the RF port, in quadrature with the LO signal, the phase-to-voltage gain is $K_\theta = 32$ mV/rad. ■

Heterodyne Measurement of Oscillators

The heterodyne method (Figure 2-71) is a good option to extend the range of a phase noise test set to higher frequencies by exploiting a low-frequency beat at $f_b = |f_i - f_r|$, with $f_b \ll f_i$, and also $f_b \ll f_r$. In a typical case, we compare two microwave oscillators by bringing the beat down to the HF region. Of course, a suitable reference oscillator must be available, and some auxiliary pieces of hardware. In open-loop conditions, the phase fluctuation of the beat note is

$$\theta_b = \theta_i - \theta_r \tag{2-174}$$

thus

$$S_{\theta,b}(f) = S_{\theta,i}(f) + S_{\theta,r}(f) \tag{2-175}$$

Interestingly, the scheme of Figure 2-71 takes benefit from a leverage effect, which relaxes the frequency-stability specification for the VCO and for the synthesizer by a factor of f_b/f_i. This leverage effect is a direct consequence of the fact that the beat mechanism stretches the time associated to a unit of phase (radian) by the factor f_i/f_b. This is particularly useful in the $1/f^2$, $1/f^3$ and steeper regions of $L(f)$. For the purpose of extending the frequency range, the heterodyne scheme is preferred to a frequency divider because of the lower background noise.

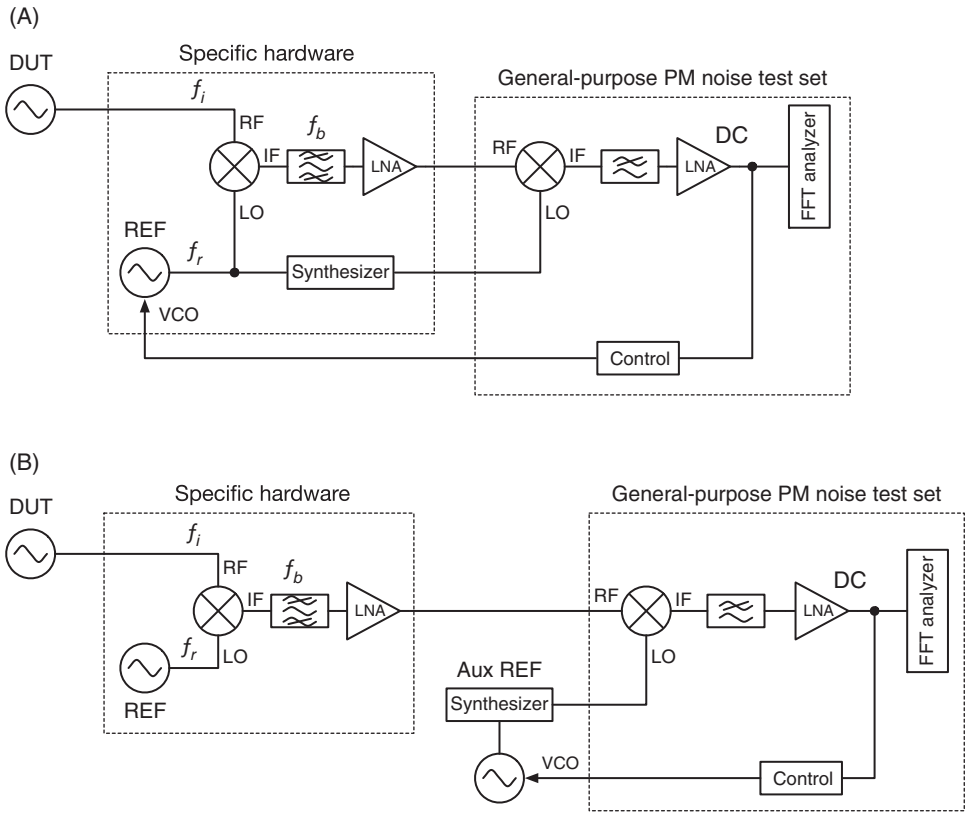


Figure 2-71 Heterodyne (beat) method for the phase noise measurement of oscillators with a single VCO (A), and with an auxiliary VCO (B). Reprinted from [1], CC BY Rubiola, and adapted to our notation. ER Slideshows, public domain material.

In the scheme of Figure 2-71A, the reference oscillator also drives the synthesizer. This may be impractical because commercial synthesizers accept only some round values of the reference frequency, typically 5–10–100 MHz. An alternate scheme is possible, shown in Figure 2-71B. In this case, the main reference oscillator is free running, with no control, and the auxiliary reference is phase-locked to the beat note $f_b = |f_i - f_r|$. The hardware is clearly simpler than on Figure 2-71A, and the benefit of the leverage effect is the same. Besides the microwave practice, Figure 2-71B solves some difficult problems of PM noise measurements, beyond the scope of this book. For example, the metal-semiconductor (Schottky) diode can be used to down convert from the THz region to HF or VHF. Similarly, the fast PIN InGaAs photodetector is routinely used in metrology labs to beat 1550-nm telecom lasers down to microwaves.

The Measurement of Amplifiers and Other Two-Port Components

In the case of two-port components, we opt for the differential measurement scheme shown in Figure 2-72. Once the quadrature condition is set, the mixer delivers a voltage proportional to the instantaneous phase fluctuation of the DUT. The oscillator PM noise is common mode, thus it is rejected. In spite of this, practical measurements are way more difficult than Figure 2-72 lets us believe. The PLL scheme (Figure 2-68) is simple to use, to the extent that the quadrature condition is set automatically and precisely by the feedback. By contrast, in Figure 2-72 the quadrature condition relies on an adjustable phase shifter manually set by the operator. The reference arm is the preferred location for this phase shifter because it is independent of the DUT. A tuning range of 180°, with a comfortable margin, is sufficient because any of the two quadrature points at ±90° can be used, with equivalent results. Different types of phase shifters can be used, depending on frequency. Mechanical phase shifters (U-shaped line stretchers) are appealing for their low noise, fine tuning capability, and wide frequency range. One of us (ER) has used extensively the phase shifters manufactured by ARRA for research applications. A problem with the line stretchers is the small delay range, related to the physical size. For reference, a range of 1 ns is equivalent to 30 cm change in the electrical length, thus of approximately 25 cm physical excursion. Of course, the range can be extended with a set of electrical cables of known length, but the operation is tedious and time consuming. A 90° directional coupler terminated to varactors at two ports is an excellent phase shifter, provided the noise of such varactors is low enough compared with the DUT. The frequency range is limited by the 90° coupler. For lower noise, the varactors can be replaced with variable capacitors, but in this case the adjustment is difficult and time consuming. A classic solution suitable to HF-VHF (Figure 2-73) is found in an article by Phillips [85].

In summary, experience suggests that it is almost impossible to combine the suitable range of phase with a wide range of frequency. The reason is that electronics gives wideband control on delay, or narrowband control on phase. The fact that delay and phase are related does not really help to get the >180° excursion we need.

The measurement of two-port components challenges the background noise of the instrument. This happens because these components often exhibit very low noise and because the noise processes are of the same type of those of the instrument, that is, white and flicker PM. For example, the flicker PM noise of an RF amplifier may be of the same order of that of a DBM. The background noise is discussed in section "Background Noise, Spurs, and Other Experimental Issues".

The measurement of amplifiers is always tricky because it is necessary to match both input power and output power to the instrument. A problem is that the mixer has a narrow power range. Another problem is that white

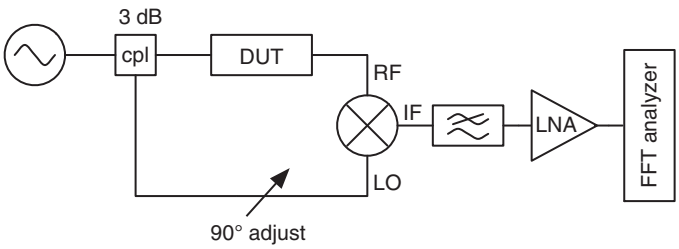


Figure 2-72 Phase noise measurement of a two-port component. Reprinted from [1], CC BY Rubiola.

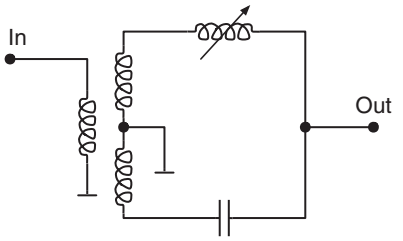


Figure 2-73 Example of variable phase shifter.

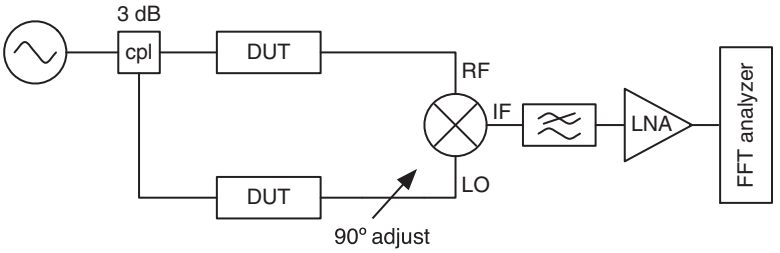


Figure 2-74 Phase noise measurement of frequency dividers and multipliers, and other devices whose output frequency is not equal to the input frequency. Reprinted from [1], CC BY Rubiola.

phase noise increases at low input power. In practice, it is often necessary to introduce appropriate attenuators at both input and output of the amplifier, whose attenuation must be determined for each case.

Finally, frequency multipliers, dividers, and synthesizers are a special case because they deliver an output frequency that is not equal to the input frequency. The scheme of Figure 2-74 solves the problem by using two equal DUTs, so that the mixer receives the same frequency at the two inputs. Of course, this method gives the total noise of the two DUTs, with no means to divide the noise contribution of each. We rely on the assumption that the phase noise of the two DUTs is the same, and we take away 3 dB for the phase noise of one. This method may also be useful in other cases, for example, in LNAs, where the enhanced sensitivity due to the presence of two DUTs helps to get out of the background noise.

The Discriminator Method

Figure 2-75 shows a method to measure the PM noise of an oscillator using a delay line as the frequency reference, so that the signal at the mixer output is $K_\theta[\theta(t) - \theta(t-\tau)]$. The measurement is possible because the delay line de-correlates the phase noise, under some conditions. This method is useful for fast phenomena, not for random walk and drift. The dynamic range is limited by the amount of delay that can be introduced without excessive attenuation and by the background noise of the mixer and of the following circuits. Lance et al. [86] used coaxial cables, enhancing the sensitivity with the cross-spectrum method discussed later in Chapter 7. For long delay, up to 10–20 μs, the optical fiber proved to be an efficient solution [87] because of the extremely low attenuation, 0.2 dB/km, or 0.04 dB/μs delay. The delay at microwave frequency is obtained by modulating and detecting the intensity of a laser beam. Improved sensitivity is achieved with the cross-spectrum method, using two statistically independent instruments, which measure simultaneously the same oscillator [88, 89].

The response of the system is defined as

$$|T(f)|^2 = \left|\frac{V(f)}{\Theta(f)}\right|^2 \tag{2-176}$$

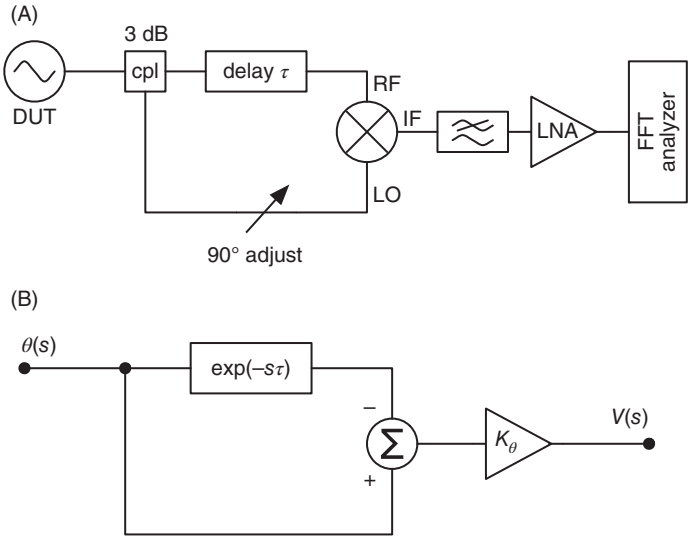


Figure 2-75 (A) Phase noise measurement of an oscillator using a delay line as the reference. (B) The phase-noise equivalent circuit. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

where $V(f)$ and $\Theta(f)$ are the Fourier transform of the output voltage, and of the oscillator random phase. This transfer function is easy to derive analytically using the phase step method that we have seen in section "The Resonator and Its Impulse Response" with the response of the resonator. We use the Laplace transforms $V(s)$ and $\Theta(s)$, where $s = \sigma + j\omega$ is the complex variable. By inspection on Figure 2-75, the line delays the phase perturbation and the impulse of phase by the same amount τ. The output voltage is

$$V(s) = K_\theta \left[1 - e^{-s\tau}\right] \Theta(s) \tag{2-177}$$

With simple manipulations, we find

$$\begin{aligned} |V(f)|^2 &= \left| K_\theta \left[1 - e^{-j2\pi f\tau}\right] \right|^2 |\Theta(f)|^2 \\ &= K_\theta^2 \left[1 - e^{-j2\pi f\tau}\right] \left[1 - e^{j2\pi f\tau}\right] |\Theta(f)|^2 \\ &= 4K_\theta^2 \sin^2(2\pi f\tau)\, |\Theta(f)|^2 \end{aligned}$$

and finally

$$|T(f)|^2 = 4K_\theta^2 \sin^2(2\pi f\tau) \tag{2-178}$$

The aforementioned equation is exploited to calculate

$$L(f) = \frac{1}{2} \frac{1}{4K_\theta^2 \sin^2(2\pi f\tau)} S_v(f) \tag{2-179}$$

from the PSD $S_v(f)$ of the voltage measured by the FFT analyzer.

Notice that (2-179) has singularities at $f = n/2\tau$, integer n, where $L(f)$ cannot be calculated. At $f \to 0$, the transfer function is approximated with $|T(f)|^2 = 16K_\theta^2 \pi^2 \tau^2 f^2$, and the instrument has a poor sensitivity due to background noise. For $n \geq 1$, $L(f)$ shows large and sharp peaks due to the background noise. In practice, the system is usable up to $f \approx 0.8/2\tau$.

The delay line can be replaced with a reference resonator, as shown on Figure 2-76. In the first scheme from the top, the resonator is used as the reference for the measurement of an oscillator. Of course, it is necessary that the resonator is more stable than the oscillator.

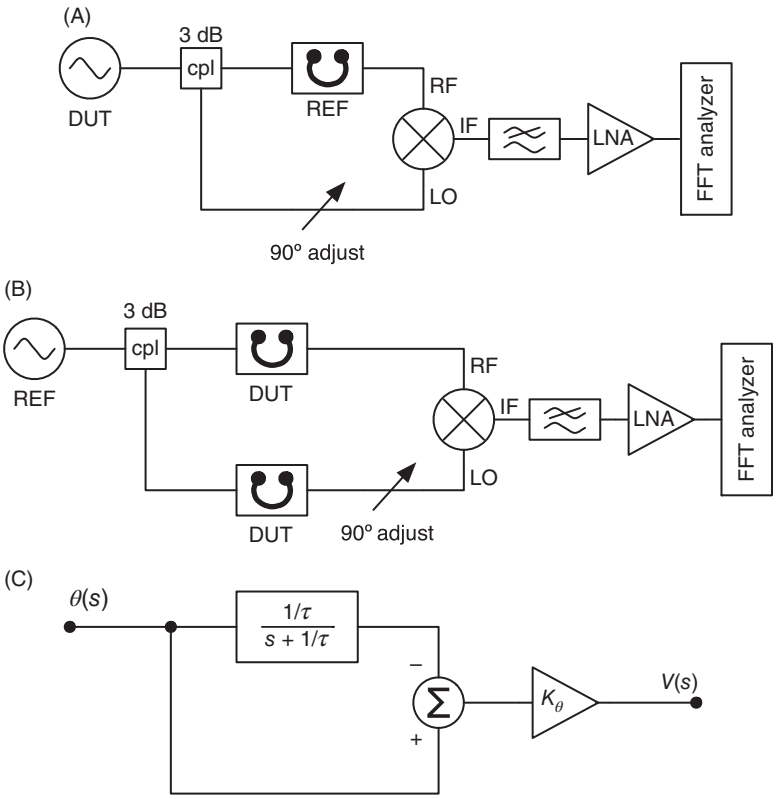


Figure 2-76 Phase noise measurement of an oscillator using a resonator as the reference (A). The roles can be inverted (B), using the oscillator as the reference for the measurement of a resonator. In this case, it is convenient to use two equal DUTs. (C) We see the phase-noise equivalent circuit of the first scheme. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

In the second scheme the roles are interchanged, and the resonator is the device under test. In this case, it is convenient to use two equal DUTs having the same resonant frequency and the same Q because in this case the noise of the reference oscillator is rejected.

The third scheme, on the bottom of Figure 2-76, is the phase-noise equivalent circuit used to measure the input oscillator versus the reference resonator. We use this scheme to derive the frequency transfer function $|T(f)|^2$ assuming that the resonator natural frequency f_n is equal to the carrier frequency f_0. We follow the same methods just used for the delay line, but the resonator's phase response is $B(s) = (1/\tau)/(s + 1/\tau)$, as seen in section "The Resonator and Its Impulse Response". There follows that

$$T(s) = K_\theta \left[1 - \frac{1/\tau}{s + 1/\tau}\right] = K_\theta \frac{s}{s + 1/\tau} \tag{2-180}$$

thus

$$|T(f)|^2 = K_\theta^2 \frac{f^2}{f^2 + \dfrac{1}{4\pi^2\tau^2}} \tag{2-181}$$

Using the quality factor Q and the natural frequency $f_n = f_0$ of the resonator, the transfer function is better rewritten as

$$|T(f)|^2 = K_\theta^2 \frac{f^2}{f^2 + \dfrac{f_n^2}{4Q^2}} \tag{2-182}$$

Finally, the oscillator phase noise is

$$S_\theta(f) = \frac{1}{|T(f)|^2} S_\nu(f) = \frac{1}{K_\theta^2} \frac{f^2 + f_n^2/(4Q^2)}{f^2} S_\nu(f) \tag{2-183}$$

At $f \to 0$, the response of the instrument is poor, and dominated by the background noise. However, the measurement does not suffer from the infinite series of singularities as in the case of the delay line. The resonator has its minimum loss at $f_n = f_0$. This enables to pump correctly the mixer at the two inputs.

2-5-2 The Cross-Spectrum Method

The scheme of the dual-channel measurement, shown on Figure 2-77, consists of two equal branches that measure the same oscillator using the PLL method. The main point is that the noise of the reference oscillators, of the mixers, and of the LNAs can be rejected using correlation and averaging. This is possible because the devices are physically separate, thus we can assume that their noise processes are statistically independent. By contrast, the DUT is common to the two branches, thus it is fully correlated, and captured by the statistical process.

The cross-PSD relates to the Fourier transform of the correlation function. Thus, averaging on m measures of $S_\theta(f)$, the single-channel background noise is rejected by a factor of approximately $1/\sqrt{m}$. It is therefore possible to measure a phase noise $S_\theta(f)$ lower than the background noise of a single branch.

Figure 2-78 shows what happens during the measurement process. The DUT noise (C) is lower than the background noise in single-channel mode (A), thus the measurement is possible only after rejecting the background. The instrument displays the cross PSD averaged no m acquisitions. The cross PSD starts from the single-channel background (A) and is progressively reduced proportionally to $1/\sqrt{m}$. With small m, the single-channel background is not sufficiently rejected, and the instrument displays the plot (B). When m is large enough, the single-channel background is well rejected (D), and the instrument displays the DUT noise (C).

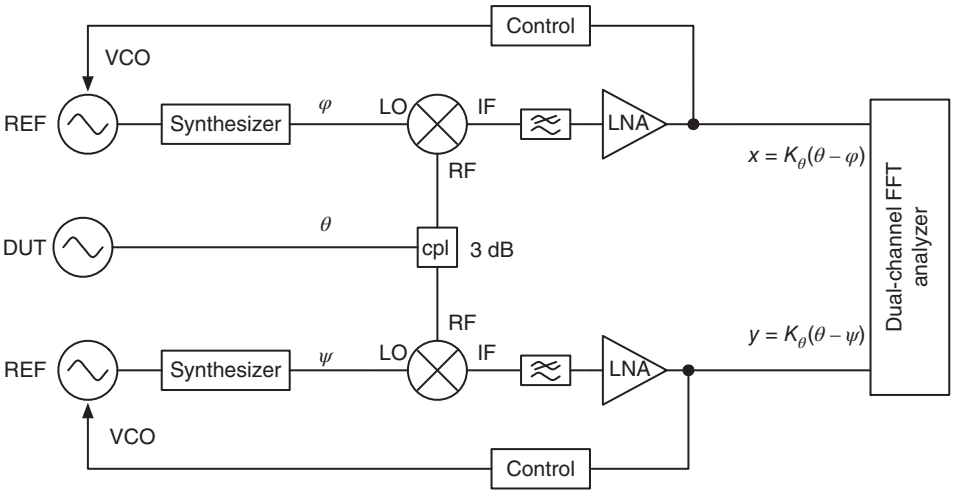


Figure 2-77 Dual-channel phase-noise measurement system. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

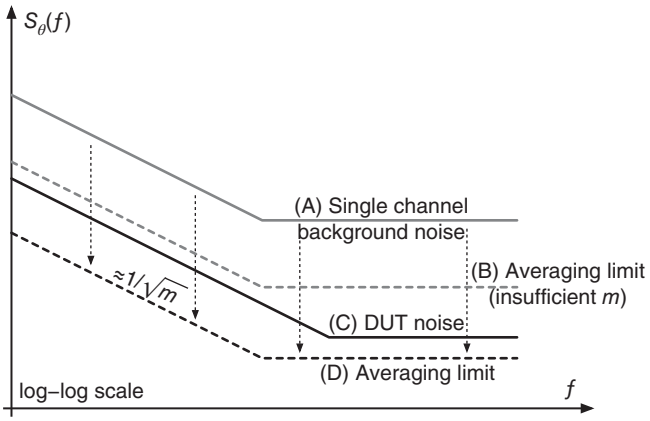


Figure 2-78 Rejection of the background noise in the dual-channel phase noise measurement.

In this version of the PLL method, we have introduced a synthesizer between the reference oscillator and the phase detector. The obvious benefit is that the system is flexible and suitable to a wide range of frequencies, without need of a separate reference oscillator for each frequency of interest. The higher noise of the synthesizer, as compared with an oscillator, can be tolerated, thanks to the noise rejection of the dual-channel scheme. Figure 2-79 shows a simpler version of the dual-channel system. It differs from the previous version in that there is only one reference oscillator, driving both the synthesizers. The trick is that each synthesizer has an internal frequency reference, locked to the main reference. The appropriate cutoff frequency inside such synthesizers may be of the order of 0.1–1 Hz, depending on the interplay between the stability and phase noise spectra of the internal and external references. Thus, for f beyond the cutoff, the two synthesizers are statistically independent, and their noise is rejected. Below the cutoff, the entire measurement relies on the stability and on the spectral purity of the main reference.

The Rejection of the Background Noise

After the heuristic reasoning, we explain the mathematics underneath the rejection of the single-channel noise. A more detailed treatise of the cross-spectrum is available in [90].

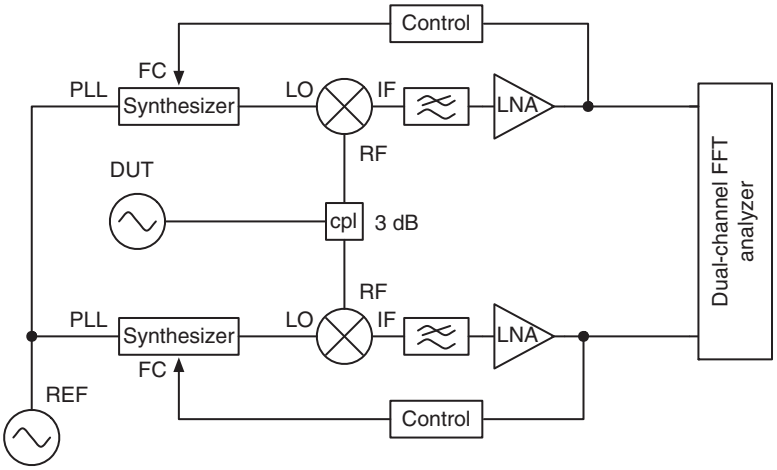


Figure 2-79 Alternate dual-channel phase-noise measurement system. Reprinted from [1], CC BY Rubiola.

With reference to Figure 2-77, the two signals at the input of the FFT analyzer are

$$x(t) = K_\theta\,[\theta(t) - \varphi(t)] \tag{2-184}$$

$$y(t) = K_\theta\,[\theta(t) - \psi(t)] \tag{2-185}$$

where the gain K_θ is the same for the two channels and includes the trivial gain of the LNAs. The random phases $\varphi(t)$ and $\psi(t)$ account for the noise of the references, the mixers, and the LNAs. Accordingly, $\theta(t)$ is the random phase of the oscillator under test, with no additional terms. It is sound to assume that $\theta(t)$, $\varphi(t)$, and $\psi(t)$ are statistically independent because they come from separate hardware. Only $\theta(t)$ appears in both $x(t)$ and $y(t)$.

As usual, we denote the Fourier transform with the uppercase letters

$$X(\omega) = K_\theta\,[\Theta(\omega) - \Phi(\omega)] \tag{2-186}$$

$$Y(\omega) = K_\theta\,[\Theta(\omega) - \Psi(\omega)] \tag{2-187}$$

The cross PSD is given by

$$S_{yx}(f) = \frac{2}{T}\,Y(f)\,X^*(f) \tag{2-188}$$

where T is the measurement time, the superscript "*" stands for complex conjugate, and the factor "2" fixes the scale factor from the two-sided Fourier transform into to the one-sided PSD. Using a lighter notation where the frequency is implied, the aforementioned formula is expanded as

$$S_{yx} = K_\theta^2 \frac{2}{T}\left(\Theta\Theta^* - \Theta\Phi^* - \Psi\Theta^* + \Psi\Phi^*\right) \tag{2-189}$$

The dual-channel FFT analyzer measures the cross-spectrum $\langle S_{yx}(f)\rangle_m$ averaged on m data records of $x(t)$ and $y(t)$ acquired simultaneously

$$\left\langle S_{yx}\right\rangle_m = K_\theta^2 \frac{2}{T}\left[\langle\Theta\Theta^*\rangle_m - \langle\Theta\Phi^*\rangle_m - \langle\Psi\Theta^*\rangle_m + \langle\Psi\Phi^*\rangle_m\right] \tag{2-190}$$

A rather intuitive theorem states that if two random variables are statistically independent in the time domain, their Fourier transforms are also statistically independent. Thus, we expect that $\langle\Theta\Phi^*\rangle_m \to 0$, $\langle\Psi\Theta^*\rangle_m \to 0$, and $\langle\Psi\Phi^*\rangle_m \to 0$ for large m. Consequently

$$\left\langle S_{yx}\right\rangle_m = K_\theta^2 \frac{2}{T}\langle\Theta\Theta^*\rangle_m = K_\theta^2\left\langle S_\theta\right\rangle_m \tag{2-191}$$

The process takes a time mT, not counting the computing time.

It is useful to write the instrument readout as the estimation, denoted with the "hat" accent

$$\widehat{S}_\theta(f) = \frac{1}{K_\theta^2}\left\langle S_{yx}(f)\right\rangle_m \tag{2-192}$$

The estimation is a powerful concept because the simple average is not the one and only option, and we can consider other estimators.

The aforementioned reasoning gives account for the most interesting feature of the cross-spectrum method, which is the possibility to measure $S_\theta(f)$ below the limit set by the single-channel background noise. However, it takes infinite averaging for (2-192) to fully eliminate the background. For finite m, the terms $\langle\Theta\Phi^*\rangle_m$, $\langle\Psi\Theta^*\rangle_m$, and $\langle\Psi\Phi^*\rangle_m$, are not completely averaged out, and set the measurement limit.

It is worth mentioning that $S_\theta(f)$ is a real and positive quantity because $\Theta\Theta^*$ is obviously real and positive. By contrast, the Fourier transform is a complex quantity, thus $\Theta\Phi^*$, $\Psi\Theta^*$, and $\Psi\Phi^*$ are complex, and consequently

(2-192) is complex. In the mixed terms $\Theta\Phi^*$, $\Psi\Theta^*$, and $\Psi\Phi^*$, the background noise is equally split between real part and imaginary part. Therefore, (2-192) can be replaced with

$$\widehat{S}_\theta(f) = \frac{1}{K_\theta^2}\left\langle \Re\left\{S_{yx}(f)\right\}\right\rangle_m \tag{2-193}$$

This results in higher sensitivity because the unnecessary part of the background noise is removed, at no cost in terms of hardware and computation complexity. It can be proved that (2-193) is the optimum estimator for white noise, that is, the estimator that converges to $S_\theta(f)$ with the lowest m, or equivalently in the shortest measurement time. Assuming that the background noise is the same for the two channels, $S_{\text{one-ch}}(f) = S_\varphi(f) = S_\psi(f)$, the averaging limit is

$$S_\theta(f) = \frac{S_{\text{one-ch}}(f)}{\sqrt{2m}} \qquad \text{averaging limit} \tag{2-194}$$

A problem with the estimator (2-193) is that negative values are incompatible with the logarithmic scale (dB rad^2/Hz). The problem is explained on Figure 2-80, which shows the probability density function (PDF) of $\widehat{S}_\theta(f)$ at a single frequency, that is, one bin of the FFT, for different values of m. The PDF is quite large at low m, where the single-channel background noise is dominant. Being the background noise dominant at small m, a significant amount of negative outcomes occur. Increasing m, the PDF shrinks and converges to the final value of $S_\theta(f)$, and the negative occurrences get progressively rare.

Most commercial instruments use the estimator

$$\widehat{S}_\theta(f) = \frac{1}{K_\theta^2}\left|\left\langle S_{yx}(f)\right\rangle_m\right| \tag{2-195}$$

instead of (2-193). This guarantees that all values are positive, and suitable to the logarithmic scale. In this case, the averaging limit is given by

$$S_\theta(f) = \frac{S_{\text{one-ch}}(f)}{\sqrt{m}} \qquad \text{averaging limit} \tag{2-196}$$

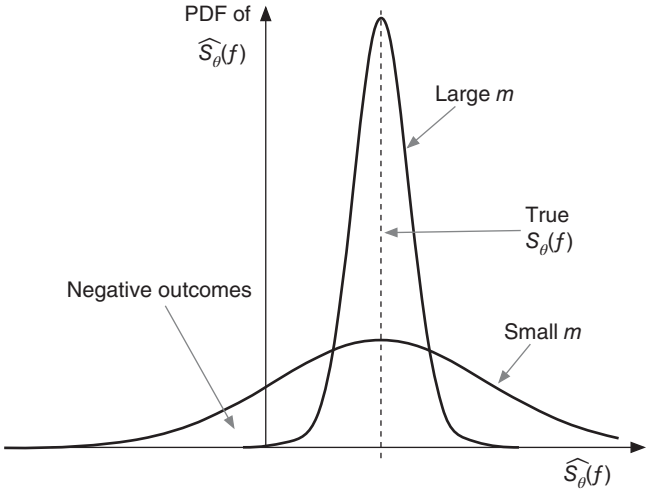


Figure 2-80 Probability density function (PDF) of $\widehat{S_\theta}(f) = \left(1/K_\theta^2\right)\langle\Re\{S_{yx}(f)\}\rangle_m$ at a single frequency f, that is, one bin of the FFT.

The consequence is that, for the same $S_{\text{one-ch}}(f)$ and for the same averaging-limit target, the value of m set by (2-195) is four times larger than that set by (2-193). Accordingly, the full measurement process takes four times longer time.

We believe that the choice of (2-195) is mainly due to historical reasons. If we want to preserve the logarithmic display, more efficient options are possible. A good choice consists of taking the real part as in (2-193), but replacing all the negative outcomes of with the smallest positive number. With this choice, the estimator discards all the noise associated to the imaginary part and reduces the bias.

The aforementioned digression is for a given number m of averaged spectra. Focusing on the measurement time $\mathcal{T}$, taken for the m acquisitions, provides a totally different perspective on the noise rejection. Given the time T for one acquisition, it holds that $m = \mathcal{T}/T$. This can be rewritten as $m = \mathcal{T}\,\Delta f$ because the resolution (distance between contiguous bins) of the FFT is $\Delta f = 1/T$. Measuring phase noise, we always represent the frequency on a log scale. Hence, we like a logarithmic frequency resolution with $\Delta f/f = C$, a constant. This gives a constant number μ of bins per decade, related to the resolution by

$$\frac{\Delta f}{f} = e^{\ln(10)/\mu} - 1 \tag{2-197}$$

Working in logarithmic resolution, we rewrite m as $m = \mathcal{T} f(\Delta f/f)$, and (2-196) becomes

$$S_\theta(f) = \frac{1}{\sqrt{\mathcal{T}(\Delta f/f)}} \frac{S_{\text{one-ch}}(f)}{\sqrt{f}} \qquad \text{averaging limit} \tag{2-198}$$

The rejection law is shown on Figure 2-81. The $1/\sqrt{f}$ term of (2-198) introduces a -5 dB/decade slope, which adds to the background noise of the instrument. Thus, the flicker region is seen as a slope of -15 dB/decade, and the white region is seen as a slope of -5 dB/decade. Of course, additional limitations apply, due to crosstalk and to other hardware problems that introduce a correlation between the two channels.

The logarithmic resolution cannot be obtained directly from the FFT algorithm. Other specific algorithms exist (see, e.g., [91]). A popular solution is the FFT implemented in segments, more or less one decade wide. The resolution Δf is constant inside each segment, but proportionally narrower Δf is adopted in the lower-frequency segments after decimating the time series. The corresponding pattern is a step function, which approximates the $1/\sqrt{f}$ term of (2-198).

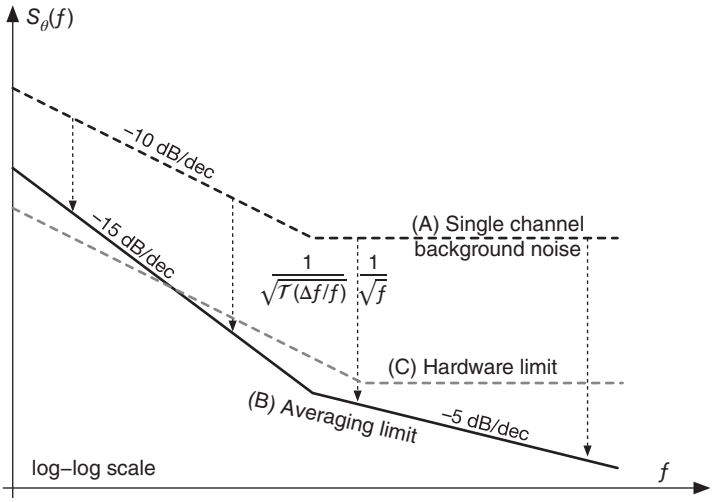


Figure 2-81 Rejection of the background noise in logarithmic resolution, with constant $\Delta f/f$ over the full span and fixed measurement time $\mathcal{T}$.

2-5-3 Digital Instruments

The DBM has been the preferred phase detector since the 1970s. More recently a new generation of digital instruments appeared, when fast ADCs were available, capable of about 12 bit resolution at 50–100 MHz sampling rate. This enables the direct digitization of an RF signal, and the extraction of the instantaneous amplitude and phase.

Figure 2-82 shows a rather general scheme of the instrument, consisting of two equal branches, which compare the input and the external reference to the internal clock. Each branch implements a classical *I*/*Q* detection in FPGA exploiting the stream of digitized data. In principle, the ADCs should operate close to the full speed because the lowest background is achieved in his condition.

The classical sampling theorem states that the input frequency must be lower than the Nyquist frequency, that is, $f_0 < f_N = f_{ck}/2$. However, the input frequency can be extended beyond f_N by under sampling the input signal. Numerous modern ADCs are intended for under sampling operation and for this purpose have an input-frequency range significantly wider than f_N. The input bands, called *Nyquist zones*, are selected by introducing an appropriate antialiasing filter at the input, which is a low-pass for the first zone, and bandpass for the subsequent zones. Of course, under sampling comes at the cost of higher background PM noise. In practice, the maximum frequency of the first Nyquist zone is of $0.8\,f_N$ because the antialiasing filter has a roll-off region before achieving the appropriate attenuation. A similar reasoning applies to the bandpass filter for the next Nyquist zone, which leaves a dark region between zones set by the roll-off region of the filters. This can be fixed by shifting the sampling frequency.

The NCO provides two orthogonal phases of a sinusoid at the same frequency of the input, or of the external reference. The digital down-conversion is free from the usual defects of analog *I*/*Q* detection, like orthogonality error and gain asymmetry. The digital low-pass filters are necessary to remove everything beyond f_N and to reduce the sampling rate to a value suitable for further processing. The maximum baseband frequency is of $0.8\,f_N$, again

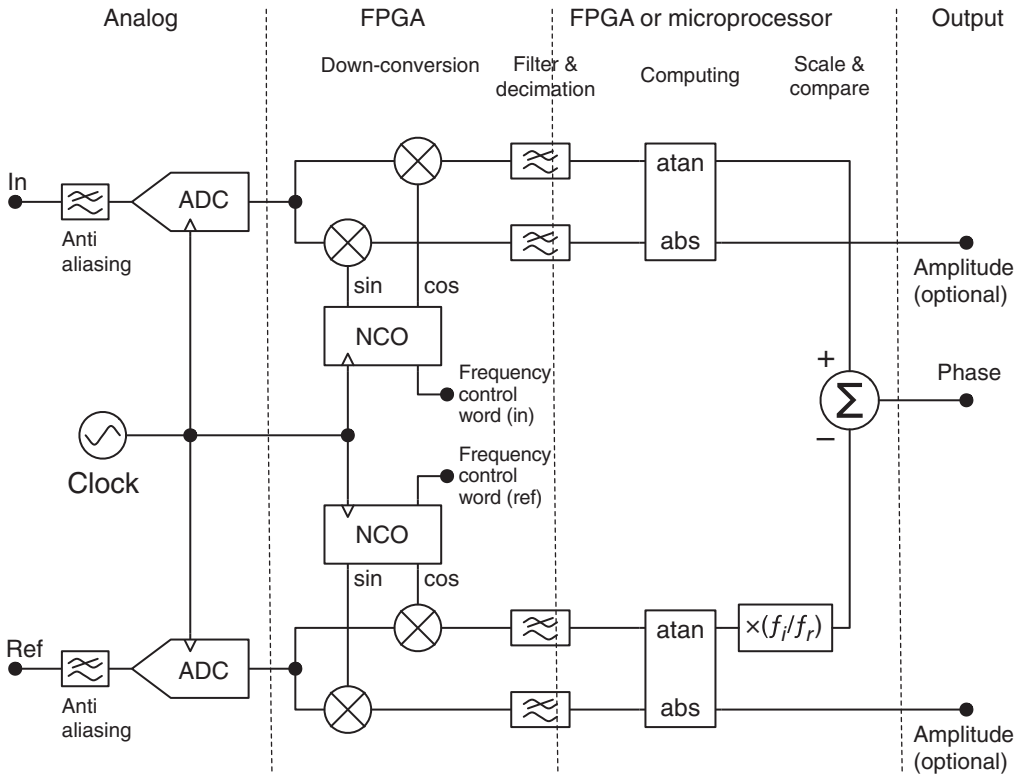


Figure 2-82 Basic scheme of the direct-digitization phase detector.

limited by the filter roll off. However, more stringent limitations may apply, due to the architecture of the instrument, and to the processing speed.

The CORDIC algorithm [92, 93] is most often used to calculate the phase. Interestingly, the digital technology enables the calculation of phase, and also of amplitude, with so high accuracy that it exceeds the general metrological performance of the instrument. The phase of the reference signal is scaled according to the frequency ratio f_i/f_r, so that it can be compared with the input phase. An alternate and elegant solution consists of converting the phase of both input and reference to phase-time. The two-branch configuration is necessary to bring the external reference (5–10–100 MHz, or arbitrary frequency) in the machine because the clock frequency takes fixed values determined by design considerations.

The configuration of Figure 2-82 has three relevant features, advantageous versus the DBM scheme

- It operates at arbitrary frequencies, with no need for the input and the external reference to be at the same frequency.
- The oscillator under test and the reference are free running, with no need of phase or frequency lock.
- Measuring a two-port device, there is no need for a line stretcher or for a variable phase shifter to set the quadrature condition.

These features enable the measurement of frequency dividers, multipliers, etc. in a straightforward way, without need of comparing two equal DUTs.

The main problem of the scheme shown is the background noise, generally limited by the noise of the ADCs. For reference, the noise of a selected 12–14 bit ADC at 100 MHz sampling frequency, operated at full range is

$$S_\theta(f) = 10^{-11}/f + 10^{-15}\ \text{rad}^2/\text{Hz} \tag{2-199}$$

that is, −110 dB rad^2 flicker, and −150 dB rad^2/Hz white floor. The flicker PM noise is a technical parameter of the ADC, as we have seen with amplifiers. The white noise results from the quantization noise and from the clock jitter

$$S_\theta(f) = S_{\theta,q} + S_{\theta,\text{ck}} \tag{2-200}$$

The quantization noise can be calculated as follows. At full range input $V_{\text{pp}} = V_{\text{FSR}}$, the carrier power on a 1-Ω resistance is

$$P = \frac{V_{\text{FSR}}^2}{8} \tag{2-201}$$

With n bits (ENOB), the quantization noise power is

$$\sigma^2 = \frac{V_{\text{LSB}}^2}{12} = \frac{V_{\text{FSR}}^2}{12 \times 2^{2n}} \tag{2-202}$$

uniformly distributed from 0 to the bandwidth $B = f_s/2$. Thus

$$N = \frac{\sigma^2}{B} = \frac{V_{\text{FSR}}^2}{6 \times 2^{2n} f_s} \tag{2-203}$$

The phase noise is given by $S_\theta(f) = N/P$, thus

$$S_{\theta,\,q} = \frac{4}{3 \times 2^{2n} f_s} \tag{2-204}$$

For example, a 14-bit ADC with ENOB = 12 bits, and sampling at 32 MS/s, has a quantization noise

$$S_{\theta,q} = \frac{4}{3 \times 2^{24} \times \left(32 \times 10^{6}\right)} = 2.5 \times 10^{-15}$$

that is, −146 dB rad^2/Hz, or −149 dBc/Hz.

The quantity $S_{\theta,\mathrm{ck}}$ is the clock-distribution PM noise, which is a technical parameter of the ADC. It hits on PM noise only, not on AM noise. For this reason, there is an asymmetry between AM and PM noise floor, and $S_{\theta,\mathrm{ck}}$ can be measured as

$$S_{\theta,\mathrm{ck}} = S_{\theta} - S_{\alpha}$$

Values of 0–3 dB and more are observed, depending on the operating conditions and on frequency. In fact, $S_{\theta,\mathrm{ck}}$ is of the time type, while $S_{\theta,q}$ is of the phase type.

Spurs and artifacts are another problem of digital systems. A first type of spurs results from sampling and digital synthesis. The sampling process produces

$$f_{\mathrm{spur}} = \mathcal{M} f_i - \mathcal{N} f_s \tag{2-205}$$

$$f_{\mathrm{spur}} = \mathcal{M} f_r - \mathcal{N} f_s \tag{2-206}$$

Additionally, the NCO produces spurs at multiples of the grand repetition rate (GRR)

$$f_{\mathrm{spur}} = \frac{f_{\mathrm{ck}}}{2^{n}} \tag{2-207}$$

where f_{ck} s the NCO clock frequency, and n is the number of bits of the NCO. However, the equivalent value of n to be used here can be smaller than the actual number of bits in the NCO register, depending on the frequency control word. Torosyan suggests that the equivalent n is the number of bits of the frequency control word from the MSB to the rightmost "1," which of course depends on the output frequency. For example, a 24-bit NCO has $n = 24$ bits when the control word is 01110101 11010111 11000001, and $n = 18$ bits when the control word is 01110101 11010111 11000000. Details are found in [94] and [95]. Distortion produces spurs at high frequencies, and aliasing brings them down to baseband. The digression we have seen with the DDS applies. At the state of the knowledge, the spurs cannot be eliminated, so they are generally removed from the displayed data in order to give the best representation of the DUT noise.

Because of the high noise of the ADCs, a cross-spectrum configuration is necessary to reduce the background noise of the instrument. Two equal blocks like Figure 2-82 are used instead of the DBM and measure simultaneously the quantity $\theta = \theta_i - \theta_r$. As a result of design choices, and probably also of marketing choices, commercial instruments often use a single input for the external reference. Thus, the noise of the external reference cannot be rejected.

A small number of digital instruments are commercially available, listed in Table 2-11. Some of them will be briefly discussed in the following pages.

The Microsemi Family of Phase Noise and Allan Deviation Tester

Microsemi (formerly Symmetricom) manufactures three instruments for the measurement of phase noise and Allan deviation. All these instruments are based on a scheme broadly similar to Figure 2-82. The background noise is rejected thanks to the cross-spectrum method. Input and reference are symmetrical, so they can be chosen independently in the range shown. Unfortunately, there is only one input for the external reference, thus it is impossible to reject the noise of the reference as we did in Figure 2-77.

Figure 2-83 shows the block diagram of the 5120A [96], and Table 2-12 shows the background noise. This instrument, probably the first implemented with fully digital architecture, has no capability to work beyond the first Nyquist zone, thus the input frequency is limited to 30 MHz.

Table 2-11 Digital phase-noise analyzers

Type and brand	Input frequency	Analysis frequency	Note
5125A Microsemi	1–400 MHz	100 μHz–1 MHz	Performs $L(f)$ and ADEV Discontinued, June 2018
5120A Microsemi	1–30 MHz	100 μHz–1 MHz	Performs $L(f)$ and ADEV
3120A Microsemi	0.5–30 MHz	1 Hz–100 kHz	Performs $L(f)$, AM noise, and ADEV Requires a host PC for all measurements Supersedes the Miles Design 5330A
PhaseStation 53100A Jackson Labs	1–200 MHz	1 mHz–1 MHz	Performs $L(f)$, AM noise, and ADEV Requires a host PC for all measurements
FSWP8 FSWP26 FSWP50 Rohde Schwarz	1 MHz–8/26.5/50 GHz	10 mHz–300 MHz	Performs $L(f)$ and AM noise Additional functions (VCO test, baseband, and microwave spectrum analyzer, pulsed signals, etc.), some optional

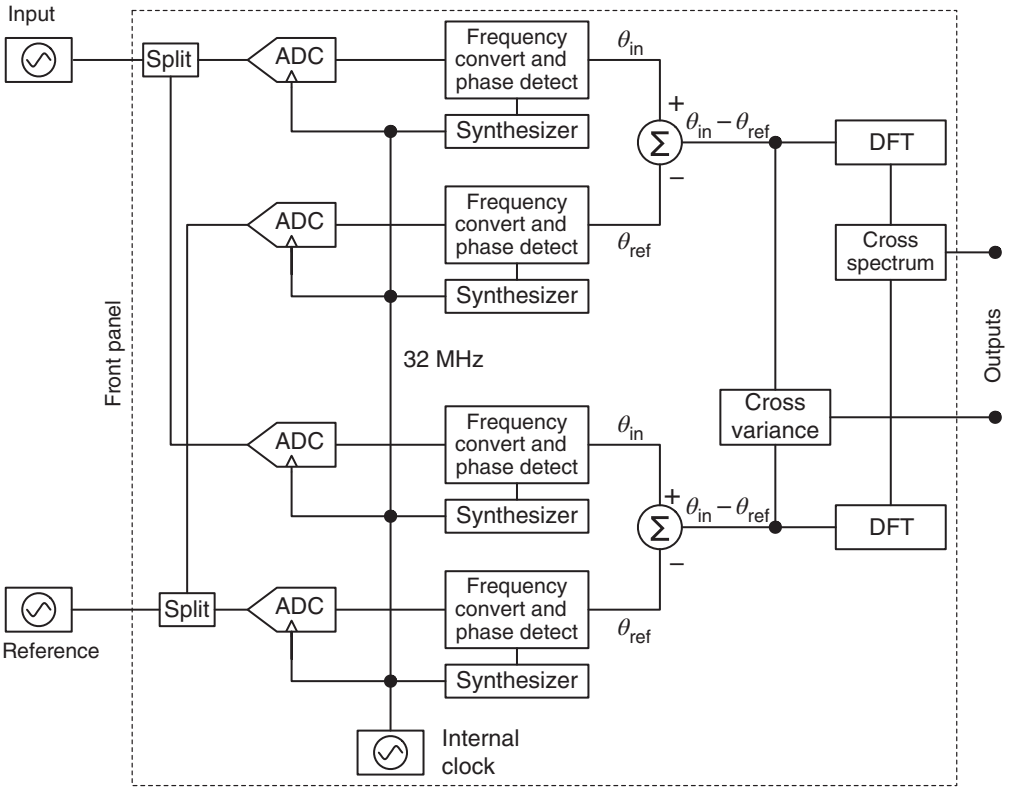


Figure 2-83 Block diagram of the Microsemi 5120A PM noise test set. Based on the documentation available from the Microsemi web site.

Table 2-12 Sensitivity of the Microsemi (Symmetricom) 5120A PM noise test set

Analysis frequency	$L(f)$ (dBc/Hz)	
	External ref	Internal ref
1 Hz	−145	−120
10 Hz	−155	—
100 Hz	−165	—
≥10 kHz	−175	−170

Data are from the documentation of the instrument.

The Microsemi 5125 is a more modern instrument, which works up to 400 MHz input frequency by exploiting several Nyquist zones. Depending on the input frequency, it switches the antialiasing input filter and optimizes the sampling frequency by choosing the value between 104 and 128 MHz. Of course, it uses the average cross-spectrum method to reduce the noise of the ADCs. The background noise is shown on Table 2-13. Unfortunately, the 5125A was discontinued in 2018.

The 3120A [97] is a low-cost solution, which derives from the TimePod designed by John Miles, and operates at the fixed sampling frequency of 78 MHz. Since the instrument is a sophisticated analog-to-digital interface, which relies on an external computer for control, data analysis, and display, it can have some additional features available as software update. The most interesting of them, according to our taste, is the measurement of AM noise.

Besides flexibility and sensitivity, the strength of the Microsemi family is the minimalist look of the front panel, however with a complete set of functions that focuses strictly on PM noise and AVAR analysis. A very small set of function keys enables to choose the quantity to display ($L(f)$, ADEV, phase versus time, etc.) and to set the vertical scale, while most parameters are set automatically. The capability to work with arbitrary input and reference frequencies makes these instruments great for the measurement of DDSs, DACs, frequency dividers, and frequency multipliers. With these instruments, we could measure the PM noise of some DACs over nine decades of Fourier frequency, observing flicker PM noise with a clean $1/f$ slope over 7.5 decades.

Three features we miss on the 5120A/5125A family. The first is the measurement of AM noise. All the building blocks are already there, thus we believe that this feature is only a matter of internal software and user interface. The second is the option to use two external references instead of sending the same reference to two input DACs. The obvious benefit is the rejection of the PM noise of the references. Based on the scheme of Figure 2-83, this feature is expected to cost only a minimum change in the internal software, and one additional connector on the front panel. The third feature is to allow some control on the software filters used to remove the spurs generated in the analog-to-digital conversions. In some cases, the user is interested in a noise component of the oscillator under test, which falls in the narrow spectral regions where the filters remove the spurs. When this happens, the results are difficult to understand. This is an advanced topic, which was discussed in three workshops on the cross-spectrum method [98–100] organized by one of us (ER).

Table 2-13 Sensitivity of the Microsemi (Symmetricom) 5125A PM noise test set

Offset frequency	Input frequency		
	10 MHz	100 MHz	400 MHz
1 Hz	−140	−120	−110
10 Hz	−150	−130	−120
100 Hz	−157	−140	−130
1 kHz	−162	−150	−140
10 kHz	−165	−160	−150
≥100 kHz	−165	−162	−155

Data are from the documentation of the instrument.

The Jackson Labs PhaseStation 53100A

The PhaseStation is a new instrument, whose production is starting at the time of writing (August 2019). Having no first-hand experience, this section is based on the material provided by the design team.

The architecture (Figure 2-84) derives from the TimePod. The core of the instrument an analog-to-digital interface with classical *I*/*Q* detection, which sends the baseband data to an external computer via upper side band (USB) interface for further processing. The bandwidth of the *I*/*Q* data is of the order of 1 MHz. Compared with the TimePod, there are significant differences. The passive power splitters (ferrite transformers) are replaced with active devices. The 1–200 MHz range is analyzed in four Nyquist zones, set by switching the antialiasing filters and the sampling frequency. The use of single-channel ADCs is an obvious choice for minimum crosstalk, because the crosstalk limits the noise rejection in the cross-spectrum analysis. The converters are now Analog Devices AD9265-125 because this component has a good thermal stability and reasonably low dissipation, in part related to the not-too-high clock frequency. These thermal characteristics help in achieving the thermal stability instrument, which is useful for the AVAR beyond 1 s measurement time.

The external computer runs the TimeLab app. TimeLab performs five conceptual tasks.

- Evaluation of amplitude, phase, and frequency from the *I*/*Q* data, with no loss of information. This feature is necessary for the data analysis down to low frequency.
- Decimation of the amplitude, phase, and frequency data for multiresolution analysis. In fact, the frequency span of AM and PM spectral analysis is of multiple decades, which must be segmented for proper operation of the FFT algorithm. Therefore, the sampling frequency has to be progressively scaled down going toward the lower decades.
- Calculation of the cross-spectrum, averaging on multiple acquisitions.
- Calculation of the ADEV, MDEV, Hadamard deviation (HDEV), and time deviation (TDEV).
- Plotting and storing the data.

The hardware of the PhaseStation contains a radical piece of innovation, however obvious it may seem: the four NCOs and *I*/*Q* detectors are completely separated and independent machines. The four ADC inputs are all accessible and can be fed by four signals of different amplitude and frequency. Albeit some limitations set by the software may apply, let us see some fancy and useful examples of what the hardware can do.

The first example is the PM-noise measurement of a 500 MHz oscillator, which is out of the range of the instrument. A frequency divider by four brings the frequency in the range ($500/4 = 125 < 200$ MHz), but does not solve the problem because the result is corrupted by the noise of the divider. The use of two dividers is expected to solve the problem. Removing some jumpers, we send the two "125 MHz" to channels 3 and 4, so that the cross-spectrum rejects the divider noise because the two dividers are statistically independent.

The second example is the stability measurement of a 5 MHz OCXO, where we expect an ADEV of less than 10^{-13} at $\tau = 1 \ldots 10$ s (we have seen an example of such oscillator in section "High-*Q* (Type B/D) Oscillators"). No OCXO is stable enough to be used as the reference, and we have no access to exotic and expensive sources, like the Hydrogen maser or the cryogenic sapphire oscillator (150–300 k$). The solution consists of using two reference OCXOs, sent to channels 1 and 2. The instability of such OCXOs can be a factor of 2–3 higher than that of the OCXO under test because their fluctuations are independent and can be rejected.

A third example is the PM-noise measurement of a low-noise 100 MHz OCXO prototype. For technical reasons the reference has to be at 100 MHz (the PM noise of the 5–10 MHz OCXO is too high), and we suspect that the measure is corrupted by RF leakage. Let us proceed with two 100-MHz OCXOs used as the reference as in the previous example, but we misalign them by random amounts (e.g., −170 Hz and +230 Hz, well in the typical range of mechanical tuning). In this way the leakage is either eliminated owing to the high *Q* of the resonators, or its effect occurs at clearly identified frequencies in the PM-noise spectrum.

The background noise of the PhaseStation is shown on Figure 2-85. This phase-noise spectrum is measured connecting one oscillator to the two inputs with the all jumpers inserted in the normal place, thus the four ADCs receive the same signal. Thus, the spectrum represents the PM noise of the machine, not including the noise of the oscillator. The latter is common mode and cancels. The FFT is calculated in segments broadly approximating the logarithmic resolution, which introduces a −5 dB/decade slope due to the reduction in the number of averages per

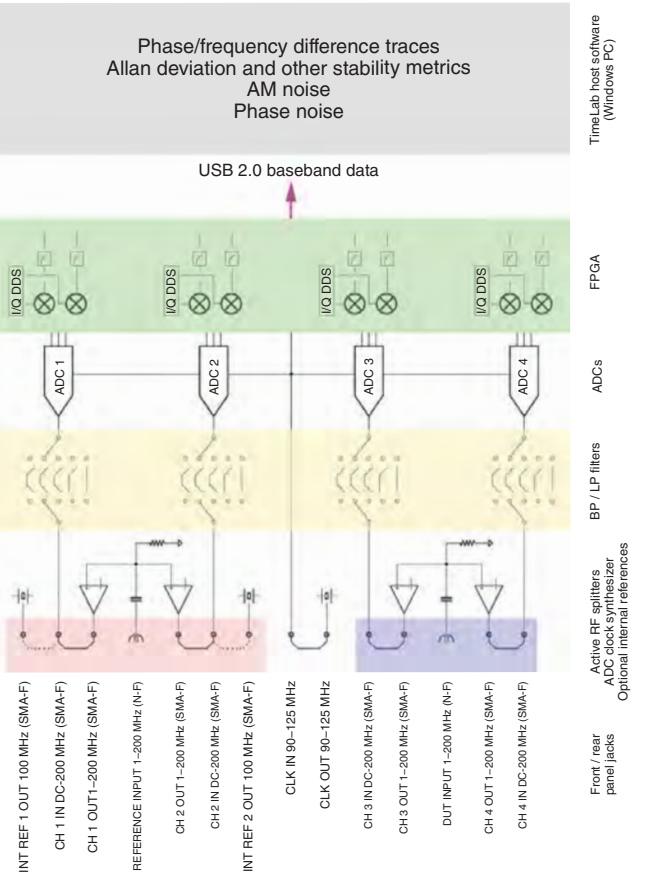
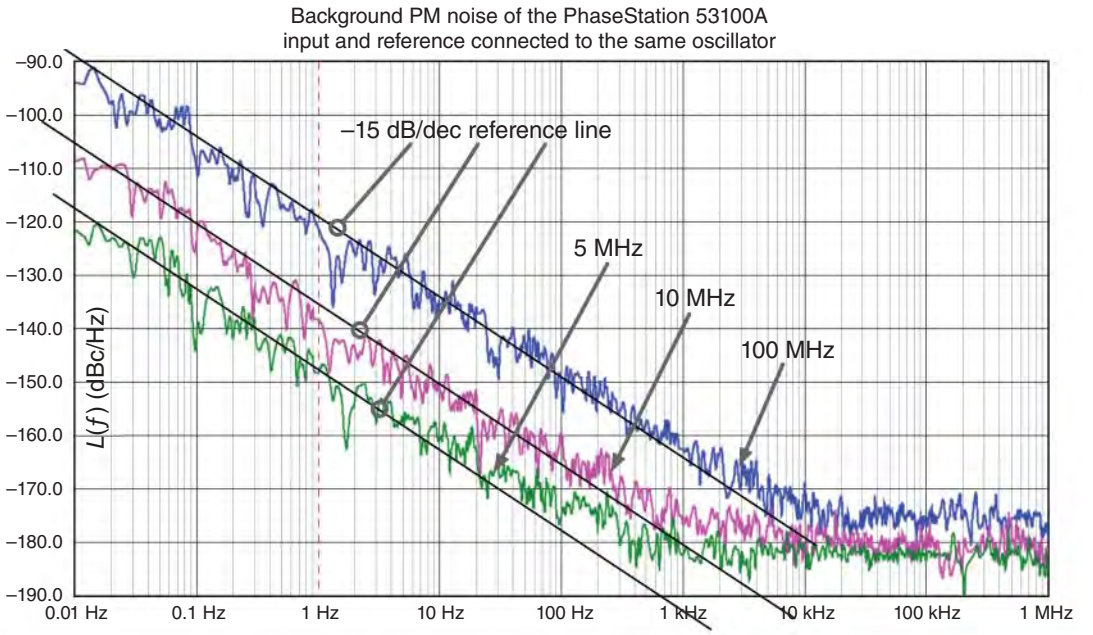


Figure 2-84 Block diagram of the PhaseStation 53100A, as it is expected to appear on the User Manual. Courtesy of Jackson Labs Technologies, Inc. and Miles Design LLC, used with permission.



Trace	Input Freq	Input amplitude	dBc/Hz at 1 Hz	Elapsed	Instrument
100 MHz residual floor	100.0 MHz	11 dBm	–121.1	58 min 49 s	PhaseStation 53100A
10 MHz residual floor	10.0 MHz	12 dBm	–138.2	33 min 5 s	PhaseStation 53100A
5 MHz residual floor	5.0 MHz	12 dBm	–148.2	8 h	PhaseStation 53100A

Figure 2-85 Background phase noise of the PhaseStation 53100A. Courtesy of Jackson Labs Technologies, Inc. and Miles Design LLC, used with permission. Graphical editing and comments are ours.

unit of time in the segments at low frequency. Accordingly, the flicker region is seen as a slope of −15 dB/decade, as expected. Because the spectrum is quite irregular in the flicker region, the frequency segments cannot be identified, and a longer measurement time may result in further reduction of the background noise. At 5 MHz the white noise appears flat and regular. This makes us think that m is large enough for the average to hit the ultimate limit set by the hardware. The same is less clear for the other plots, obtained with shorter measurement time.

The Rohde & Schwarz FSWP Family of Phase Noise Analyzers

The FSWP is a recent and highly innovative, sophisticated, and complex family of microwave phase noise analyzers working from 1 MHz up to 8/26.5/50 GHz, using the cross-spectrum technique. These instruments provide a variety of features, the AM and PM measurement of oscillators, the AM and PM measurement of two-port components via an internal synthesizer, the analysis of pulsed signals, the measurement of noise factor, and the test of VCOs, to mention the most important. Additionally, they can be used as a regular microwave spectrum analyzer, and also as a dual-channel FFT analyzer up to 10 MHz. This section is based on the product documentation available online, on the article [101], and on personal experience.

The scheme (Figure 2-86), however derived from the general principles stated earlier in this Chapter, looks rather different. The input signal is split into two channels, down-converted to an appropriate IF using two separate references, separate synthesizers, and separate mixers. The IF signal is digitized, at 100 MS/s on 16 bits, and processed by a sophisticated FPGA module (Figure 2-87).

The LO signals are derived from two different reference oscillators, one of which is phase-locked to the other with a bandwidth of less than 0.1 Hz. Consequently, the PM noise in the two channels de-correlates progressively starting from 0.1 Hz, and the full benefit of the cross-spectrum method is achieved one decade beyond, thus at

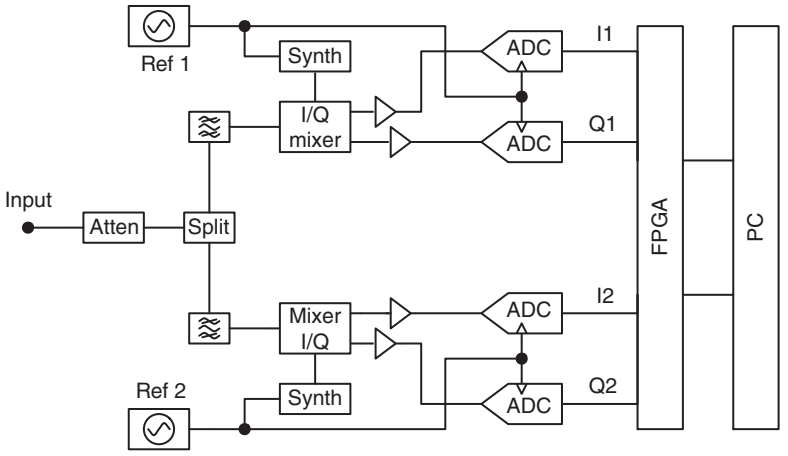


Figure 2-86 Basic scheme of the FSWP family of phase noise test sets. Based on the documentation available from the Rohde & Schwarz web site, and on [99].

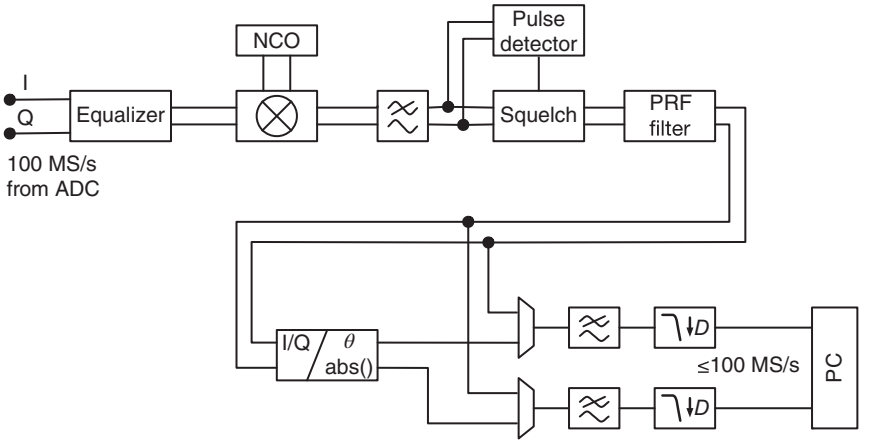


Figure 2-87 Detail of the FPGA processing inside the FSWP family of phase noise test sets. Based on the documentation available from the Rohde & Schwarz web site, and on [99].

$f \geq 1$ Hz. Two high-level *I*/*Q* mixers are used to down convert the input signal. The *I*/*Q* conversion is more complex that a regular conversion. The advantage is that it is possible to fix the asymmetry error and the quadrature errors of the mixer after digitizing the outputs, and in turn to attenuate the residual AM. With this trick, the receiver achieves a typical AM rejection of 40 dB, instead of the 20 dB usually found in regular mixers. The *I*/*Q* down-conversion does not increase the number of ADCs required with respect of the conceptual scheme of Figure 2-82. Thus, the cross-spectrum measurement is done with a total of four ADCs, two per channel.

The value of the IF frequency results from a technical tradeoff. Beyond 1 MHz Fourier frequency, the IF is set to zero (dc), where the mixer exhibits the highest gain and sensitivity. Beyond 1 MHz Fourier frequency, the IF is set to an appropriate value above 1 MHz. The reason for this choice is that the oscillator under test is free running, therefore a residual frequency offset Δf_0 is inevitable. At low Fourier frequencies, the harmonics of Δf_0 would fall in the analysis band, and produce artifacts. Beyond 1 MHz Fourier frequency, the zero IF is allowed because the harmonics of Δf_0 fall in a region where they do not interfere with the measurement.

The phase detection is based on the CORDIC algorithm. The aforementioned Δf_0 causes an increasing phase, which wraps at the limits of $\pm\pi$, incompatible with the FFT processing. This is fixed with a feed-forward structure that converts the PM signal into a non-wrapping FM signal. The 20 dB/decade slope introduced by the PM to FM conversion is later removed by a digital filter. The noise of the two references and of the two channels is rejected as explained in Section 2-5-2, using (2-195) as the estimator

$$\widehat{S}_\theta(f) = \frac{1}{K_\theta^2} \; |\langle S_{yx}(f) \rangle_m|$$

Accordingly, the single-channel noise is rejected by 5 $\log_{10}(m)$ dB. The frequency range is divided into half-decade segments, so that the ratio RBW/f between the RBW and the center frequency of each FFT bin is broadly constant. The sensitivity (background noise), versus carrier frequency f_0 and Fourier frequency f, is shown on Table 2-14 and Figure 2-88. The value shown includes the phase noise and the instability of the two internal reference oscillators. Table 2-15 shows the improvement, by the number of averaged spectra. For offset frequencies below 1 Hz, such improvement impact of correlation is limited by the coupling between the two reference oscillators. The improvement achievable in this case ranges from 15 dB (nominal) at 0.1 Hz to 3 dB (nominal) at 30 mHz. The low phase noise of the two internal synthesizers (Figure 2-89) is one of the main virtues of the FSWP because this is the reference where the correlation engine starts improving.

We have explained at the beginning of this chapter that $S_\theta(f)$, and equivalently $L(f)$ defined correctly as $L(f) = (1/2)S_\theta(f)$, give a valid measurement the phase noise even in the presence of large-angle and multiple-cycle swings, provided the phase detector work in this regime. This situation is often encountered at the highest microwave frequencies, where the phase noise gets inevitably large because of frequency-stability limitations. Figure 2-90 shows an example of measurement of 2, 20, and 40 GHz signals, where $L(f)$ greatly exceeds 0 dBc/Hz in the left-hand part of the spectrum.

2-5-4 Pitfalls and Limitations of the Cross-Spectrum Measurements

The capability of averaging out the single-channel noise is the strength and the weakness of the cross-spectrum method. Nowadays digital electronics provides so large memory and computing power for cheap, that it is easy to average over millions of cross-spectra. For example, the rejection of the single-channel noise given by (2-195) is of 30 dB with $m = 10^6$. This gives the *false impression* that it is sufficient to use larger m to increase the sensitivity of the instrument. Common sense suggests that at some point other limitations apply.

Another common belief is that the background noise results always in a positive bias to the result. In other words, most people believe that the plot of $S_\theta(f)$, or $L(f)$ seen on the display is always higher than the true phase

Table 2-14 Typical phase noise sensitivity with R&S®FSWP-B61 cross-correlation option

Start offset 1 Hz, correlation factor = 1, frequency reference internal, signal level ≥ 10 dBm

RF input frequency	Offset frequency from the carrier								
	1 Hz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz	30 MHz
1 MHz	−124	−142	−154	−172	−182	−182			
10 MHz	−121	−138	−148	−166	−176	−176	−176		
100 MHz	−101	−123	−146	−172	−176	−179	−181	−181	−181
1 GHz	−81	−103	−126	−156	−172	−179	−179	−179	−179
3 GHz	−71	−93	−116	−146	−162	−164	−169	−176	−176
7 GHz	−64	−86	−109	−139	−158	−159	−163	−172	−172
10 GHz	−61	−83	−106	−139	−158	−159	−163	−179	−181
16 GHz	−57	−79	−102	−135	−154	−155	−159	−176	−177
26 GHz	−53	−75	−98	−131	−150	−151	−155	−172	−173
50 GHz	−47	−69	−92	−125	−144	−145	−149	−166	−167

Data are provided by A. Roth, R&S.

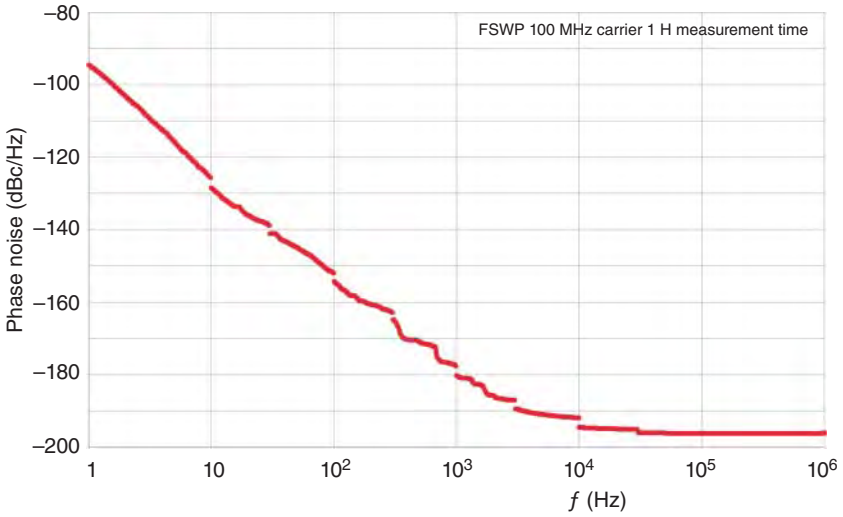


Figure 2-88 Background noise of the FSWP phase noise test set measured at 100 MHz carrier with 1 h averaging time. Reproduced with permission. © Synergy Microwave Corp.

Table 2-15 Improvement of phase sensitivity by number of correlations

Offset frequencies ≥ 1 Hz				
Correlations	10	100	1000	10 000
Improvement	5 dB	10 dB	15 dB	20 dB

Data are from the data sheet of the R&S®FSWP-B61 cross-correlation option.

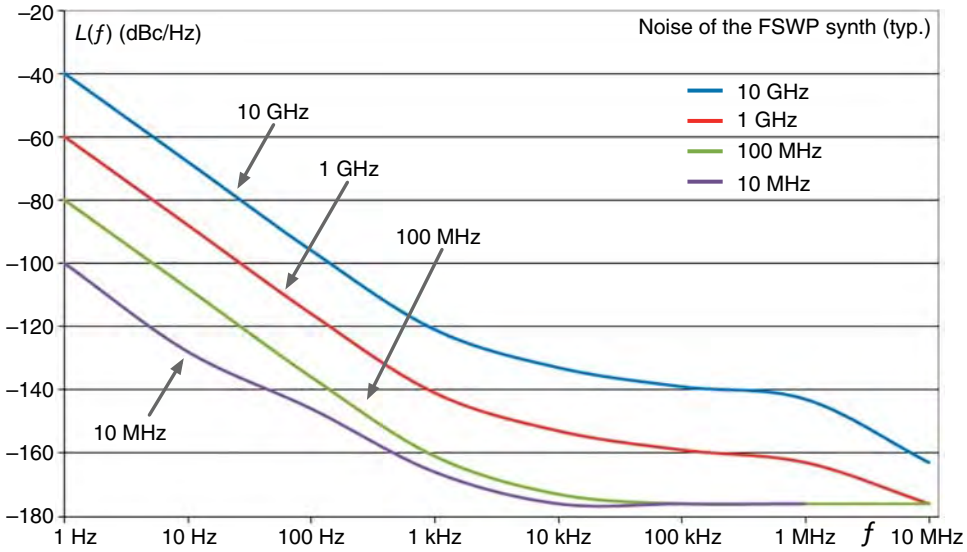


Figure 2-89 Typical phase noise of the FSWP internal synthesizer. Reproduced with permission. © Rohde & Schwarz.

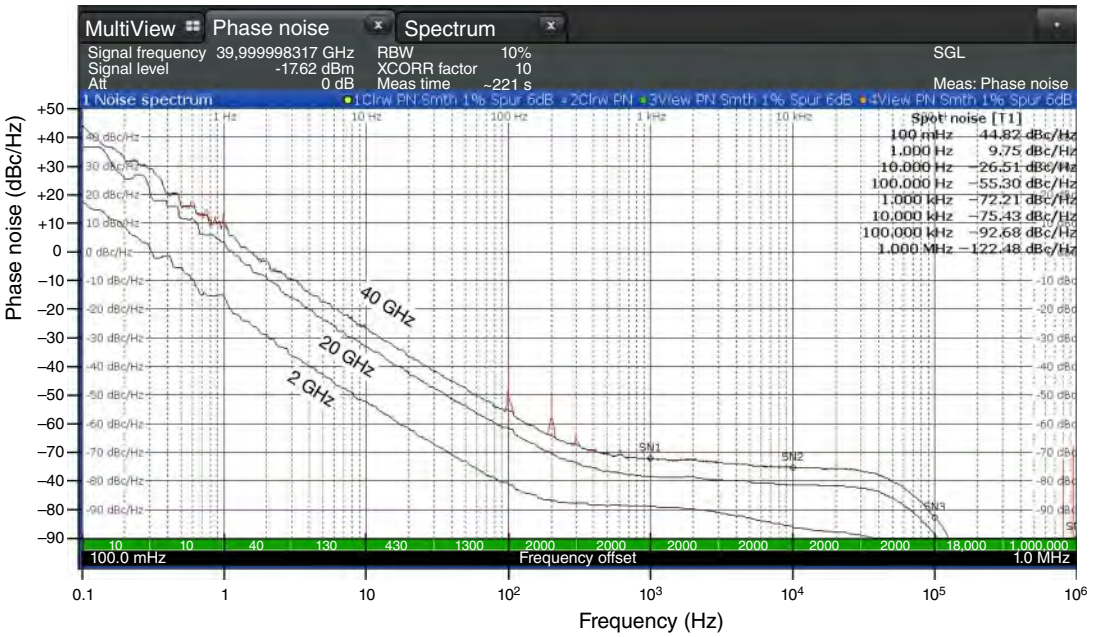


Figure 2-90 Phase noise of some microwave signals measured with an FSWP phase noise analyzer.

noise of the DUT. This is wrong in the case of cross-spectrum measurements. The instrument may *underestimate* the DUT noise.

We first show how correlated effects hit on the measurement, then we go through the concept of uncertainty, and we discuss the physical phenomena. Some of the effects are so subtle that they escaped from the attention of Manufacturers and Government Labs for a long time. Recently, the limitations of the cross-spectrum method were addressed in three dedicated workshops [98–100] organized by one of us (ER). Unlike in regular conferences, the material circulated only among the participants, and no proceedings were published. However, some relevant material is published in the Refs. [102–104].

The Effect of a Disturbing Signal

Let us introduce a disturbing signal represented as a phase $\xi(t)$, which affects the two channels with arbitrary coefficients ς_x and ς_y. Accordingly, we replace $x(t)$ and $y(t)$ with

$$x(t) = K_\theta \left[\theta(t) - \varphi(t) + \varsigma_x \xi(t)\right] \tag{2-208}$$

$$y(t) = K_\theta \left[\theta(t) - \psi(t) + \varsigma_y \xi(t)\right] \tag{2-209}$$

The quantities $\varsigma_x \xi(t)$ and $\varsigma_y \xi(t)$ can be any signal of unwanted origin impacting on the two channels. Since the amount of $\varsigma_x \xi(t)$ and $\varsigma_y \xi(t)$ is unknown, these signals fall in the category of uncertainties. The hypothesis that the two channels are equal has some practical limitations, which allow ς_x and ς_y to be different and to have different sign. For example, in a DBM the thermal coefficient comes from internal-diode mismatch. Thus, two nominally equal mixers will almost certainly have different thermal coefficient, and there is no reason for these coefficient to have the same sign. Likewise, the offset sensitivity to power.

Looking at the aforementioned definition of $x(t)$ and $y(t)$, all signals are *either* statistically independent or correlated, and *either* desired or unwanted. The following scheme accounts for all possible cases.

Correlation	Desired	Unwanted
Fully correlated	$\theta(t)$	$\xi(t)$
Fully independent	(None)	$\varphi(t)$ and $\psi(t)$

The Fourier transforms of $x(t)$ and $y(t)$ are

$$X = K_\theta\left(\Theta - \Phi + \varsigma_x \Xi\right) \tag{2-210}$$

$$Y = K_\theta\left(\Theta - \Psi + \varsigma_y \Xi\right) \tag{2-211}$$

and the cross PSD $S_{yx} = \frac{2}{T}\, YX^*$ becomes

$$S_{yx} = K_\theta^2 \frac{2}{T}\left(\Theta\Theta^* - \Theta\Phi^* + \varsigma_x \Theta\Xi^* - \Psi\Theta^* + \Psi\Phi^* - \varsigma_x \Psi\Xi^* + \varsigma_y \Xi\Theta^* - \varsigma_y \Xi\Phi^* + \varsigma\Xi\Xi^*\right) \tag{2-212}$$

where $\varsigma = \varsigma_x \varsigma_y$. When such signal is averaged on a large number of acquisitions, the cross terms $\Theta\Phi^*$, $\Theta\Xi^*$, $\Psi\Theta^*$, $\Psi\Phi^*$, $\Psi\Xi^*$, $\Xi\Theta^*$, and $\Xi\Phi^*$ null. There results

$$S_{yx} = K_\theta^2 \frac{2}{T}\left(\Theta\Theta^* + \varsigma\Xi\Xi^*\right) \tag{2-213}$$

The instrument readout is based on an estimator. For example, choosing the estimator (2-192), that is, $\widehat{S_{yx}} = \langle S_{yx}\rangle_m$, we get

$$\widehat{S_\theta} = \frac{2}{T}\langle\Theta\Theta^*\rangle_m + \frac{2}{T}\langle\Xi\Xi^*\rangle_m \tag{2-214}$$

and therefore

$$\widehat{S_\theta} = \langle S_\theta\rangle_m + \varsigma\langle S_\xi\rangle_m \tag{2-215}$$

The measure is affected by the error term

$$\Delta S_\theta = \varsigma S_\xi \tag{2-216}$$

Interestingly, $S_\theta(f)$ and $S_\xi(f)$ are both positive because $\Theta\Theta^* = |\Theta|^2$ and $\Xi\Xi^* = |\Xi|^2$, but the sign of ς is arbitrary. Therefore, the error ςS_ξ can be positive or negative. Measuring a very-low-noise DUT, or in other extreme cases, a negative error term may prevail at some frequencies, where $\widehat{S_\theta}(f) < 0$. Such outcome is a total nonsense. If we choose the absolute-value estimator (2-195), that is, $\widehat{S_{yx}} = |\langle S_{yx}\rangle_m|$, the result is always positive, with no warning.

Some Concepts Related to the Measurement Uncertainty

Whoever is faced to serious measurements of any physical quantity will at some point come across the concepts of uncertainty explained in the *International Vocabulary of Metrology* (VIM) [105], the *Guide to the Expression of Uncertainty in Measurement* (GUM) [106], and a bundle of related documents from the Joint Committee for Guides in Metrology (JCGM). All these documents are available free of charge from the BIPM web site www .bipm.org.

The approach described by the JCGM is formally correct, and also operational, and it is used routinely in the laboratories of primary metrology. Unfortunately, this culture is still absent in the practice of phase noise measurement, and learning it may require effort and patience. We will summarize the main points, and explain their implications on cross-spectrum measurements.

The components of measurement uncertainty are grouped into two categories, called Type A and Type B, depending on how the available data and information are combined to form the overall uncertainty.

The ***Type A evaluation*** of uncertainty is done by a statistical analysis of a time series of data obtained under defined measurement conditions.

The ***Type B evaluation*** of uncertainty is determined by means other than a Type A evaluation. The evaluation relies on authoritative published data, for example, from metrological institutes, on calibration certificates, on environmental parameters like temperature and humidity, on available knowledge of aging, drift, etc., and also on personal experience. Ensemble statistics applies to this type of evaluation, but the uncertainty cannot be reduced by increasing the number of measurements or by increasing the measurement time.

We have seen in section "The Rejection of the Background Noise" that the single-channel background noise can be reduced by increasing m. This type of noise is suited to the *Type A* analysis. Conversely, the signals $\varsigma_x\xi(t)$ and $\varsigma_y\xi(t)$ yield $\Delta S_\theta = \varsigma S_\xi$. This falls in the *Type B* evaluation, and the uncertainty cannot be reduced with statistical analysis on the time series.

A third concept found in the JCGM documents is the ***null measurement uncertainty***. This concept applies to the measurement of a quantity that cannot be negative (in some cases, cannot be positive), when the outcome of the measurement is close to zero. The null measurement uncertainty is the smallest signal that the instrument can detect with a given probability. If the error bar crosses zero, the instrument gives only the upper bound.

The reader may be used to a format like a measured value S_θ with uncertainty ΔS_θ, usually meaning that the "true value" of S_θ falls in the interval $S_\theta \pm \Delta S_\theta$ with a probability of 95%. What happens if the lower error bar $S_\theta - \Delta S_\theta$ crosses zero in a region of f? Of course, a negative PM noise is not allowed for physical reasons. In this case, the *null measurement uncertainty* applies. In proper metrological terms, the outcome of the experiment is that we have *measured zero phase noise*, with *zero uncertainty* equal to ΔS_θ. The nonsense associated to the negative outcomes of S_θ is no longer a problem.

In the case of the null measurement uncertainty, expressing the uncertainty in dB is often the result of a wrong approach.

After learning about the null measurement uncertainty, whenever we come across measurements taking large values of m, long measurement time, or too low phase noise spectra, we should try to understand better the uncertainty. For reference, a measurement time in excess of a few minutes starting at $f = 100$ Hz is probably the maximum that can be accepted without warning.

Thermal Energy in the Input Power Divider

A power divider is necessary to split the DUT signal into the two channels. In most cases, the power divider is a directional coupler internally terminated at one port (Figure 2-91). This choice provides low, uniform loss in a

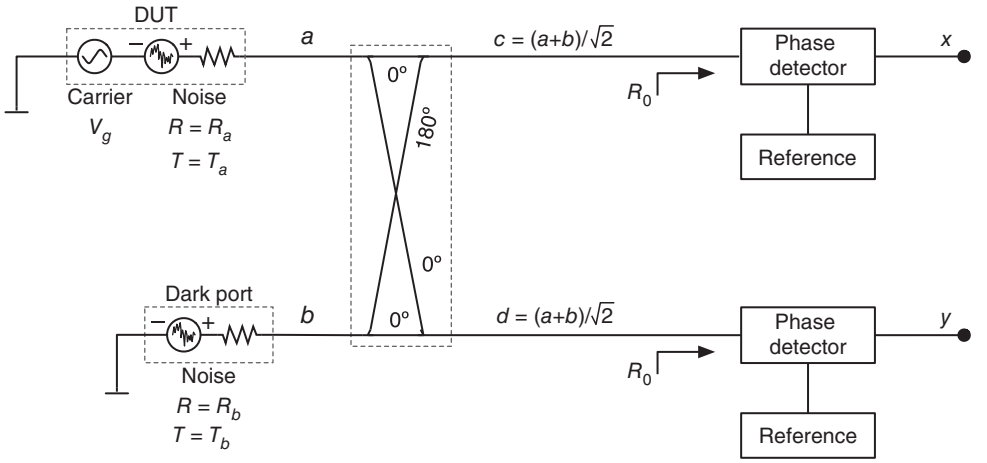


Figure 2-91 A loss-free power splitter is a directional coupler terminated to one port. To the extent of our digression about the thermal energy, the 90° version of the directional coupler is fully equivalent to that shown.

wide range of frequency, good isolation between the two outputs, and the good impedance matching at all ports. The Y resistive power splitter is seldom used because of the inherent 6-dB loss and poor isolation. However, the resistive power splitter is superior to the directional coupler in impedance matching and in loss flatness over extreme frequency range.

The problem is that the thermal energy kT inherent in the splitter's internal dissipation introduces a systematic error, or bias, in the spectrum. The same type of error is found in the directional coupler and in the Y resistive coupler, just with a different value of the bias. We explain what happens with the directional coupler, addressing the reader to the Refs. [102, 104] the details of both.

Let us recall that the random voltage e_n across a resistor R at temperature T has mean square value $\langle e_n^2 \rangle = 4kTR$ in 1 Hz bandwidth. We apply this signal to the inputs of a power splitter, as shown on Figure 2-91. The circuit is impedance matched to R_0 at all ports. We focus on the white PM noise region, where $S_\theta(f)$ is the lowest. The oscillator under test delivers a power P_0, and its output resistor R_a has the equivalent temperature T_a that results from $S_\theta = kT_a/P_0$. The dark port is terminated to the resistor R_b at the temperature T_b, the room temperature, or the temperature inside the instrument. The two signals at the power-splitter output are

$$c = \frac{V_g}{2\sqrt{2}} + \frac{e_a - e_b}{2\sqrt{2}} \tag{2-217}$$

$$d = \frac{V_g}{2\sqrt{2}} + \frac{e_a + e_b}{2\sqrt{2}} \tag{2-218}$$

The term "2" at the denominators is necessary because of impedance matching at the left-hand side of the coupler, and the term "$\sqrt{2}$" is due to the energy conservation in the loss-free power splitter. The negative sign, represented as a 180° phase shift on Figure 2-91, is necessary for energy conservation in a loss-free device. The explanation is found in most microwave textbooks, for example [107], in the section about the Scatter Matrix. Now we expand the cross PSD as we did earlier in this chapter:

$$S_{\mathrm{dc}} = \frac{2}{\mathcal{T}}\, YX^* = \frac{2}{\mathcal{T}}\, \frac{E_a - E_b}{2\sqrt{2}}\, \frac{E_a^* + E_b^*}{2\sqrt{2}} = \frac{2}{\mathcal{T}}\, \frac{E_a E_a^* + E_b E_b^*}{8} \tag{2-219}$$

Notice that the measurement time is temporarily denoted with $\mathcal{T}$ because here T is the temperature. Using the PSD of the thermal voltage $S_e = (2/\mathcal{T})\, EE^* = 4kTR_0$, we get

$$S_{\mathrm{dc}} = \frac{1}{2} k \left(T_a - T_b\right) R_0 \tag{2-220}$$

Interestingly, this technique has been known long time ago as a noise comparator tool [108], and in the early time of radio astronomy [109]. For phase noise measurements, the trivial factor ½ cancels with half the input power going in each output of the coupler. The relevant fact about (2-220) is that S_{dc} is proportional to $k(T_a - T_b)$, instead of kT_a. Obviously, the same happens with S_{yx} after phase detection. If this error is not accounted for, the instrument readout is

$$S_\theta = \frac{k\left(T_a - T_b\right)}{P_0} \qquad \text{instead of} \qquad S_\theta = \frac{kT_a}{P_0} \tag{2-221}$$

with a systematic error

$$\Delta S_\theta = -\frac{kT_b}{P_0} \tag{2-222}$$

Example 22 A 125-MHz OCXO has output power of 13 dBm, and the white PM noise floor displayed by the test set is of −186 dBc/Hz at $f \geq 10$ kHz. We evaluate the error due to the thermal energy in the input coupler at the internal instrument temperature of 40 °C.

First, we convert the data into proper SI units. Thus, the dark port temperature is $T_C = 313$ K, the carrier power is $P_0 = 20$ mW, and the white PM noise is $S_\theta = 5 \times 10^{-19}$ rad²/Hz. Using $S_\theta = kT_{\mathrm{read}}/P_0$, we get the equivalent temperature $T_{\mathrm{read}} = 724$ K associated to the noise floor, from the instrument readout. Since the measure is biased by the thermal energy as explained, the correct value is $T_{\mathrm{eq}} = T_{\mathrm{read}} + T_C = 1038$ K, hence

$S_\theta = kT_{eq}/P_0 = 7.16\times10^{-19}$ rad²/Hz. The bias error is $5\times10^{-19} - 7.16\times10^{-19} = -2.16\times10^{-19}$rad²/Hz, that is, −1.5 dB referred to the instrument readout.

Notice that the fractional error gets larger as the displayed floor approaches kT_C/P_0. With a displayed noise of −190 dBc/Hz and 13 dBm power, the error exceeds 3 dB. ■

The Effect of AM Noise

The measurement of phase noise should be independent of amplitude noise. However, the saturated mixer suffers from a residual sensitivity to AM noise through the sensitivity of the dc offset to power. In simple terms, when RF and LO are in quadrature, a residual dc offset is present at the IF output. Such offset is due to the imperfect balance of baluns and diodes, and it is affected by the power at both inputs. Hence, a power fluctuation (AM noise) ends into a fluctuation of the dc offset, which adds to the regular signal $K_\theta\theta$. This concept is described quantitatively by replacing $V = K_\theta\theta$ with

$$V = K_\theta\theta + K_{RF}\alpha_{RF} + K_{LO}\alpha_{LO} \tag{2-223}$$

where the AM noise of the RF and LO inputs appears explicitly. Of course, looking at the mixer output it is impossible to divide which part of V is due to phase noise and which is due to power fluctuations. Notice that K_{RF} and K_{LO} can be unpredictably positive or negative, and change with power and frequency.

Our treatise is limited to the DBM. The ADCs used in digital phase detectors suffer from AM noise leakage into the estimation of PM noise because of nonlinearity and other problems. This is an open issue, still not addressed in the technical literature.

When the mixer is saturated correctly, we expect a rejection of AM of the order of 20 dB. This means that the overall effect of K_θ/K_{LO} and K_θ/K_{RF} of the order of 10, a comfortable value in most cases, but poor or insufficient in other cases. For example, microwave-photonic devices often have larger $1/f$ AM noise than $1/f$ PM noise. Likewise, some quartz oscillators optimized for the lowest PM noise floor have larger AM noise.

In the cross-spectrum measurement, the effect of AM noise may lead to wrong or nonsensical results because the DUT AM noise is not rejected and becomes comparatively large after averaging out the instrument background noise. This idea is sketched on Figure 2-92. We apply the simple concept expressed by (2-223) to the scheme of Figure 2-77 (or equivalently, to Figure 2-79), adapting the notation. The two signals at the input of the FFT analyzer are

$$x = K_\theta(\theta - \varphi) + K_A\alpha_A + K_X\alpha \tag{2-224}$$

$$y = K_\theta(\theta - \psi) + K_B\alpha_B + K_Y\alpha \tag{2-225}$$

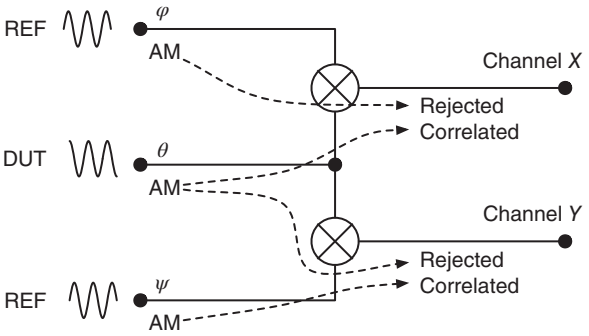


Figure 2-92 The effect of AM noise on a cross-spectrum PM noise test system. Reprinted from [1], CC BY Rubiola, and adapted to our notation.

where K_A and K_X are the offset sensitivity of the upper mixer to the amplitude α_A of the reference, and to the amplitude α of the DUT; K_B and K_Y are the same sensitivities for the lower mixer. Applying the statistical reasoning we are now familiar with, for large m we get

$$S_{yx}(f) = K_\theta^2 S_\theta(f) + K_Y K_X S_\alpha(f) \tag{2-226}$$

In fact, by inspection on the scheme, α, α_A, and α_B are statistically independent, and only α is common to the two channels. As before, θ, φ, and ψ are statistically independent, and only θ is common to the two channels. Consequently, the usual readout formula gives the wrong value

$$S_\theta(f) = \frac{1}{K_\theta^2} S_{yx}(f) \qquad \text{instead of} \qquad S_\theta(f) = \frac{1}{K_\theta^2} S_{yx}(f) - \frac{K_Y K_X}{K_\theta^2} S_\alpha(f) \tag{2-227}$$

The "error" term

$$\Delta S_\theta(f) = -\frac{K_Y K_X}{K_\theta^2} S_\alpha(f) \tag{2-228}$$

is actually a Type-B uncertainty because $S_\alpha(f)$, K_X, and K_Y are not known. One may object that the error can be easily fixed by measuring these quantities. At a closer sight, only $S_\alpha(f)$ can be measured in a simple way. Eventually, some commercial instruments already have the additional hardware for the measurement of AM noise. Conversely, K_X and K_Y depend on the carrier power and frequency, and on the experimental conditions. Thus, a factory characterization is not an option. The direct measurement is not simple because it requires an amplitude modulator in series to the DUT, and such modulator leaves a residual PM.

When the sensitivity to AM noise is really annoying, it is sometimes possible to find a working point where the effect of AM is mitigated [110, 111]. The two main options are

- Setting LO and RF slightly off the quadrature
- Inject a weak dc current at the mixer IF output.

In all cases, the working point must be found experimentally, by measuring the output in the presence of a small and controlled AM in the same conditions of the PM noise measurement. Experience indicates that an optimum point is more easily found in microwave mixers (microstrip balun) than in RF mixers (transformer balun) and that it may not exist at all.

In the end, fixing $\Delta S_\theta(f)$ makes the difference between an industrial measurement and a scientific experiment.

2-5-5 The Bridge (Interferometric) Method

The bridge method, shown on Figure 2-93, enables the measurement of two-port components with the lowest background noise, and the highest rejection of spurs and interferences.

After adjusting the phase and the amplitude in the bridge, the carrier is nulled in the $\Delta(t)$ signal. Thus, all the carrier power goes to $\Sigma(t)$ and is dissipated in the termination. However, the signal $\Delta(t)$ contains the noise sidebands of the DUT, after the obvious loss of the directional coupler. The noise sidebands are amplified and down-converted to dc by the mixer. The latter detects the DUT phase or amplitude, or any combination of, depending on the phase of the LO signal.

The appealing features of this method rely on the following concepts.

- The bridge is implemented with passive components (directional couplers, attenuators, and phase shifters), which exhibit low PM noise as compared with active components.
- The amplifier works in small-signal regime, where it is fully linear. We have seen earlier in this chapter that the $1/f$ PM noise originates by up-conversion of the near-dc flicker, thus the noise sidebands introduced

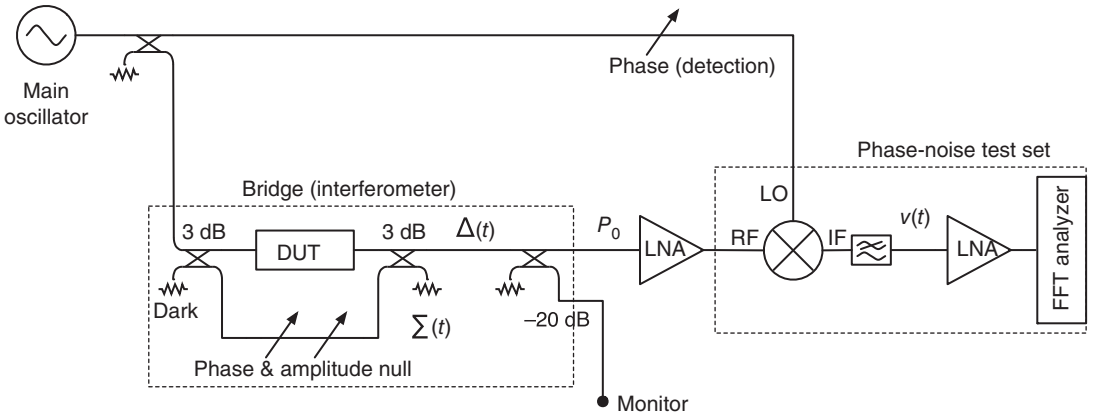


Figure 2-93 Scheme of the bridge phase measurement.

by the amplifier are approximately proportional the input power. In turn, PM noise is proportional to the sideband-to-carrier ratio. Consequently, with high carrier suppression the $1/f$ PM noise is virtually absent.

- Microwave amplification raises the useful signal (the DUT noise) from the background before down-conversion. This results in low interference from 50–60 Hz lines because the sensitivity of microwave circuits to low-frequency magnetic fields is very low. Additionally, amplification helps to achieve low residual white PM noise because the low-noise figure of the amplifier is more favorable than the relatively high conversion loss of a saturated mixer.
- Unlike the traditional systems described earlier, the mixer operates in linear regime, with the LO input saturated and $P_{RF} \ll P_{LO}$. Thus flicker comes only from the LO, and its impact is reduced proportionally to the microwave gain.

The method was first proposed by Sann in 1968 for the measurement of microwave amplifiers [112]. At that time, the bridge was followed immediately by the mixer, with no microwave amplification. The amplifier was introduced by Labaar in 1982, implementing an RF version of the method [113]. Further development had to wait until 1998, when this method was used extensively at the University of Western Australia and at the Laboratoire de Physique et Metrologie des Oscillateurs (now FEMTO-ST Institute) in France for rather extreme measurements [114, 115]. For example, the flicker frequency fluctuations of high-stability HF quartz resonators (σ_y as low as a few parts in 10^{-14}) can only be measured with this method [116]. A more sophisticated version uses the cross-spectrum method at the output of the bridge [117]. With this scheme, we could measure the $1/f$ phase noise of VHF power splitters (of the order of -170 dBc/Hz at $f = 1$ Hz, with 100 MHz carrier). The measurements reported are a challenge for scientists. By contrast, for less demanding applications, still out of reach for commercial instruments, the bridge method is not difficult for an experienced engineer or for a skilled amateur.

Phase-to-Voltage Gain and Background Noise

The phase-to-voltage gain K_θ is given by

$$K_\theta^2 = \frac{A^2 R_0 P_0}{\ell^2} \tag{2-229}$$

where A^2 is the power gain of the amplifier, R_0 is he characteristic impedance, P_0 is the DUT output power, and ℓ^2 is the SSB loss of the mixer. This is easily proved taking a signal of carrier power is P_0 with sinusoidal PM where each sideband has power P_s. Combining the two sidebands, the mean square PM is $\langle \varphi^2 \rangle = 2P_s/P_0$. Now we follow the signal path on Figure 2-93, from the DUT to the mixer. Neglecting the loss of the second coupler

for monitoring, one sideband has power $P_s/2$ at the amplifier input, $P_sA^2/2$ at the amplifier output, and $P_sA^2/2\ell^2$ at the mixer output. Combining the two sidebands at the mixer output, we get a power $2P_sA^2/\ell^2$, thus a mean square voltage $\langle V^2\rangle = 2\,P_sA^2R_0/\ell^2$. Finally, the gain results from $K_\theta^2 = \langle V^2\rangle/\langle\varphi^2\,\rangle$.

The background noise is

$$S_\theta(f) = 2\frac{FkT}{P_0} \qquad \text{background noise} \tag{2-230}$$

To prove this, we start from the random noise FkT at the amplifier input, hence A^2FkT at the amplifier output. The PSD at the mixer output is $2A^2FkT/\ell^2$, where the factor 2 comes from adding USB and LSB as statistically independent signals. Thus, the voltage PSD is $S_v = 2A^2FkTR/\ell^2$, and the background results from $S_\theta = S_v/K_\theta^2$.

Trivial losses in the bridge, and in the directional coupler used to monitor he carrier suppression, apply. They impact on K_θ and on the background noise.

Building Your Own System

This kind of system has to be assembled for specific DUT. The best approach consists of assembling the bridge first, and pre-adjusting it using a network analyzer. At microwave frequencies, the phase difference inside the bridge is difficult to predict, but setting it is rather simple because commercially available line stretchers enable precise phase adjustment in a comfortable range. For reference, a range of 100 ps is equivalent to one period at 10 GHz. Conversely, in the HF and VHF region the wavelength is too long for line stretchers, but the phase can be predicted based on the components. In this case, phase match is achieved by try-and-error with cables, and fine-tuned with a narrow-range variable phase shifter. Semirigid cables are preferred. Inspecting on the bridge with a network analyzer, we observe a dip at an unpredictable frequency determined by the delay difference between the two arms. The dip can be deepened by adjusting the attenuation and shifted to the frequency of interest by adjusting the delay. Because we need only the absolute value of the transfer function, the network analyzer can be replaced with a spectrum analyzer with tracking oscillator. Fairly high carrier suppression at the desired frequency is usually obtained after a small number of iterations. Fine tuning should be done with the complete system, with a spectrum analyzer at the monitor tap.

Best results are obtained with 20–45 dB RF/microwave gain. Higher gain results in higher K_θ and lower 50–60 Hz spurs, but it is more difficult to adjust the bridge for sufficiently low residual carrier at mixer input. For full linear operation, the total integrated noise should be kept at least 30 dB lower than the 1-dB compression point of the amplifier. Bandpass filtering at an intermediate stage of the amplifier may be useful.

The phase shifter at the LO input of the mixer must be set for the detection of PM noise. A low-index AM in the DUT path is the best choice. Driving this modulator with an audio-frequency tone, we adjust the phase shifter to null the corresponding spectral line on the FFT analyzer. A lock-in amplifier, if available, provides the best result.

Interestingly, the components in the dashed rectangle on the right-hand side of Figure 2-93 (mixer, dc LNA, and FFT analyzer) are the basic ingredients of a traditional single-channel saturated-mixer phase noise analyzer. If available, a commercial instrument should be used as a replacement, keeping the power at the RF port of the mixer low as described. More than the hardware, the reader will appreciate the computer interface, the software, and the ergonomics of the commercial instrument.

A Practical Example

Figure 2-94 shows an example intended for the measurement of phase noise in the 8–10 GHz band [115]. This implementation relates to our early experiments. At that time, we focused on the lowest background noise, rather than seeking for a decent compromise between complexity, manpower, and background noise. The bridge is implemented with a Wilkinson power splitter, a multi-turn variable attenuator, a micrometric line stretcher, and a 4-port hybrid junction. Unlike shown on Figure 2-93, the Σ port of the hybrid junction is re-used to pump the mixer, instead of dissipating the power in a termination. This choice was made before collecting extensive experience, and is not recommended. The problem is that adjusting the phase at the mixer LO input interacts with the bridge balance, and consequently multiple interactions are needed to null the carrier and to achieve proper detection of PM noise

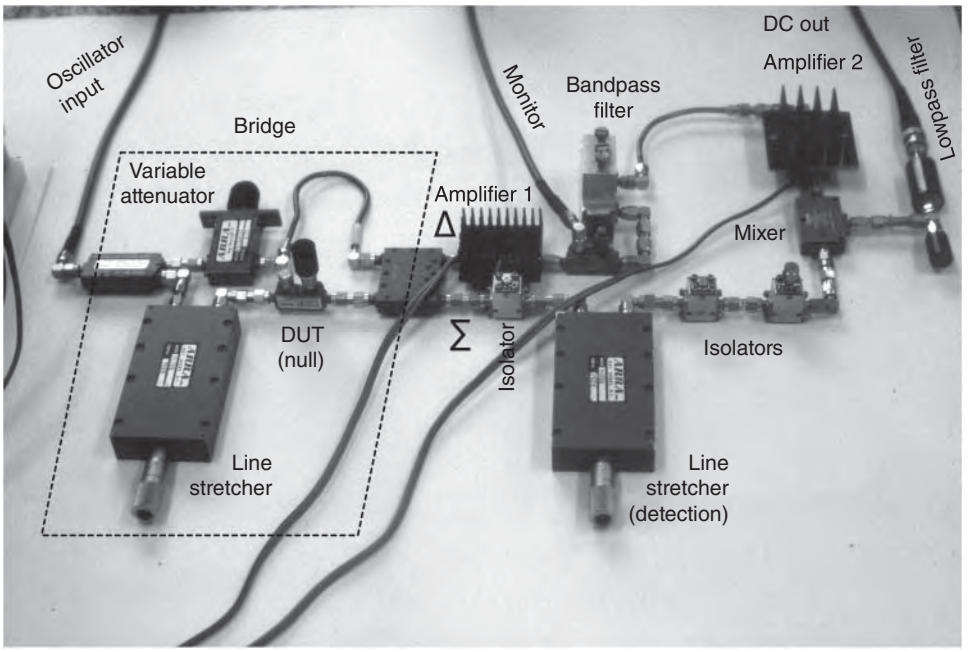


Figure 2-94 Example of implementation intended for 8–10 GHz operation. Reprinted from [115], with the permission of AIP Publishing. Comments are ours.

with minimum interference from AM noise. The amplifier has a gain of 42.5 dB in two stages, with a ≈30 MHz bandpass between the first and the second stage, and a noise figure of 2 dB. Isolators here and there proved to be useful. Accounting for gain and losses, we measured $K_\theta = 34.3$ dB rad^2/Hz, fairly close to the calculated value of 33.9 dB rad^2/Hz. The background noise (Figure 2-95), measured at +14 dBm DUT power with a null DUT in the bridge (short cable), is of −154 dB rad^2/Hz flicker extrapolated to 1 Hz, and −182 dB rad^2/Hz white.

2-5-6 Artifacts and Oddities Often Found in the Real World

We provide some typical examples of artifacts, spurs, and other problems often found in the measurement of phase noise.

Figure 2-96 shows an example of phase noise spectrum of a two port device, measured with a saturated mixer. Two nominally equal 2.3 GHz Al-N-Sapphire high-overtone bulk acoustic resonators (HBARs) are inserted, one in each arm of the mixer, because this configuration rejects the noise of the master oscillator. The background noise consists of flicker and white noise, −132 dB rad^2 and −162 dB rad^2/Hz respectively, thus

$$S_\theta(f) = 6.3 \times 10^{-14}/f + 6.3 \times 10^{-17} \text{ rad}^2/\text{Hz}$$

This is in agreement with earlier discussions and examples in this chapter. Let us look closer at this spectrum.

In the region A, we see that the fractional frequency resolution, that is, the number of points per decade, is significantly smaller than in the other regions. This is rather usual because the frequency resolution in this region is limited by the measurement time. In the region B, we see spurs from the power grid at 50 Hz and multiples (these experiments are done in Europe) on both DUT and background noise spectra. In most cases, these spurs are picked up at the input of the LNA that follows the mixer. As usual, odd-order harmonics (50, 150, 250 … Hz) are quite strong, while even-order harmonics (100, 200 … Hz) are barely noticeable. These spurs seem to end at 1 kHz, leaving room to a bump in the small region C. At closer sight, this bump is the envelope of the power-grid spurs.

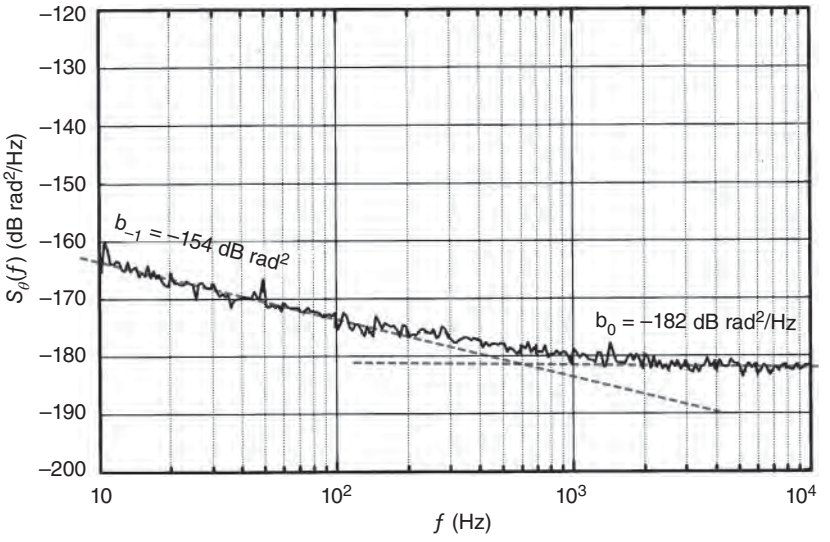


Figure 2-95 Background noise of the implementation shown on Figure 2-89, measured at +14 dBm DUT output power, and 9.13 GHz carrier frequency. Reprinted from [115], with the permission of AIP Publishing. Graphical editing and comments are ours.

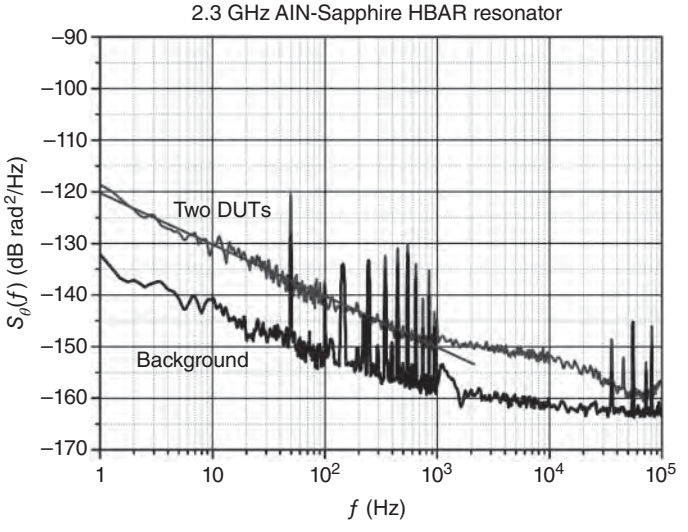


Figure 2-96 Example of phase noise spectrum (2.3 GHz AlN-Sapphire HBAR resonator). Reprinted from [118], with the permission of AIP Publishing. Comments are ours.

These spurs cannot be seen separately because the analyzer has not sufficient resolution in this region. Other spurs show up in the region D, between 35 kHz and 80 kHz. This type of spurs is usually due to switching power circuits in the experiment, or around in the room, conducted through cables. Common-mode filters (ferrites) often help to reduce these spurs.

Figure 2-97 shows the phase noise of a 100 MHz OCXO, measured with the cross-spectrum method using saturated DBM. At $f \leq 200$ Hz, the plot is quite smooth, and we identify clearly the $1/f^4$ and the $1/f^3$ regions, typical of

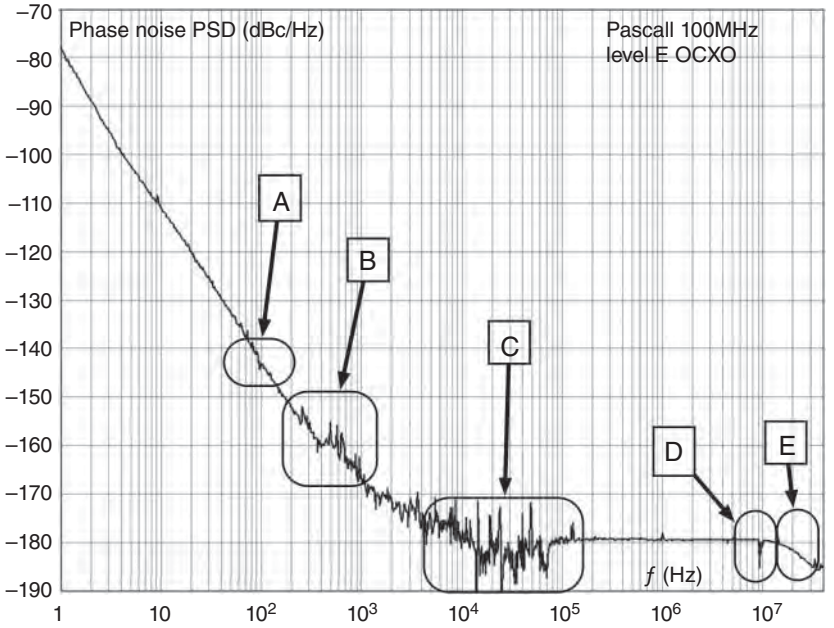


Figure 2-97 Phase noise spectrum of a 100 MHz oscillator. The spectrum is from DDC Electronics Ltd., a subsidiary of Data Device Corporation (DDC). Graphical editing and comments are ours.

quartz oscillators. The white PM noise is also well identified, in the region between 100 kHz and 10 MHz. By contrast, the spectrum is quite irregular between 200 Hz and 100 kHz. There is something wrong in the measurement, and we are unable to identify the $1/f$ or $1/f^2$ terms of the polynomial law we expect.

Starting from the left-hand side of the plot, we see a small discontinuity in A, at the transition between two decades. The most probable explanation is a change in the sampling frequency, affecting the white noise floor of the ADC. However small in this case, a signature like this is often seen in PM noise spectra. In B we see a bump, where the plot is quite irregular. The best interpretation we have is that the averaging process, necessary in the cross-spectrum method, is still not converging. This may also reveal B-type (systematic) uncertainty. The region C is weird because the plot is most irregular, and lower than the white PM floor. We have good reasons to believe that there is some anti-correlated process polluting the measure in this region, probably due to AM noise. The cross-spectrum may even be negative, and made positive by the absolute-value estimator. Of course, this region of the PM noise spectrum cannot be trusted. The region D contains an artifact, which appears as a notch. The narrowness recalls a spur, but spurs take the shape of a peak, not of a notch. The one and only credible explanation for this pattern is the presence of a spur with negative correlation in the two branches. However narrow and irrelevant it seems, this spur provides the evidence of anti-correlated artifacts, and reinforces the hypothesis that something similar happens in the region C. The region E is the signature of a low-pass filter. This pattern is the bandwidth limit of the system, which is in principle known, and should not be regarded as an artifact.

The last piece of our collection is the set of phase noise spectra shown on Figure 2-98. The device under test is a 1-GHz source having unusually high level of third harmonic distortion, −6.9 dBc. This source is measured with DBMs and the cross-spectrum method. The different curves are obtained by shifting the third harmonic from 0° to 360° in 30° steps. This plot is intended to alert the reader that large harmonic distortion and impedance mismatch should always be avoided in PM noise measurement. Why this large spread of values occurs, up to 12 dB at 10 kHz, and why the effect of the distortion is so irregular versus frequency, is not clear. The mixer is highly nonlinear, and for this reason it cannot be impedance matched at the inputs. Impedance mismatch and back reflections are not the same for first harmonic and for third harmonic. Furthermore, impedance mismatch affects the out-to-out isolation of the input power splitter, and in turn introduces coupling between the two channels of the instruments. Of course,

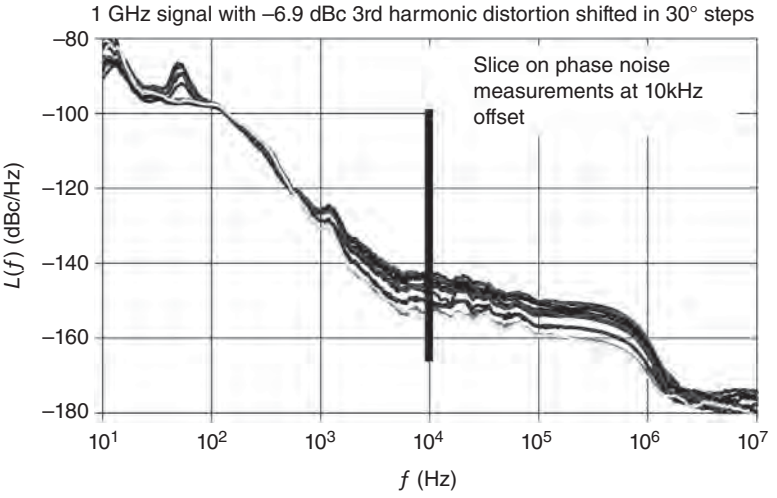


Figure 2-98 Phase noise of a 1-GHz oscillator having −6.9 dBc third harmonic distortion. The third harmonics is shifted from 0° to 360° in 30° steps. Reproduced with permission. © Synergy Microwave Corp.

none of these effects is under control, and erratic inconsistent results are around the corner. Experience suggests that a 3-dB attenuator inserted on each input connector of the mixer improves the impedance matching and helps significantly in avoiding inconsistencies. Introducing a low-pass filter at the input of the instrument is also a good idea when the source under test has significant harmonic distortion. In the laboratory practice, even a small set of filters covers most cases. A relatively new generation of filters is now commercially available, impedance matched also in the stopband. The use of these filters is highly recommended.

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3

SPECIAL LOOPS

3-1 INTRODUCTION

Chapters 1 and 2 have familiarized us with the phase-locked loop (PLL), the fundamental building block of all modern frequency synthesizers. We now understand the various types and orders of loops, the performance of the loop, and the evaluation of the loop. This chapter deals with special loops that are basically one-loop synthesizers. These systems can be combined, as we will see later, in multi-loop synthesizers, or some of them can be used as stand-alone systems.

The resolution or step size of the synthesizer, as we have learned, is equal to the reference frequency. There is a conflict between speed and step size, and this chapter deals with ways of minimizing this conflict. First, we will take a look at a system generating frequencies digitally with the help of logic circuitry and/or a computer. As today's technology provides us with fast microprocessors, these systems, using microprocessors and lookup tables, are capable of ultrafine-resolution synthesizers.

Then, we take a look at multi-loop sampler loops, where the various samplers are used to speed up the response of the very narrow loops commonly required in high-resolution systems. Loops with sequential phase shifters allow increased resolution at the expense of absolute accuracy.

Next, we will see how a delay line can be used to improve noise performance. This is almost the reverse technique of what we saw in Chapter 2, where the delay line was used to measure the phase noise.

Finally, we acquaint ourselves with the fractional *N* PLL, a spin-off of the *digiphase* system.

3-2 DIRECT DIGITAL SYNTHESIS TECHNIQUES

This chapter deals with modern digital synthesis concepts and implementations. Rapid advances in digital electronic circuitry, as well as digital-to-analog converters (DACs), have led to some very attractive solutions in frequency synthesis based on a totally digital approach.

Fractional *N* implementations are essentially PLL solutions to which digital logic has been added to perform certain useful functions. In particular, fractional *N* is an effective and economic way of increasing the frequency resolution of PLL frequency synthesis, while maintaining an acceptable level of spurious sidebands. The approach still suffers from some inherent constraints. The main ones are relatively long settling times, when the frequency is switched and limited phase modulation (PM) bandwidth. Recent trends toward the use of a spread spectrum in radar and communications are driving the need for faster switching and more PM of bandwidth in synthesizers.

We will examine the potential for increasing the speed of fractional *N* implementations before reviewing the field of direct digital synthesis (DDS). An interesting question arises: Will DDS implementations be limited to those applications requiring fast switching or will they find a natural place (dictated by economics) in general-purpose frequency synthesis? It is hoped that this chapter will provide significant insight into this matter, as we discuss DDS architectures and their advantages and drawbacks, modulation signal quality, and future prospects.

Particular attention is paid to the quality of the signal being synthesized. It is important that the minimum requirements for the application be met. Digital synthesis has traditionally suffered from high spurious sidebands, precluding its use in many radar and communications applications. It is important to set some realistic standards for spurious sideband levels and to evaluate the potential for various competing approaches.

Contributions to this chapter were made by Albert W. Kovalick and Roland Hassun, of Hewlett-Packard Co., Palo Alto, California.

3-2-1 A First Look at Fractional *N*

This topic is reviewed extensively in Section 3-3 and an analysis of spurious sideband levels is given in Refs. [1, 2]. The method has led to cost effective implementations for slow switching narrowband requirements. What are the prospects for improving the efficacy of fractional *N* and extending it to faster switching, wider band applications?

The bandwidth of the PLL in fractional *N* implementations is an important parameter in determining its ability to switch rapidly and to sustain a high rate of PM. An important variation on the traditional fractional *N* implementation is presented in [3].

Figure 3-1 shows a traditional fractional *N* configuration. The frequency divider modulus is set by the overflow indicator or the most significant bit (MSB) from the phase accumulator. This allows the creation of fractional divisors, as explained more fully in Section 3-3. Fractional divisors give rise to frequencies at the voltage-controlled oscillator (VCO) that are related to the reference frequency, at the phase detector, in a non-integral way. The spurious sidebands caused by the dithering of the divider are canceled by introducing appropriate PM through a DAC that is connected to the phase accumulator.

This configuration has been implemented in the past in a large number of Hewlett-Packard synthesizers and measuring instruments. The reference frequency has been 100 kHz and was more recently increased to 400 kHz.

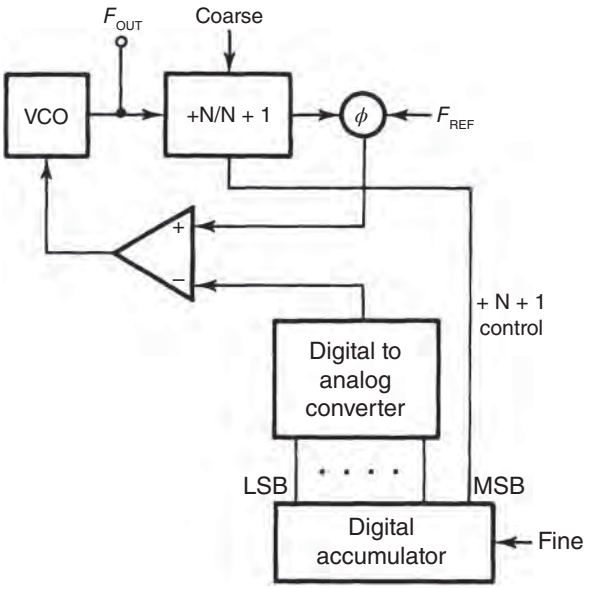


Figure 3-1 Traditional fractional *N* loop block diagram.

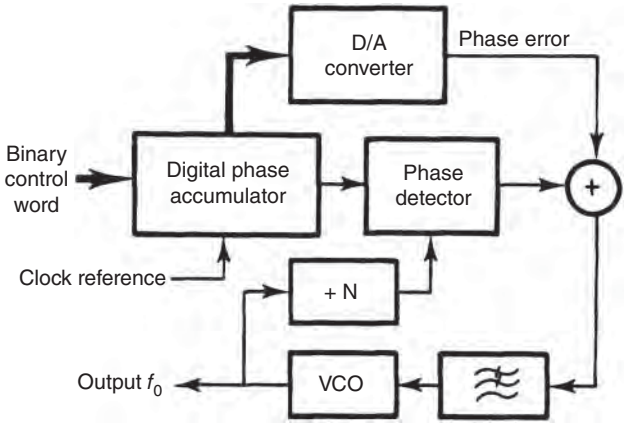


Figure 3-2 Simplified block diagram of configuration developed in Ref. [3].

A different fractional *N* configuration is shown in Figure 3-2. It was reported in 1976 [3]. In this approach, the reference frequency is the overflow or MSB output of the phase accumulator. This signal is not periodic when a non-integer value of binary control word is used. This corresponds to a fractional frequency condition in the traditional fractional *N* approach. The DAC is used for correction. The main differences between the two configurations are that Figure 3-2 uses a fixed divider in the feedback and Figure 3-1 uses the accumulator output as the reference. A higher VCO frequency is possible with the use of fixed dividers and a higher reference frequency is possible with the use of the accumulator, as shown.

It is interesting to note that fractional *N* benefits from the same advances in digital and conversion technologies have propelled DDS. The key factor is to increase the reference frequency to the phase detector. This has two important benefits: improvement in phase noise and the ability to extend the bandwidth of the PLL, which leads to faster switching.

After reading Section 3-2-2, it will become apparent that the method proposed in Ref. [3] is a combination of DDS, frequency multiplication, and filtering by means of a PLL. There is no evidence of this approach being implemented commercially to date.

3-2-2 Digital Waveform Synthesizers

This class of synthesizer uses sampled data methods to produce waveforms. Three methods will be discussed:

- Digital recursion oscillator
- Phase accumulator based
- Direct table lookup method

A block diagrams for all three processes is shown in Figures 3-3a–3-3c.

The digital hardware block provides a data stream of *K* bits per clock cycle for the DAC. Ideally, the DAC is a linear device with glitch-free performance. The practical limits of the DAC will be discussed later in this chapter. The DAC output is the desired signal plus replications of it around the clock frequency and all of the clock's harmonics. Also present in the DAC output signal is a small amount of quantization noise from the effects of finite math in the hardware block.

Fundamentals of the DDS Architecture

With the widespread use of digital techniques in instrumentation and communications systems, a digitally controlled method of generating multiple frequencies from a reference frequency source has evolved called

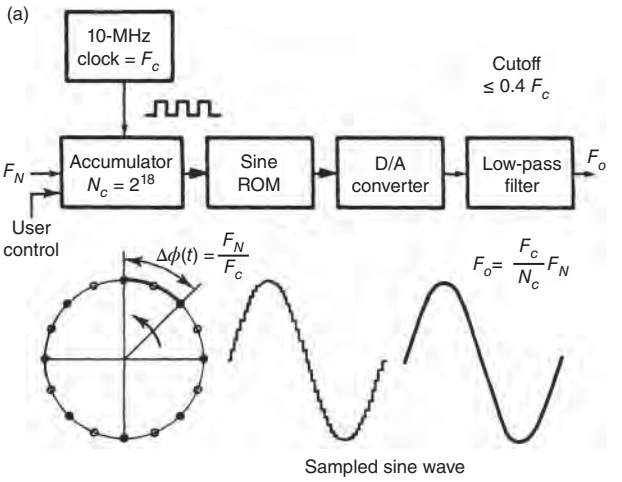


Figure 3-3a Direct digital frequency synthesizer.

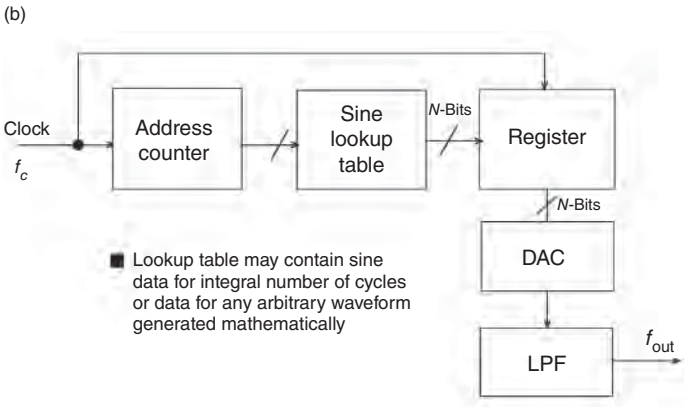


Figure 3-3b Fundamental direct digital synthesis system [[4], Analog Devices MT-085].

DDS. The basic architecture is shown in Figure 3-3a. In this simplified model, a stable clock drives a programmable-read-only-memory (PROM), which stores one or more integral number of cycles of a sinewave (or other arbitrary waveform, for that matter). As the address counter steps through each memory location, the corresponding digital amplitude of the signal at each location drives a DAC which in turn generates the analog output signal. The spectral purity of the final analog output signal is determined primarily by the DAC. The phase noise is basically that of the reference clock.

Because a DDS system is a sampled data system, all the issues involved in sampling must be considered: quantization noise, aliasing, filtering, etc. For instance, the higher-order harmonics of the DAC output frequencies fold back into the Nyquist bandwidth, making them unfilterable, whereas, the higher-order harmonics of the output of PLL-based synthesizers can be filtered. There are other considerations that will be discussed shortly.

A fundamental problem with this simple DDS system is that the final output frequency can be changed only by changing the reference clock frequency or by reprogramming the PROM, making it rather inflexible. A practical DDS system implements this basic function in a much more flexible and efficient manner using digital hardware called a numerically controlled oscillator (NCO). A block diagram of such a system is shown in Figure 3-3c.

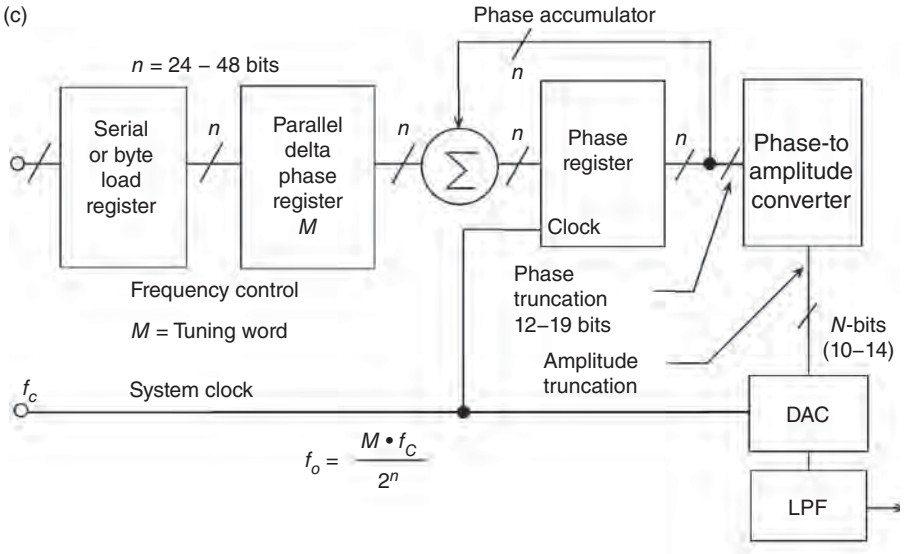


Figure 3-3c A very flexible DDS system [4].

The heart of the system is the *phase accumulator* whose contents are updated once each clock cycle. Each time the phase accumulator is updated, the digital number, M, stored in the *delta phase register* is added to the number in the phase accumulator register. Assume that the number in the delta phase register is 00 … 01 and that the initial contents of the phase accumulator are 00 … 00. The phase accumulator is updated by 00 … 01 on each clock cycle. If the accumulator is 32-bits wide, 232 clock cycles (over 4 billion) are required before the phase accumulator returns to 00 … 00, and the cycle repeats.

The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each address in the lookup table corresponds to a phase point on the sinewave from 0° to 360°. The lookup table contains the corresponding digital amplitude information for one complete cycle of a sinewave. (Actually, only data for 90° is required because the quadrature data is contained in the two MSBs.) The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC. This is shown graphically using the "phase wheel" in Figure 3-3d.

Consider the case for $n = 32$, and $M = 1$. The phase accumulator steps through each of 232 possible outputs before it overflows and restarts. The corresponding output sinewave frequency is equal to the input clock frequency divided by 232. If $M = 2$, then the phase accumulator register "rolls over" twice as fast, and the output frequency is doubled. This can be generalized as follows.

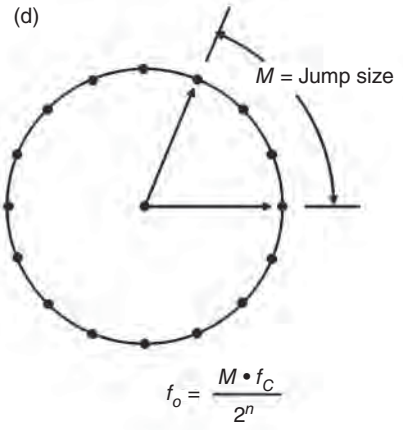
For an n-bit phase accumulator (n generally ranges from 24 to 32 in most DDS systems), there are $2n$ possible phase points. The digital word in the delta phase register, M, represents the amount the phase accumulator is incremented each clock cycle. If f_c is the clock frequency, then the frequency of the output sinewave is equal to

$$f_0 = \frac{M \cdot f_c}{2^2}$$

This equation is known as the DDS "tuning equation." Note that the frequency resolution of the system is equal to $f_c/2n$. For $n = 32$, the resolution is greater than one part in 4 billion! In a practical DDS system, all the bits out of the phase accumulator are not passed on to the lookup table, but are truncated, leaving only the first 13–15 MSBs. This reduces the size of the lookup table and does not affect the frequency resolution. The phase truncation only adds a small but acceptable amount of phase noise to the final output (see Figure 3-3e).

The resolution of the DAC is typically 2 to 4 bits less than the width of the lookup table. Even a perfect N-bit DAC will add quantization noise to the output. Figure 3-3e shows the calculated output spectrum for a 32-bit phase

(d)



n	Number of points = 2^n	
8	256	• 10*log(2^8) = 24 dB
12	4096	• 10*log(2^{12}) = 36 dB
16	65,536	• 10*log(2^{16}) = 48 dB
20	1,048,576	• 10*log(2^{20}) = 60 dB
24	16,777,216	• 10*log(2^{24}) = 72 dB
28	268,435,456	• 10*log(2^{28}) = 84 dB
32	4,294,967,296	• 10*log(2^{32}) = 96 dB
48	281,474,976,710,656	• 10*log(2^{48}) = 144 dB

Figure 3-3d Digital phase wheel [4].

(e)

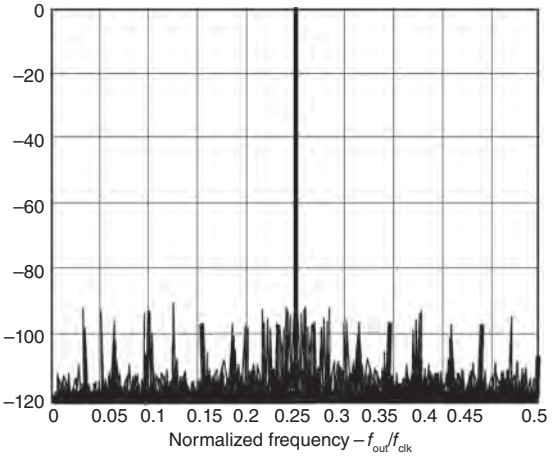


Figure 3-3e Calculated output spectrum shows 90 dB spurious free dynamic range (SFDR) [4].

accumulator, 15-bit phase truncation. Figure 3-3f shows the two-tone spectral plot. The value of *M* was chosen so that the output frequency was slightly offset from 0.25 times the clock frequency. Note that the spurs caused by the phase truncation and the finite DAC resolution are all at least 90 dB below the full-scale output. This performance far exceeds that of any commercially available 12-bit DAC and is adequate for most applications.

The basic DDS system described earlier is extremely flexible and has high resolution. The frequency can be changed instantaneously with no phase discontinuity by simply changing the contents of the *M*-register. However, practical DDS systems first require the execution of a serial or byte-loading sequence to get the new frequency word into an internal buffer register, which precedes the parallel-output *M*-register. This is done to minimize package pin count. After the new word is loaded into the buffer register, the parallel-output delta phase register is clocked, thereby changing all the bits simultaneously. The number of clock cycles required to load the delta-phase buffer

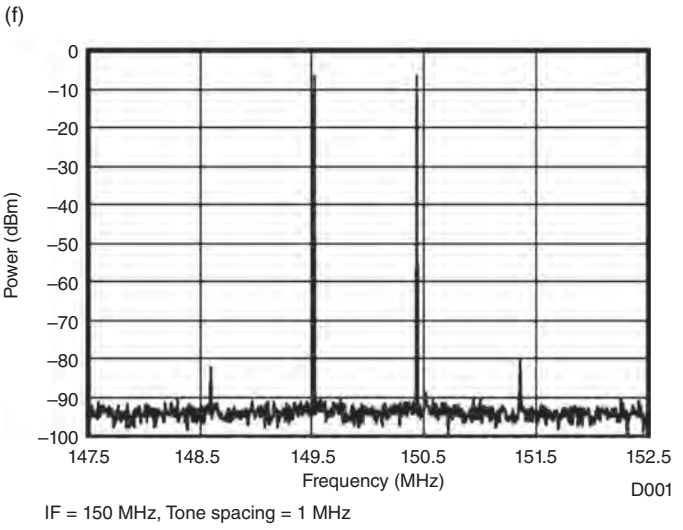


Figure 3-3f Two-tone spectral plot [4].

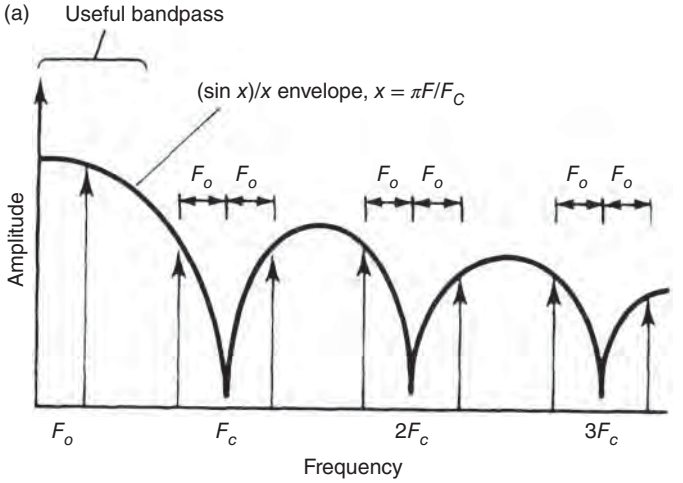


Figure 3-4a Ideal DAC output with F_o, a sampled-and-held sine wave, at its output. Notice the (sin *x*)/*x* envelope roll-off. As F_o moves up in frequency, an aliased component $F_c - F_o$ moves down into the passband. More details can be seen in Figure 3-4b.

register determines the maximum rate at which the output frequency can be changed. [[4] Based on Analog Devices MT-085 Tutorial; used with permission.]

Figures 3-4a and 3-4b show the frequency spectrum of an ideal DAC output with a digitally sampled sine-wave data stream at its input. Note that the desired signal, F_0 (a single line in the frequency domain), is replicated around all clock terms. Figure 3-5 shows the same signal in the time domain.

Note that the amplitude response of the DAC output (before filtering) follows a $\sin(x)/x$ response with zeros at the clock frequency and multiples thereof. The exact equation for the normalized output amplitude, $A(f_0)$ is given

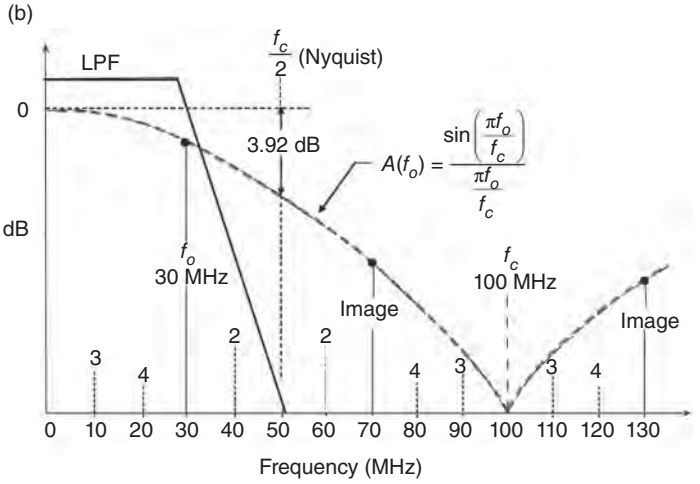


Figure 3-4b Aliasing in a DDS System [4].

by

$$A(f_0) = \frac{\sin\left(\frac{\pi f_0}{f_c}\right)}{\frac{\pi f_0}{f_c}}$$

where f_0 is the output frequency and f_c is the clock frequency.

This roll-off is because the DAC output is not a series of zero-width impulses (as in a perfect re-sampler), but a series of rectangular pulses whose width is equal to the reciprocal of the update rate. The amplitude of the $\sin(x)/x$ response is down 3.92 dB at the Nyquist frequency (1/2 the DAC update rate). In practice, the transfer function of the antialiasing filter can be designed to compensate for the $\sin(x)/x$ roll-off so that the overall frequency response is relatively flat up to the maximum output DAC frequency (generally 1/3 the updated rate).

Another important consideration is that, unlike a PLL-based system, the higher-order harmonics of the fundamental output frequency in a DDS system will fold back into the baseband because of aliasing. These harmonics cannot be removed by the antialiasing filter. For instance, if the clock frequency is 100 MHz, and the output frequency is 30 MHz, the second harmonic of the 30 MHz output signal appears at 60 MHz (out of band), but also at $100 - 60 = 40$ MHz (the aliased component). Similarly, the third harmonic (90 MHz) appears inband at $100 - 90 = 10$ MHz, and the fourth at $120 - 100$ MHz $= 20$ MHz. Higher-order harmonics also fall within the Nyquist bandwidth (dc to $f_c/2$). The location of the first four harmonics is shown in the figure.

Modern digital techniques allow high-order filter to be designed, to clean up the output down to −100 dB (see Figure 3-4c).

Figure 3-5 is typical of a single-tone DAC output, $F_o = F_{\text{clock}}/16$. After low-pass filtering; only the sine envelope is present. The low-pass filter (LPF) removes the sampling energy. Each amplitude step is held for a clock period.

The DAC performs a sample-and-hold operation as well as converting digital values to analog voltages. The sample occurs on each rising edge of the clock; the hold occurs during the clock period. The transfer function of a sample-and-hold operator is a $(\sin x)/x$ envelope response with linear phase. In this case, $x = (\pi F/F_{\text{clock}})$ (see Ref. [6]).

It should be noted that the sine function roll-off affects the passband flatness. A 2.4-dB drop should be expected at 40% of F_{clock}. See Ref. [7] for a solution to this roll-off problem that uses a method called *half-hold sampling*.

Referring again to Figure 3-3a, the output of the DAC is passed through an LPF. With proper attention to design, an LPF may be realized that has linear phase in a flat passband with width of 0.4 F_{clock}. With this design, the maximum available bandwidth is achieved. For example, with $F_{\text{clock}} = 125$ MHz a useful synthesized bandwidth of about 50 MHz is attained. The LPF output is the desired signal without any sampling artifacts. Viewing the LPF

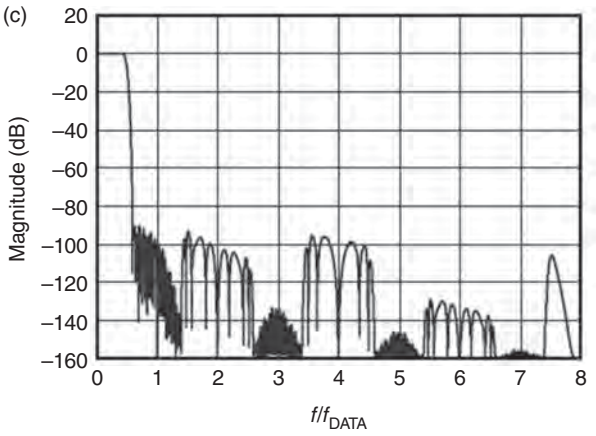


Figure 3-4c Composite frequency response of a high-order clean-up filter [5].

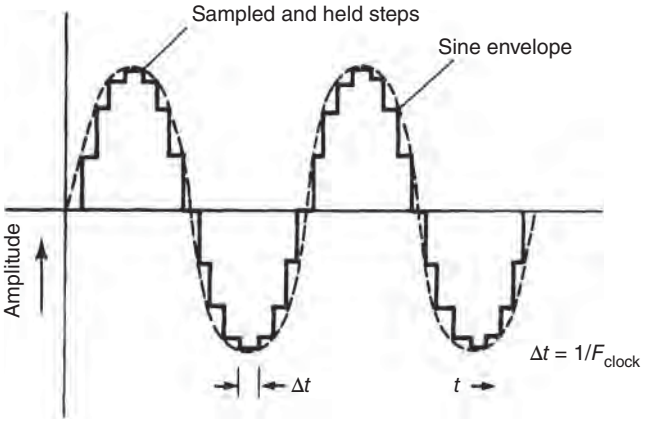


Figure 3-5 Samples/cycle sine wave.

strictly as a device to remove sampling energy, it is obvious why the output contains only the desired signal. It is also instructive to view the LPF from the time domain. From this point, the LPF may be seen as the perfect interpolator. It fills the space between time samples with a smooth curve to reconstruct perfectly the desired signal.

In general, the theory of sampled data is based on Nyquist's sampling theorem. For complete coverage, see Ref. [8].

Systems Concerns

If the desired signal, F_o (or the highest component in the desired signal if it is composed of many frequencies), is greater in frequency than $F_{\text{clock}}/2$, then an aliased version of it will appear in the passband at $F_{\text{clock}} - F_o$ (see Figure 3-4a). Some aliasing will always occur when non-band-limited signals, like square waves, triangular waves, or wideband FM waves, are desired. This is so because the desired signal has energy in it that extends beyond $F_{\text{clock}}/2$. Careful signal design will always guarantee that the aliasing contribution is below some specified minimum. In the case of a pure carrier, that is, a synthesizer without any modulation, aliasing is not a concern as long as $F_{\text{carrier}} < F_{\text{clock}}/2$.

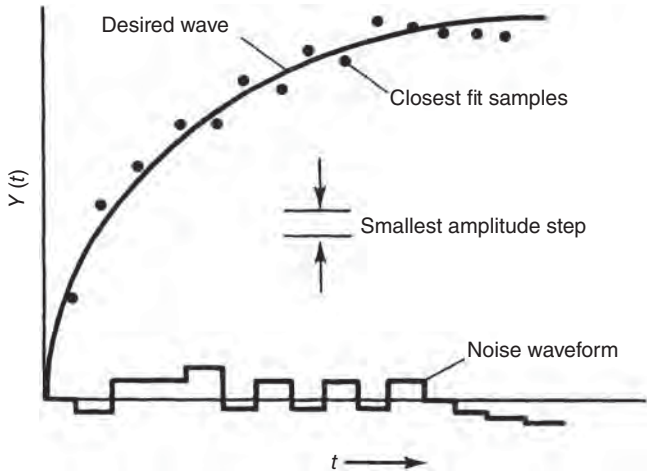


Figure 3-6 Example of amplitude quantization noise.

Another general concern is that of finite wordlength effects. The digital hardware block of Figure 3-3a outputs a K-bit value each clock cycle. This word is typically formed through either roundoff or truncation (roundoff with a bias). In any event, the desired signal must be quantized into at most 2^K amplitude levels. Commercial DACs are of fixed-point design ranging from about 6 to 20 bits.

The effect of truncation/roundoff error is quantization noise in the final output. Since each sample has an error ranging from −LSB/2 to +LSB/2, a sequence of noisy values is created. Figure 3-6 shows how amplitude quantization noise is formed. This noise may be made as small as desired by selecting the value K. It is a fact of life, however, that as K increases the DAC must be clocked slower. This is the big trade-off in designing digital synthesizers. Another strategy is to contour the effects of the noise. This may be accomplished with the aid of a dither source. Reference [9] gives a complete analysis of this scheme.

Now that the basics have been covered, let's investigate each of the three ways to generate synthesized waveforms. Hybrid combinations are possible too.

Digital Recursion Oscillator

This method is simple in concept. Build a second-order structure with its z transform poles on the unit circle. Ideally, this structure will oscillate at the location of the poles with unity amplitude. The following difference equation describes such a second-order structure:

$$Y(n) = Y(n-1)\,(2\cos\,\omega\,t) - Y(n-2) \tag{3-1}$$

with initial conditions

$$Y(n-2) = \cos\,\phi \tag{3-2}$$

$$Y(n-1) = \cos\,\phi - \omega t \tag{3-3}$$

where ϕ = starting phase

ω = desired radial frequency = $2\pi(F_{\text{desired}}/F_{\text{clock}})$

$n = N$h clock pulse

$Y(n-1)$ = the desired sinusoidal output

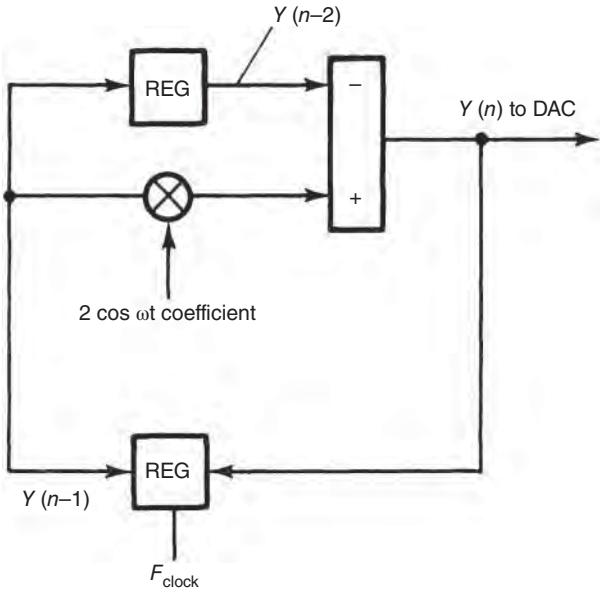


Figure 3-7 Hardware implementation required to compute *Y*(*n*). This hardware fills the hardware block in Figure 3-3a.

Figure 3-7 shows the hardware implementation required to compute $Y(n)$. This hardware fills the hardware block in Figure 3-3a.

The beauty of this realization is seen in its simplicity. For certain applications it performs as required. For example, for slow rate tones, which may be computed with floating point hardware (or computed in a software loop), this method is ideal. This method has been used successfully with a variety of digital signal processing (DSP) chips.

However, the realization of Figure 3-7 in fixed point hardware will not produce a pure sine wave. In most cases, due to recursion, limit-cycle noise will build up. The resulting signal-to-noise ratio (SNR) may be unacceptable. Limit cycles are the nemeses of DSP designs that use recursion. Typically, infinite impulse response (IIR) type filters exhibit limit-cycle noise (see Jackson's classic paper [10]). The resulting $Y(n)$ output will have small amounts of undesired amplitude modulation (AM) and PM due to noise contribution.

Modulating the recursion oscillator is a painful chore. If the synthesizer is to have FM or PM, the $2\cos\omega t$ coefficient must be computed for each modulation data point. For this reason, other structures should be considered when modulation is needed. Note, too, that the output frequency of $Y(n)$ is determined by the fixed coefficient term $2\cos\omega t$. Representing the coefficient with a finite wordlength means that the computed sinusoidal frequency may not be exactly what is required.

In general, this method is used infrequently for hardware synthesizers. It shows more promise as a method to generate sine waves using software. It is relatively inflexible regarding FM and PM modulation.

Phase Accumulator Method

This method relies on the direct computation of $Y(n) = \sin\omega t$. The computation requires a phase ramp ωt and phase to sine amplitude converter (PAC). Figure 3-8 shows a block diagram of the digital hardware block. In this case, the radial frequency ω is determined by

$$\omega = d\phi/dt$$

$$\text{where } dt = 1/F_{\text{clock}}$$

$$d\phi = \text{phase increment per clock cycle}$$

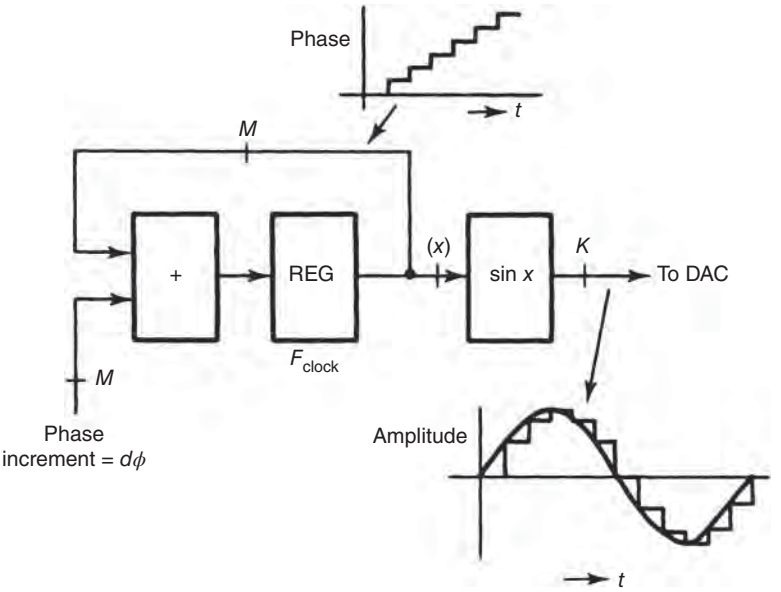


Figure 3-8 Phase accumulator-based, digital synthesizer hardware block.

The register output is a quantized version of the pure ramp, ωt. The adder is binary and modulo (2^M). By definition, $2^M = 2\pi$ radians. So, the adder overflow is exactly at the 2π position. Any overflow remainder phase will foldover into the next cycle of the output sinusoid. This overflow phase is exactly the required amount. For example, if the register is holding a value 350° at clock N and if $d\phi$ is 36° ($F_{sig} = F_{clock}/10$), the register will contain 350 + 36 Mod(360) degrees at clock $N + 1$. So, at clock $N + 1$, the register contains 26° as desired.

There are four main design variables that affect performance:

M	Phase increment bit width
L	Truncated phase for PAC
K	PAC output width (DAC bit width)
F_{clock}	Phase update rate

Let's consider the contribution of each term to the final output performance.

The phase accumulator width M determines the frequency resolution of the synthesizer; that is, $F_{res} = F_{clock}/2^M$. So, for $M = 30$ and $F_{clock} = 2^{27} = 134.27$ MHz, the resolution is exactly 0.125 Hz. Using a binary-coded decimal (BCD) adder instead of a binary adder would yield a different F_{res}. The advantage of a BCD adder is that F_{clock} may be a clean power of 10 (e.g., 100 MHz) and the resulting F_{res} is also a "nice" frequency. The choice of a BCD adder will cause the entire system design to be affected. When using a binary adder, the clock needs to be a power of 2 if F_{res} is to be a "nice" frequency. If F_{clock} is not a power of 2, then certain cardinal frequencies cannot by synthesized. For example, if $M = 30$ and $F_{clock} = 100$ MHz, then $F_{res} = 0.093132$ Hz. In this case, commonplace frequencies such as 1, 5, or 10 MHz cannot be generated exactly. As usual, the choice must be made depending on end requirements.

The bit width input to the PAC is L. Ideally, $L = M$. This is impractical if M is large. In practice, $L = K + 2$ is a good choice. Let us see why. The L bits represent the truncated phases of the carrier. However, phase truncation causes quantization noise. Also, amplitude quantization noise is present due to K, the DAC width, as mentioned earlier.

So, both K and L contribute to the total quantization noise. It would help us to know the SNR of each process so that the K/L trade-off will become clearer. First, let us derive the phase noise SNR assuming that $K = \infty$. In this way there is only phase truncation noise in the output.

$$Y(n) = \sin\ \omega t + N(t) \tag{3-4}$$

where $N(t)$ is the phase truncation noise. So

$$Y(n) = \sin(\omega t)\cos[N(t)] + \cos(\omega t)\sin[N(t)] \tag{3-5}$$

assuming $\cos[N(t)] = 1$ and $\sin[N(t)] = N(t)$ since $N(t) \ll 1$. Then

$$Y(n) = \sin(\omega t) + \cos(\omega t) \times N(t) \tag{3-6}$$

So

$$\text{SNR} = \frac{\text{power in } \sin(\omega t)}{\text{power in } \cos(\omega t) \times N(t)} \tag{3-7}$$

The normalized power in $\sin(\omega t)$ and $\cos(\omega t)$ is 0.5 W ($R_{\text{load}} = 1\ \Omega$). So

$$\text{SNR} = \frac{1}{\text{power in } N(t)}$$

Assuming a uniform distribution of error states in $N(t)$, the noise power can be derived to be

$$\text{Power}(N(t)) = (Q^2)/12 \tag{3-8}$$

where $Q = 2\pi/2^L$ is the smallest phase step size. So SNR $= 12/Q^2$ or SNRdB $= 10\ 1\text{og}(12/Q^2)$

$$\text{SNRdB} = 6.02L - 5.17\ \text{dB (phase quantization noise)} \tag{3-9}$$

The noise energy falls between 0 and F_{clock}. If we assume that only 40% of the noise bandwidth is preserved at the output of the LPF, then the SNR is enhanced by 4 dB. So, the $\text{SNRdB}_{\text{fil}} = 6.02L - 1.17$ dB. As an example, if $L = 12$, the $\text{SNRdB}_{\text{fil}} = 71.1$ dB.

For sufficiently long noise sequences, the spectral distribution is nearly evenly spread across the passband. The SNR value is the *total* power in all the noise spectra and *not* the height of the individual noise lines. If the noise sequence is very long, the noise will be distributed in many lines very close together and low in level. The sum of all the noise lines will always equal the SNR value.

Next, we derive the SNR for a finite DAC width, K. In this derivation we may assume that $L = \infty$ and only K is of finite length. For a sinusoid the quantized signal may be expressed as

$$Y(n) = \sin(\omega t) + N(t) \tag{3-10}$$

where $N(t)$ is the quantization noise due to amplitude truncation. The power in $\sin(\omega t)$ is 1/2 normalized into a 1-Ω resistor.

Now, assuming that the noise states in $N(t)$ are uniformly distributed, the noise power is [11]

$$\text{Power}\,(N(t)) = Q^2/12 \tag{3-11}$$

where $Q = 2/2^K$ is the smallest amplitude step size.

$$\text{SNR} = \frac{\text{power}(\sin(\omega t))}{\text{power}(N(t))} \tag{3-12}$$

$$\text{SNR} = 0.5/(4/2^{2K})/12 = (3/2)(2^{2K}) \tag{3-13}$$

$$\text{SNRdB} = 6.02K + 1.8 \text{ dB (amplitude quantization noise)} \tag{3-14}$$

Using the reasoning of the previous derivation, the SNR at the LPF output is enhanced by 4 dB. So, the final SNR is

$$\text{SNRdB}_{\text{fil}} = 6.02K + 4.8 \text{ dB} \tag{3-15}$$

So, for $K = 12$, the SNR is

$$\text{SNRdB}_{\text{fil}}(K = 12) = 78 \text{ dB} \tag{3-16}$$

Now if both K and L are of finite length, the total noise comes from a contribution from each noise term. A good design practice is to make one noise source subordinate. As may be seen from the SNR results, for equal values of K and L, the phase noise is about 7 dB higher than the amplitude noise. Typical DAC bit widths are 8, 10, and 12 bits for fast DACs. So, if $K = 12$, the phase noise would be subordinate if L were chosen to be 14. Also, a value of $L = 14$ is a reasonable choice for practical hardware design. A value of $L > 14$ would not improve system performance measurably since the amplitude quantization noise would always predominate. So, $L = K + 2$ is a reasonable design guideline.

Finally, the designer has a choice of F_{clock}. Due to the Nyquist sampling theorem and practical LPF filter design considerations, the maximum useful output frequency is 0.4 F_{clock}. The choice will often depend on the DAC speed and the rate at which one can economically generate the required sampled digital data.

Other Considerations

The design of the PAC poses some interesting design challenges. A brute force method uses a ROM (or RAM) with 2^L addresses and an output width of K bits. With $L = 14$, a $16K \times 12$ bit lookup ($K = 12$) table would be needed. An alternative to straight lookup is a structure that uses piecewise interpolation and quadrant logic to form the sin x output. One design uses 32 segments per quadrant to form the output. It uses only 640 bits of coefficient ROM (see Ref. [12]).

Piecewise methods are frequently based on the partitioning of the PAC phase term. One method splits the input phase into upper and lower pieces. Let us call these terms the bottom (B) and top (T). In this case,

$$\text{PAC input phase} = B + (2^J)T$$

where the top bits are shifted by J bits from the LSB position. So

$$\sin(\text{phase}) = \sin(B)\cos(2^J) + \sin(2^J T)\cos(B) \tag{3-17}$$

For small B,

$$\cos(B) = 1 \quad \text{and} \quad \sin(B) = B \tag{3-18}$$

So

$$\sin(\text{phase}) = B\cos(2^J T) + \sin(2^J T) \tag{3-19}$$

Let us look at an example with $K = 12$ bits. If the top term, T, is only 6 bits wide then the ROM storage needed is 128 words. This is so since you must store 654 points of sin $(2^J T)$ and 64 points of $\cos(2^J T)$. Also, B is 6 bits, so the required multiplication is 6×12. For $T = B - 6$ bits, the error using this approximation is less than 0.015%,

which is better than the required 12-bit resolution. Implementing this architecture yields good results when the synthesizer must be compact and composed of only a few very large scale integration (VLSI)-type chips.

Incidentally, the piecewise approximation method of sine generation surprisingly is spectrally clean. For only two segments from 0° to 90°, the total harmonic distortion is only 2.3% (see Refs. [13, 14]).

Another scheme to increase the sample rate is through parallelism. Using multiple channels of computation/PAC yields very favorable results [15].

The phase accumulator structure is flexible and lends itself to modification for implementing AM, FM, and PM. For an example of a commercial product, see the Hewlett-Packard 8791 synthesizer.

Modulation with the Phase Accumulator Synthesizer

Fortunately, this structure is amenable to AM, PM, and FM simultaneously and in real time. Let us investigate a structure with all three modulations. The expression that describes the filtered output is

$$Y(n) = \mathrm{Am}(t)\ \sin[\Sigma F_i(t) + \mathrm{Pm}(t)] \tag{3-20}$$

where $\mathrm{Am}(t)$ = desired AM
$\mathrm{Pm}(t)$ = desired PM
$\sum$ = phase accumulator operator (identical to discrete integrator)
$F_i(t)$ = instantaneous frequency

F_i is composed of a carrier term and any desired modulation. So

$$F_i(t) = F_{\text{carrier}} + \mathrm{Fm}(t) \tag{3-21}$$

The AM may be added with a real-time hardware multiplier after the PAC. The PM is easily implemented by adding the $\mathrm{Pm}(t)$ term to the phase accumulator register output. Likewise, the $F_i(t)$ term is formed with the inclusion of an FM adder block. The output of this adder is the input to the phase accumulator. So, with minor architectural adjustments, real-time modulation is available. The hardware must be designed so that a new point on $Y(n)$ is computed each clock cycle.

From where will the $\mathrm{Am}(t)$, $\mathrm{Pm}(t)$, and $\mathrm{Fm}(t)$ data come? In general, the data come from two sources. One is a real-time user-suppled input. Here, the user must be able to supply high-speed digital data to the synthesizer. Another source of modulation data is the RAM. In this case the AM, PM, and FM data are stored in different dedicated RAMs. The RAMs are addressed and the data are combined to produce $Y(n)$.

Adding modulation to the phase accumulator structure provides a very flexible synthesizer. For signals that may be described by their AM, PM, or FM components, this method provides a completely deterministic approach to signal synthesis.

RAM-Based Synthesis

The third architecture to be discussed is RAM-based synthesis. Figure 3-9 shows a block diagram of such a synthesizer. The major blocks are:

- Fast static RAM for waveform storage
- Memory address sequencer
- DAC/LPF subassembly (as in Figure 3-3a)
- Waveform development station
- Waveform development station

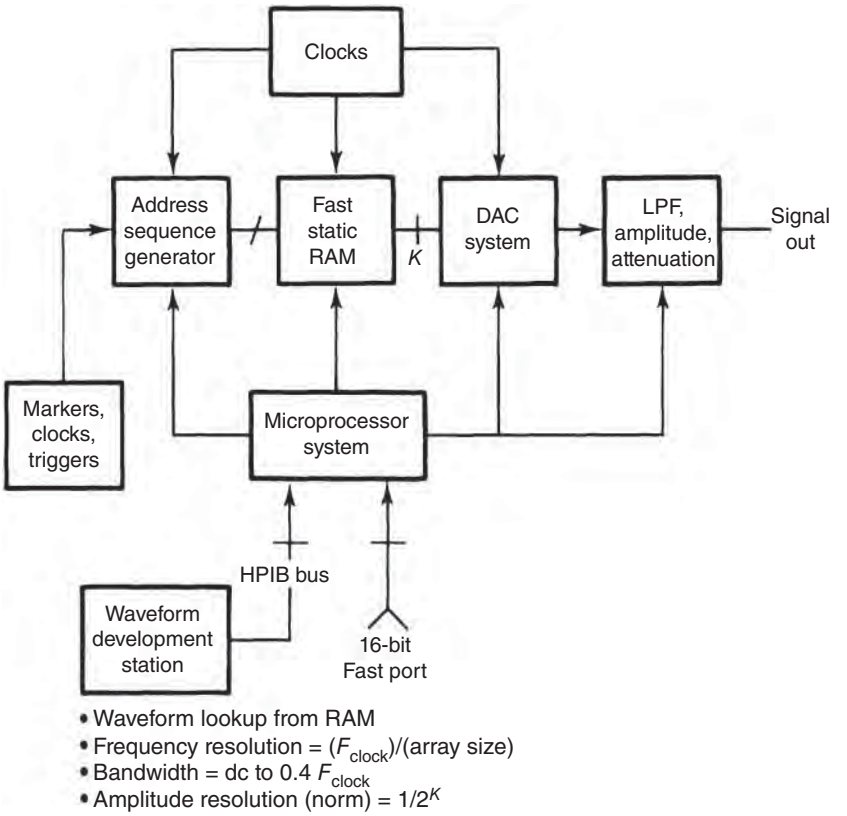


Figure 3-9 Block diagram of a RAM-based synthesizer.

In essence, the method uses a sampled image of the desired final waveform. This image is stored in the waveform RAM. The sequencer scans the desired waveform samples and these samples, in turn, are sent to the DAC for conversion to the analog domain.

The theory of sampled data referred to and discussed in the section on the Phase Accumulator Method is the basis for understanding this method as well.

Before the components are discussed, let us consider an analogy to the RAM-based synthesizer, namely, the compact disc (CD) player.

The CD player has a rotating platter that contains the music as sampled data. In the RAM-based synthesizer, a memory contains the sampled data to be played back.

In a CD player, the data are sampled at a 44.1-kHz rate. In a memory-based synthesizer, the rate is selected by the user and is usually much higher.

CD players feature two 16-bit DACs, one per channel. The synthesizer has one DAC per output channel as well. For speed reasons, the DAC width is more likely to be in the 8- to 12-bit range.

Most CD players have a sequencer that lets you play back the tracks in any order. A memory-based synthesizer has a memory sequencer that allows playing back the "tracks" in any order.

An example of a RAM-based synthesizer is the HP8770A waveform synthesizer (see Ref. [7]).

Components in a RAM-Based Synthesizer

The RAM stores the sampled data. It is a key component. The RAM must be clocked at F_{clock}, so its access time will be a limiting factor in useful bandwidth. A successful way to increase the RAM output data rate is to form a

parallel RAM array and multiplex the individual RAMs to form a very high speed data path. The size of the RAM is a major design variable, as we will see.

The RAM is useless unless it is addressed by a sequencer. In the simplest sense, a sequencer scans a wave segment of data in the RAM. A wave segment is defined as a block of sampled waveform data. The simplest sequencer is an address counter with stop and start address parameters. A more sophisticated sequencer has a mini-program that directs the addressing. In this type, several levels of looping are allowed. In many waveforms there are wave segments that are repeated often. These segments may be scanned by the sequencer to form a complex final output. In effect, the sequencer allows for the RAM data to be compressed.

A simple example will shed some light on the method. It is desired to synthesize an NSTC color bar test pattern. This pattern has redundancy. Many horizontal lines have the same color. A brute force RAM lookup would require about 525,000 points with a 14,317,816-Hz clock (this is exactly four times the color burst frequency). Careful analysis of the signal reveals that there are many wave segments that repeat. By loading the RAM with only the nonredundant data, the RAM size need only be 20K addresses. So, the sequencer has given us a data compression ratio of about 26:1.

Another component in a RAM-based synthesizer is the waveform development environment. The user needs a methodology to compose the desired waveform. For simple waves, like pure carriers or simple AM carriers, the user may choose to write dedicated software routines to calculate the sampled data. A more general solution is to provide the user with a waveform design language. Using this language, the user may create any waveform within the limits of creativity, the synthesizer's bandwidth, and amplitude resolution. An example of this is the waveform generation language (WGL) that is a companion product of the HP8770A waveform synthesizer [5].

Understanding the Design Variables in RAM Synthesis

The output spectral purity is limited by the DAC bit width. For random data, the SNR of the system is nearly $6.02K$. However, since the DAC is nonideal (it glitches), the actual limiting performance may come from the DAC produced spurious energy. Another source of spurious spectra comes from the digital data feed-through. The output picks up crosstalk from the digital section of the system.

Besides the value of K, another design parameter is the size of the memory. Even though the RAM can contain the image of any arbitrary time, finite length, or waveform, insight into the method is gained by investigating the simple case of producing a single-frequency tone. Let F_{low} be the lowest frequency that may be produced. Thus

$$F_{\text{low}} = \frac{F_{\text{clock}}}{\text{sequence length}} \tag{3-22}$$

This tone would be a single cycle in Q points, assuming that the sequence length is Q points. In general, the single-tone output may be described by

$$Y(n) = \sin[2\pi(P/Q)/I + P_{\text{off}}] \tag{3-23}$$

where P_{off} = any desired phase offset
I = Ith point in the sequence
P = number of cycles of the desired tone in Q points
Q = number of sampled data points for P cycles

Both P and Q must be integers. Also,

$$F_{\text{out}} = F_{\text{clock}}(P/Q)\ \text{Hz} \tag{3-24}$$

Note that $2\pi(P/Q)I$ is just another equivalent way to write ωt with $\omega = 2\pi(P/Q)$ and I the time index. The Q points of $Y(n)$ are stored in the RAM.

So, if F_{clock} is 100 MHz and a 28-MHz tone is desired, then $F_{\text{out}} = (100\,\text{MHz})\,(P/Q)$. By inspection with $P = 7$ and $Q = 25$, an F_{out} of 28 MHz would be realized. This tone would only have 25/7 or about 3.5 points per cycle.

This is fine as long as the LPF is designed to remove the sampling energy at frequencies greater than and equal to 100 − 28 MHz.

By adjusting P/Q, many different tones may be generated. For this example, the user observes an analog output with the tone at exactly 28 MHz (actually the only error would be due to F_{clock} not being exactly at the desired frequency). In the tone, each cycle would be identical to all the others. However, the data feeding the DAC are composed of seven cycles of the desired tone before the sequence repeats. Each cycle has exactly the same frequency. The difference is that each cycle has a different distribution of sample points compared with any of the other six cycles. Try computing $\sin[2\pi(7/25)I]$ for all 25 points to see this effect for yourself.

As an aside, well-designed waveforms exhibit closure; that is, the last point in the sampled data is immediately followed by the first point in the RAM stored sequence. This allows the address counter to return to the first point in the sequence immediately after the last, and the final output has no discontinuity. If either P or Q is not an integer, closure will not be maintained. In this case, the spectrum will be salted with unwanted spurious signals. Again, try an example for yourself using a simple software loop and you will see that closure will not be obtained.

Given that the problem is to find P and Q for any desired F_{out}, some interesting results surface. It turns out that for some maximum value of Q (Q_{max}), there is a solution set of P/Q such that there is no better fit to the desired tone. It is true that there will usually be an error in the resulting frequency, but it may be made very small by choosing Q_{max} large enough.

The analysis is complicated by the fact that P and Q may only be whole numbers. To make matters worse, many combinations of P/Q yield identical frequencies. For example, for $P = 21$ and $Q = 75$, we obtain the same 28-MHz tone as with $P = 7$ and $Q = 25$. Only for P and Q relatively prime (no common factors) is F_{out} obtained with a minimum value of Q. Naturally, we want Q to be small since it conserves memory space.

The problem of finding P and Q is the same one mathematicians face when asked to find the best rational approximation to a fraction number like 0.*dddddddd*. With the help of Euler's method of continued fractions, P and Q may be found given the desired fraction (P/Q) of F_{clock} that is to be synthesized. For an excellent study in this area, refer to Ref. [16].

Some results of solving for P and Q may be summarized.

The frequency resolution of a RAM-based synthesizer is not a constant. In fact, there is no simple expression that you may use to find the exact resolution versus frequency. However, a typical or expected resolution may be expressed as

$$F_{res} = F_{clock}(2\pi^2/3Q_{max}^3) \tag{3-25}$$

This odd expression may be derived by finding how many pairs of relatively prime P/Q fractions (with $P/Q < 1$) are available given an upper limit on Q of G_{max}. In this analysis, Euler's totient function is used to find the sum of the pairs. On average, a unique tone will be found at a spacing of F_{res}. For $Q_{max} > 32$, F_{res} as computed is accurate to <1%.

Fortunately, F_{res} drops as the square of Q_{max}. Let us consider an example. For $G_{max} = 1024$ points and $F_{clock} = 10$ MHz,

$$F_{res} = (10\text{ MHz}\,(19.74))/(3 \times 1{,}048{,}576) = 62\text{ Hz} \tag{3-26}$$

This means that there are about 162,000 unique frequencies spanning dc to 10 MHz spaced approximately by 62 Hz. The available frequencies higher than 0.4 F_{clock} are not used, but this does not affect the resolution.

With $Q_{max} = 4096$ points,

$$F_{res} = 62/16 = 4\text{ Hz} \tag{3-27}$$

There is no guarantee, however, that you will get the desired frequency within F_{res}. But it is highly likely.

Figure 3-10 shows a plot of the percentage error in $F_{desired}$ for a 4K RAM size. The worst-case error expected is 100/size. For this case, worst case = 0.024%. Examining the figure, we find almost no errors that are worst case. In fact, 95% of all desired tones fall within 0.004% of desired frequency and 75% are within 0.0005% of $F_{desired}$. The Y axis is the percentage of all possible frequencies (using P/Q) that fall within any given error bin. A curious side effect of the P/Q relationship is that 61% of all possible P/Q values are relatively prime, assuming that $P_{max} = Q_{max}$.

It should be mentioned, however, that if Q is fixed and only P is a variable, then $F_{res} = F_{clock}/Q$ and is much larger than if Q is also a variable.

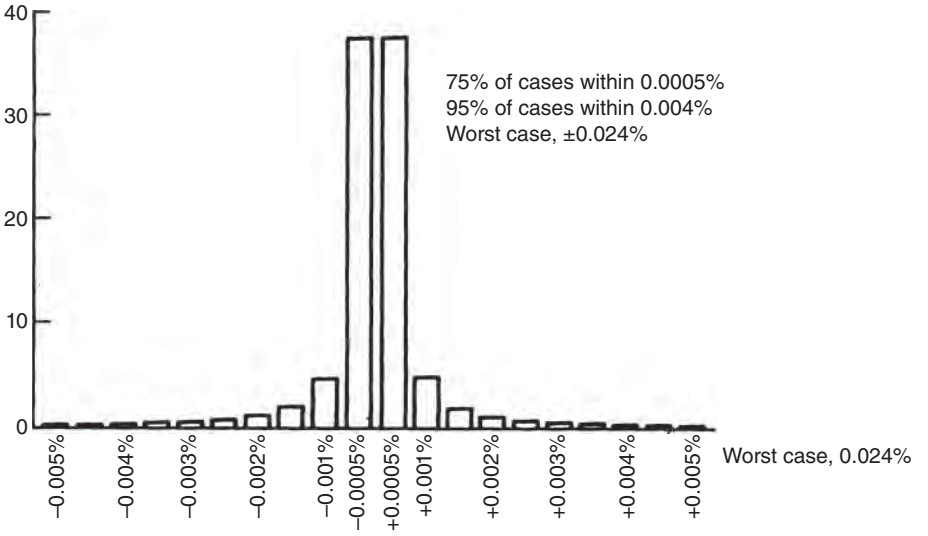


Figure 3-10 Percentage error in desired frequency for a 4K RAM size.

Another way to analyze the frequency resolution is given in Ref. [7]. The method utilizes partial derivatives to solve for F_{res}.

RAM-based synthesis is well suited for the generation of arbitrary time functions. Any desired waveform of finite length may be sampled and stored in the RAM. Generating a carrier with AM, PM, or FM is just as easy as generating a pure carrier with no modulation. Depending on user needs, this method may be employed with success for generating a large class of waveforms.

Applications

Applications fall into several broad categories. At the low end, there are some simple single-tone, low-frequency oscillators. With just a few chips such an oscillator can be built. At the high end, a group of synthesizers classified as signal simulators exist. These units can generate very complex signal scenarios with independent AM, PM, FM, and frequency hopping. Such systems find application in radar, multiple satellite signal generation, and communication channel simulation, for example.

RAM-based systems may be used to simulate, read, and serve waveforms from a disc drive read head. This technique provides very flexible waveforms for disc drive testing and development (see Ref. [17]).

For communications systems that use *I*/*Q* modulation techniques, two synthesizers may be paired to generate synchronously the *I* and *Q* components. With this method, for example, two 50-MHz bandwidth synthesizers may be used to modulate an *I*/*Q* modulator and the resulting bandwidth is 100 MHz. In this application, the *I* and *Q* channels must be matched in amplitude and phase to better than 0.01 dB and 0.35°, respectively, for good performance.

With this design requirement, the prudent choice is a digital synthesizer. Achieving this match with two analog instruments is almost impossible (see Ref. [18]).

New applications are being discovered every day. By applying DSP techniques to signal problems, designers are discovering the joy of digital synthesis. Increasingly, what used to be done awkwardly with analog methods may now be done with finesse using digital methods.

Summary of Methods

Three architectures for digital synthesizers have been discussed. The major design elements of each method have been analyzed. In brief, now, here are some reasons to choose one architecture over another.

- *Recursion Method*. Simple to implement. Needs floating point multiply to achieve excellent frequency resolution and low limit-cycle noise. Difficult to modulate. Good for software simulation of single tones.
- *Phase Accumulator*. Practical synthesizer using fixed point hardware. Easy to achieve constant, useful F_{res} values. Modulation may be implemented with additional hardware. Allows for real-time modulation of a carrier with user data. Very flexible, long scenario lengths attained. Amount of hardware required depends on the modulation capabilities needed. The system can become large when AM, PM, and FM are required.
- *RAM-Based Method*. Stored sample image lookup. Non-uniform frequency resolution is typical. Any desired waveform may be generated. Scenario time is a direct function of the amount of RAM available and how the sequencer is programmed. No real-time modulation allowed (AM would be easy, however). All waveforms must be precomputed. This may be time-consuming depending on the application. A waveform generation software package will often be needed for all but the simplest signals.

In conclusion, the choice is really between the last two methods for flexible, hardware synthesizers. Each has its advantages/disadvantages depending on the application. As more designers become aware of the advantages of digital synthesis, new applications will emerge.

There are a number of companies producing DDS synthesizers. As an example, Figure 3-11 shows the datasheet of AD9914 of Analog Devices and Figure 3-12 show the AS9912. This DDS offers 14 bit resolution resulting in 4 μHz resolution.

DDS synthesizers produced by Analog Devices can serve as examples of the capabilities offered by such devices. These chips and boards are available in different operating ranges and frequency ranges. A good targeted use of these digital direct synthesizers is application in synthesized signal generators, high frequency (HF) radios, and ultra high frequency (UHF) applications.

Figures 3-13 and 3-14 show examples of an HF synthesizer, using a DDS for fine resolution. The 20-MHz temperature-compensated crystal oscillator (TCXO) is used as the frequency standard for the DDS synthesizer. Its output frequency, which operates from 1 to 2 MHz, is then up-converted from 21/22 MHz. The output is then divided by 4 and fed into a phase detector. A second loop, operating from 147 to 410 MHz in 1-MHz steps, is also divided by 4 and serves as the auxiliary frequency to mix down the output frequencies into a range of approximately 5 MHz.

3-2-3 Signal Quality

Modern DDS systems like the 9911–9914 series have some hard-wired signals that are used for cellular telephones, as an example. The architecture shown earlier is flexible enough to generate in the true sense, arbitrary waveforms. In addition to this, mathematical tools can generate the necessary entries to lookup tables, not only for sine and cosine values, but truly determine any mathematical functions.

It is important to discuss this subject in some detail since digital synthesis has acquired a reputation for having poor signal quality, especially with regard to spurious sidebands.

Signal quality is a measure of the purity of a desired signal. In the case of sinusoidal signals, a single infinitesimally wide spectral line is the highest form of purity by definition. Broadening of the spectral line is caused by amplitude or phase noise. For a number of reasons outside the scope of this chapter, phase noise is the more important parameter of the two. Nonharmonically related sidebands, commonly referred to as "spurs," are another signal-corrupting factor and are measured with respect to the level of the carrier. Harmonic distortion is the third corrupting factor but is harmless in many applications.

The effect of quantization on signal quality has been treated earlier in this chapter. It represents the best that can be achieved theoretically by digital synthesis. There are a number of practical effects that affect the signal in a more serious way. These important effects will be considered here.

Spurious Sideband Mechanisms

In this section we will examine the various factors that cause spurious sidebands in digital synthesizers.

Quantization Effects These have been analyzed earlier in this chapter.

Data Sheet AD9914

GENERAL DESCRIPTION

The AD9914 is a direct digital synthesizer (DDS) featuring a 12-bit DAC. The AD9914 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 1.4 GHz. The AD9914 enables fast frequency hopping and fine tuning resolution (64-bit capable using programmable modulus mode). The AD9914 also offers fast phase and amplitude hopping capability. The frequency tuning and control words are loaded into the AD9914 via a serial or parallel input/output port. The AD9914 also supports a user defined linear sweep mode of operation for generating linear swept waveforms of frequency, phase, or amplitude. A high speed, 32-bit parallel data input port is included, enabling high data rates for polar modulation schemes and fast reprogramming of the phase, frequency, and amplitude tuning words.

The AD9914 is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section).

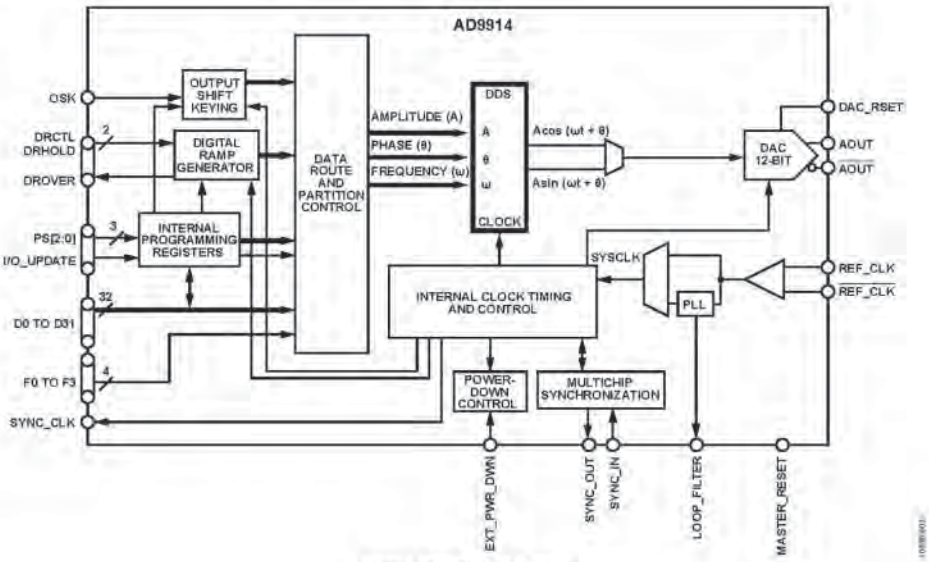


Figure 2. Detailed Block Diagram

Figure 3-11 Part of the datasheet of AD9914. Reproduced with permission.

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltage; DAC R_{SET} = 3.3 kΩ, T_A = 25°C, unless otherwise noted.

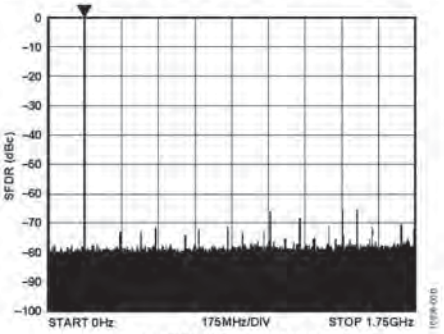


Figure 4. Wideband SFDR at 171.5 MHz
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

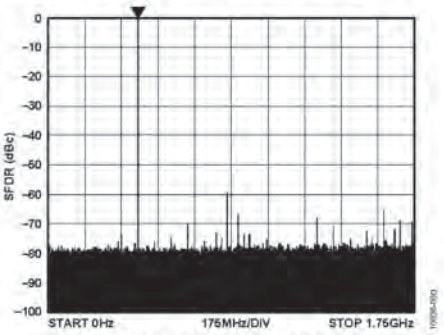


Figure 5. Wideband SFDR at 427.5 MHz
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

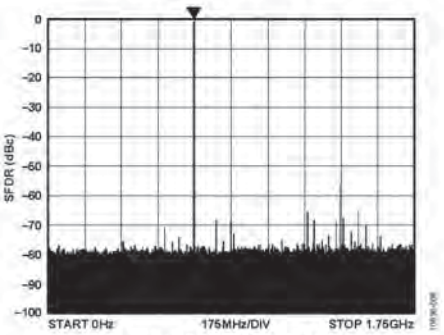


Figure 6. Wideband SFDR at 696.5 MHz,
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

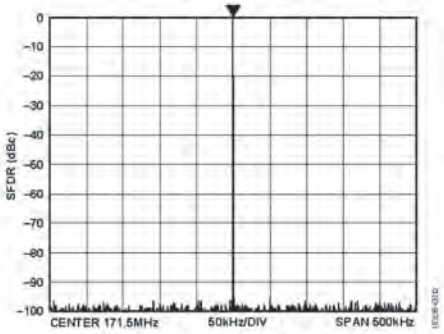


Figure 7. Narrow-Band SFDR at 171.5 MHz,
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

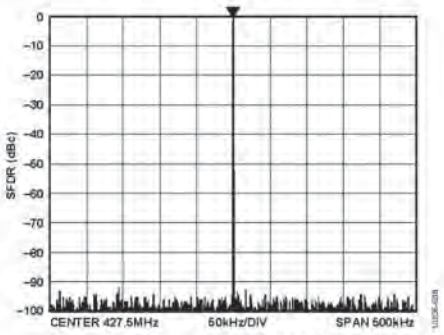


Figure 8. Narrow-Band SFDR at 427.5 MHz,
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

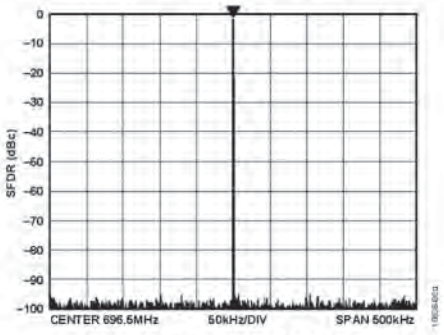


Figure 9. Narrow-Band SFDR at 696.5 MHz,
SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

Figure 3-11 (*Continued*)

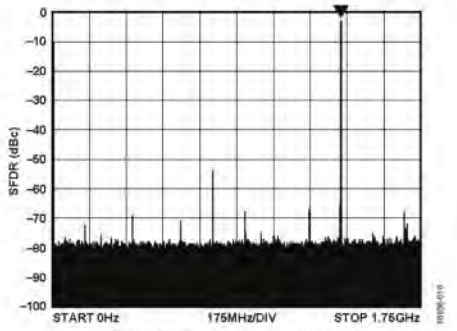


Figure 10. Wideband SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

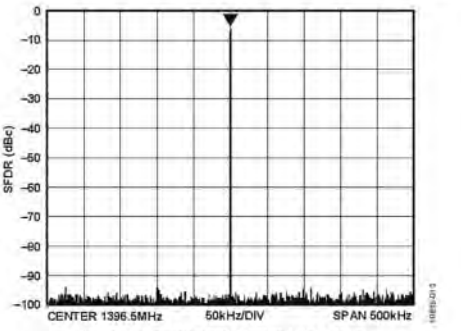


Figure 13. Narrow-Band SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

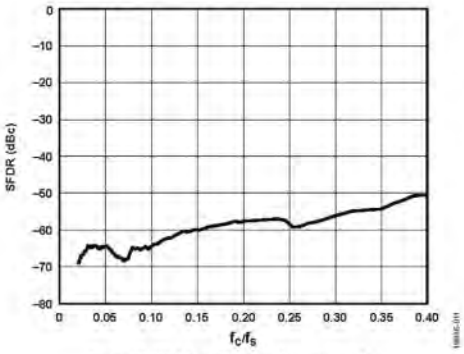


Figure 11. Wideband SFDR vs. Normalized f_{OUT} SYSCLK = 3.5 GHz

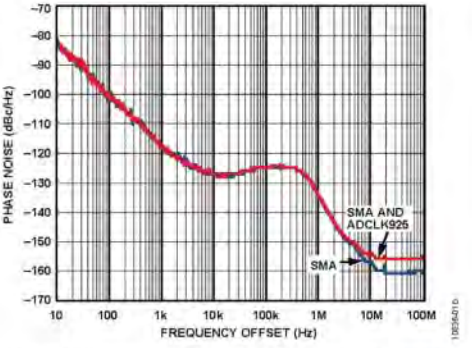


Figure 14. Absolute Phase Noise of REF CLK Source Driving AD9914 Rohde & Schwarz SMA100 Signal Generator at 3.5 GHz Buffered by Series ADCLK925

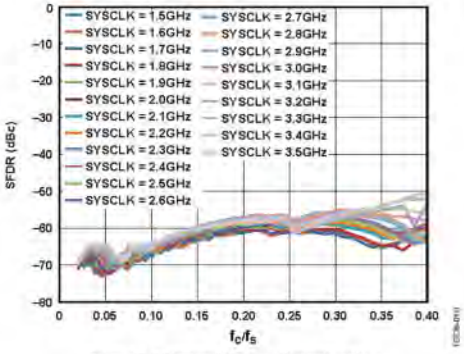


Figure 12. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 2.5 GHz to 3.5 GHz

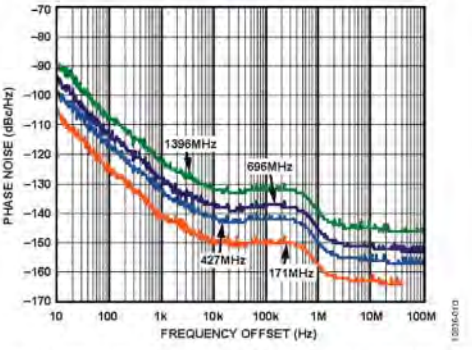


Figure 15. Absolute Phase Noise Curves of DDS Output at 3.5 GHz Operation

Figure 3-11 (*Continued*)

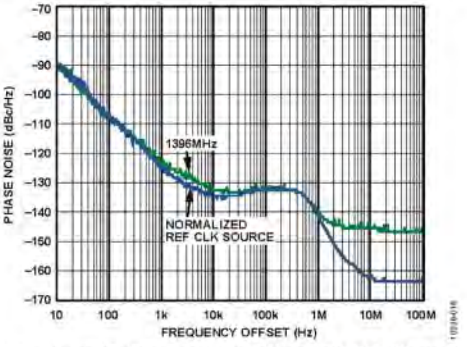


Figure 16. Absolute Phase Noise Curves of Normalized REF CLK Source to DDS Output at 1396 MHz (SYSCLK = 3.5 GHz)

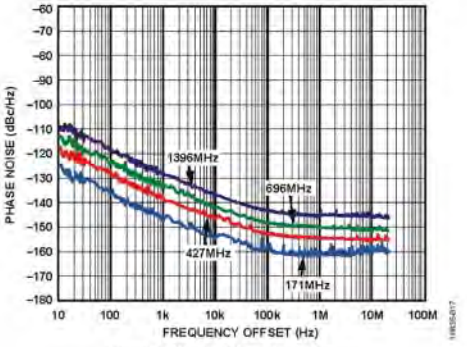


Figure 17. Residual Phase Noise Curves

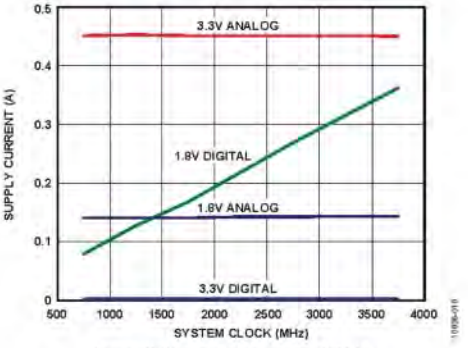


Figure 18. Power Supply Current vs. SYSCLK

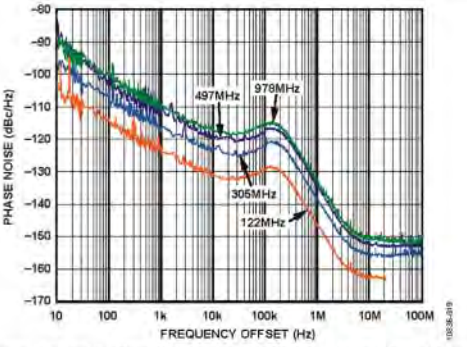


Figure 19. Absolute Phase Noise Curves of DDS Output Using Internal PLL at 2.5 GHz Operation

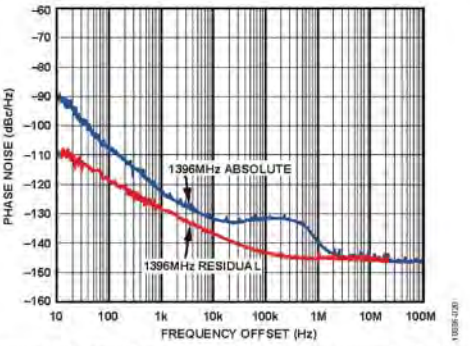


Figure 20. Residual PN vs. Absolute PN Measurement Curves at 1396 MHz

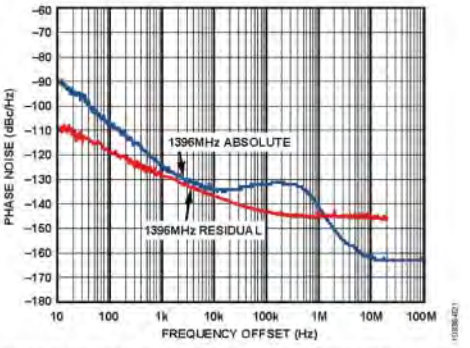


Figure 21. Residual Phase Noise vs. Normalized Absolute REF CLK Source Phase Noise at 1396 MHz

Figure 3-11 (*Continued*)

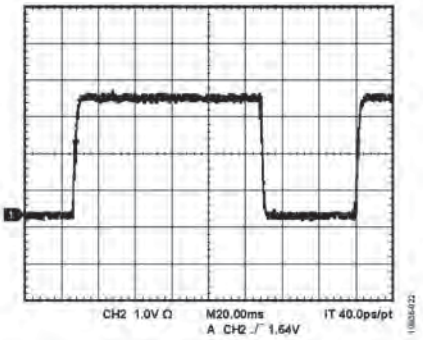


Figure 22. SYNC_OUT ($f_{SYSCLK}/384$)

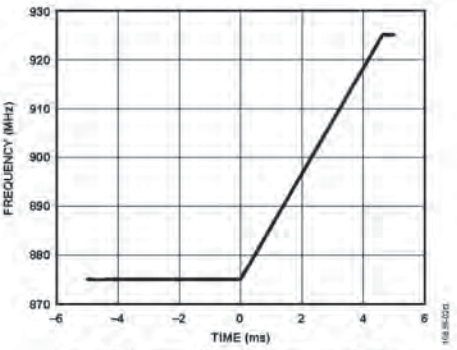


Figure 24. Measured Rising Linear Frequency Sweep

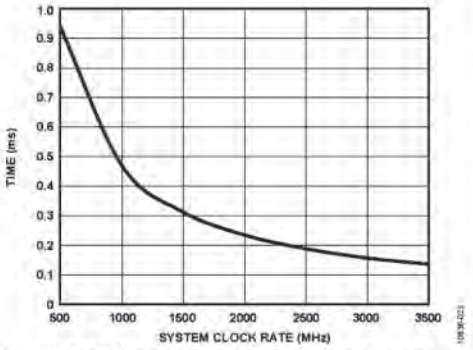


Figure 23. DAC Calibration Time vs. SYSCLK Rate. See the DAC Calibration Output Section for Formula.

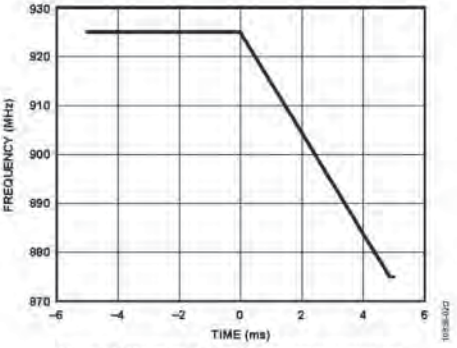


Figure 25. Measured Falling Linear Frequency Sweep

Figure 3-11 (*Continued*)

THEORY OF OPERATION

The AD9914 has five modes of operation.

- Single tone
- Profile modulation
- Digital ramp modulation (linear sweep)
- Parallel data port modulation
- Programmable modulus mode

The modes define the data source supplies the DDS with the signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is established based on the mode and/or specific control bits and function pins.

Although the various modes are described independently, they can be enabled simultaneously. This provides an unprecedented level of flexibility for generating complex modulation schemes. However, to avoid multiple data sources from driving the same DDS signal control parameter, the device has a built-in priority protocol.

In single tone mode, the DDS signal control parameters come directly from the profile programming registers. In digital ramp modulation mode, the DDS signal control parameters are delivered by a digital ramp generator. In parallel data port modulation mode, the DDS signal control parameters are driven directly into the parallel port.

The various modulation modes generally operate on only one of the DDS signal control parameters (two in the case of the polar modulation format via the parallel data port). The unmodulated DDS signal control parameters are stored in programming registers and automatically routed to the DDS based on the selected mode.

A separate output shift keying (OSK) function is also available. This function employs a separate digital linear ramp generator that affects only the amplitude parameter of the DDS. The OSK function has priority over the other data sources that can drive the DDS amplitude parameter. As such, no other data source can drive the DDS amplitude when the OSK function is enabled.

SINGLE TONE MODE

In single tone mode, the DDS signal control parameters are supplied directly from the profile programming registers. A profile is an independent register that contains the DDS signal control parameters. Eight profile registers are available. Note that the profile pins must select the desired register.

PROFILE MODULATION MODE

Each profile is independently accessible. For FSK, PSK, or ASK modulation, use the three external profile pins (PS[2:0]) to select the desired profile. A change in the state of the profile pins with the next rising edge on SYNC_CLK updates the DDS with the parameters specified by the selected profile. Therefore, the profile change must meet the setup and hold times to the SYNC_CLK rising edge. Note that amplitude control must also be enabled using the OSK enable bit in the CFR1 register (0x00[8]).

DIGITAL RAMP MODULATION MODE

In digital ramp modulation mode, the modulated DDS signal control parameter is supplied directly from the digital ramp generator (DRG). The ramp generation parameters are controlled through the serial or parallel input/output port.

The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp. The upper and lower boundaries of the ramp, the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp are all programmable.

The ramp is digitally generated with 32-bit output resolution. The 32-bit output of the DRG can be programmed to affect frequency, phase, or amplitude. When programmed for frequency, all 32 bits are used. However, when programmed for phase or amplitude, only the 16 MSBs or 12 MSBs, respectively, are used.

The ramp direction (rising or falling) is externally controlled by the DRCTL pin. An additional pin (DRHOLD) allows the user to suspend the ramp generator in the present state. Note that amplitude control must also be enabled using the OSK enable bit in Register CFR1.

PARALLEL DATA PORT MODULATION MODE

In parallel data port modulation mode, the modulated DDS signal control parameter(s) are supplied directly from the 32-bit parallel data port. The function pins define how the 32-bit data-word is applied to the DDS signal control parameters. Formatting of the 32-bit data-word is unsigned binary, regardless of the destination.

Parallel Data Clock (SYNC_CLK)

The AD9914 generates a clock signal on the SYNC_CLK pin that runs at 1/24 of the DAC sample rate (the sample rate of the parallel data port). SYNC_CLK serves as a data clock for the parallel port.

PROGRAMMABLE MODULUS MODE

In programmable modulus mode, the DRG is used as an auxiliary accumulator to alter the frequency equation of the DDS core, making it possible to implement fractions that are not restricted to a power of 2 in the denominator. A standard DDS is restricted to powers of 2 as a denominator because the phase accumulator is a set of bits as wide as the frequency tuning word (FTW).

When in programmable modulus mode, however, the frequency equation is:

$$f_O = (f_S)(FTW + A/B)/2^{32}$$

where $f_O/f_S < ½$, $0 \le FTW < 2^{31}$, $2 \le B \le 2^{32} - 1$, and $A < B$.

This equation implies a modulus of $B \times 2^{32}$ (rather than 2^{32}, in the case of a standard DDS). Furthermore, because B is programmable, the result is a DDS with a programmable modulus.

Figure 3-11 (*Continued*)

FUNCTIONAL BLOCK DETAIL

DDS CORE

The direct digital synthesizer (DDS) block generates a reference signal (sine or cosine based on Register 0x00, Bit 16, the enable sine output bit). The parameters of the reference signal (frequency, phase, and amplitude) are applied to the DDS at the frequency, phase offset, and amplitude control inputs, as shown in Figure 30.

The output frequency (f_{OUT}) of the AD9914 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. The relationship among f_{OUT}, FTW, and f_{SYSCLK} is given by

$$f_{OUT} = \left(\frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (1)$$

where *FTW* is a 32-bit integer ranging in value from 0 to 2,147,483,647 ($2^{31} - 1$), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).

The FTW required to generate a desired value of f_{OUT} is found by solving Equation 1 for FTW, as given in Equation 2.

$$FTW = \text{round}\left(2^{32}\left(\frac{f_{OUT}}{f_{SYSCLK}}\right)\right) \quad (2)$$

where the round(*x*) function rounds the argument (the value of x) to the nearest integer. This is required because the FTW is constrained to be an integer value. For example, for f_{OUT} = 41 MHz and f_{SYSCLK} = 122.88 MHz, FTW = 1,433,053,867 (0x556AAAAB).

Programming an FTW greater than 2^{31} produces an aliased image that appears at a frequency given by

$$f_{OUT} = \left(1 - \frac{FTW}{2^{32}}\right) f_{SYSCLK}$$

for FTW ≥ 2^{31}

The relative phase of the DDS signal can be digitally controlled by means of a 16-bit phase offset word (POW). The phase offset is applied prior to the angle to amplitude conversion block internal to the DDS core. The relative phase offset (Δθ) is given by

$$\Delta\theta = \begin{vmatrix} 2\pi\left(\frac{POW}{2^{16}}\right) \\ 360\left(\frac{POW}{2^{16}}\right) \end{vmatrix}$$

where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees.

To find the POW value necessary to develop an arbitrary Δθ, solve the preceding equation for POW and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

The relative amplitude of the DDS signal can be digitally scaled (relative to full scale) by means of a 12-bit amplitude scale factor (ASF). The amplitude scale value is applied at the output of the angle to amplitude conversion block internal to the DDS core. The amplitude scale is given by

$$Amplitude\ Scale = \begin{vmatrix} \frac{ASF}{2^{12}} \\ 20\log\left(\frac{ASF}{2^{12}}\right) \end{vmatrix} \quad (3)$$

where the upper quantity is amplitude expressed as a fraction of full scale and the lower quantity is expressed in decibels relative to full scale.

To find the ASF value necessary for a particular scale factor, solve Equation 3 for ASF and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

When the AD9914 is programmed to modulate any of the DDS signal control parameters, the maximum modulation sample rate is 1/24 f_{SYSCLK}. This means that the modulation signal exhibits images at multiples of 1/24 f_{SYSCLK}. The impact of these images must be considered when using the device as a modulator.

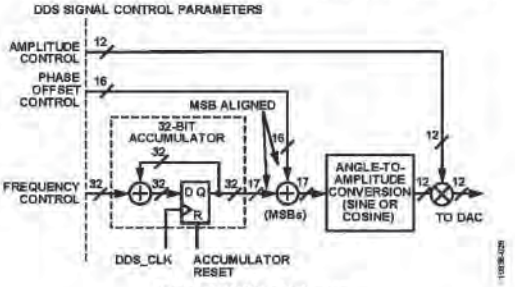


Figure 30. DDS Block Diagram

Figure 3-11 (*Continued*)

12-BIT DAC OUTPUT

The AD9914 incorporates an integrated 12-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor (R_{SET}) connected between the DAC_RSET pin and AGND establishes the reference current. The recommended value of R_{SET} is 3.3 kΩ.

Attention must be paid to the load termination to keep the output voltage within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.

DAC CALIBRATION OUTPUT

The DAC CAL enable bit in the CFR4 control register (0x03[24]) must be manually set and then cleared after each power-up and every time the REF CLK or internal system clock is changed. This initiates an internal calibration routine to optimize the setup and hold times for internal DAC timing. Failure to calibrate may degrade performance and even result in loss of functionality. The length of time to calibrate the DAC clock is calculated from the following equation:

$$t_{CAL} = \frac{469{,}632}{f_S}$$

RECONSTRUCTION FILTER

The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth.

Because the DAC constitutes a sampled system, the output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd numbered images (shown in Figure 31) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample-and-hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter must preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains significant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a third-, fifth-, or seventh-order elliptic low-pass filter is common.

Some applications operate from an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter. The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

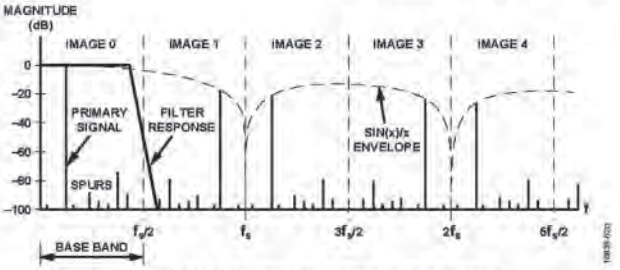


Figure 31. DAC Spectrum vs. Reconstruction Filter Response

Figure 3-11 (*Continued*)

ANALOG DEVICES

1 GSPS Direct Digital Synthesizer with 14-Bit DAC

AD9912

FEATURES

1 GSPS internal clock speed (up to 400 MHz output directly)
Integrated 1 GSPS 14-bit DAC
48-bit frequency tuning word with 4 µHz resolution
Differential HSTL comparator
Flexible system clock input accepts either crystal or external reference clock
On-chip low noise PLL REFCLK multiplier
2 SpurKiller channels
Low jitter clock doubler for frequencies up to 750 MHz
Single-ended CMOS comparator; frequencies of <150 MHz
Programmable output divider for CMOS output
Serial I/O control
Excellent dynamic performance
Software controlled power-down
Available in two 64-lead LFCSP packages
Residual phase noise @ 250 MHz
10 Hz offset: −113 dBc/Hz
1 kHz offset: −133 dBc/Hz
100 kHz offset: −153 dBc/Hz
40 MHz offset: −161 dBc/Hz

APPLICATIONS

Agile LO frequency synthesis
Low jitter, fine tune clock generation
Test and measurement equipment
Wireless base stations and controllers
Secure communications
Fast frequency hopping

GENERAL DESCRIPTION

The AD9912 is a direct digital synthesizer (DDS) that features an integrated 14-bit digital-to-analog converter (DAC). The AD9912 features a 48-bit frequency tuning word (FTW) that can synthesize frequencies in step sizes no larger than 4 µHz. Absolute frequency accuracy can be achieved by adjusting the DAC system clock.

The AD9912 also features an integrated system clock phase-locked loop (PLL) that allows for system clock inputs as low as 25 MHz.

The AD9912 operates over an industrial temperature range, spanning −40°C to +85°C.

BASIC BLOCK DIAGRAM

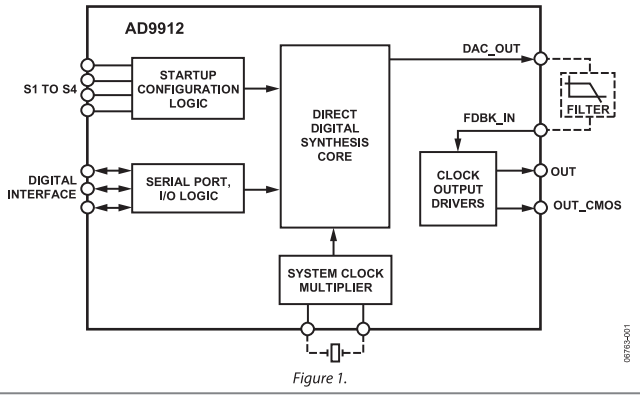


Figure 1.

Figure 3-12 Part of the datasheet of AD9912. Reproduced with permission.

Nonlinear Transition Effects in the DAC This occurs entirely during the transition from one state to the other. The spurs created by this mechanism are determined in the frequency by the same formula that governs quantization spurs, $F_{spur} = MF_{clock} + -NF_{signal}$. The difference is that values of M and N are fairly low. M is usually less than 3 and N is less than 10. If the nonlinear effects are very pronounced, these values could increase. For the values mentioned, the spurs generated are well above those created by the ideal quantization process. It is not unusual to find spurs around −30 dBc when a high conversion rate is attempted. A good deglitching circuit (sample/hold or simple sampler) can reduce these spurs by up to 30–40 dB. The deglitcher, of course, introduces its own set of spurs, but these are lower and tend to be limited to values of $M < 2$ and $N < 5$. A good way to evaluate this effect is to generate signals at frequencies close, but not equal, to fractions of the clock. At approximately 1/3 of the clock

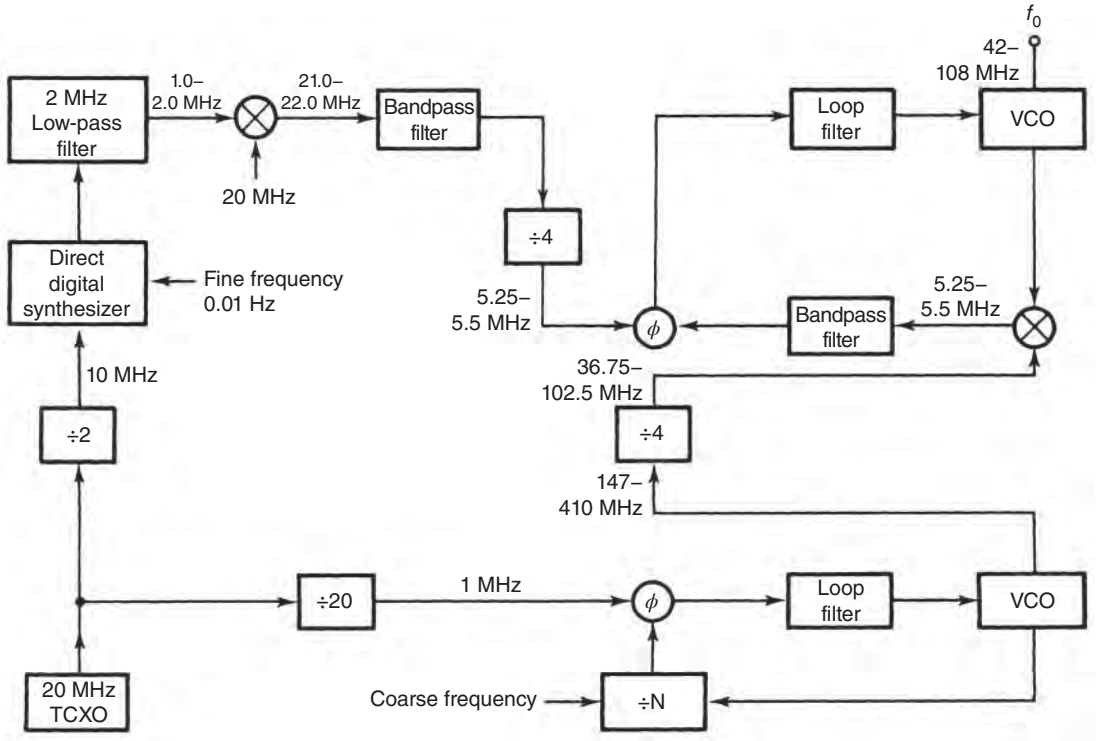


Figure 3-13 Block diagram of a HF synthesizer.

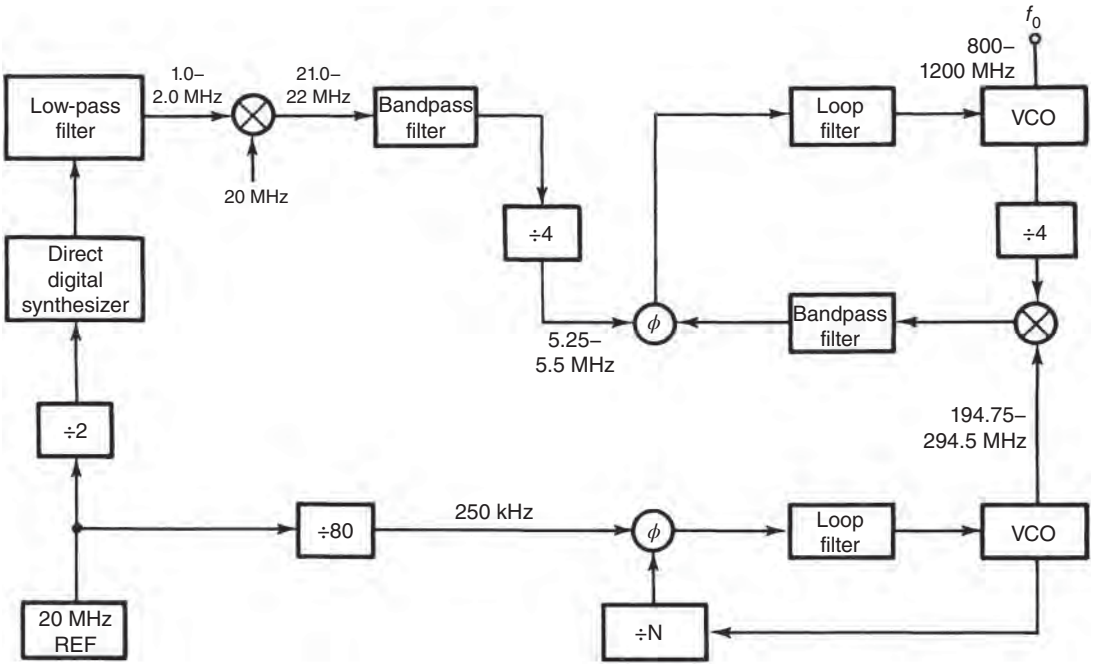


Figure 3-14 Synthesizer with extension to L-band frequencies.

frequency, one would observe on a spectrum analyzer in proximity to the signal frequency, spurs caused by $M = 1$ and $N = 2$ among others that satisfy the equation stated earlier. One should repeat this process for 1/4, 1/5, 1/6 of the clock frequency until the level of the spurs drops below the level of interest (see Ref. [19]).

Data Skew If the data are presented to the DAC with some skew in time, this causes the various switches in the DAC to turn on at slightly different instances. This causes a transition period that has a signal that is dependent on the data being supplied. The effect leads to results that are identical to those mentioned in the previous paragraph and can be examined in the same way. A reduction in the data skew, by reclocking the data in a high-speed register, for example, can contribute significantly to alleviate this effect.

Implementation Effects This primarily relates to spur-generating mechanisms that are not inherent in the arithmetic or conversion process, but show up on the output signal nevertheless. One such mechanism is clock and clock subharmonic leakage and mixing in the DAC. Thus, if a strong $F_{\text{clock}}/2$ component were present in the system, it could give rise to a spur at $F_{\text{clock}}/2 - F_{\text{signal}}$. In general, this can lead to spurs at frequencies given by $(M/K)F_{\text{clock}} + -\text{NF}_{\text{signal}}$. where $K = 1, 2, 4, 8$, because it is likely to encounter power of two subharmonics of the clock in the digital processing system.

Two-Tone Intermodulation Distortion This is a measure of the dynamic linearity of the signal-generating process. Two equilevel tones at frequencies F_1 and F_2 give rise to spectral lines at $\text{MF}_1 - \text{NF}_2$ that are undesired. The ratio of the undesired tones to the desired ones in dBc is a figure of merit for the signal generator. Note that quantization gives rise to intermodulation distortion, but this is usually at a level well below that caused by the DAC or the output amplifier for a 12-bit system.

Output Transfer Function Characteristics Any departure from flat amplitude and linear phase as a function of frequency introduces an error in the signal being created. This is especially apparent when the carrier is being modulated. Thus, anti-aliasing filters must be especially precise in these characteristics to reduce the signal distortion arising from this effect. It is possible to compensate for nonideal effects by predistorting the desired signal with just the right amount of amplitude/phase offset to undo the ill effects of the LPF nonlinearities (see Ref. [20] for further details).

Phase Noise This is caused by the fact that there is jitter in the phase of the signal that is being created. The zero crossings for a sine wave are not distributed uniformly in time; they exhibit some randomness. This leads to a broadening of the spectrum of the otherwise infinitesimally wide spectral line of a sine wave with no phase noise. A figure of merit for phase noise is the ratio of the power or voltage in spectral range 1 Hz wide to that of the carrier itself. A detailed treatment of phase noise can be found in Ref. [21].

There is only one source of phase noise in DDS as opposed to multiple sources for PLL synthesis. That source is the phase noise on the clock signal. In general, any PM on the clock signal is transmitted to the output signal by the ratio $F_{\text{signal}}/F_{\text{clock}}$. This means that there is a 20-dB reduction in the PM of a signal that is at 1/10 the clock frequency compared with the PM that exists on the clock signal.

The problem of cleaning up the phase noise in DDS is therefore simply that of cleaning up the clock signal. It should be noted, however, that when discreet spurs become very numerous, their effect becomes indistinguishable from that of phase noise for practical applications. The following two pictures show the obtainable quality. Figure 3-15 shows the two-tone intermodulation in the HP8770A undesired tones 74 dB down with respect to the two tones at +5 dBm. Figure 3-16 shows the HP8770A signal generator with a carrier frequency of 37 MHz. The spurious signals are 72 dB down. The internal clock rate for this is 125 MHz.

In many DDS applications, the spectral purity of a DAC output is of primary concern. Unfortunately, the measurement prediction and analysis of this performance is complicated by a number of interacting factors.

Even an ideal N-bit DAC will produce harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. This is because the spectral content of the DAC quantization noise varies as this ratio varies, even though its theoretical rms value remains equal to $q/\sqrt{12}$ (where q is the weight of the LSB). The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is simply not true in a DDS system (it is more apt to be a true

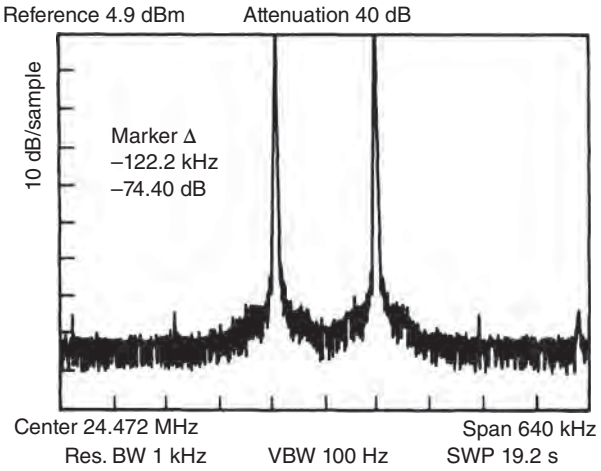


Figure 3-15 Two-tone intermodulation in the HP8770A undesired tones 74 dB down with respect to the two tones at +5 dBm.

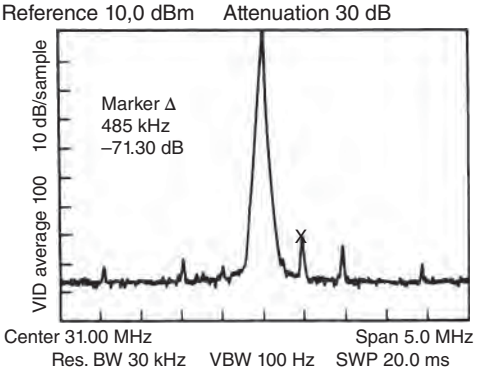


Figure 3-16 HP8770A signal generator with a carrier frequency of 37 MHz. The spurious signals are 72 dB down. The internal clock rate for this is 125 MHz.

assumption in an analog/digital converter (ADC)-based system, because the ADC adds a certain amount of noise to the signal which tends to "dither" or randomize the quantization error. However, a certain amount of correlation still exists). For instance, if the DAC output frequency is set to an exact submultiple of the clock frequency, then the quantization noise will be concentrated at multiples of the output frequency; that is, it is highly dependent. If the output frequency is slightly offset, however, the quantization noise will become more random, thereby giving an improvement in the effective spurious free dynamic range (SFDR).

This is illustrated in Figure 3-17, where a 4096 (4K) point fast Fourier transform (FFT) is calculated based on digitally generated data from an ideal 12-bit DAC. In the left-hand diagram (A), the ratio between the clock frequency and the output frequency was chosen to be exactly 40, yielding an SFDR of about 77 dBc. In the right-hand diagram, the ratio was slightly offset, and the effective SFDR is now increased to 94 dBc. In this ideal case, we observed a change in SFDR of 17 dB just by slightly changing the frequency ratio.

The best SFDR can therefore be obtained by the careful selection of the clock and output frequencies. However, in some applications, this may not be possible. In ADC-based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system as shown in Figure 3-18 (see Refs. [10–12]). The pseudo-random digital noise generator output is added to

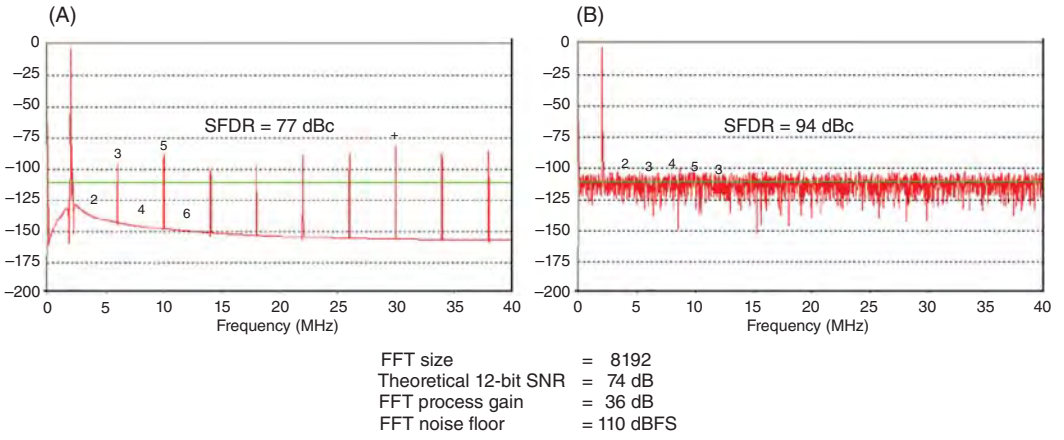


Figure 3-17 Effect of radio of clock to output frequency on theoretical 12-bit DAC SFDR using 4096 point FFT. (A) f_{out} = 2.0000 MHz, f_s = 80.0000 MHz, (B) f_{out} = 2.0111 MHz, f_s = 80.0000 MHz [4].

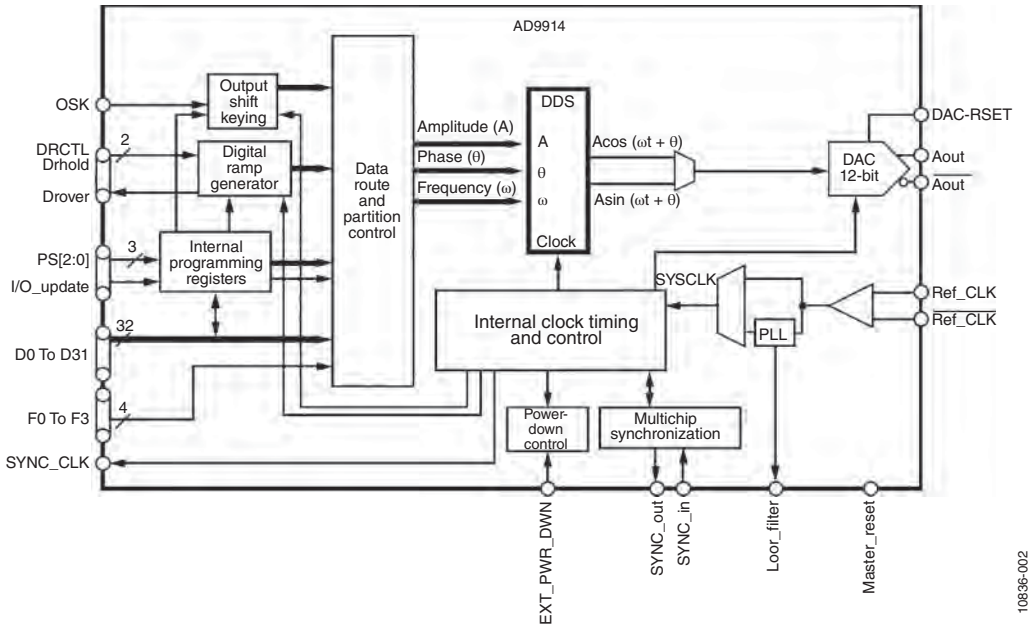


Figure 3-18 Detailed block diagram of the AD9914 [14].

the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about ½ LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that dithering is not required.

Figure 3-18 is a block diagram of the very powerful AD9914, which is used for much higher frequencies.

The detailed block diagram of the AD9914 requires some comments. The desired output frequency is delivered from the 12-bit DAC where $2^{12} = 4096$ is the resolution. The actual frequency is generated in the DDS portion on the left. It mentions sine and cosine functions. However, the entire left block can be setup to generate arbitrary waveforms.

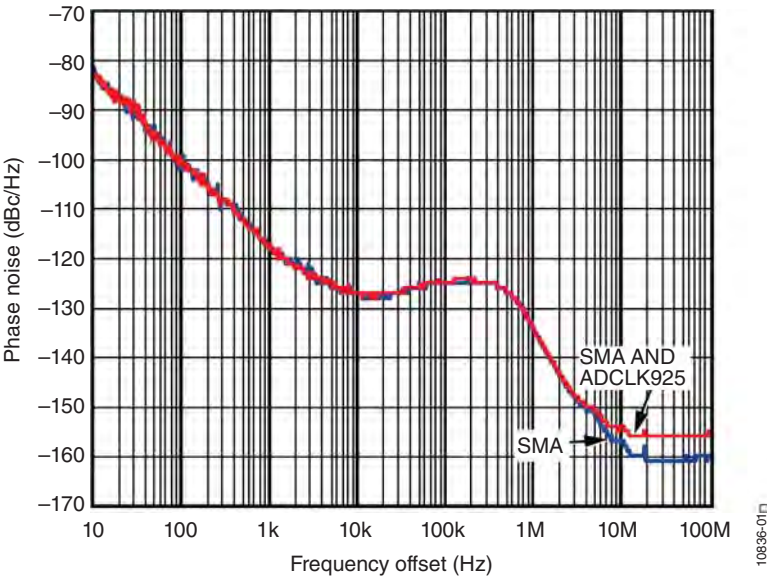


Figure 3-19 Absolute phase noise of the REF CLK source driving AD9914 Rohde and Schwarz SMA100 signal generator at 3.5 GHz buffered by series ADCLK925, Analog Devices AD9914 3.5 GSPS Direct Digital Synthesizer with 12-Bit DAC Data Sheet].

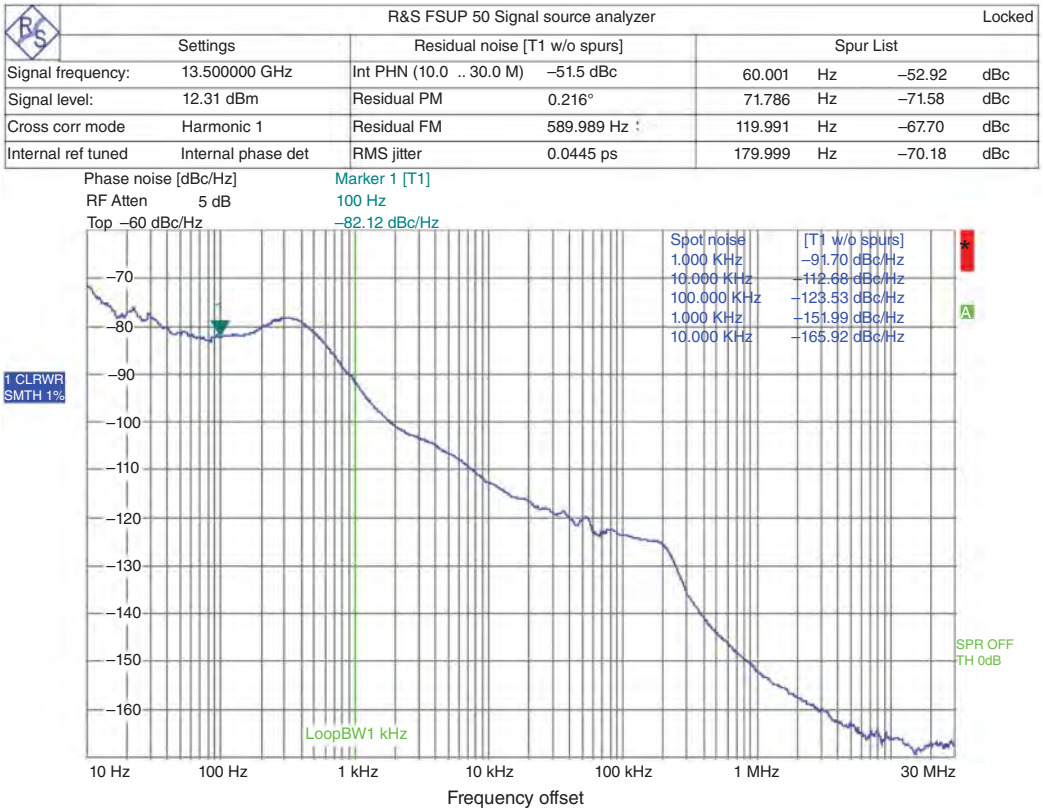


Figure 3-20 13.5 GHz dual loop synthesizer.

As to the clock generation, which should be as high as possible, but not higher than 3.5 GHz, the built-in PLL on the lower right side of the block diagram, labeled as REF_CLK can be used to generate such a frequency. However, much better performance is obtained from an ultra-stable clock synthesizer, like the R&S SMA100B (see Figure 3-19).

3-2-4 Future Prospects

As an introduction to complete synthesizers, here are some examples of oscillators based on high-Q resonators using different sources in a simple PLL. These are oscillators needed as auxiliary frequency sources in generators.

The following are examples of high Q resonators locked against a simple PLL. The configuration of each case is explained. They are oscillators as used as auxiliary frequency sources in generators.

- *13.5 GHz Dual Loop Synthesizer* (see Figure 3-20). First loop: internal 800 MHz surface acoustic wave (SAW) oscillator locked to 10 MHz, PLL IC is HMC698 Integer *N*. Second loop: 13.5 GHz dielectric resonator oscillator (DRO) locked to 800 MHz SAW, PLL IC is RFDIV3 IC.
- *KSFLOD1280-12-1280* (see Figure 3-21). Single loop phase locked DRO, 1280 MHz reference. 12.8 GHz DRO locked to 1280 MHz, PLL IC is RFDIV3.
- *FSFLO13G00-100-1* (see Figure 3-22). Single loop phase locked VCO, 100 MHz reference. 100 MHz multiplied by 8, 13 GHz is locked to 800 MHz. PLL IC is RFDIV3.

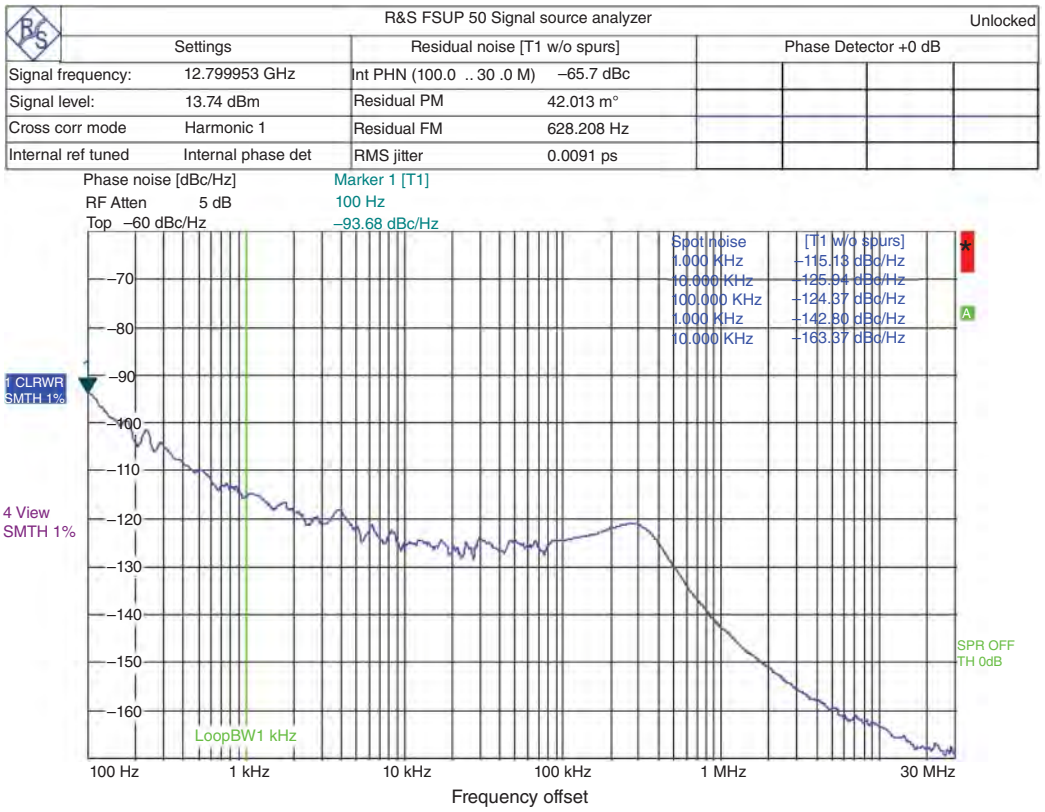


Figure 3-21 Single loop phase locked DRO, 1280 MHz reference.

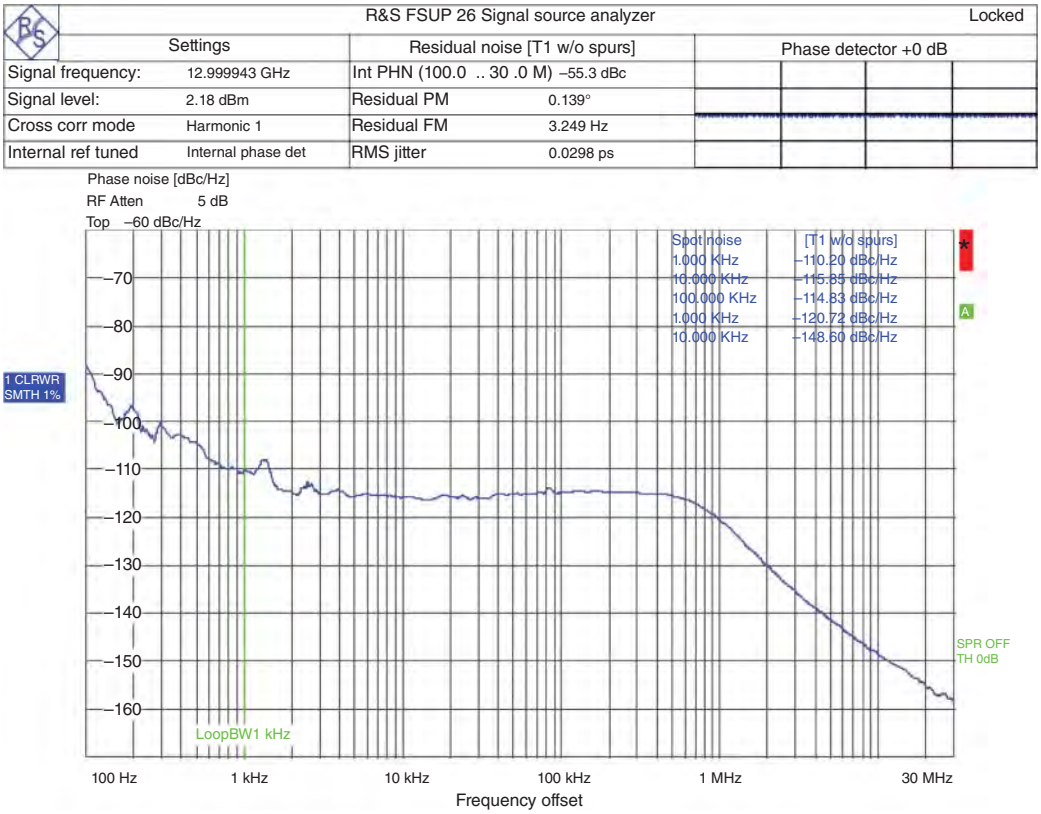


Figure 3-22 Single loop fractional-*N* phase locked 13 GHz VCO with 100 MHz reference.

- *KSFLO27R1-12-100* (see Figure 3-23). Single loop phase locked VCO, 100 MHz reference. Comparison frequency is 100 MHz; PLL IC is HMC703 fractional-*N* synthesizer. VCO output at 13.55 GHz, followed by a doubler.
- *FXLNS-1000* (see Figure 3-24). Phase locked SAW oscillator at 1 GHz. The trick used in here is that both a mixer and a PLL IC are used to control the SAW oscillator. The PLL IC (ADF4106) is used to provide frequency lock, and the mixer is used to clean up the phase noise.

3-3 LOOPS WITH DELAY LINE AS PHASE COMPARATORS

The circuits we have just studied, if absolutely ideal components without drift and tolerances were available, would theoretically enable us to come up with infinite resolution. However, the introduction of this circuit will result in some switching noise, probably spikes, and the LPF of the phase/frequency comparator will cure part of it. However, it is a discontinuous arrangement, and we will now take a look at a system that allows continuous adjustment based on a principle that we have used earlier.

When measuring the phase noise of a frequency synthesizer, for all practical purposes we can assume that the delay time τ_d is a constant over time and change of environment, which, of course, is an assumption. We can, by making the phase shifter variable, measure a certain offset from the carrier.

The voltage that is obtained from the mixer was connected to the oscilloscope or the wave analyzer. By integrating this voltage and feeding it through an amplifier back to the VCO, we can close the loop. This arrangement is a

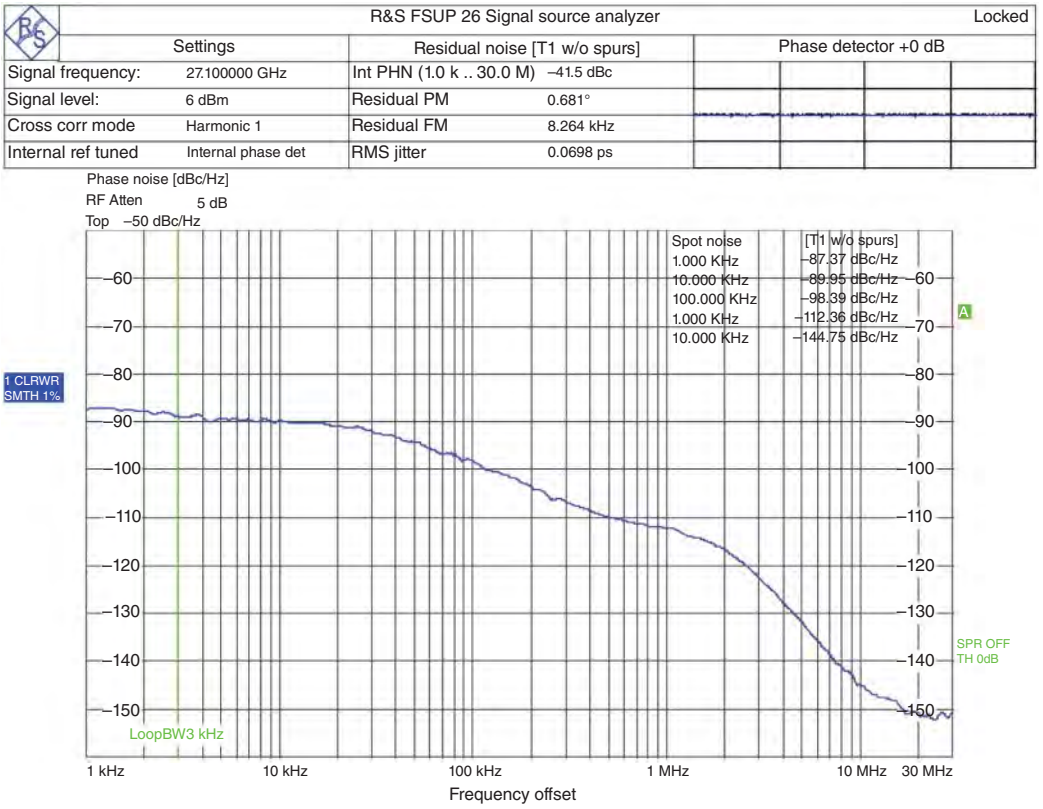


Figure 3-23 Single loop fractional-*N* phase locked VCO with 100 MHz reference.

noise feedback system. Figure 3-25 shows a circuit in which a PAL delay line and a variable phase shifter are used to stabilize an oscillator if the proper bandwidth and phase offset are chosen. The close-in noise sideband performance of the oscillator can drastically be improved. This circuit has actually been used in some German ham equipment and in the Fluke synthesized signal generator Models 6070A and 6071A. In the case of the Fluke model, a SAW delay line is used, and, as shown in Figure 3-26, by using a subsynthesizer system, a 240- to 520-MHz oscillator is improved by this technique, and the subsynthesizer from 0.8 to 1.2 MHz provides increased resolution down to 1 Hz.

The ultimate resolution of this system is determined by the subsynthesizer, which, as discussed earlier, might be a direct digital synthesizer.

The special loops we have seen so far showed an increase in resolution with the trade-off of losing accuracy.

The very new topics for delay-line use are the opto-electric synthesizers; see Appendix F on Opto-electronic Oscillators.

The fractional division *N* synthesizer offers, theoretically, unlimited resolution and extremely fast settling time. We will learn more about this in Section 3-4.

3-4 FRACTIONAL DIVISION *N* SYNTHESIZERS

Conventional single-loop synthesizers use frequency dividers where the division ratio *N* is an integer value between 1 and several hundred thousand, and the step size is equal to the reference frequency. Because of the loop filter

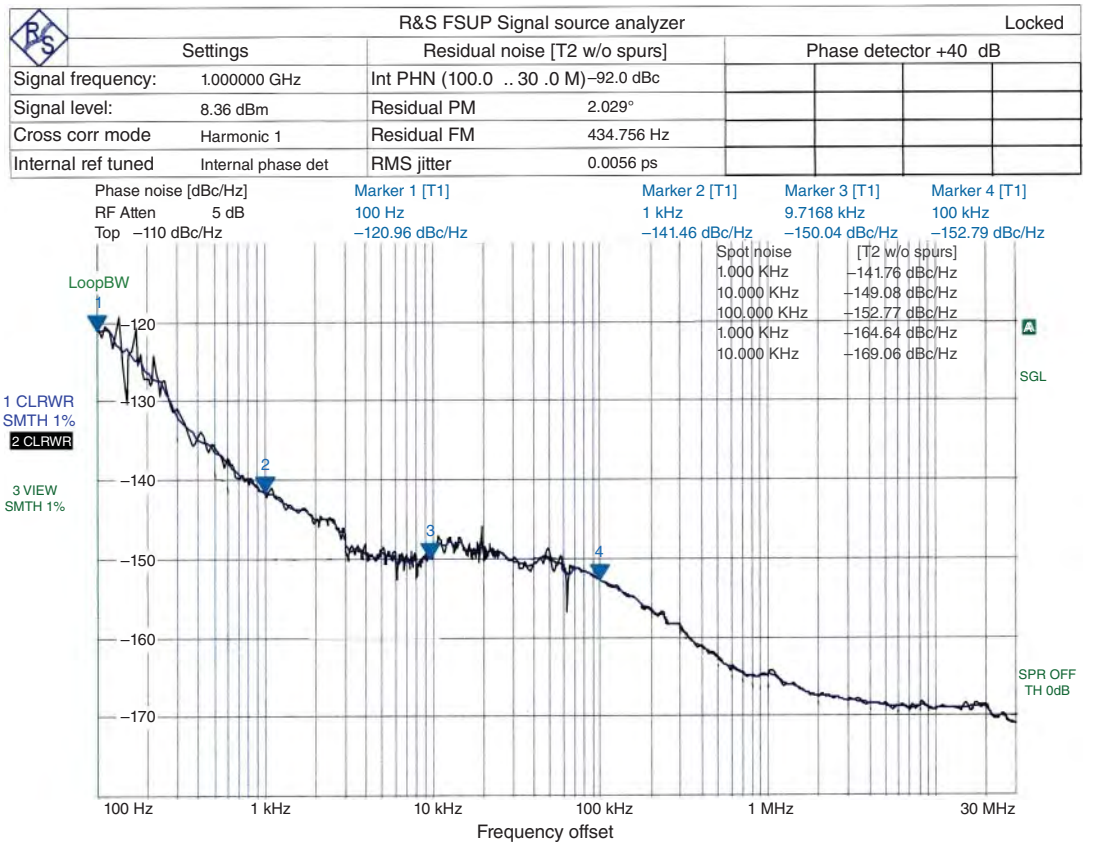


Figure 3-24 Phase-locked SAW oscillator at 1 GHz.

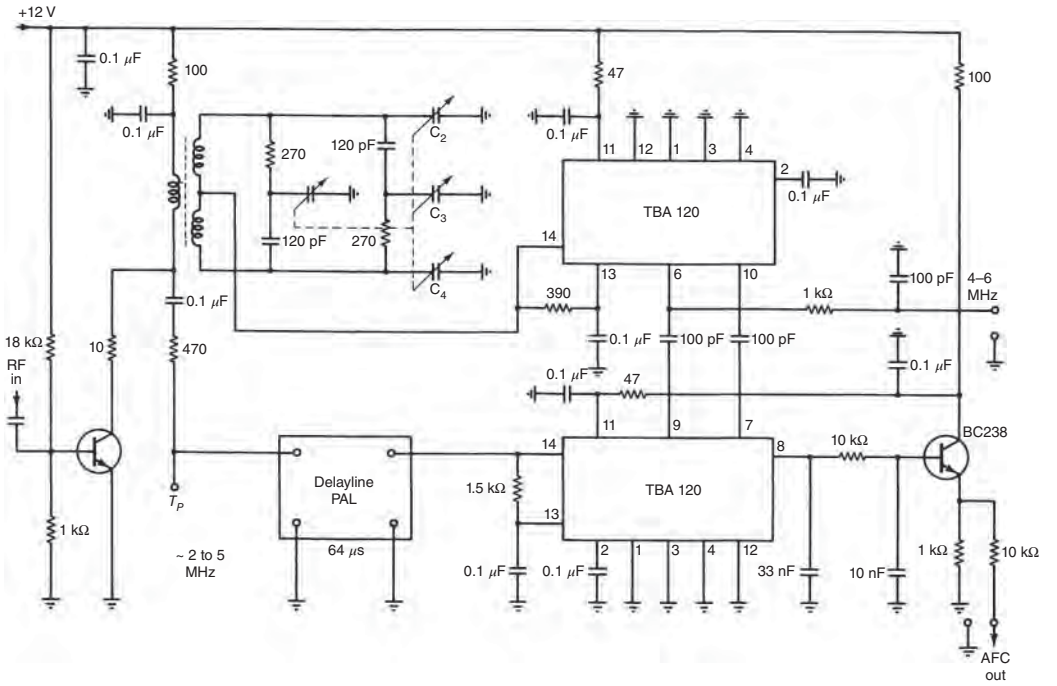


Figure 3-25 Schematic of a delay-line-stabilized oscillator system.

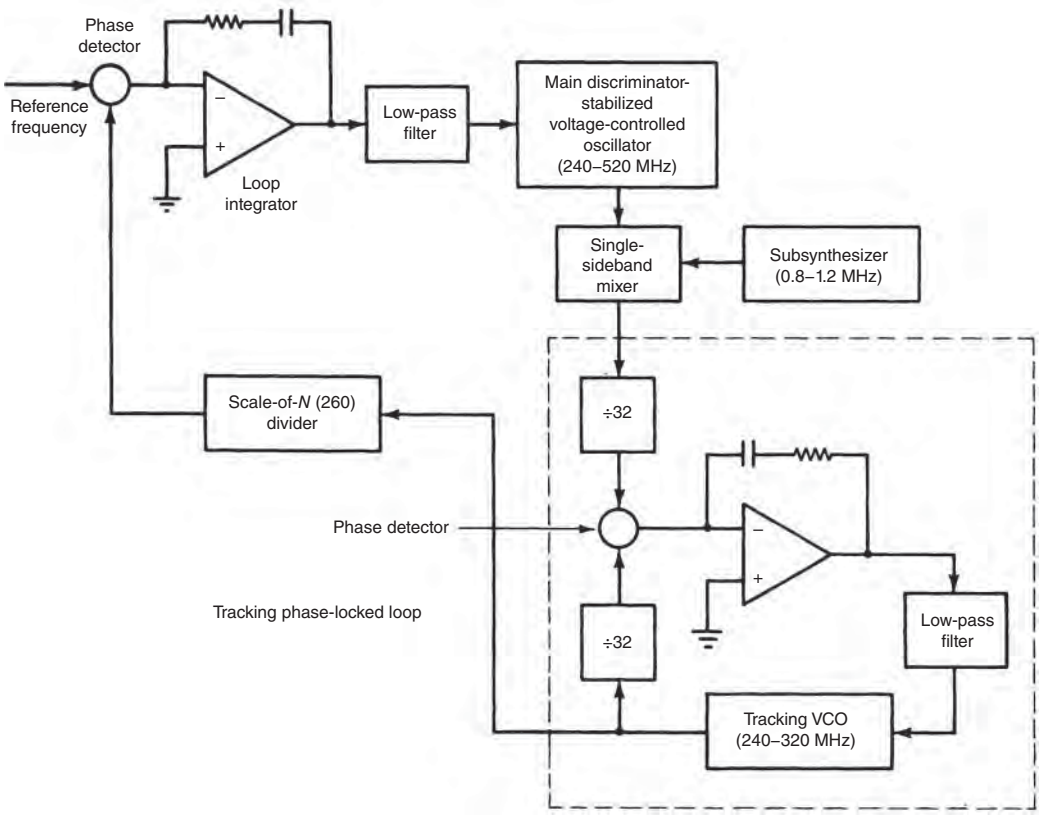


Figure 3-26 Block diagram of the Model 6070A delay-line-stabilized Fluke synthesizer.

requirements, the decrease of reference frequency automatically means an increase of settling time. It would be unrealistic to assume that a synthesizer with lower than 100-Hz reference can be built, because the large division ratio in the loop would reduce the loop gain so much that tracking would be very poor, and the settling time would be several seconds.

If it were possible to build a frequency synthesizer with a 100-kHz reference and fine resolution, this would be ideal because the VCO noise from 2 or 3 kHz off the carrier could determine the noise sideband, while the phase noise of frequencies from basically no offset from the carrier to 3 kHz off the carrier would be determined by the loop gain, the division ratio, and the reference. Because of the higher reference frequency, the division ratio would be kept smaller. Traditionally, this conflicting requirement resulted in multiloop synthesizers.

An alternative would be for N to take on fractional values. The output frequency could then be changed in fractional increments of the reference frequency. Although a digital divider cannot provide a fractional division ratio, ways can be found to accomplish the same task effectively. The most frequently used method is to divide the output frequency by $N + 1$ every M cycles and to divide by N the rest of the time. The effective division ratio is then $N + 1/M$, and the average output frequency is given by

$$f_o = \left(N + \frac{1}{M}\right) f_r \tag{3-28}$$

This expression shows that f_0 can be varied in fractional increments of the reference frequency by varying M. The technique is equivalent to constructing a fractional divider, but the fractional part of the division is actually implemented using a phase accumulator. The phase accumulator approach is illustrated by the following example.

3-4-1 Example Implementation

Consider the problem of generating 455 kHz using a fractional N loop with a 100-kHz reference frequency. The integral part of the division $N = 4$ and the fractional part $1/M = 0.55$ or $M = 1.8$ (M is not an integer); the VCO output is to be divided by $5(N + 1)$ every 1.8 cycles, or 55 times every 100 cycles. This can easily be implemented by adding the number 0.55 to the contents of an accumulator every cycle. Each time the accumulator overflows (the contents exceed 1) the divider divides by 5 rather than 4. Only the fractional value of the addition is retained in the phase accumulator.

Arbitrarily fine frequency resolution can be obtained by increasing the length of the phase accumulator. For example, with a 100-kHz reference a resolution of $10^5/10^5 = 1$ Hz can be obtained using a five-digit BCD accumulator.

This method[1], which we will analyze now in greater detail, is used in a number of instruments, such as Hewlett-Packard generators and spectrum analyzers, where it is called fractional N synthesizer, whereas the earlier version, called the digiphase system, is used in the Dana series 7000 synthesizers. A modification of the digiphase system that reduces the low-frequency content of the phase detector output is used in the Racal receiver RA6790. Racal has applied for a patent for this method.

We will now discuss the advantages and drawbacks of this system. At first it may appear that the fractional N loop has unlimited advantages. However, in reality, it is a compromise between resolution, spurious response, and lockup time. Reference [2] may help to clarify the applications further. In reality, the expression fractional N is not quite correct. The loop does not supply a fractional division ratio but rather changes the division ratio periodically over a certain period with the help of an adder driven by the fraction register.

The fractional N phase-locked loop (*NF loop*) is a modified divide-by-N loop. Its unique feature is that it can operate at fractional multiples of the reference signal instead of steps. In the NF loop, N refers to the integer part and F to the fractional part of the divide-by-N number. This number multiplied by the reference signal represents the loop frequency. The integer part is that of a divide-by-N loop. The fractional part represents the offset frequency of the VCO with respect to the integer component of frequency.

The description of the NF loop is divided into two parts. The first is a general discussion of the NF loop concept using example frequencies. The second describes the NF loop using simplified block diagrams.

Consider the divide-by-N loop phase detector output under open-loop condition. Assume a reference frequency of 100 kHz, $N = 10$, and VCO frequency of 1.01 MHz ($N = 1.0$ MHz; $F = 0.01$ MHz). The VCO operates at a fractional multiple (10.1) of the reference signal (10.1×0.1 MHz $= 1.01$ MHz). This configuration is shown in the block diagram of Figure 3-27. The phase detector compares the low-to-high transitions of the reference and divide-by-N signals. Since the VCO is not operating at N times the reference but with a fractional component ($F = 0.01$ MHz), the signal from the divide-by-N block advances on the reference signal. Each time the divide-by-N signal makes a low-to-high transition, the phase detector compares it with the reference and generates an output

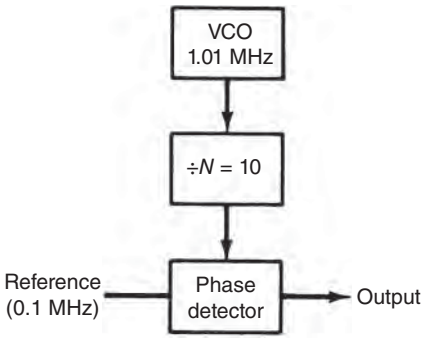


Figure 3-27 Basic diagram of an open-loop divide-by-N loop.

[1]Part of this description is based on the Hewlett-Packard 3335A signal generator and reproduced with permission.

Table 3-1 Phase relationship of $N \times f_{ref}$ and NF.

Number of reference periods (f_{ref} = 100 kHz = 0.1 MHz)	Number of completed cycles of:		Phase advancement of NF on $N \times f_{ref}$
	$N \times f_{ref}$ = 1 MHz (N = 10)	NF = 1.01 MHz	
1	10	10.1	0.1 cycle of phase
2	20	20.2	0.2 cycle of phase
3	30	30.3	0.3 cycle of phase
4	40	40.4	0.4 cycle of phase
.	.	.	.
.	.	.	.
.	.	.	.
9	90	90.9	0.9 cycle of phase
10	100	101.0	1 full cycle of phase (360°)

proportional to the period between the two low-to-high transitions. In the phase-locked condition of a divide-by-*N* loop, this period remains constant. In the open-loop example, where the VCO contains a fractional component, the period between low-to-high transitions continuously increases, resulting in an increasing phase detector output voltage.

When analyzing the open-loop divide-by-*N* loop, it is of interest to view the operation in terms of *reference periods*. A reference period is defined as the time required for the reference signal to complete one cycle. Each reference period, the reference signal goes through one cycle while the VCO, which is operating 10.1 times as fast, goes through 10.1 cycles. We can say the VCO has advanced one-tenth of a cycle of phase on the integer part $N \times f_{ref}$ (f_{ref} = reference frequency) in one reference period. In two reference periods, the VCO has gone 20.2 cycles or advanced two-tenths of a cycle of phase on $N \times f_{ref}$. When the VCO operates with a fractional offset (F), it continually advances phase on $N \times f_{ref}$ each reference period. From the example of Figure 3-25, in 10 reference periods, the VCO signal will have gone 101 cycles, or advanced one cycle of phase (360°) with respect to $N \times f_{ref}$. Table 3-1 illustrates the phase relationship of $N \times f_{ref}$ and NF.

While the VCO signal advances phase on $N \times f_{ref}$, the divide-by-*N* VCO signal applied to the phase detector advances phase on the reference frequency.

In a divide-by-*N* loop, the VCO is phase locked to a reference signal and operates at a multiple *N* of the reference frequency ($N \times f_{ref}$). In an NF loop, the VCO operates at an integer-plus-fractional multiple of the reference frequency ($N \times f_{ref} + F$ = NF). As previously illustrated in Figure 3-25, assume again that the VCO operates at 1.01 MHz, the reference is 0.1 MHz, and *N* equals 10. Each time the reference signal goes through one cycle, the VCO goes through 10.1 cycles. After 10 reference cycles (10 reference periods), the VCO has gone 101 cycles. The VCO has advanced one full cycle of phase (360°) on $N \times f_{ref}$. If a VCO cycle is removed from the VCO pulse train applied to the divide-by-*N* block at the point a full VCO cycle has advanced, the phase advancement on the average is canceled and the average frequency applied to the divide-by-*N* block is $N \times f_{ref}$ or, in this example, 1 MHz.

Because of the continual removal of a VCO cycle (removal of one cycle of phase) at each point the VCO advances one cycle on $N \times f_{ref}$, the phase detector output becomes a sawtooth waveform (see Figure 3-28). The waveform increases linearly due to the advancing phase of the VCO until the VCO has advanced one cycle of VCO phase (360°). At this point a cycle is removed from the VCO pulse train, canceling the previous advancement of a cycle of phase. The phase detector responds to this sudden one-cycle (360°) phase loss by returning to its initial output. The sequence is repetitive, generating the sawtooth waveform. The maximum amplitude reached represents one cycle of VCO phase. As the VCO frequency is increased, the time interval for the VCO to go through one cycle of phase is less. Therefore, the maximum phase detector amplitude is decreased. The phase detector maximum amplitude is inversely proportional to the VCO frequency.

The necessity to remove one VCO cycle from the VCO output each time the output advances one cycle of phase $N \times f_{ref}$ requires that we use a pulse remover block in the divide-by-*N* loop block diagram (see Figure 3-29). If a VCO pulse is removed each time the VCO advances one cycle of phase, the average frequency applied to the divide-by-*N* block is $N \times f_{ref}$ and the average frequency applied to the phase detector is f_{ref}. The relationship of the phase detector sawtooth output and the pulse trains is illustrated in Figure 3-30. A method of determining when the

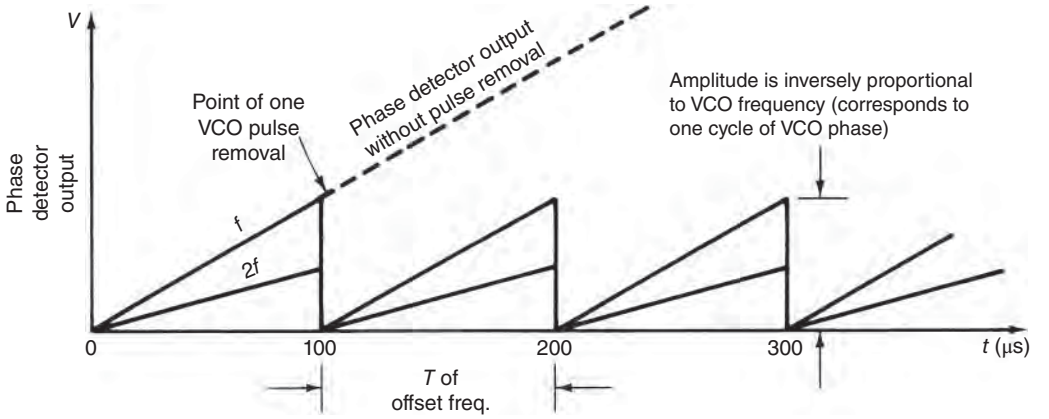


Figure 3-28 Phase detector sawtooth output.

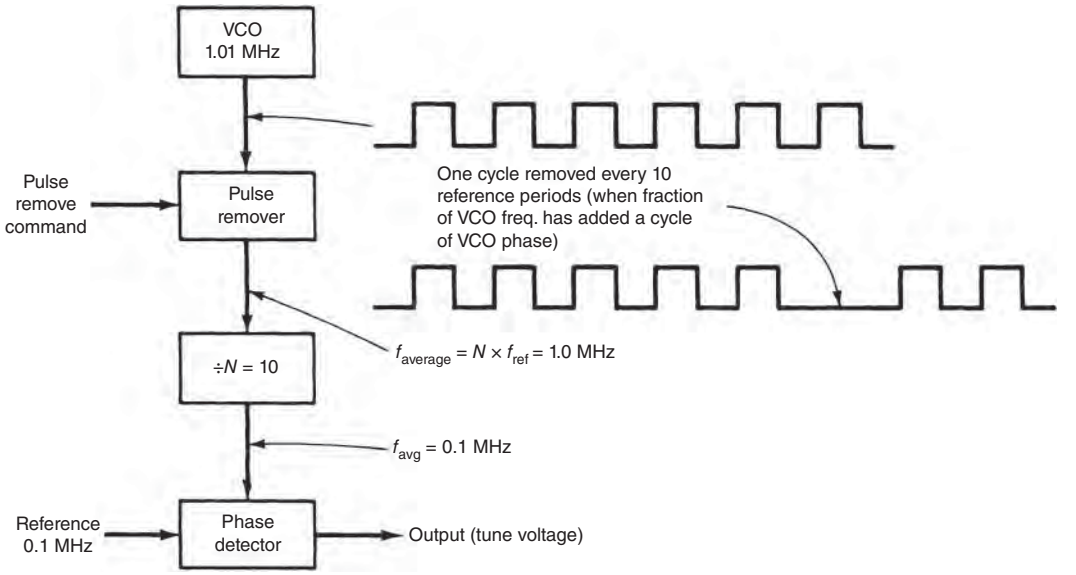


Figure 3-29 Divide-by-*N* loop with pulse remover block.

VCO has advanced one cycle of phase is required. Such information can then be used to trigger the pulse remover block and a VCO cycle removed at the appropriate time.

The fractional part of the VCO frequency determines the time required for the VCO to advance one cycle of phase $N \times f_{ref}$. The time required is the period of the fractional offset frequency and corresponds to a certain number of reference periods. If the fractional part of the VCO is stored in a register added to a second register each reference period, the second register will contain a running total that represents the VCO phase advancement at any point in time. For this reason the second register is called a *phase register* and the entire configuration is called an *accumulator* (see Figure 3-31). The phase register will reach unity after the same reference period during, which the VCO has advanced one full cycle of phase. (Recall the preceding example: in one reference period the VCO has gone 10.1 cycles, in two reference periods the VCO has gone 20.2 cycles, and so on. The summing register will contain 0.1 after one reference period, 0.2 after the second, and so on.) When unity is reached, the phase register

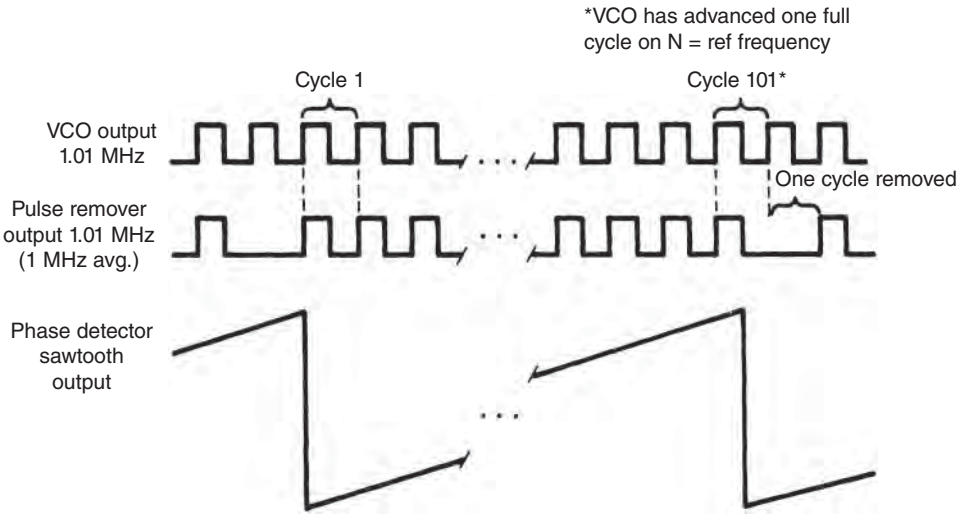


Figure 3-30 Phase detector sawtooth output with respect to pulse remover output.

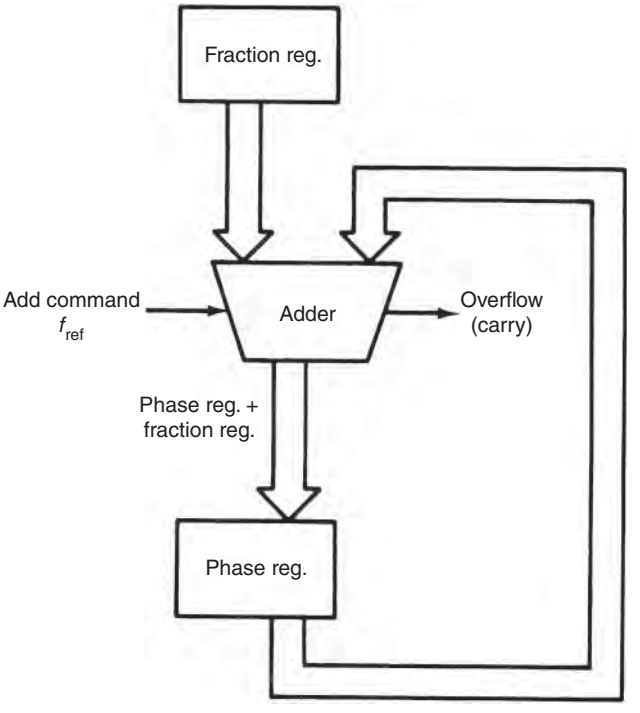


Figure 3-31 Accumulator.

overflows and transmits an overflow signal. This signal occurs at the time the VCO has advanced one cycle of phase on $N \times f_{ref}$ and is applied to the pulse remover block as a pulse remove signal.

If the VCO operates with an offset frequency not evenly divisible into 1 (such as 0.03), a fractional overflow can result when the phase register reaches unity. For example, if the VCO operates at 1.03 MHz instead of 1.01 MHz, after one reference period it has gone 10.3 cycles, 20.6 after two, 30.9 after three, and 41.2 after the fourth reference period. Prior to the fourth reference period, the phase register has accumulated 0.9. The fourth reference period 0.3 is added to the 0.9 from the phase register and results in 1.2. This causes an overflow as the pulse remove signal and the fractional overflow of 0.2 is loaded into the phase register and the next sequence phase begins to accumulate from 0.2 instead of zero.

Up to this point, the discussion has developed the NF loop to include the pulse remove command section. Figure 3-32 is a block diagram of the NF loop with the pulse remove command section. This structure provides a means of automatically removing a VCO cycle whenever the VCO advances one full cycle of phase on the frequency $N \times f_{ref}$.

The open-loop phase detector output of Figure 3-29 is a sawtooth waveform superimposed on a dc voltage. Only the dc voltage of this output is of interest. A VCO requires a dc tune voltage to maintain a stable output signal. A sawtooth ac signal superimposed on the dc VCO tune voltage would cause VCO frequency modulation (FM). The ac component must be canceled or removed, leaving the dc component to tune the VCO to the proper frequency.

We know that the VCO output advances a fraction of a cycle of phase on $N \times f_{ref}$ each reference period. The fraction of a cycle of phase that the VCO is advanced at any one reference period is represented by the fractional sum in the phase register. (Recall that the phase register is incremented by the fractional VCO output each reference period.) For the example of Figure 3-29, the contents of the phase register when viewed with respect to time can be represented as a staircase resetting to zero once unity is reached (see Figure 3-33). The staircase approximates a sawtooth waveform (see dashed lines). The "front edge" of each step represents the phase detector output for that reference period. (Recall that the phase detector does not generate a ramp but samples the VCO with respect to the reference each reference period.)

If the contents of the summing register are applied to a digital-to-analog (D/A) converter, the D/A converter output will follow the steps of the summing register and approximate a sawtooth output. Inverting the D/A converter

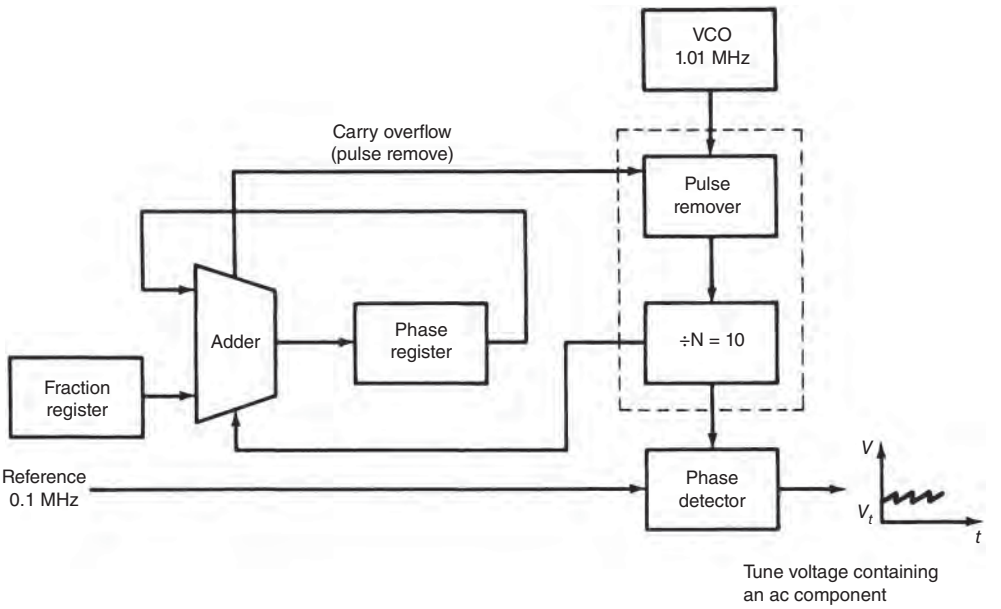


Figure 3-32 NF loop with pulse remove command section.

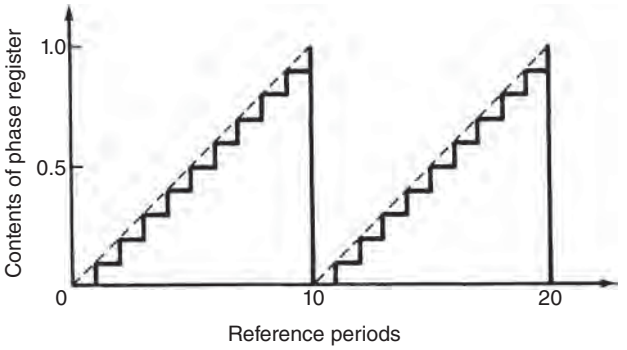


Figure 3-33 Phase register contents.

output and summing it with the phase detector output essentially cancels the ac component (sawtooth) of the phase detector output. This leaves the dc component required as a VCO control signal.

Two requirements exist for the waveform generated by the D/A converter to approximate the phase detector sawtooth output.

- It must have a variable amplitude.
- It must have a variable period.

The amplitude is inversely proportional to the frequency of the VCO and changes whenever the VCO frequency is changed. To demonstrate the amplitude dependency on the VCO frequency, refer to Figure 3-34.

In the figure a reference of 0.1 MHz is used (horizontal axis plotted in reference periods) and plots of the phase detector output for VCO frequencies of 1.01 MHz and 2.01 MHz are shown. Note that each VCO frequency example contains a 0.01-MHz offset or fractional frequency. In terms of reference periods (10 μs), the period of the 0.01-MHz offset is 10 reference periods. At this point the offset frequency has completed one cycle and added a cycle of phase to the VCO signal. Since the period of 2 MHz is half the interval of 1 MHz, the phase detector output representing one cycle of phase at 2 MHz is half the amplitude of the output, representing one cycle of 1 MHz phase. When the VCO cycle is removed, a 360° phase loss is detected by the phase detector and it responds by returning to its initial output, causing the high-to-low transition of the sawtooth. If the offset or fractional part of the VCO frequency is changed, the period of the sawtooth changes for these two periods are the same. The sawtooth

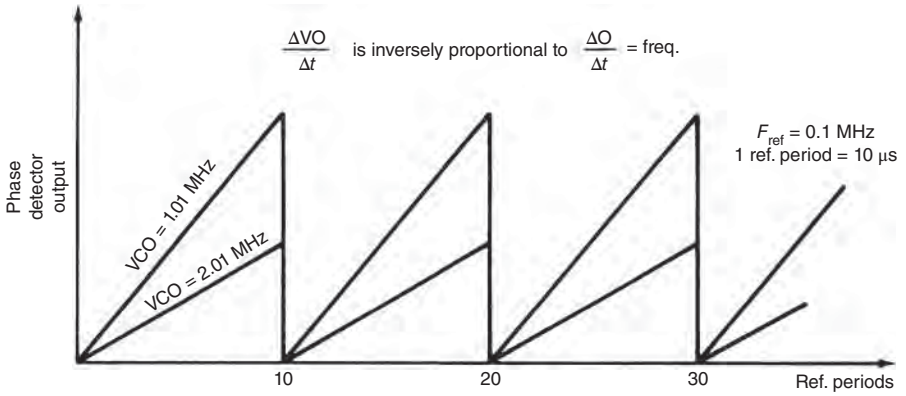


Figure 3-34 Phase detector output for two VCO frequencies with the same offset.

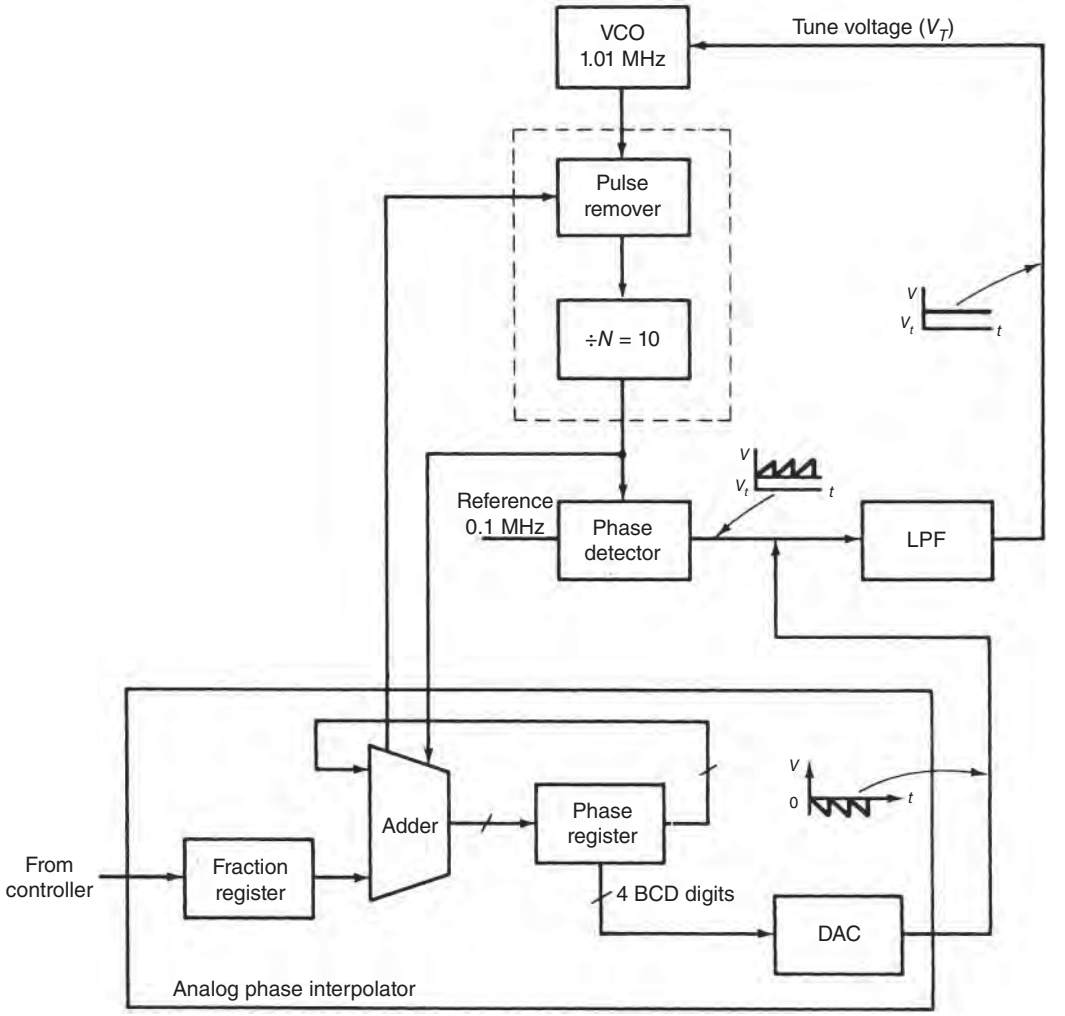


Figure 3-35 General block diagram of an NF loop.

generated by the D/A converter must change amplitude and period as the phase detector output changes and must be superimposed on zero volts dc. It can then be inverted and summed with the phase detector output to remove the sawtooth from the tune voltage applied to the VCO.

A general block diagram of an NF loop is shown in Figure 3-35. The basic elements of a divide-by-*N* loop are present: the VCO, divide-by-*N* counter, phase detector, and LPF. In addition to these, a fraction register, adder, and phase register provide the "bookkeeping system," recording the phase advancement from reference period to reference period. This system is known as a *phase interpolator*, and in conjunction with a DAC the system is referred to as an *analog phase interpolator* (API). During each reference period it generates an analog voltage equal and opposite in polarity to the phase advancement voltage generated by the phase detector. The voltage applied to the LPF is then the net VCO tune voltage. Since the "bookkeeping system" must update each reference period (the phase detector output changes each reference period after the VCO/*N* and reference signal comparison), the system receives its add command (update command) at a VCO/*N* rate.

The NF loop is a modified divide-by-*N* loop. It contains all the basic elements of the divide-by-*N* loop with the addition of several other sections. Figure 3-36 illustrates the additions made to the "loop." These additions are a

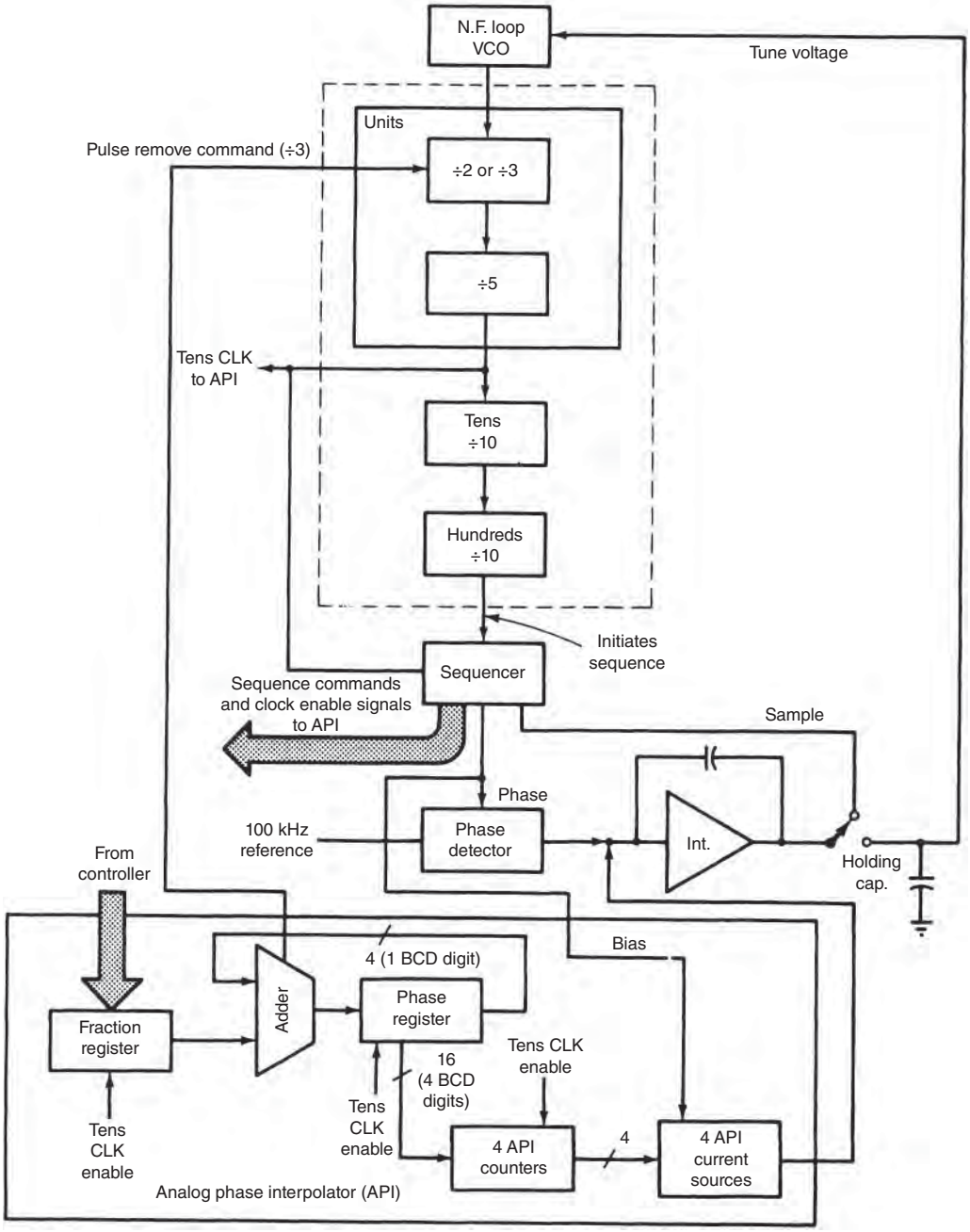


Figure 3-36 Basic block diagram of an NF loop.

sequencer, an N counter that can be changed to an $(N + 1)$ counter, and an integrator and sample/hold, which are used to develop the tune voltage. Compare this diagram with Figure 3-33.

The NF loop operates according to an established sequence of events that occur once each reference period. The sequence is initiated at a rate equal to the VCO/N signal. This is accomplished by initiating each sequence of events with the N counter output. The sequencer generates a number of enable and command signals, which are summarized here.

(1) *API Tens Clock Enable Signals*. These signals enable the Tens Clock to update the data in the API registers (bookkeeping system).
(2) *API Counter Tens Clock Enable*. This signal enables the Tens Clock to clock the four API counters, which are preset each reference period by the four most significant digits of the phase register, which keeps a running total of the phase advancement.
(3) *Bias Command*. This signal turns on the four API current sources to establish a current reference point.
(4) *Phase Command*. This signal is the Bias command reclocked to the Tens Clock and again reclocked to the NF loop VCO. It is compared with the reference each reference period by the phase detector.
(5) *Sample Command*. This signal initiates the sampling of the integrator output each reference period. Once the integrator has settled following the summation of the phase detector and API signals, the integrator voltage is transferred to the holding capacitor.

The rate of events is determined by the Tens Clock, which is the NF loop VCO divided by 10. The sequence of events is initiated once each reference period, but once initiated, the events occur at a rate determined by the VCO frequency.

Figure 3-37 illustrates the loop by a heavy line and separates between digital and analog halves of the loop. The basic structure is shown in Figure 3-38. The major sections of the loop structure are input, decode and data registers, divide-by-N with pulse remove, sequencer, phase detector, API, integrator, sample-and-hold, and VCO.

The input decode section interfaces the loop with the data transmitted by the controller. These data include the loop frequency and instructions that set up the operating modes of the data registers in the phase interpolator. Data register operation is controlled by a steering section.

The data registers comprise the bookkeeping scheme of the phase interpolator. There are three data registers:

(1) f_1 frequency register
(2) f_2 frequency register
(3) Phase register

Only one of the frequency registers is active at a time. The frequency register will always contain the current frequency of operation and these data will be circulated (output connected to input and the data shifted until the starting state is reached) once each reference period. The other frequency register contains the previous frequency of operation and rests idle but enabled to accept new data when a new output is programmed.

The data steering logic controls the operating modes of the f_1 and f_2 frequency registers. The Load Data command enables the idle frequency register to be clocked by the controller line Load Data Clock (LDC) to enter a new frequency. During this time the operation of the loop is not interrupted because the circulating frequency register continues operation while data are being loaded. Once the data are entered, the Set Freq command interchanges the functions of the f_1 and f_2 registers and the new data now circulate to operate the loop at the new frequency.

Frequency data in the f_1 or f_2 register consist of 16 BCD digits, which are loaded least significant digit first. The 12 least significant digits represent the fractional portion of the frequency, and the next three digits contain the integer or N portion of the frequency. This accounts for 15 of the 16 digits in the f_1 or f_2 register. The sixteenth digit, which is the last digit loaded, is not required and therefore is always loaded as a zero. During circulation of the data in the f_1 or f_2 register, this digit is truncated and does not affect the operation of the loop.

During each reference period the divide-by-N counter initiates a sequence of events by triggering the sequencer. Part of the sequence is the enabling of the f_1 or f_2 register clock, the phase register clock, and the N register clock.

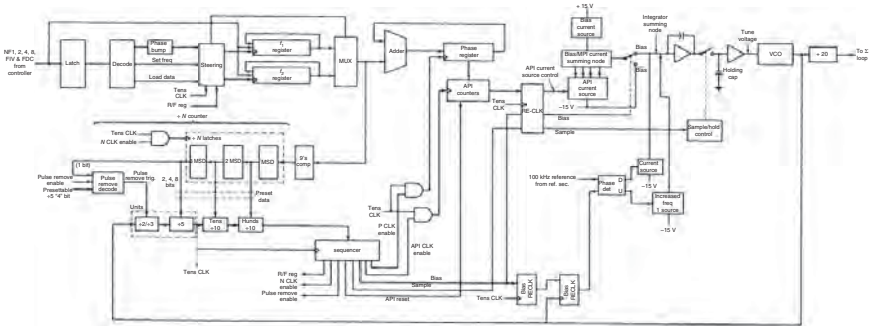


Figure 3-37 Block diagram of a fractional *N* loop.

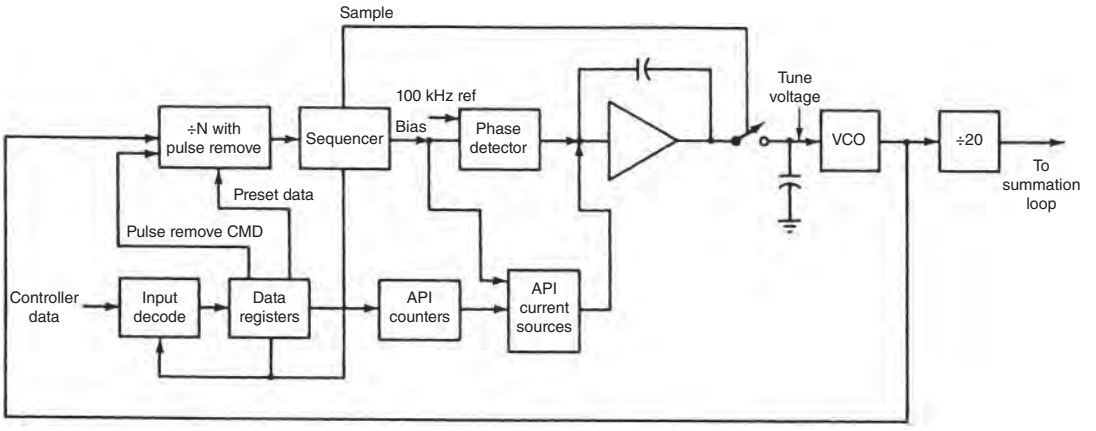


Figure 3-38 Basic structure of an NF loop.

The phase register is clocked for the first 12 digits circulated by the f_1 or f_2 register, the N register for the next three. When the 16th digit is circulated by the f_1 or f_2 register, neither phase register nor N register is clocked; therefore, this digit has no effect on the loop operation. As a result of the sequence of clocking the registers and N register, the phase register quantity has been increased by the fractional component of the f_1 or f_2 register. The N register contains the three N number digits used to preset the divide-by-N counter.

The phase register serves two purposes:

- Records the total phase advancement of the VCO with respect to each reference period.
- Causes the adder to overflow in the reference period during which the VCO has advanced a full cycle of phase.

The record of total phase advancement is used each reference period to drive the API section. The four most significant digits of the 12 digits in the phase register are used to preset four API counters. When these counters are clocked by the API clock, they generate an output pulse inversely proportional to the preset number and drive the API section, which develops a signal that counteracts the changing phase detector signal, resulting in an unchanging tune voltage. The overflow of the adder indicates the reference period in which the NF loop VCO has advanced a full cycle of VCO phase. The overflow decode triggers the units counter during the pulse remove enable interval of the loop sequence to divide by 3 for one output pulse of the first stage. Since this stage has been providing an output for every two input pulses (divide by 2), it effectively has removed a VCO cycle by dividing by 3 for one output pulse. The cycle of phase the NF loop VCO has advanced has been removed and the phase relationship of the NF loop VCO and N times the reference is reset.

The API section consists of two parts:

- The API counters
- The API current sources

All API current sources are turned on by the Bias command each reference period. The four most significant digits of the phase register preset the API counters, which control when each of the four API current sources turn off. The smaller the phase register digits, the longer the API current sources are on.

The phase detector compares the sequencer output "Bias" with a 100-kHz reference signal. The Bias signal is first reclocked to Tens Clock (VCO/10) and then to the NF loop VCO signal itself. If the NF loop VCO is operating with a fractional component, the reclocked Bias signal applied to the phase detector gains phase each reference

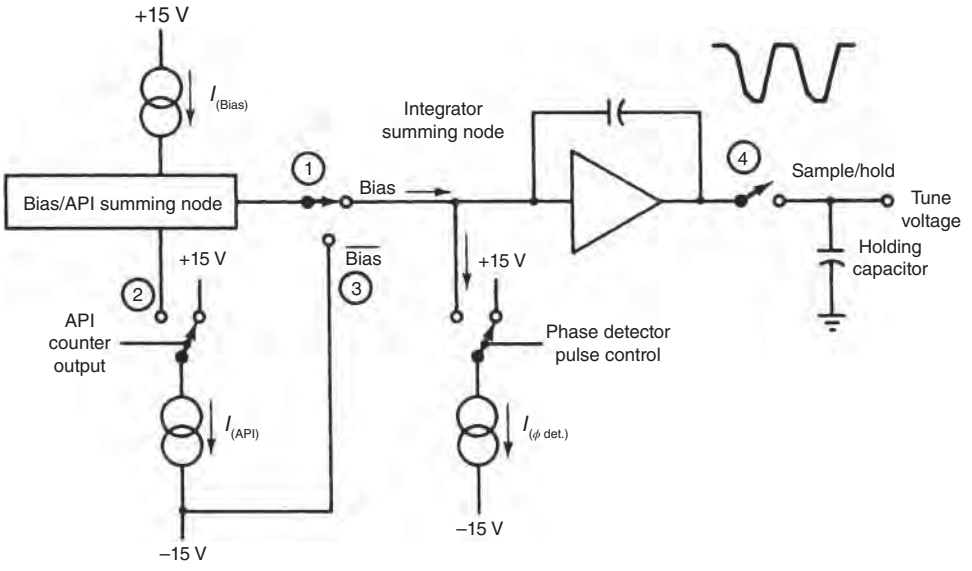


Figure 3-39 NF loop integrated currents.

period with respect to the reference signal. The output applied to the integrator is an increasing voltage. The purpose of the API section is to negate the effects of the increase in the phase detector output.

The method used to generate the NF loop VCO tune voltage is similar to that used in the divide-by-*N* loop. Currents are integrated and the integrated voltage is transferred to a holding capacitor.

A block diagram of the currents integrated by the NF loop in a phase-locked condition is shown in Figure 3-39. Figure 3-40 illustrates the integrator waveform, showing the contributions of the different currents. A constant-current source, *I* (Bias), supplies current at all times to the Bias/API summing node. The Bias command from the sequencer goes high each reference period to connect this node to the integrator summing node. Following the Bias command, the phase register data cause the API current source to draw current from

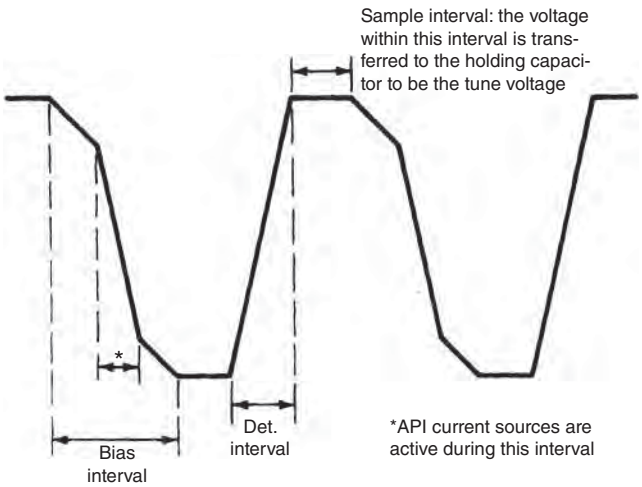


Figure 3-40 Integrator waveform showing the contributions of the different currents.

the Bias/API summing node and therefore keep this current from being integrated. The amount of API current is determined by the magnitude of the phase register number. Once the Bias event has occurred and the Bias/API summing node is disconnected from the integrator summing node, the phase detector pulse occurs and draws current out of the integrator summing node. When the loop is phase locked, the current entering the integrator node from the Bias/API current sources is equal to the current drawn out by the phase detector current source and the integrated voltage remains constant. After integrating the two currents, the voltage is transferred to a holding capacitor and becomes the tune voltage.

The sequence of events is as follows:

(1) The Bias/API summing node is connected to the integrator and the Bias current is integrated.
(2) The API current source is connected to the Bias/API summing node, decreasing the amount of Bias current integrated.
(3) The Bias/API summing node is disconnected and the phase detector is connected to the integrator. The phase detector current is integrated.
(4) After the phase detector current has been integrated and the voltage has settled, the voltage is transferred to a holding capacitor. This voltage is the NF loop VCO tune voltage.

Note: When phase locked, the Bias/API current is equal to the phase detector current. The API current tracks the increasing phase detector current, canceling the fractional component of VCO phase.

Refer again to Figure 3-35. Assume that the loop operates without a fractional component (data in the phase register remain constant). The loop can be viewed as just a divide-by-*N* loop with an elaborate method of developing the tune voltage. The data in the phase register are constant; therefore, the API current sources are sinking the same amount of current from the Bias/API summing node each reference period. Since the current entering the integrator from the Bias/API summing node is always a constant value, the phase detector changes the tune voltage just as it does in the divide-by-*N* loop. A change in the phase relationship causes the phase detector pulse to change in duration, which changes the amount of current the phase detector source draws from the integrator. The result is a change in the integrated voltage after this reference period, and therefore the tune voltage has been changed. The direction of change is such that the NF loop VCO is pulled back into a phase-locked condition.

The Sample command from the sequencer transfers the integrated voltage to the holding capacitor at the appropriate period of the integrator output. This period occurs after the Bias/API summing interval and the phase detector interval have occurred and the integrator output has returned to an unchanging value. This value is the tune voltage.

The increase-frequency current source is shown on the simplified block diagram of Figure 3-35. This current source is also connected to the integrator summing node and is responsible for rapidly changing the tune voltage if a large increase in frequency is programmed; the phase detector connects this current source to the integrator in place of the phase detector current source. Instead of sinking current from the integrator, the current source drives current into the integrating node to add to the current already supplied by the Bias/API interval. This causes the tune voltage to change the NF loop VCO frequency rapidly. Once the newly programmed frequency has been reached, the phase detector again begins operation using the phase detector current source.

The NF loop VCO signal is divided by 20 to aid spur attenuation and reduce phase noise. The division by 20 results in an improvement of 26 dB in the noise sideband and phase noise.

While this system allows extremely high resolution, the synthesizer, so to speak, consists of two loops, one being a 100-kHz loop with the lockup time probably 8–20 cycles of reference or 800 μs to 2 ms, depending on the loop filter.

The fractional portion of the loop theoretically would lock up within one cycle of reference or 10 μs. However, because of active LPFs and speed requirements for the D/A converter, the actual lockup time is somewhat of a compromise between these values and should be in the vicinity of 1–2 ms and, therefore, about the same as the 100 kHz loop.

Modern integrated circuits having frequency synthesizers on one chip can be used to build such systems. The Philips Semiconductor SA 7025 low-voltage 1-GHz Fractional-*N* Synthesizer works on the principle just outlined and is ideal for use in cellular telephones.

The noise sideband performance of this synthesizer depends highly on the accuracy of the D/A converter and its ability to remove the reference noise sideband. Reference [22] discusses a method used in the Racal receiver for which Racal has applied for a patent, and this phase detector output has a zero-running average area. This is effective in reducing the low frequencies produced when the output is near a multiple of the reference and when many corrections are made during each period of the phase detector output (see Refs. [18–38].)

3-4-2 Some Special Past Patents for Fractional Division *N* Synthesizers

1. Latched accumulator fractional *N* synthesis with residual error reduction
   Alexander W. Hietala, Cary, IL; Duane C. Rabe, Rolling Meadows, IL Motorola, Inc., Shaumburg, IL
   United States Patent, Patent No. 5,093,632, March 3, 1992
2. Frequency synthesizers having dividing ratio controlled sigma-delta modulator
   Thomas A. D. Riley, Osgoode, Canada Carleton University, Ottawa, Canada
   United States Patent, Patent No. 4,965,531, October 23, 1990
3. Phase-locked loop variable frequency generator
   Nigel J. R. King, Wokingham, England Racal Communications Equipment Limited, England
   United States Patent, Patent No. 4,204,174, May 20, 1980
4. Frequency synthesizers
   John Norman Wells, St. Albans, Hertfordshire (GB) Marconi Instruments, St. Albans, Hertfordshire (GB)
   European Patent, Patent No. 0125790B2, July 5, 1995
5. Improvement in or relating to synthesizers
   Thomas Jackson, Twickenham, Middlesex (GB) Plessey Overseas Limited, Ilford, Essex (GB)
   European Patent, Patent No. 0214217B1, June 6, 1996
6. Improvement in or relating to synthesizers
   Thomas Jackson, Twickenham, Middlesex (GB) Plessey Overseas Limited, Ilford, Essex (GB)
   European Patent, Patent No. WO86/05046, August 28, 1996
7. PLL including an arithmetic unit
   Robert J. Bosselaers
   United States Patent, Patent No. 3913928, October 1975
8. Frequency synthesizer
   R. G. Cox, Hewlett-Packard
   United States Patent, Patent No. 2976945
9. Device for synthesizing frequencies with fractional multiplier of a fundamental frequency
   C. A. Kingford-Smith, Hewlett-Packard
   United States Patent, Patent No. 3928813
10. PLL frequency synthesizer including fractional digital frequency divider
    A. T. Crowley, RCA
    United States Patent, Patent No. 4468632
11. Enhanced analog phase interpolation for fractional-TV frequency synthesizer
    J. K. Crowford, Hughes Aircraft Company
    United States Patent, Patent No. 4586005
12. Frequency synthesizer having jitter compensation
    Y. D. McCann, U.S. Phillips
    United States Patent, Patent No. 4599579
13. Frequency synthesizer with spur compensation
    F. L. Martin, Motorola
    United States Patent, Patent No. 4816774
14. Frequency synthesizer with spur compensation
    F. L. Martin, Motorola
    United States Patent, Patent No. 4918403

15. Fractional-N synthesizer having modulation spur compensation
W. P. Sheperd et al., Motorola
United States Patent, Patent No. 5021754

16. Multiple modulation fractional-N divider
B. M. Miller, Hewlett-Packard
United States Patent, Patent No. 5038117

17. Frequency-modulated PLL with fractional-N divider and jitter compensation
M. A. Wheatley et al., Racal Dana
United States Patent, Patent No. 5038120

18. Digital frequency synthesizer
W. G. Greken, General Dynamics
United States Patent, Patent No. 3882403

19. Frequency synthesizer having fractional-N frequency divider in PLL
W. J. Tanis, Engelman Microwave
United States Patent, Patent No. 3959737

20. Frequency synthesizer with fractional-N division ratio and jitter compensation
N. G. Kingsbury, Marconi
United States Patent, Patent No. 4179670

21. Frequency synthesizer including a fractional-N multiplier
J. Remy, Adret
United States Patent, Patent No. 4458329

22. Frequency synthesizer of the fractional-N type
T. Jackson, Plessey
United States Patent, Patent No. 4800342

23. Fractional-N frequency synthesizer with modulation compensation
C. Attenborough, Plessey
United States Patent, Patent No. 4686488

24. Fractional-N division FS for digital angle modulation
A. Albarello, Thomson-CSF et al.
United States Patent, Patent No. 4492936

25. Fractional-N frequency divider
R. O. Yeager, RCA
United States Patent, Patent No. 4573176

26. Low phase noise radio frequency synthesizer
A. P. Edwards, Hewlett-Packard
United States Patent, Patent No. 4763083

27. Programmable fractional-n frequency synthesizer
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E. J. Nossen
United States Patent, Patent No. 4206425, June 1980

31. Digital FS with random jittering for reducing discrete spectral spurs
    C. E. Wheatley
    United States Patent, Patent No. 4410954, October 1983
32. Digital FS
    Leland Jackson
    United States Patent, Patent No. 3735269, May 1973
33. Spurless fractional divider direct digital synthesizer and method
    V. S. Reinhardt, Hughes Aircraft
    United States Patent, Patent No. 4815018

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4

LOOP COMPONENTS

4-1 INTRODUCTION TO OSCILLATORS AND THEIR MATHEMATICAL TREATMENT

Modern communications systems need oscillators as part of the design. In most cases these oscillators are part of a synthesizer and they are voltage-controlled, meaning that the frequency is determined by tuning diodes, frequently called *varactors*. The applied dc voltage varies the frequency. For high-performance circuits the Colpitts oscillator is most frequently selected [1–30]. A large part of this work is taken from our books [5, 31] and reproduced with permission.

4-2 THE COLPITTS OSCILLATOR

The Colpitts oscillator comes in three flavors. Figure 4-1a shows the conventional circuit configuration. This type of circuit is based on a design developed by Edwin Henry Colpitts, known for his invention of this oscillator and hence carries his name [1]. It uses a capacitive voltage divider and an inductor. In reality, this simple circuit is not used but rather a derivation of this. This is shown in Figure 4-1b. The advantage of this circuit is that the values for C_1 and C_2 are fixed and the frequency change occurs by changing C_3. If the frequency of Figure 4-1a needs to be changed, a better choice is to vary the inductor L.

Colpitts colleague Ralph Hartley invented an inductive coupling oscillator [2]. The advantage of such an oscillator having capacitors C_1 and C_2 replaced with a tap of the inductor has been used together with helical resonators. The frequency tuning is achieved purely capacitively. To minimize loading, the transistor of choice here is an field effect transistor (FET), which has very high input impedance and provides minimum loading to the circuit. The disadvantage is that this circuit, using junction FETs, is limited to about 400 MHz. The transition frequency f_T is about 500 MHz. FETs can also be used in the Colpitts oscillator as shown in Figure 4-1a, because of relatively lower loading than the bipolar transistor. The drawback of Figure 4-1a is the heavy loading of the tuned circuit by the transistor. The circuit shown in Figure 4-1b is frequently referred to as the Clapp–Gouriet circuit [3].

At any frequencies, both GaAs FETs and complementary metal–oxide–semiconductor (CMOS) FETs are not a good choice because of their high flicker noise contribution.

For the circuit of Figure 4-1b, it is theoretically possible to have L and C_3 in resonance in which case the oscillator will cease to work. It is important to note here that the same circuit is used also for crystal oscillators; here the inductor L is replaced by the crystal. The crystal is a series combination of L_S, R_S, and C_S with $Q = \omega L/R$. In practice, the product of crystal Q and frequency is a constant. For 5 MHz, a typical Q of 2.5×10^6 is possible,

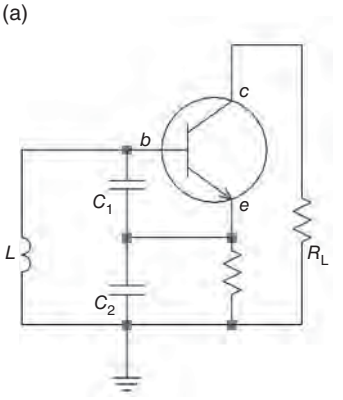


Figure 4-1a Conventional Colpitts configuration.

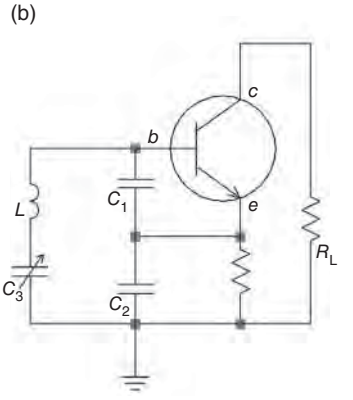


Figure 4-1b Modified Colpitts (Clapp–Gouriet) configuration.

resulting in a product of 12.5×10^{12}. If this is scaled to a crystal oscillator operating at 100 MHz, the Q would be 125,000. Manufacturers typically guarantee values greater than 100,000.

Again, this crystal oscillator also falls into the category of Colpitts oscillator. A third variation is shown in Figure 4-1c. Here, we have a parallel-tuned circuit that is coupled loosely to the transistor. This circuit is found when building oscillators using ceramic resonators (CROs). Figure 4-2 shows such a design.

This chapter summarizes the various methods of oscillator analysis and presents a step-by-step design procedure, showing the simulated, measured, and calculated results for phase noise and other important parameters, and concludes with a discussion on the effect of tuning diodes.

4-2-1 Linear Approach

For many years, until recently, oscillators were analyzed with a linear approach as will be shown below. Figures 4-3a and 4-3b illustrates the oscillator sub-circuit for the purpose of calculating the negative resistance.

From Figure 4-3b, the circuit equation is given from Kirchhoff's voltage law (KVL) as

$$V_{\text{in}} = I_{\text{in}}(X_{C_1} + X_{C_2}) - I_b(X_{C_1} - \beta X_{C_2}) \tag{4-1a}$$

$$0 = -I_{\text{in}}(X_{C_1}) + I_b(X_{C_1} + h_{ie}) \tag{4-1b}$$

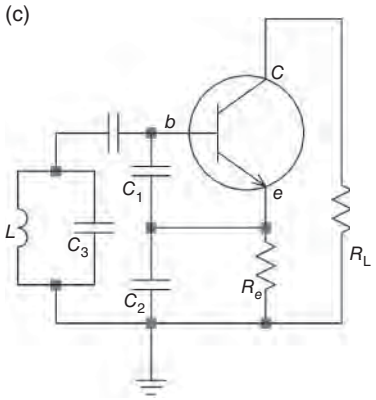


Figure 4-1c Modified Colpitts oscillator.

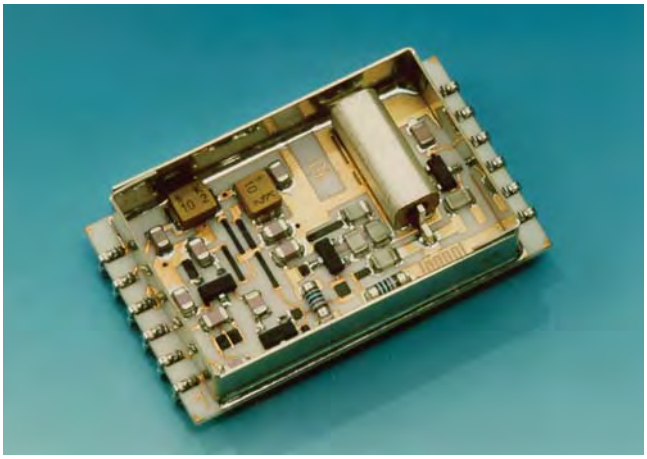


Figure 4-2 Photograph of 1 GHz CRO.

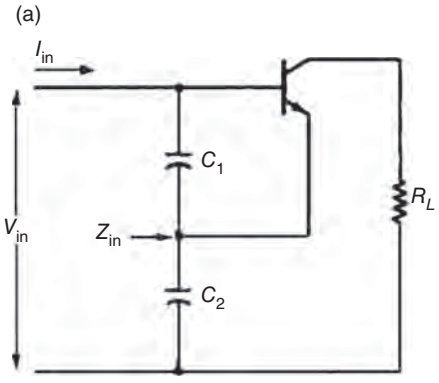


Figure 4-3a Oscillator sub-circuit for impedance analysis.

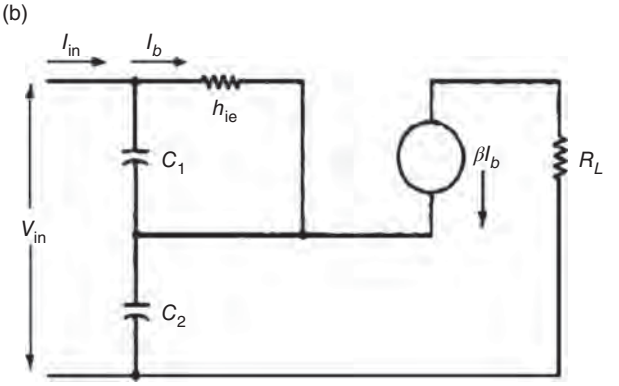


Figure 4-3b Equivalent sub-oscillator circuit for the calculation of the negative resistance.

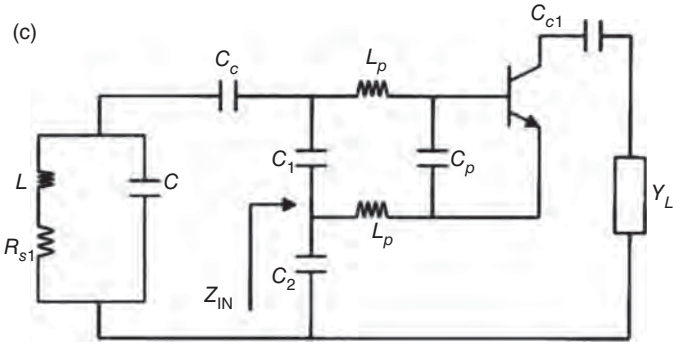


Figure 4-3c Colpitts oscillator with base lead inductances and package capacitance.

Considering, $\frac{1}{Y_{11}} = h_{ie}$

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{(1+\beta)X_{C_1}X_{C_2} + h_{ie}(X_{C_1} + X_{C_2})}{X_{C_1} + h_{ie}} \tag{4-1c}$$

$$Z_{\text{in}} = \frac{\left(-\frac{(1+\beta)}{\omega^2 C_1 C_2} + \frac{(C_1+C_2)}{j\omega\, C_1 C_2}\frac{1}{Y_{11}}\right)}{\left(\frac{1}{Y_{11}} + \frac{1}{j\omega\, C_1}\right)} \tag{4-1d}$$

The input impedance (Z_{in}) of this Colpitts oscillator circuit, including the parasitics, is given as [4, 5]

$$Z_{\text{in}}|_{\text{pacakage}} = -\left[\frac{Y_{21}}{\omega^2(C_1 + C_p)C_2}\frac{1}{(1+\omega^2 Y_{21}^2 L_p^2)}\right] - j\left[\frac{(C_1 + C_P + C_2)}{\omega\,(C_1 + C_P)C_2} - \frac{\omega Y_{21} L_P}{(1+\omega^2 Y_{21}^2 L_p^2)}\frac{Y_{21}}{\omega\,(C_1 + C_P)C_2}\right] \tag{4-2}$$

The resonator losses are expressed by the R_{S1}. Now splitting the Z_{in} of the Colpitts oscillator into real and imaginary parts, including parasitics, we obtain

$$R_{NEQ} = \frac{R_N}{(1 + \omega^2 Y_{21}^2 L_p^2)} \tag{4-3}$$

$$\frac{1}{C_{EQ}} = \left\{ \left[\frac{1}{\frac{(C_1+C_P)C_2}{(C_1+C_2+C_P)}} \right] - \left[\frac{\omega^2 Y_{21} L_P}{(1 + \omega^2 Y_{21}^2 L_P^2)} \right] \left[\frac{Y_{21}}{\omega (C_1 + C_P) C_2} \right] \right\} \tag{4-4}$$

$$R_N = -\frac{Y_{21}}{\omega^2 C_1 C_2} \tag{4-5}$$

where

R_N = negative resistance without lead inductance and package capacitance
R_{NEQ} = negative resistance with base-lead inductance and package capacitance
C_{EQ} = equivalent capacitance with base-lead inductance and package capacitance

The method shown earlier is called *one-port* oscillator design [6]. Figure 4-4 shows the general schematic diagram of a one-port negative-resistance model. The negative real part of Z_{in} is used to compensate the losses of the parallel tuned circuit.

A Quick Look at Some Important Parameters

A more complete expression for a resonator oscillator's phase noise spectrum is

$$\begin{aligned} s_\phi(f_m) = {} & [\alpha_R F_0^4 + \alpha_E (F_0/(2Q_L))^2]/f_m^3 \\ & + [(2GFKT/P_0)(F_0/(2Q_L))^2]/f_m^2 \\ & + (2\alpha_R Q_L F_0^3)/f_m^2 \\ & + \alpha_E/f_m + 2GFKT/P_0 \end{aligned}$$

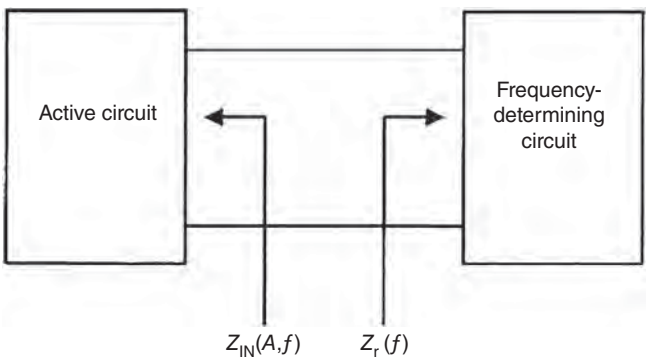


Figure 4-4 Schematic diagram of a one-port negative resistance model.

where

G = compressed power gain of the loop amplifier
F = noise factor of the loop amplifier
K = Boltzmann′s constant
T = temperature in K
P_0 = carrier power level (in watts) at the output of the loop amplifier
F_0 = carrier frequency in Hz
f_m = carrier offset frequency in Hz
$Q_L = \pi F_0 \tau_g$ = loaded Q of the resonator in the feedback loop
α_R and α_E = flicker noise constants for the resonator and loop amplifier, respectively

See Figure 4-5.

In frequency synthesizers, we have no use for *LC* oscillators without a tuning diode, but it may still be of interest to analyze the low-noise fixed-tuned *LC* oscillator first and later make both elements, inductor and capacitor, variable.

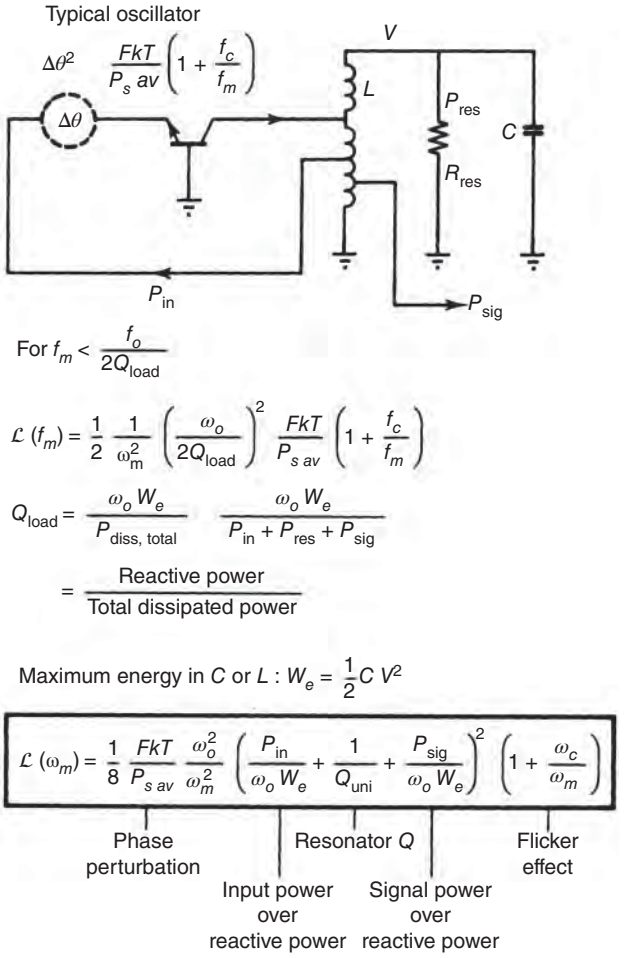


Figure 4-5 Diagram for a feedback oscillator illustrating the principles involved and showing the key components considered in the phase noise calculation and its contribution.

Linear S-Parameters Approach

It may be interesting for readers to see how an oscillator can be analyzed using *S*-parameters. It should be noted that this method is based on linear approximations and works for practically all microwave oscillator designs [6, 28, pg. 741]. The equivalent criteria of the negative resistance can be calculated in the form of *S*-parameters. The detailed definitions of *S*-parameters can be found in [32]. This negative resistance will cause oscillations if the following conditions are satisfied. Assume that the oscillation condition is satisfied at port 1 and is given by

$$\frac{1}{S_{11}} = \Gamma_G \tag{4-6}$$

Thus,

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4-7}$$

$$\frac{1}{S'_{11}} = \frac{1 - S_{22}\Gamma_L}{S_{11} - D\Gamma_L} = \Gamma_G \tag{4-8}$$

From expanding (4-7) we get

$$\Gamma_G S_{11} - D\Gamma_L\Gamma_G = 1 - S_{22}\Gamma_L \tag{4-9}$$

$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G \tag{4-10}$$

$$\Gamma_L = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{4-11}$$

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G} \tag{4-12}$$

$$\frac{1}{S'_{22}} = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{4-13}$$

Comparing Eqs. (4-9) and (4-12), we find that

$$\frac{1}{S'_{22}} = \Gamma_G \tag{4-14}$$

where S_{11} and S_{22} are the input and output reflection coefficients, respectively.

The discussion earlier means that the oscillation condition is also satisfied at port 2; which proves the simultaneous oscillation condition at both ports. Thus, if either port is oscillating, the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in Γ_L, the output termination.

It is helpful to use the common-source based amplifier to compute the oscillator output power. For oscillators, the objective is to maximize $(P_{\text{out}} - P_{\text{in}})$ of the amplifier, which is the useful power to the load. An empirical expression for the common-source amplifier output power found by Johnson [29] is

$$P_{\text{out}} = P_{\text{sat}}\left(1 - \exp\frac{-GP_{\text{in}}}{P_{\text{sat}}}\right) \tag{4-15}$$

Where P_{sat} is the saturated output power of the amplifier and G is the tuned small-signal common-source transducer gain of the amplifier, which is identical to $|S_{21}|^2$. Since the objective is to maximize $(P_{\text{out}} - P_{\text{in}})$, where P_{out} and P_{in} are the output and input power of the amplifier,

$$d(P_{\text{out}} - P_{\text{in}}) = 0 \tag{4-16}$$

$$\frac{\partial P_{\text{out}}}{\partial P_{\text{in}}} = 1 \tag{4-17}$$

$$\frac{\partial P_{\text{out}}}{\partial P_{\text{in}}} = G_{\text{exp}} - \frac{GP_{\text{in}}}{P_{\text{sat}}} = 1 \tag{4-18}$$

$$\exp \frac{GP_{\text{in}}}{P_{\text{sat}}} = G \tag{4-19}$$

$$\frac{P_{\text{in}}}{P_{\text{sat}}} = \frac{\ln G}{G} \tag{4-20}$$

At the maximum value of $(P_{\text{out}} - P_{\text{in}})$, the amplifier output is

$$P_{\text{out}} = P_{\text{sat}} \left(1 - \frac{1}{G}\right) \tag{4-21}$$

and the maximum oscillator output power is

$$P_{\text{osc}} = (P_{\text{out}} - P_{\text{in}}) \tag{4-22}$$

$$= P_{\text{sat}} \left(1 - \frac{1}{G} - \frac{\ln G}{G}\right) \tag{4-23}$$

Thus, the maximum oscillator output power can be predicted from the common-source amplifier saturated output power and the small signal common source transducer gain G. For high oscillator output power, high (loop) gain is of importance. Another definition of gain that is useful for large-signal amplifier or oscillator design is the *maximum efficient gain*, defined by

$$G_{\text{ME}} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{in}}} \tag{4-24}$$

For maximum oscillator power the maximum efficient gain from (4-20) and (4-21) is

$$G_{\text{MEmax}} = \frac{G - 1}{\ln G} \tag{4-25}$$

The RF gain G_{MEmax} is a considerably smaller value compared with G, the small-signal gain [7–12].

Designing oscillators based on S-parameters in a linear mode has been quoted by many authors using first approximation for large signals, as shown in [8]. The problem with this published approach is that it uses a GaAs FET, where only the transconductance g_m has a major influence. S_{11} changes very little under large-signal conditions, as does S_{22}. Reliable large-signal S-parameters for bipolar transistors and FETs are difficult to get.

Time Domain-Based Analysis of Transistor Nonlinearities A correction for the frequency dependent parameters will follow, based on "simulation" for larger drive level.

The voltage $v(t)$ across the base–emitter junction consists of a dc component and a driven signal voltage $V_1 \cos(wt)$. It can be expressed as

$$v(t) = V_{\text{dc}} + V_1 \cos(wt) \tag{4-26}$$

As the driven voltage $V_1 \cos(wt)$ increases and develops enough amplitude across the base–emitter junction, the resulting current is a periodic series of pulses whose amplitude depends on the nonlinear characteristics of the device and is given as

$$i_e(t) = I_s e^{\frac{qv(t)}{kT}} \tag{4-27}$$

$$i_e(t) = I_s e^{\frac{qV_{\text{dc}}}{kT}} e^{\frac{qV_1 \cos(wt)}{kT}} \tag{4-28}$$

$$i_e(t) = I_s e^{\frac{qV_{\text{dc}}}{kT}} e^{x \cos(wt)} \tag{4-29}$$

assuming $I_c \approx I_e(\beta > 10)$,

$$x = \frac{V_1}{(kT/q)} = \frac{qV_1}{kT} \tag{4-30}$$

$i_e(t)$ is the emitter current and x is the drive level, which is normalized to kT/q.

From the Fourier series expansion, $e^{x\cos(wt)}$ is expressed as

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) \tag{4-31}$$

$a_n(x)$ is a Fourier coefficient and given as

$$a_0(x)|_{n=0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}d(wt) = I_0(x) \tag{4-32}$$

$$a_n(x)|_{n>0} = \frac{1}{2\pi}\int_0^{2\pi} e^{x\cos(wt)}\cos(nwt)d(wt) = I_n(x) \tag{4-33}$$

$$e^{x\cos(wt)} = \sum_n a_n(x)\cos(nwt) = I_0(x) + 2\sum_1^{\infty} I_n(x)\cos(nwt) \tag{4-34}$$

$I_n(x)$ is the modified Bessel function.

As

$$x \to 0 \Rightarrow I_n(x) \to \frac{(x/2)^n}{n!} \tag{4-35}$$

$I_0(x)$ are monotonic functions having positive values for $x \geq 0$ and $n \geq 0$; $I_0(0)$ is unity, whereas all higher-order functions start at zero.

The short current pulses are generated from the growing large-signal drive level across the base–emitter junction, which leads to strong harmonic generation [5, 27]. The advantage of this pulse performance is the reduction of phase noise, due to the smaller duty cycle of the transistor [4]. The emitter current represented earlier can be expressed in terms of harmonics as

$$i_e(t) = I_s e^{\frac{qV_{\rm dc}}{kT}} I_0(x)\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \tag{4-36}$$

$$I_{\rm dc} = I_s e^{\frac{qV_{dc}}{kT}} I_0(x) \tag{4-37}$$

$$V_{\rm dc} = \frac{kT}{q}\ln\left[\frac{I_{\rm dc}}{I_s I_0(x)}\right] \Rightarrow \frac{kT}{q}\ln\left[\frac{I_{\rm dc}}{I_s}\right] + \frac{kT}{q}\ln\left[\frac{1}{I_0(x)}\right] \tag{4-38}$$

I_s = collector saturation current

$$V_{\rm dc} = V_{{\rm dc}Q} - \frac{kT}{q}\ln I_0(x) \tag{4-39}$$

$$i_e(t) = I_{\rm dc}\left[1 + 2\sum_1^{\infty}\frac{I_n(x)}{I_0(x)}\cos(nwt)\right] \tag{4-40}$$

$V_{{\rm dc}Q}$ and $I_{\rm dc}$ are the operating dc bias voltage and the dc value of the emitter current, respectively. Furthermore, the Fourier transform of $i_e(t)$, a current pulse or series of pulses in the time domain, yields a number of frequency harmonics common in oscillator circuit designs using nonlinear devices.

The peak amplitude of the harmonic content of the output current is defined as $\left[\frac{I_N(x)}{I_1(x)}\right]$.

The dc offset voltage is calculated analytically in terms of the drive level, as shown in Table 4-1. This data provides insight into the nonlinearities involved in oscillator design.

It may be of interest to see the start-up condition of an oscillator; the transient response is shown in Figure 4-6.

Table 4-1 For $T = 300$ K, data are generated at a different drive levels

Drive level	Drive voltage	Offset coefficient	dc offset	Fundamental current	Second harmonic
$[x]$	$\left(\left[\frac{kT}{q}\right] * x\right)$ mV	$\ln[I_0(x)]$	$\frac{kT}{q}[\ln I_0(x)]$ mV	$2[I_1(x)/I_0(x)]$	$[I_2(x)/I_1(x)]$
0.00	0.000	0.000	0.000	0.000	0.000
0.50	13.00	0.062	1.612	0.485	0.124
1.00	26.00	0.236	6.136	0.893	0.240
2.00	52.00	0.823	21.398	1.396	0.433
3.00	78.00	1.585	41.210	1.620	0.568
4.00	104.00	2.425	63.050	1.737	0.658
5.00	130.00	3.305	85.800	1.787	0.719
6.00	156.00	4.208	206.180	1.825	0.762
7.00	182.00	5.127	330.980	1.851	0.794
8.00	208.00	6.058	459.600	1.870	0.819
9.00	234.00	6.997	181.922	1.885	0.835
10.00	260.00	7.943	206.518	1.897	0.854
15.00	390.00	12.736	331.136	1.932	0.902
20.00	520.00	17.590	457.340	1.949	0.926

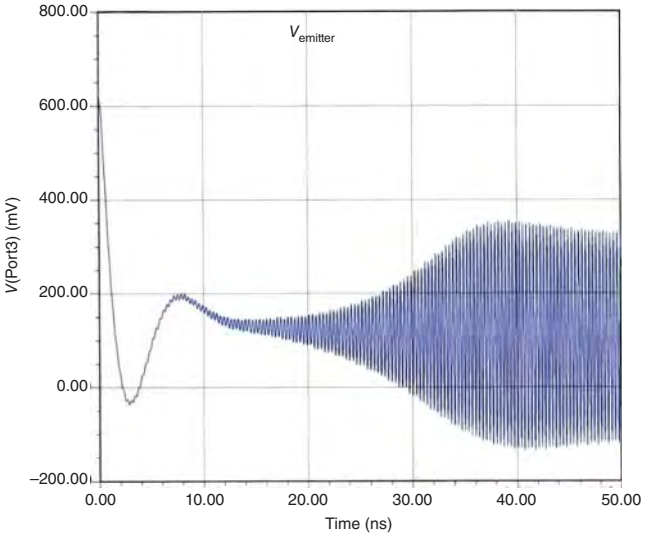


Figure 4-6 Example of the transient simulation of a ceramic resonator-based high-*Q* oscillator showing the dc-offset as listed in column 4, Table 4-1. (The voltage displayed is taken from the emitter.)

Selecting the Right Transistor

The basic design of a Colpitts oscillator is the same, whether one uses an FET or bipolar junction transistor (BJT). Bipolar transistor-based oscillators can now easily be designed up to 20 GHz. The basic advantage of the bipolar transistor (also known as BIP) is the lower flicker noise corner frequency. Currently, transistor chips with F_{max} up to 300 GHz are available in the foundry environment, commercially up to about 150 GHz. For the purpose of this design synthesis, we have decided to use a BFG520, which is a highly linear transistor. It is validated with a 3-tone test (the typical 2-tone test is easier to meet), as found from the datasheet; the mixing products are better

than −60 dB suppressed relative to the carrier. Based on past experience for its good linearity, the BFG520 also has low distortion and low noise. The key parameters are:

- $V_{CEO} = 15\,V$
- $I_c = 70\,mA$
- $P_{tot} = 300\,mW$
- Noise Figure F_{min} at 350 MHz is less than 1 dB
- At 5 mA the associated gain is more than 17 dB

4-2-2 Design Example for a 350 MHz Fixed-Frequency Colpitts Oscillator

The following is an exact mathematical solution for designing the 350 MHz Colpitts oscillator. The circuit consists of the Colpitts configuration following Figure 4-1c. In order to have enough loop gain, a microwave transistor (BFG520) is used. At the proposed starting dc current of 6 mA, being close to the minimum noise figure current and as a first trial to meet the output power, f_T is 6 GHz. When selecting a transistor with a higher f_T, there is always a possibility of unwanted microwave oscillation and higher flicker noise. When comparing microwave transistors with audio transistors, it becomes apparent that at much lower frequencies there is much less flicker noise contribution. This transistor can safely be operated at 30 mA but the rule of thumb is, when using 10–15% of Ic_{max}, the flicker contribution is much less. For low-noise operation, the datasheet indicates 1.1 dB spot noise figure at 900 MHz at 5 mA.

The 350 MHz oscillator, using the bipolar transistor BFG520, is designed based on analytical equations and is later verified with simulation results. Based on the output power requirement and harmonics at a given load, the drive level is fixed. The normalized drive level (of $x = 15$) is chosen to allow adequate drive level to sustain oscillation and yet, not to produce excessive harmonic content. Figure 4-7 shows the values of the optimized circuit. While simulating for a series-resonant configuration, the value of $C_P = 8.2\,pF$ was used as a place-holder, based on impedance considerations.

C_P was set to 8.2 pF for parallel resonant configuration, the value of $L = 21\,nH$, and $C_c = 3.3\,pF$ was set to achieve oscillation at 350 MHz. Experimenting with the simulation, it turns out that "L_b" set to 0.5 µH gives a much better phase noise, about 10 dB better at 100 Hz offset, but this could not be verified yet in a real circuit.

The output power is taken from the collector and following is the design procedure. The goal is to obtain an output power over 10 dBm, using a simple design for good understanding.

Step 1: Basic Parameters

The normalized drive level will be set at 15, for which the fundamental peak current $I_{1\,(fundamental)} = 1.932\,I_{dc}$ (given from Table 4-1). I_1 is the fundamental current specified by the output power needed for the designated load. The primary impedance of the transformer is 200 Ω and we calculate the RF voltage for $R_L = 200\,\Omega$ and for an output power of $P_{out} \approx 11\,dBm \approx 14\,mW$.

$$V_{out} = \sqrt{P_{out}(mW) \times 2R_L} = \sqrt{14 \times 10^{-3} \times 2 \times 200} = 2.37\,V \tag{4-41}$$

No saturation voltage assumed! This results in slight variation between calculated, simulated, and measured values of P_{out}.

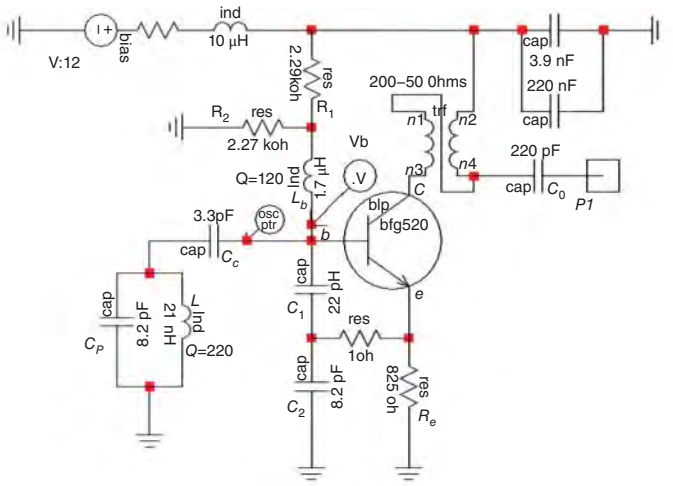
$$I_1 = \frac{V_{out}}{200} = \frac{2.37}{200} \cong 11.85\,mA \tag{4-42}$$

$$I_e = I_{dc} = \frac{I_1}{1.932} = \frac{11.85}{1.932} = 6.13\,mA \tag{4-43}$$

Step 2: Biasing

The transistor uses a 12 V power supply and an 825 Ω emitter resistor at ~6 mA, resulting in ~5 V drop, so the transistor can afford a large voltage swing between base and ground. This reduces flicker noise (resistive feedback)

(A)



(B)

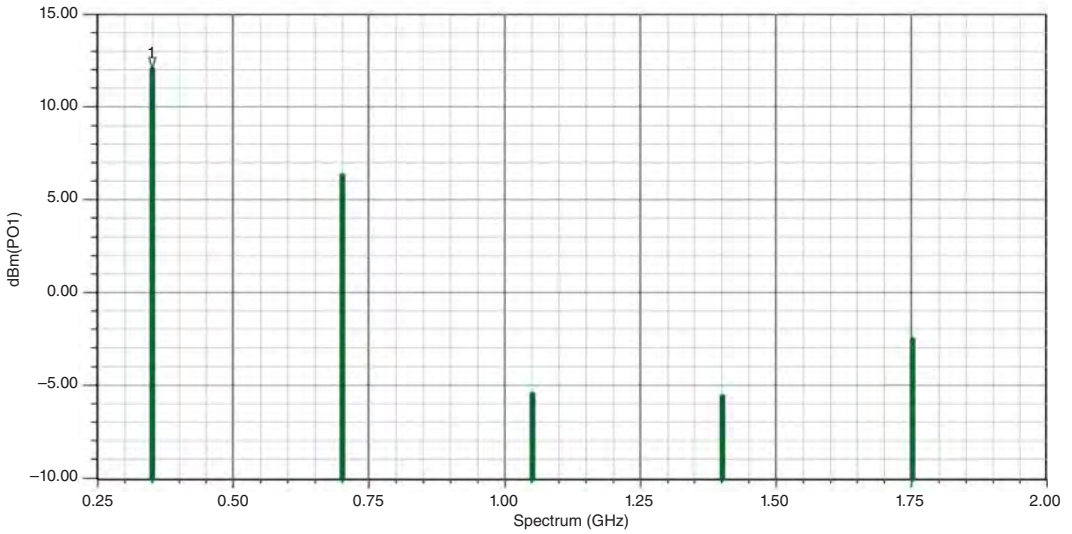


Figure 4-7 Design of 350 MHz Colpitts oscillator optimized for phase noise.

and distortion. The base voltage divider, for reasons pertaining to temperature stability uses a higher than normal dc current, is isolated from the base using a RF choke. Frequently, in designs, this circuit trick is not used.

$$V_b = I_e \left[R_e + \frac{R_e}{\beta + 1} \right] + V_{\text{be}} = 5.96 \text{ V} \tag{4-44}$$

β is assumed to be around 100 and V_{be} is approximately 0.8 V. Bias resistors R_1 and R_2 are given as

$$V_b = \frac{R_2}{R_1 + R_2} V_{\text{cc}} = 5.96 \text{ V} \Rightarrow \frac{R_1}{R_2} \approx 1 \tag{4-45}$$

$$R_1 = 2270\,\Omega \tag{4-46}$$

$$R_2 = 2290\,\Omega \tag{4-47}$$

$$V_{cc} = 12\text{ V} \tag{4-48}$$

Resistor bias current is ~2.6 mA ($V_{cc}/(R_1 + R_2)$).
Base current is 43 μA, so the safety factor is 2.6/0.043 ≅ 60.

Step 3: Determination of the Large-Signal Transconductance

Based on Table 4-1, and $x = 15$, the "dc transconductance" equals

$$Y_{21} = \left.\frac{I_1}{V_1}\right|_{\text{fundamental-freq}} = \frac{1.932 I_{dc}}{1000\text{ mV}} = \frac{11.85\text{ mA}}{1000\text{ mV}} \cong 12\text{ mS} \tag{4-49}$$

This is the dc transconductance, meaning the frequency dependence has not been considered.

An analysis of the transistor shows that the small signal transconductance at 6 mA (dc) is about $6 \times 39 \approx 240$ mS. At 350 MHz, this reduces itself to 200 mS down from 240 mS. This is valid only if the transistor does not have any emitter feedback. In the case of the Colpitts oscillator, we have an emitter resistor that reduces the transconductance; therefore, we have to multiply Y_{21} with

$$\left(\frac{1}{(1/g_m) + R_e}\right) \tag{4-50}$$

The resulting large-signal loop transconductance Y_{21L} is

$$\frac{1}{\left(\frac{1}{12\times10^{-3}}\right) + 825} \cong 1.1\text{ mS}$$

which is an acceptable approximation, as the exact value of x is about 20 (see simulation results, Figure 4-10) [26, pg. 177].

Based on Kirchhoff's law, the following set of equations can be used to determine the feedback factor "n." $Y_{21L} = 1.1$ mS (dc transconductance—no high frequency effects included) Where $\alpha = 0.99$.

Large-signal transconductance as a function of drive level based on Bessel function calculations are given in Table 4-2.

Table 4-2 $G_m(x)/g_m = 2[I_1(x)/xI_0(x)]$ as a function of drive level (x)

Drive level x	$G_m(x)/g_m = 2[I_1(x)/xI_0(x)]$
0.00	1
0.50	0.970
1.00	0.893
2.00	0.698
3.00	0.540
4.00	0.432
5.00	0.357
6.00	0.304
7.00	0.264
8.00	0.233
9.00	0.209
10.00	0.190
15.00	0.129
20.00	0.0975
25.00	0.075

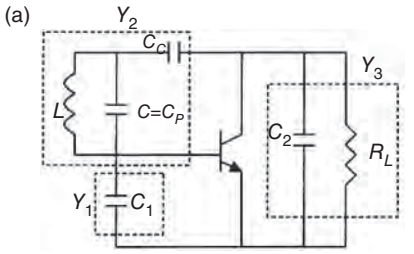


Figure 4-8a Oscillator circuit with the passive components Y_1, Y_2, and Y_3.

The oscillator circuit with passive component parameters is shown in Figure 4-8a.
Where:

$$Y_1 = G_1 + jB_1 \Rightarrow j\omega C_1 \quad \text{For } G_1 = 0 \tag{4-51a}$$

$$Y_2 = G_2 + jB_2 \Rightarrow G_2 + j\left[\frac{(\omega^2 LC - 1)\omega C_c}{\omega^2 L(C_c + C) - 1}\right] \tag{4-51b}$$

G_2 = loss parameter/load conductance of the resonator connected parallel to the resonator component C_1, C_2, and L, respectively.

$$Y_3 = G_3 + jB_3 \Rightarrow G_3 + j\omega C_2 \tag{4-51c}$$

G_3 = conductance of the bias resistor placed across C_2, $1/R_L$ in Figure 4-8a.

The large-signal transconductances Y_{21} and G_1 are transformed to the current source through the voltage divider $\frac{V_{eb}}{V_{cb}}$. The voltage V_{eb} must be added to V_{ce} to calculate the transformation ratio, which is also the inverse of the feedback factor and can be written as

$$\frac{V_{eb}}{V_{cb}} = \frac{C_2}{C_1 + C_2} = \frac{1}{n} \tag{4-51d}$$

and

$$\frac{V_{ce}}{V_{cb}} = \frac{C_1}{C_1 + C_2} = \frac{n-1}{n} \tag{4-51e}$$

The conductance G_2 is already in parallel with the current source so it remains unchanged. The factor "n" represents the ratio of the collector–base voltage to the emitter–base voltage at the oscillator resonant frequency.

$$G_1 \rightarrow \frac{G_1}{n^2} \tag{4-51f}$$

$$Y_{21} \rightarrow \frac{Y_{21}}{n^2} \Rightarrow \frac{G_m}{n^2} \tag{4-51g}$$

$$G_3 \rightarrow \left[\frac{n-1}{n}\right]^2 G_3 \tag{4-51h}$$

G_2 remains constant.

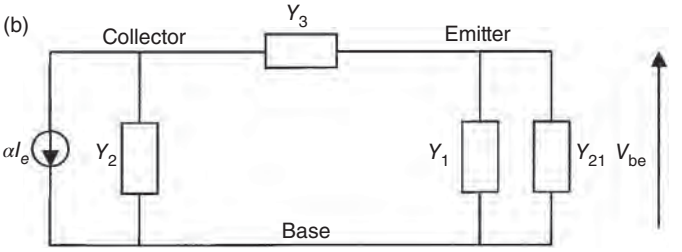


Figure 4-8b Equivalent oscillator circuit for the analysis of the transformed conductance seen by the current source.

The transformed conductance is proportional to the square of the voltage ratios given in Eqs. (4-51d) and (4-51e), producing a total conductance as seen by the current source at resonance as

$$G_{\text{total}} = G_2 + \frac{G_m + G_1}{n^2} + \left[\frac{n-1}{n}\right]^2 G_3 \tag{4-51i}$$

For sustained oscillation, the closed loop gain at resonance is given as

$$\left[\frac{\left(\frac{V_{\text{be}} Y_{21}\alpha}{nG_{\text{total}}}\right)}{V_{\text{be}}}\right] = 1 \Rightarrow nG_{\text{total}} = Y_{21}\alpha \tag{4-51j}$$

$$\frac{Y_{21}}{nG_{\text{total}}} = \frac{1}{\alpha} \Rightarrow \frac{Y_{21}}{nG_{\text{total}}} > 1 \tag{4-51k}$$

α is assumed to be 0.99 and variation in the value of α does not influence the previous expression greatly. Rearranging the device conductance and circuit conductance, the general oscillator equation, after multiplying (4-51i) with n on both sides, is written as

$$nG_{\text{total}} = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{4-51l}$$

$$Y_{21}\alpha = n\left[G_2 + \frac{Y_{21} + G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \Rightarrow \left[\frac{-(1-n\alpha)}{n^2}\right] Y_{21} = \left[G_2 + \frac{G_1}{n^2} + \left(\frac{n-1}{n}\right)^2 G_3\right] \tag{4-51m}$$

$$n^2(G_2 + G_3) - n(2G_3 + Y_{21}\alpha) + (G_1 + G_3 + Y_{21}) = 0 \tag{4-51n}$$

$$n = \frac{(2G_3 + Y_{21}\alpha) \pm \sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{4-51o}$$

$$n_1 = \frac{(2G_3 + Y_{21}\alpha)}{2(G_2 + G_3)} + \frac{\sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{4-51p}$$

$$n_2 = \frac{(2G_3 + Y_{21}\alpha)}{2(G_2 + G_3)} - \frac{\sqrt{(2G_3 + Y_{21}\alpha)^2 - 4(G_2 + G_3)(G_1 + G_3 + Y_{21})}}{2(G_2 + G_3)} \tag{4-51q}$$

From the quadratic equation earlier, the value of the factor n can be calculated, and thereby an estimation of the capacitance can be done a priori.

To ensure higher loop gain, n_1 is selected from $n_{\max}[n_1, n_2]$. Once the value of n is fixed, then the ratio of the capacitance is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \tag{4-51r}$$

$$C_2 = \frac{C_1}{n-1} \Rightarrow \frac{C_1}{C_2} = n - 1 \tag{4-51s}$$

If G_3 and G_1 are zero, then the quadratic equation (4-51n) reduces to

$$n^2 G_2 - nY_{21}\alpha + Y_{21} = 0 \tag{4-51t}$$

$$Y_{21} \cong \frac{n^2}{1-n} G_2 \Rightarrow Y_{21} = \left[\frac{n^2}{1-n}\right] \frac{1}{R_P} \tag{4-51u}$$

$$\frac{Y_{21} R_P}{n} = \frac{n}{1-n} \tag{4-51v}$$

$$R_P = \frac{1}{G_2}, \frac{Y_{21} R_P}{n} \rightarrow \text{Loop Gain} \tag{4-51w}$$

$$\text{Loop Gain } \frac{Y_{21} R_P}{n} \rightarrow 1 \tag{4-51x}$$

From Eqs. (4-51r) and (4-51u)

$$Y_{21} \Rightarrow G_m(x) = \frac{1}{R_P}\frac{[C_1 + C_2]^2}{C_1 C_2} \tag{4-51y}$$

The quadratic equation for n (from (4-51n)) is reduced to

$$n^2(G_3) - n(2G_3 + Y_{21}\alpha) + (G_3 + Y_{21}) = 0 \tag{4-52a}$$

$$G_3 = \frac{1}{R_e} = \frac{1}{825} = 1.21 \text{ mS}$$

$$n^2(1.21) - n(2 \times 1.21 + 1.1 \times 0.99) + (1.21 + 1.1) = 0 \tag{4-52b}$$

$$1.21n^2 - 3.514n + 2.313 = 0 \tag{4-52c}$$

$$n = \frac{3.514 \pm \sqrt{(3.514)^2 - 4 \times 1.21 \times 2.313}}{2 \times 1.21} \tag{4-53}$$

$$n \Rightarrow n_1 = 1.888 \text{ and } n_2 = 1.01 \tag{4-54}$$

The higher value of the transformation factor, n, is selected as $n = 1.888$.
The ratio for the values of C_1 and C_2 is calculated as

$$\frac{C_2}{C_1 + C_2} = \frac{1}{n} \Rightarrow C_2 = \frac{C_1}{n-1} \tag{4-55}$$

$$C_2 = \frac{C_1}{n-1} = \frac{C_1}{0.888} \Rightarrow \frac{C_1}{C_2} \cong 0.9 \approx 1 \tag{4-56}$$

The ratio of the capacitor C_1 to C_2 is 1; for larger transconductance Y_{21}, $(C_1/C_2) > 1$.

Drive Level and Noise The plot in Figure 4-9 [5] shows the impact of the normalized drive level "x" on the phase noise. The exact values have to be assessed for individual circuits, but the general trend follows the plot shown.

In Figure 4-10, $x = 1$ is the linear case (Class-A operation) and the values above $x = 15$ produce narrow pulses. Class-A operation gives higher output power but is not optimized for phase noise. However, at higher drive levels, the transistor is "on" for shorter duration, thus less loading and better phase noise, but at the cost of lower power output. If the transistor is overdriven at the base, the collector current folds back (dips) and the actual current gain falls to values of 1.4 in our case (from Figure 4-10).

For the uncompressed current gain $(Y_{21}/Y_{11}) \approx (C_2/C_1) \approx 270$ pF/10 pF, the circuit will actually oscillate but does not have acceptable phase noise (low value of x, $n = 28$, where $n = (C_1/C_2) + 1$).

By changing the capacitors C_1/C_2 to 33 pF/10 pF, $n = 4.3$, the phase noise performance is optimized, as shown in Figure 4-11. This circuit is a series-tuned oscillator and now we move on to a high Q (from $Q = 220$ to $Q = 450$) circuit, where the resonator is loosely coupled to the transistor. The tuned circuit consists of a 22 nH inductor and 8.2 pF capacitor. The following shows the design calculation for the parallel tuned circuit as found in ceramic resonator-based oscillators.

The quality factor of the inductor is assumed 60 at 350 MHz, a low Q case. The value of inductor is obtained as

$$Q_T = \frac{R_P}{\omega_0 L} \Rightarrow L = \frac{3649}{60 \times \omega_0}, \text{ where } R_P \text{ is calculated using } G_m(x) = \frac{1}{R_P}\frac{C_1}{C_2}\left[1 + \frac{C_2}{C_1}\right]^2 \tag{4-57}$$

$$L = \frac{3649}{60 \times 2\pi \times 350 \times E6} \approx 27 \text{ nH} \tag{4-58}$$

$$\omega = \sqrt{\frac{1}{L}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]} \tag{4-59}$$

$$\omega^2 = \frac{1}{L}\left[\frac{1}{C_1} + \frac{1}{C_2}\right] = \frac{C_1 + C_2}{LC_1C_2} \tag{4-60}$$

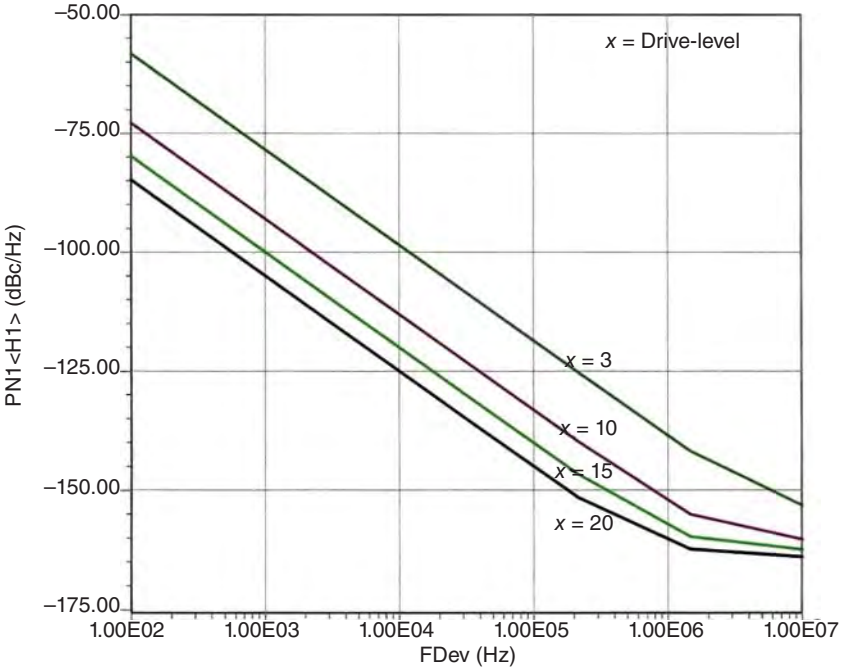


Figure 4-9 Example for the single sideband phase noise as a function of the normalized drive level *x* for a high-*Q* 1 GHz oscillator.

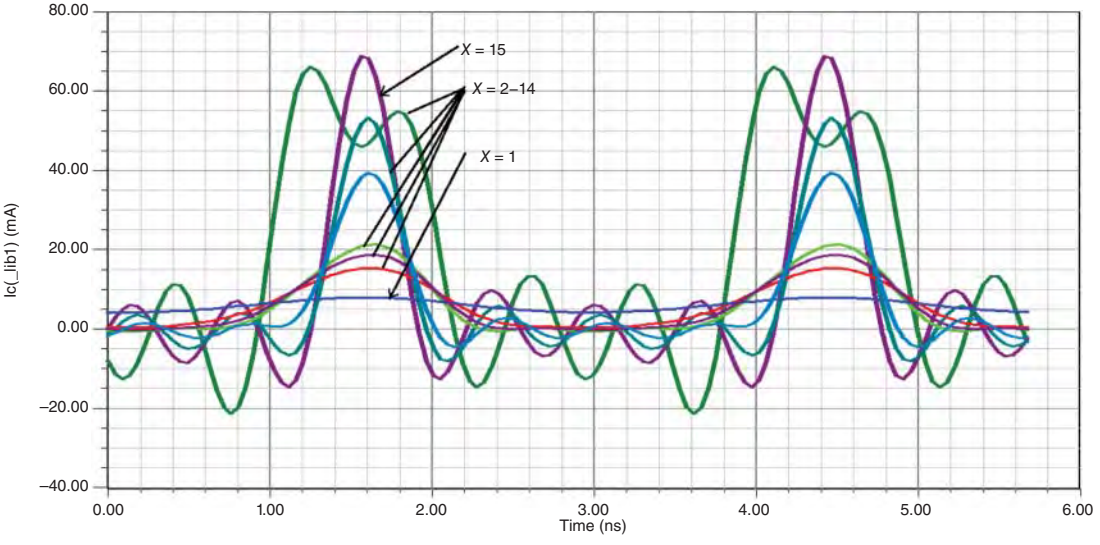


Figure 4-10 Characteristics of I_c as a function of drive level *x*.

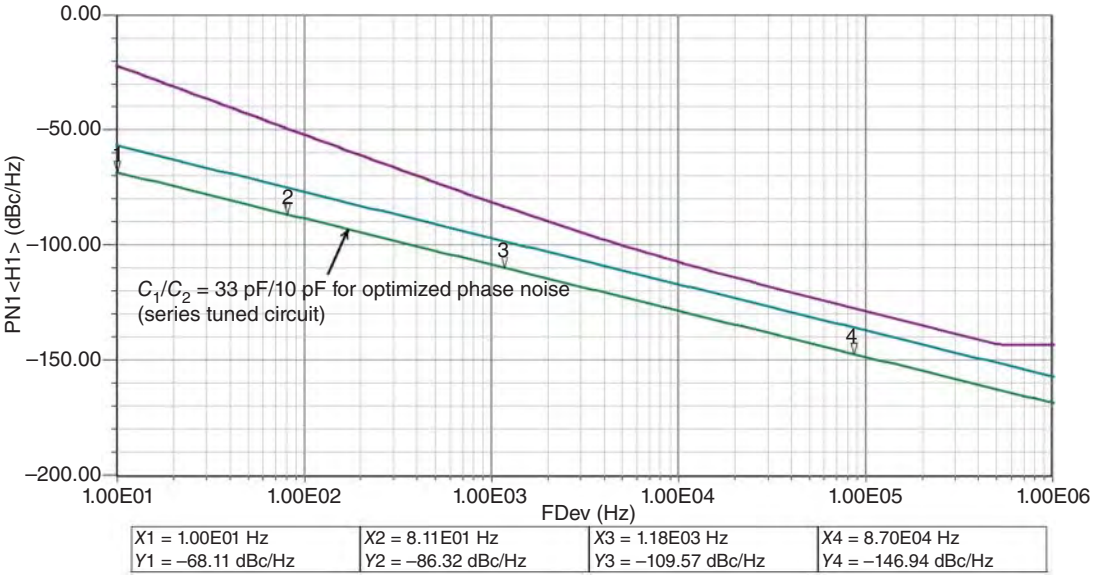


Figure 4-11 Optimization of phase noise for the series tuned circuit.

The value of the capacitor is determined as

$$C_2 = \frac{2.55}{\omega^2 \times 17E-9} \approx 14\,\text{pF} \tag{4-61}$$

$$C_1 \approx C_2 \approx 14\,\text{pF} \tag{4-62}$$

Taking into consideration the actual parasitics and RF parameters of the transistor, the optimized values are $C_1 = 12\,\text{pF}$ and $C_2 = 8.2\,\text{pF}$.

Step 4: Calculation of the Coupling Capacitor C_c

The expression for the coupling capacitor is [5, eq. (C-23)]

$$\frac{C}{10} > C_C > \left\{ \frac{(\omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)}{[Y_{21}^2 C_2 - \omega^2 C_1 C_2)(1+\omega^2 Y_{21}^2 L_P^2)(C_1 + C_P + C_2)]} \right\} \tag{4-63}$$

$$C_c = 3.3\,\text{pF} \tag{4-64}$$

Step 5: Calculation of the Phase Noise of the Colpitts Oscillator

The mathematical expression of the phase noise of a Colpitts Oscillator is [5, pg. 180]

$$L(\omega) = 10\,\log\left\{\left[4kTR + \left[\frac{4qI_c g_m^2 + \frac{K_f I_b^{AF}}{\omega} g_m^2}{\omega_0^2 C_1^2 \left(\omega_0^2 (\beta^+)^2 C_2^2 + g_m^2 \frac{C_2^2}{C_1^2}\right)}\right]\right]\left[\frac{\omega_0^2}{4\omega^2 V_{cc}^2}\right]\left[\frac{1}{Q^2} + \frac{[C_1+C_2]^2}{C_1^2 C_2^2 \omega_0^4 L^2}\right]\right\} \tag{4-65}$$

where

$$\beta^{+} = \left[\frac{Y_{21}^{+}}{Y_{11}^{+}}\right] \left[\frac{C_1}{C_2}\right]^{p}$$

$$g_m = [Y_{21}^{+}] \left[\frac{C_1}{C_2}\right]^{q}$$

The values of p and q depend upon the drive level (x)

Y_{21}^{+}, Y_{11}^{+} = large-signal [Y] parameter of the active device
K_f = flicker noise coefficient
AF = flicker noise exponent
$\pounds(\omega)$ = ratio of sideband power in a 1 Hz BW at ω to total power in dB
ω = frequency offset from the carrier
ω_0 = center frequency
Q_L = loaded Q of the tuned circuit
Q_O = unloaded Q of the tuned circuit
kT = 4.1×10^{-21} at 300 K (room temperature)
R = equivalent loss resistance of the tuned resonator circuit
I_c = RF collector current
I_b = RF base current
V_{cc} = RF collector voltage
C_1, C_2 = feedback capacitor

Using a Mathcad calculation, we obtain the results shown in Figure 4-12, [5, eq. 8-109], which compares well with the measured data.

Measured Results for a 350 MHz Oscillator

The measured phase noise of the oscillator shown in Figure 4-13 is not quite comparable with the mathematics because it has a two-stage buffer amplifier that isolates the oscillator from the output termination. This explains the limit of −146 dBc/Hz at far-offset. At close-in, the phase noise is influenced by an AFC circuit. The real comparison should be done between 10 Hz and 10 kHz offsets.

In order to optimize the phase noise for this type of oscillator, using discrete components, the selection of the following values:

$$C_P = 8.2\,\text{pF}$$
$$L = 21\,\text{nH}$$
$$C_1 = 22\,\text{pF}$$
$$C_2 = 8.2\,\text{pF}$$
$$C_c = 3.3\,\text{pF}$$

These improved the phase noise from −122 to −125 dBc/Hz at 10 kHz offset. This is a result of trial-and-error, as we do not know all the parasitics. Figure 4-14a shows the simulated phase noise plot, and Figure 4-14b shows further improvement after optimizing the circuit for phase noise.

If we replace the parallel tuned circuit with a ceramic resonator, at this frequency range, ε_r will be 88, the L/C ratio will be 0.048 nH/pF versus 2.44 nH/pF in case of discrete components used in our case, and the simulated phase noise is 105 dBc/Hz at 10 kHz offset.

Note: This is due to the fact that the characteristic impedance of a ceramic resonator is much lower, than the discrete case.

$$Z_0 = 60\,\Omega \frac{1}{\sqrt{\varepsilon_r}} \ln \frac{D}{d}$$

Phase noise equation

$Ic := 6.2\times10^{-3}$ $Ib := 43.2\times10^{-6}$ $L := 22\times10^{-9}$ $C_1 := 12\times10^{-12}$ $C_2 := 8.2\times10^{-12}$ $C_c := 3.3\times10^{-12}$

$K := 1.3806\times10^{-23}$ $T := 300$ $KT := 4.143\times10^{-21}$ $R := 0.3$ $Kf := 1\times10^{-7}$ $AF := 2$

$Q := 60$ $Vcc := 12$ $f := 350\cdot10^{6}$ $\omega0 := 2\,\pi\cdot f$ $\beta := 140$

$r_e := \frac{26\times10^{-3}}{Ic}$ $gm1 := \frac{1}{r_e}$ $gm1 := 0.238$ $q := 1.602\times10^{-19}$ $i := 0..7$ $fo_i := 10^i$

$\omega0_i$ is the frequecny offset from the carrier $\omega0_i := 2\cdot\pi\cdot fo_i$

$$L\omega_i := 10\cdot\log\left[\left[4\cdot KT\cdot R + \left[\frac{4\cdot q\cdot Ic\cdot gm1^2 + \frac{Kf\cdot Ib^{AF}}{\omega0_i}\cdot gm1^2}{(\omega0)^2\cdot C_1^{\,2}\cdot\left[(\omega0)^2\cdot\beta^2\cdot C_2^{\,2} + gm1^2\cdot\frac{C_2^{\,2}}{C_1^{\,2}}\right]}\right]\right]\cdot\left[\frac{\omega0^2}{4\cdot(\omega0_i)^2\cdot Vcc^2}\cdot\left[\frac{1}{Q^2} + \frac{(C_1+C_2)^2}{C_1^{\,2}\cdot C_2^{\,2}\cdot(\omega0)^4\cdot L^2}\right]\right]\right]$$

fo_i	$L\omega_i$
1	–5.227
10	–35.222
100	–65.165
1×10^3	–94.633
1×10^4	–121.303
1×10^5	–143.272
1×10^6	–163.529
1×10^7	–183.555

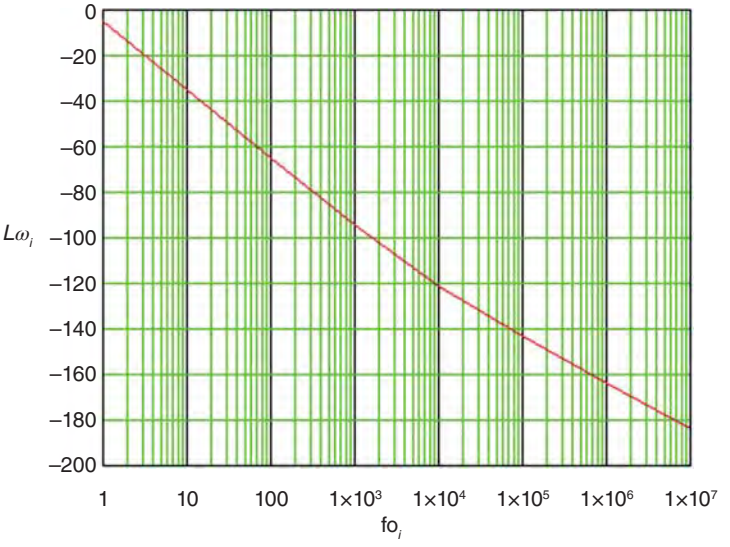


Figure 4-12 Mathcad calculation for phase noise.

where D = the outer diameter and d = the inner diameter of the ceramic resonator [12, pg. 754]. The prediction agrees well with the measured phase noise [12, Fig. (5-37)].

Figure 4-15 shows the plots of the collector and base currents I_c and I_b for the optimized case:

$C_P = 8.2$ pF
$L = 21$ nH ($Q = 60$ at 350 MHz)
$C_c = 3.3$ pF
$C_1 = 12$ pF
$C_2 = 8.2$ pF

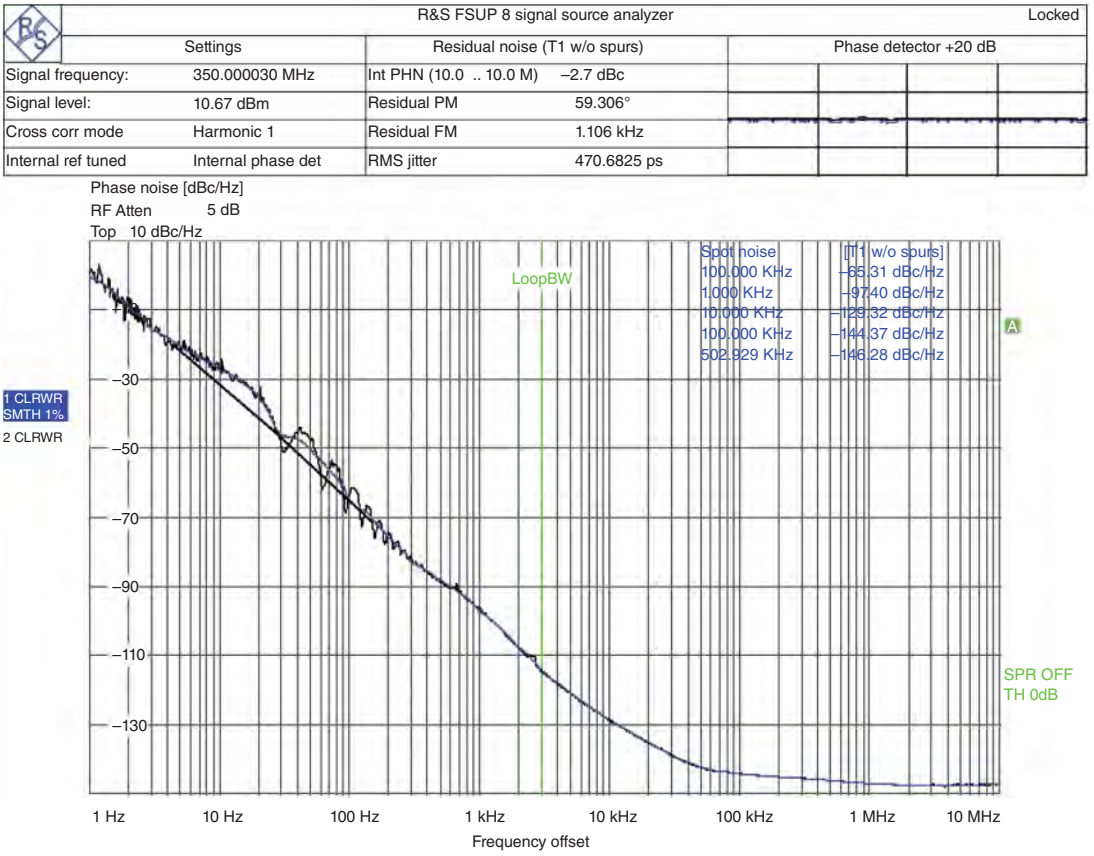


Figure 4-13 Measured phase noise result for a 350 MHz oscillator.

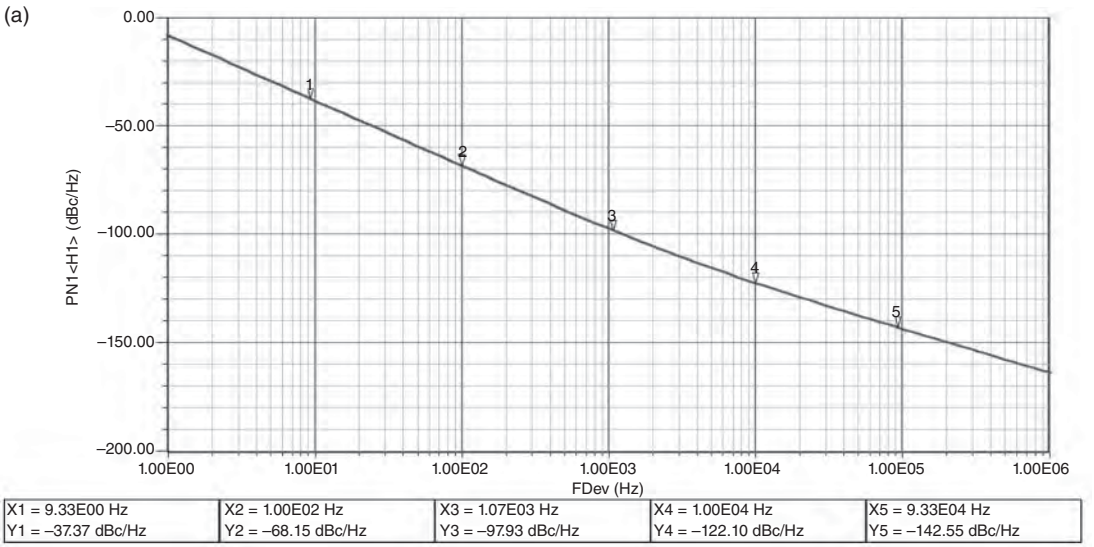


Figure 4-14a Simulated phase noise for the 350 MHz parallel-tuned Colpitts configuration.

(b)

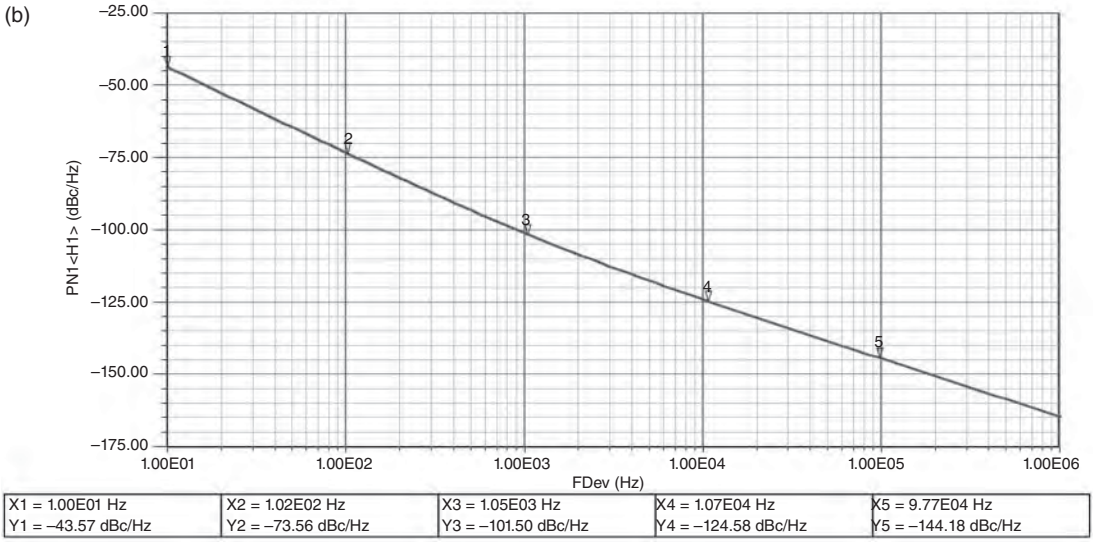


Figure 4-14b Optimized simulated phase noise for the 350 MHz parallel-tuned Colpitts configuration.

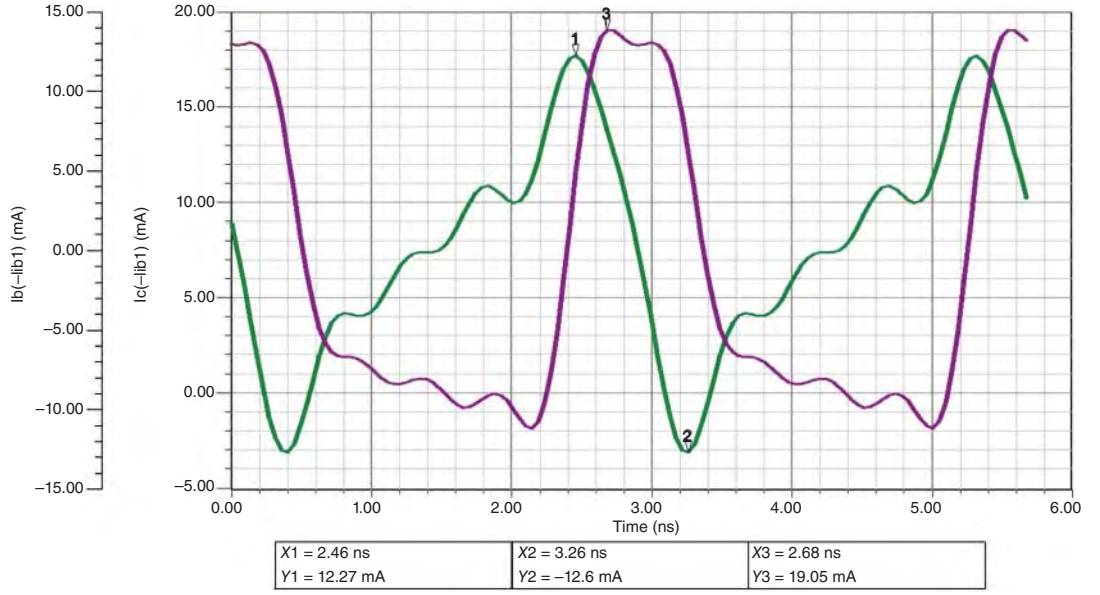


Figure 4-15 Y_{21}/Y_{11} large-signal condition.

From the plot in Figure 4-15, we can determine that the ratio of large signal $(Y_{21}/Y_{11}) = \beta = 1.4$. The next critical parameter, shown in Figure 4-16, is for the normalized drive level $(x)V_1/(kT/q)$.

From Figure 4-16, the RMS value of V_{be} is used to determine the approximate drive level. Since $V_{be} = V_1$,

$$\text{drive level } (x) \approx \frac{500\ \text{mV}_{\text{RMS}}}{26\ \text{mV}} \approx 20 \tag{4-66}$$

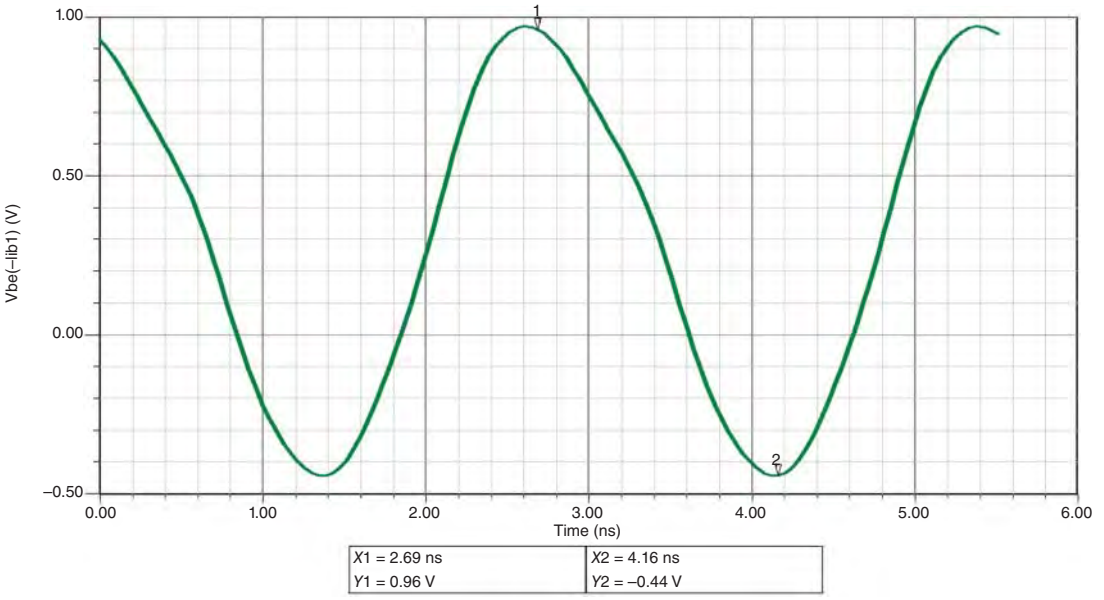


Figure 4-16 V_{be} to calculate the drive level.

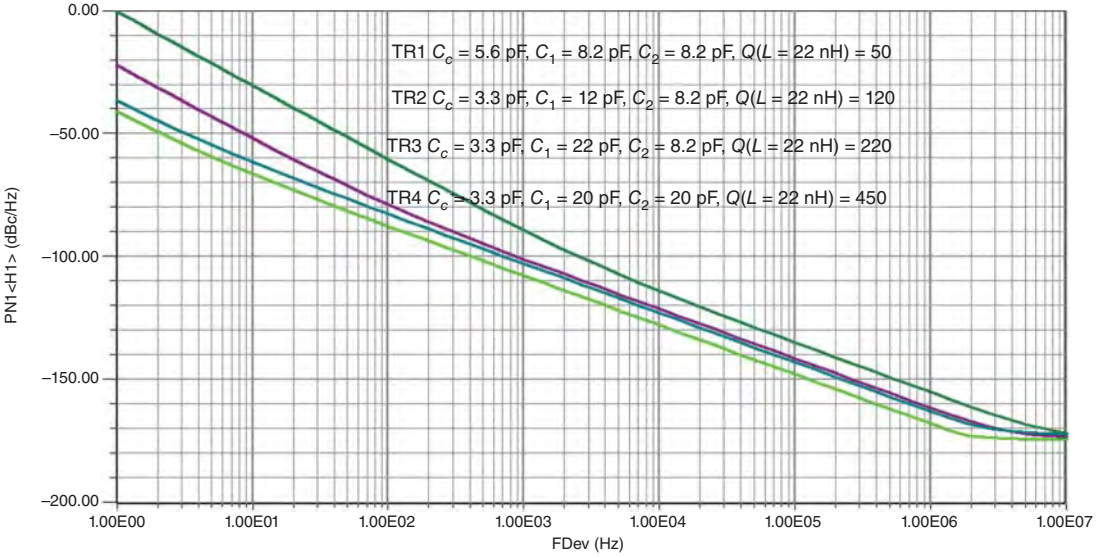


Figure 4-17 Optimized phase noise for different values of inductor *Q*.

A table of normalized transconductance as a function of the drive level, including the large values, is given in Table 4-2 [5].

Figures 4-17–4-19 show the phase noise variation with variation in Q (L = 22 nH) in the LC resonator. The output power, collector current, and base voltage (V_b) and (V_{be}) plots are also shown for the same combinations.

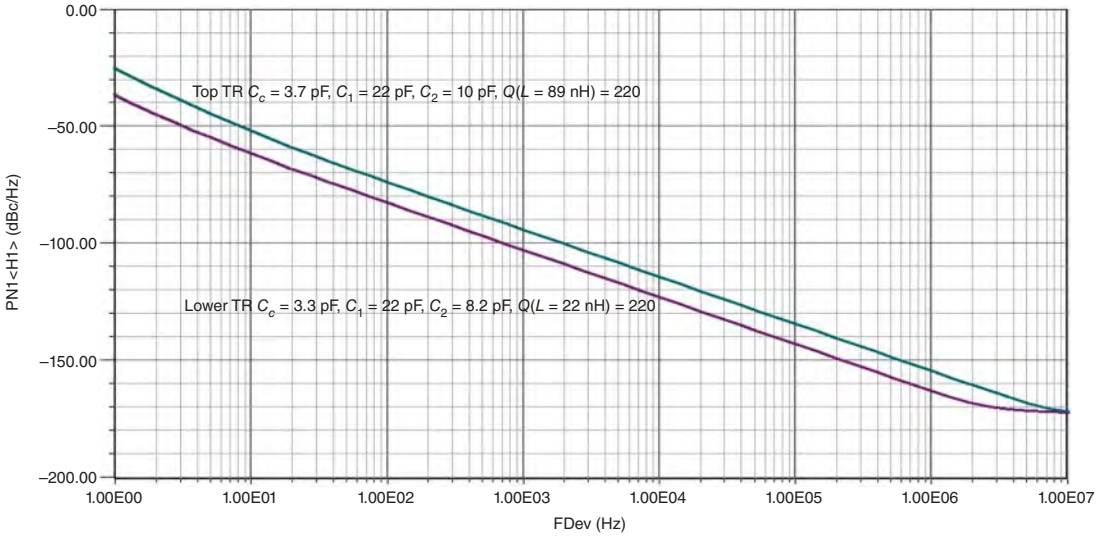


Figure 4-18 Results of series and parallel tuned circuits for same value of inductor *Q*.

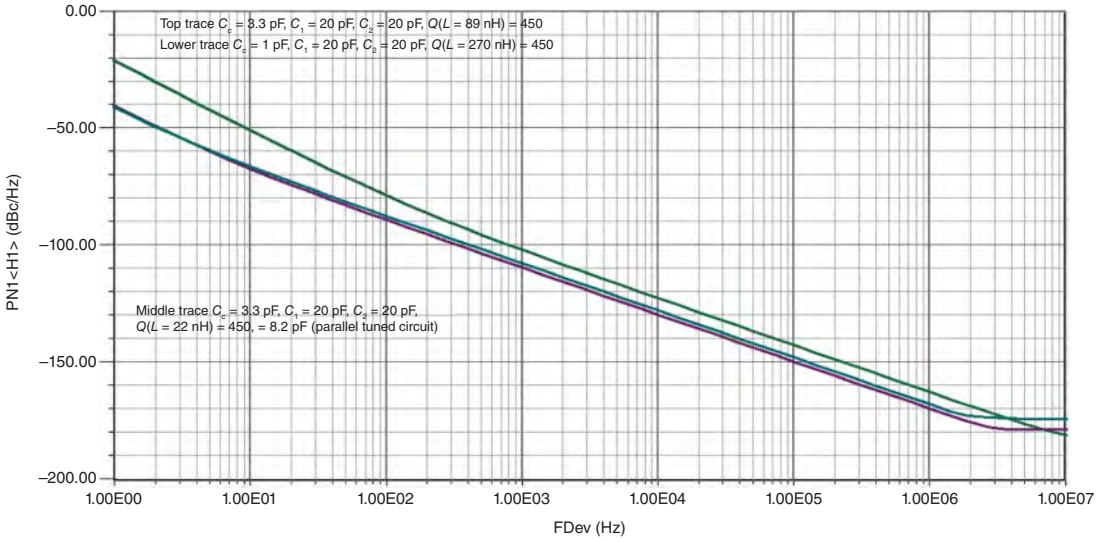


Figure 4-19 Results of series and parallel tuned circuits for higher value of inductor *Q*.

4-2-3 Validation Circuits

The next step is to validate the synthesis of the circuits. The following circuits have been chosen for validation [5]:

- 100 MHz crystal oscillator
- 1000 MHz bipolar transistor-based oscillator with ceramic resonator
- 4100 MHz bipolar transistor-based oscillator with transmission line resonators
- 2000 MHz GaAs FET-based oscillator with transmission line resonators

- 77 GHz SiGe oscillator
- 900–1800 MHz half-butterfly resonator-based oscillator

Design Example for a 100 MHz Crystal Oscillator

For many synthesizers a 100 MHz frequency standard is required [5]. This section describes a design example based on the Phase Noise Analysis of the Feedback Model. Up to here we have calculated both the large-signal drive condition and the optimum choice of the feedback capacitance. Now, we are going to consider the oscillator as a feedback loop with a noisy transistor, looking at all typical noise contributions. Based on a fixed set of values of C_1 and C_2, we can now calculate the accurate phase-noise behavior of the oscillator and analyze the various noise contributions.

First, the noisy bipolar transistor will be introduced. Figure 4-20 shows the familiar hybrid-π transistor circuit, and Figure 4-21 shows the equivalent circuit with the relevant noise sources included.

The mean square value of the noise generators in Figure 4-21, in a narrow frequency offset Δf, are given by

$$\overline{i_{bn}^2} = 2qI_b\Delta f \tag{4-67}$$

$$\overline{i_{cn}^2} = 2qI_c\Delta f \tag{4-68}$$

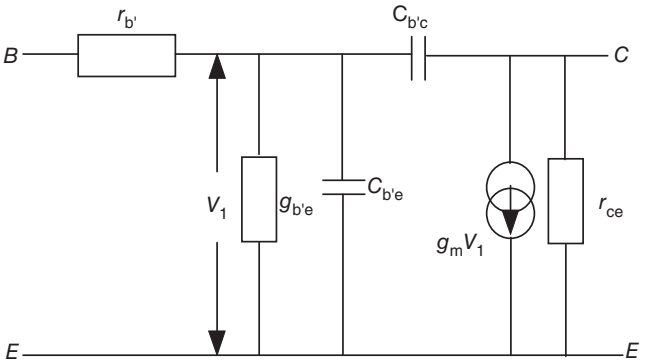


Figure 4-20 Grounded emitter bipolar transistor [5].

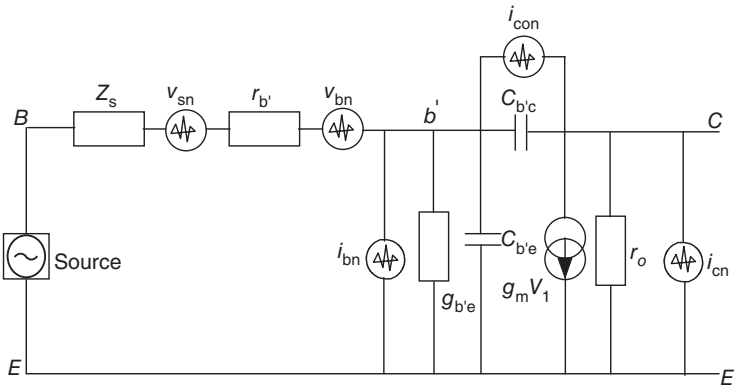


Figure 4-21 Hybrid-π configuration of the grounded bipolar transistor with noise sources [5].

$$\overline{i_{\text{con}}^2} = 2qI_{\text{cob}}\Delta f \tag{4-69}$$

$$\overline{v_{\text{bn}}^2} = 4kTR_b\Delta f \tag{4-70}$$

$$\overline{v_{\text{sn}}^2} = 4kTR_S\Delta f \tag{4-71}$$

where I_b, I_c, and I_{cob} are average dc currents over the Δf noise bandwidth.

The noise power spectral densities due to these noise sources are

$$S(i_{\text{cn}}) = \frac{\overline{i_{\text{cn}}^2}}{\Delta f} = 2qI_c = 2KTg_m \tag{4-72}$$

$$S(i_{\text{bn}}) = \frac{\overline{i_{\text{bn}}^2}}{\Delta f} = 2qI_b = \frac{2KTg_m}{\beta} \tag{4-73}$$

$$S(i_{\text{fn}}) = \frac{K_f I_b^{\text{AF}}}{f} \tag{4-74}$$

$$S(v_{\text{bn}}) = \frac{\overline{v_{\text{bn}}^2}}{\Delta f} = 4KTr_b' \tag{4-75}$$

$$S(v_{sn}) = \frac{\overline{v_{sn}^2}}{\Delta f} = 4KTR_s \tag{4-76}$$

where r_b' and R_s are base and source resistance, respectively, and Z_s is the complex source impedance.

Figure 4-22 shows the feedback arrangement for the Colpitts oscillator with the noise sources.

The transistor is acting like a gain block. The feedback network includes the load conductance, and a small part of the output signal goes to the input of the bipolar transistor through the resonant circuit. The ABCD chain matrix will be used for the analysis.

Figure 4-23 shows the linear representation of the Colpitts oscillator with the input white noise source $i_n(\omega)$.

This is not consistent with Figure 4-22, but useful because all non-active components are now in the feedback network.

The input noise power spectral density can be given as

$$S_{in} = \frac{\left|\overline{i_n^2}\right|}{\Delta f} \tag{4-77}$$

where

$$\left|\overline{i_n^2}\right| = \sum_{i=1}^{i=N}\left|\overline{i_{ni}^2}\right| = \left|\overline{i_{n1}^2}\right| + \left|\overline{i_{n2}^2}\right| + \left|\overline{i_{n3}^2}\right| + \cdots + 2C_{ii}[i_{ni}i_{n(i+1)}^{\bullet}] \tag{4-78}$$

C_{ii} = the noise correlation coefficient

The [*ABCD*] matrix of the aforementioned oscillator circuit can be given as

$$[A] = 1 + \left[\left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\right)\left(j\omega C_2 + \frac{1}{R_E}\right)\right]$$

$$[B] = \frac{1}{j\omega Cc_2} + \left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\right)\left[1 + \left(j\omega C_2 + \frac{1}{R_E}\right)\left(\frac{1}{j\omega Cc_2}\right)\right]$$

$$[C] = j\omega C_1 + \left(j\omega C_2 + \frac{1}{R_E}\right)\left[1 + j\omega C_1\left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\right)\right]$$

$$[D] = \frac{C_1}{Cc_2} + \left[\left(1 + j\omega C_1\left(\frac{1}{j\omega C_c} + \frac{j\omega L_0}{1-\omega^2 L_0 C_0}\right)\right)\left(1 + \left(j\omega C_2 + \frac{1}{R_E}\right)\left(\frac{1}{j\omega Cc_2}\right)\right)\right] \tag{4-79}$$

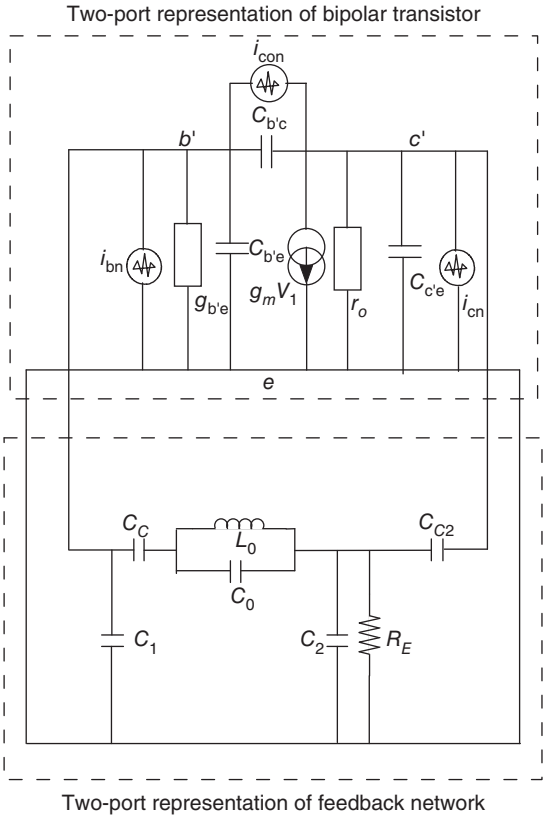


Figure 4-22 Feedback arrangement for the Colpitts oscillator with the noise sources [5].

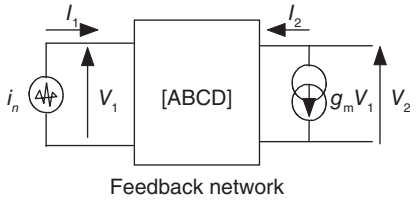


Figure 4-23 Linear representation of feedback Colpitts oscillator with input white noise source $i_n(\omega)$ [5].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{4-80}$$

$$V_1 = AV_2 - BI_2 \tag{4-81}$$

$$I_1 = CV_2 - DI_2 \tag{4-82}$$

$$Z_{\text{in}} = \left[\frac{V_1}{I_1}\right]_{I_{2=0}} = \frac{A}{C} \tag{4-83}$$

where

$$I_1 = i_n \tag{4-84}$$

$$I_2 = -g_m V_1 \tag{4-85}$$

The equivalent input noise voltage due to the input noise current, $I_1 = i_n$, is

$$v_n(\omega) = I_1 Z_{\text{in}} = I_1 \left[\frac{V_1}{I_1}\right]_{I_{2=0}} = I_1 \left[\frac{A(\omega)}{C(\omega)}\right] = i_n \left[\frac{A(\omega)}{C(\omega)}\right] \tag{4-86}$$

The input noise voltage $v_n(\omega)$ will produce two narrowband (1 Hz) uncorrelated components in the frequency domain located at $\omega - \omega_0$ and $\omega + \omega_0$ as $[v_n(\omega)]_{\omega=\omega_0-\Delta\omega}$ and $[v_n(\omega)]_{\omega=\omega_0+\Delta\omega}$.

In presence of the two uncorrelated components of the input noise voltage, $[v_n(\omega)]_{\omega=\omega_0-\Delta\omega}$ and $[v_n(\omega)]_{\omega=\omega_0+\Delta\omega}$, the peak carrier signal of amplitude V_c at frequency $\omega = \omega_0$ is modulated with an input phase noise signal $S_{\Delta\phi_{\text{in}}}(\omega)$.

The input phase noise spectral density at an offset of $\Delta\omega$ is

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = \frac{\left|\overline{[v_n(\omega)]^2_{\omega=\omega_0-\Delta\omega}}\right| + \left|\overline{[v_n(\omega)]^2_{\omega=\omega_0+\Delta\omega}}\right|}{\left|\overline{V_c^2(\omega)}\right|} \tag{4-87}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) \cong \frac{2\left|\overline{[v_n(\omega)]^2}\right|}{\left|\overline{V_c^2(\omega)}\right|} \tag{4-88}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = \frac{2\left|\overline{[v_n(\omega)]^2}\right|}{\left|\overline{V_c^2(\omega)}\right|} = 2\frac{\left|\overline{[i_n(\omega)]^2}\right|}{\left|\overline{V_c^2(\omega)}\right|}\frac{\left|\overline{A^2(\omega)}\right|}{\left|\overline{C^2(\omega)}\right|} \tag{4-89}$$

$$\left|\overline{i_n^2}\right| = S_{\text{in}}\Delta f \tag{4-90}$$

$$\left|\overline{i_n^2}\right|_{\Delta f=1\text{ Hz}} = S_{\text{in}} \tag{4-91}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = 2\frac{S_{\text{in}}}{\left|\overline{V_c^2(\omega)}\right|}\frac{\left|\overline{A^2(\omega)}\right|}{\left|\overline{C^2(\omega)}\right|} \tag{4-92}$$

where S_{in} and $S_{\Delta\phi_{\text{in}}}$ are the input noise power and phase noise spectral density, respectively.

Based on [33, 34],

$$S_{\Delta\phi_{\text{out}}}(\omega) = S_{\Delta\phi_{\text{in}}}(\omega)\left[1 + \frac{1}{(\omega^2)}\left(\frac{\omega_0}{2Q_L}\right)^2\right] \tag{4-93}$$

$$Q_L(\omega = \omega_0) = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega_0} \tag{4-94}$$

The open loop gain is

$$G_{\text{open}}(\omega = \omega_0) = -\left[\frac{g_m}{C(\omega_0)}\right] \tag{4-95}$$

For sustained oscillation $G_{\text{open}}(\omega = \omega_0) = 1 \ \ldots\ -\left[\frac{g_m}{C(\omega_0)}\right] = 1 \Rightarrow C(\omega)_{\omega=\omega_0}$ is real and negative.

$$C(\omega_0) = C_{\text{Real}}(\omega_0) + jC_{\text{Imag}}(\omega_0) \tag{4-96}$$

$$C_{\text{Imag}}(\omega_0) = 0 \tag{4-97}$$

$$C_{\text{Real}}(\omega_0) = -g_m \tag{4-98}$$

$$\left[\frac{d\phi}{d\omega}\right]_{\omega=\omega_0} \approx -\frac{1}{C_{\text{Real}}(\omega_0)}\left[\frac{dC_{\text{Imag}}(\omega)}{d\omega}\right]_{\omega=\omega_0} \tag{4-99}$$

$$Q_L(\omega=\omega_0) = \frac{\omega_0}{2}\left|\frac{d\phi}{d\omega}\right|_{\omega=\omega_0} \tag{4-100}$$

$$Q_L(\omega=\omega_0) = \frac{\omega_0}{2}\left|\frac{1}{C_{\text{Real}}(\omega_0)}\left[\frac{dC_{\text{Imag}}(\omega)}{d\omega}\right]\right|_{\omega=\omega_0} \tag{4-101}$$

$$S_{\Delta\phi_{\text{out}}}(\Delta\omega) = S_{\Delta\phi_{\text{in}}}(\Delta\omega)\left[1+\frac{1}{(\Delta\omega^2)}\left[\frac{C_{\text{Real}}(\omega_0)}{\left(\frac{dC_{\text{Imag}}(\omega)}{d\omega}\right)}\right]^2_{\omega=\omega_0}\right] \tag{4-102}$$

$$S_{\Delta\phi_{\text{in}}}(\Delta\omega) = 2\frac{S_{in}}{\left|\overline{V_c^2(\omega)}\right|}\frac{\left|\overline{A^2(\omega)}\right|}{\left|\overline{C^2(\omega)}\right|} \tag{4-103}$$

$$S_{\Delta\phi_{\text{out}}}(\Delta\omega) = 2\frac{S_{\text{in}}}{\left|\overline{V_c^2(\omega_0)}\right|}\frac{\left|\overline{A^2(\omega_0)}\right|}{\left|\overline{C^2(\omega_0)}\right|}\left[1+\frac{1}{(\Delta\omega^2)}\left[\frac{C_{\text{Real}}(\omega_0)}{\left(\frac{dC_{\text{Imag}}(\omega)}{d\omega}\right)}\right]^2_{\omega=\omega_0}\right] \tag{4-104}$$

We now perform the noise analysis of the Colpitts oscillator.

Individual Contribution of all Four Noise Sources The following contribute to the noise of the oscillator:

- Thermal noise associated with the loss resistance of the resonator
- Thermal noise associated with the base resistance of the transistor
- Shot noise associated with the base bias current
- Shot noise associated with the collector bias current

If we now use the oscillator circuit with a noisy resonator, we can calculate the total noise of the oscillator as shown in Figure 4-24.

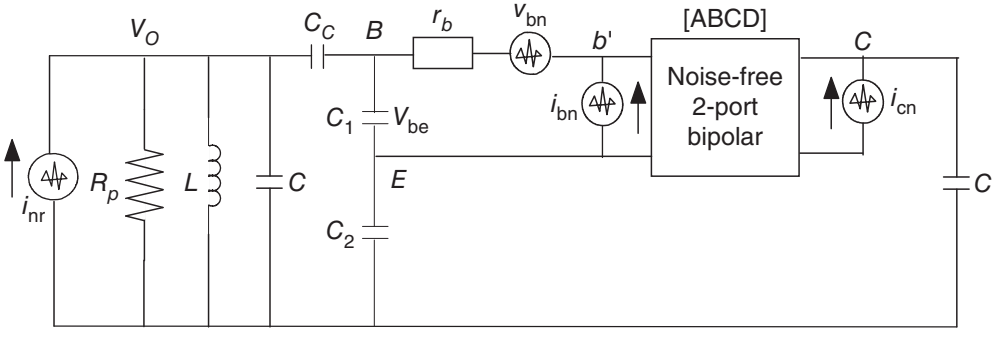


Figure 4-24 The oscillator circuit with 2-port [ABCD] matrix, consistent with the approach of Figure 4-21.

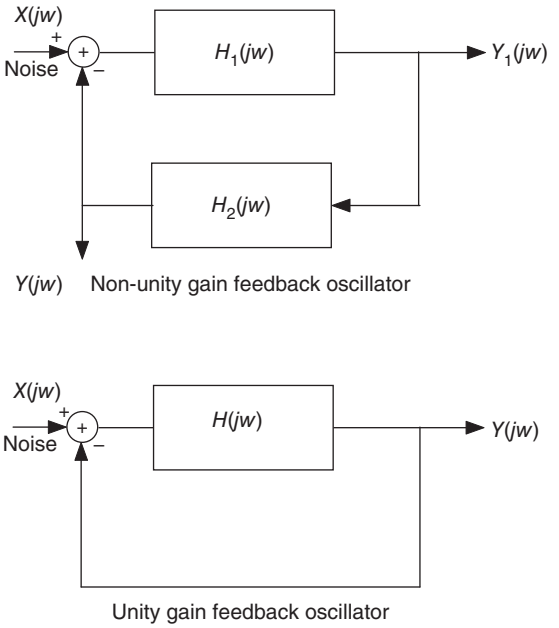


Figure 4-25 Feedback oscillator with noise source.

Noise Shaping Function of the Resonator For phase noise analysis, the oscillator is considered as a feedback system and a noise source is present in the input as shown in the Figure 4-25.

Oscillator output phase noise is a function of

- The amount of the source noise present at the input of the oscillator circuit
- The amount the feedback system rejects or amplifies various noise components

The unity-gain system closed loop transfer function is

$$[TF(j\omega)]_{\text{closed-loop}} = \frac{Y(j\omega)}{X(j\omega)} = \frac{H(j\omega)}{1 + H(j\omega)} \tag{4-105}$$

$$[H(j\omega)]_{\omega=\omega_0} = -1 \tag{4-106}$$

For frequencies close to $\omega = \Delta\omega + \omega$ the open loop transfer function is

$$[H(j\omega)]_{\omega=\omega_0+\Delta\omega} \approx \left[H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega}\right] \tag{4-107}$$

The noise transfer function is

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right] = \left[\frac{H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega}}{1 + H(j\omega_0) + \Delta\omega \frac{dH(j\omega)}{d\omega}}\right] \tag{4-108}$$

Since $H(j\omega_0) = -1$ and for most practical cases $\Delta\omega \frac{dH(j\omega)}{d\omega} \ll 1$, we can write

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right] \approx \left[\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}}\right] \tag{4-109}$$

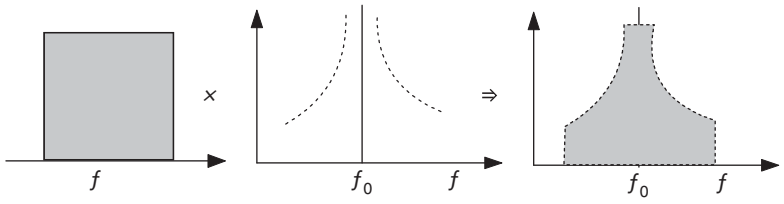


Figure 4-26 Noise shaping in the oscillator.

From the noise transfer function, it appears that the noise component at $\omega = \Delta\omega + \omega_0$ is multiplied by the term

$$\left[\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}}\right]$$

relative to the output.

The broadband white noise is shaped by the resonator as seen in Figure 4-26.

Therefore, the noise power spectral density can be explained as

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left|\frac{-1}{\Delta\omega \frac{dH(j\omega)}{d\omega}}\right|^2 \tag{4-110}$$

for

$$H(j\omega) = A(j\omega)\exp[j\varphi(j\omega)] \tag{4-111}$$

$$\frac{dH(j\omega)}{d\omega} = \left[\frac{dA(j\omega)}{d\omega} + jA(j\omega)\frac{d\varphi(j\omega)}{d\omega}\right]\exp[j\varphi(j\omega)] \tag{4-112}$$

Assume $\omega = \Delta\omega + \omega_0$, $\omega \to \omega_0$, and $|A(j\omega_0)| \to 1$, then the aforementioned equation is reduced to

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left[\frac{1}{(\Delta\omega)^2\left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0} \tag{4-113}$$

The open loop Q_L becomes

$$Q_L = \frac{\omega_0}{2}\sqrt{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2} \tag{4-114}$$

and

$$\left|\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \left[\frac{1}{(\Delta\omega)^2\left\{\left[\frac{dA(j\omega)}{d\omega}\right]^2 + \left[\frac{d\varphi(j\omega)}{d\omega}\right]^2\right\}}\right]_{\omega=\Delta\omega+\omega_0} = \frac{1}{4Q_L{}^2}\left[\frac{\omega_0}{\Delta\omega}\right]^2 \tag{4-115}$$

For the LC resonator $\left[\frac{dA(j\omega)}{d\omega}\right]$ at resonance ($\omega \to \omega_0$) becomes zero and $Q_L = \frac{\omega_0}{2}\frac{d\phi}{d\omega}$.

Non-unity Gain For the non-unity gain feedback case where $H(j\omega) = H_1(j\omega)H_2(j\omega)$, it follows that

$$\left[\frac{Y(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right]_{\omega=\Delta\omega+\omega_0} \approx \left[\frac{-1}{\Delta\omega\frac{dH(j\omega)}{d\omega}}\right] \tag{4-116}$$

and

$$\frac{Y_1(j\omega)}{X(j\omega)} = \frac{H_1(j\omega_0)}{1 + H(j\omega_0)} \tag{4-117}$$

then the noise power is shaped by the transfer function as

$$\left|\frac{Y_1(j\omega + j\Delta\omega)}{X(j\omega + j\Delta\omega)}\right|^2 = \frac{|H_1(j\omega)|^2}{(\Delta\omega)^2\left|\frac{dH(j\omega)}{d\omega}\right|^2} \tag{4-118}$$

For the lossy RLC resonator see Figure 4-27.
Then,

$$H(\omega_0 + \Delta\omega) = \left[\frac{V_{\text{out}}(\omega_0 + \Delta\omega)}{i_n(\omega_0 + \Delta\omega)}\right]_{\omega=\Delta\omega+\omega_0} = \left[\frac{1}{g_{\text{resonator}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\left[\frac{1}{2Q_L}\right] \tag{4-119}$$

$$g_{\text{resonator}} = \frac{1}{R_P} \tag{4-120}$$

where R_P is the equivalent loss resistance of the resonator.

Noise Transfer Function and Spectral Densities The noise transfer function for the relevant sources is described in this section.

Noise transfer function of the thermal loss resistance of the resonator:

$$\text{NFT}_{\text{inr}}(\omega_0) = \frac{1}{2}\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \rightarrow \tag{4-121}$$

Noise transfer function of the transistor's base resistance noise:

$$\text{NFT}_{V_{\text{bn}}}(\omega_0) = \frac{1}{2}\left[\frac{C_1 + C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \rightarrow \tag{4-122}$$

Noise transfer function of the transistor's base current flicker noise:

$$\text{NFT}_{i_{\text{bn}}}(\omega_0) = \frac{1}{2}\left[\frac{C_2}{C_1 + C_2}\right]\left[\frac{1}{2\omega_0 Q C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \rightarrow \tag{4-123}$$

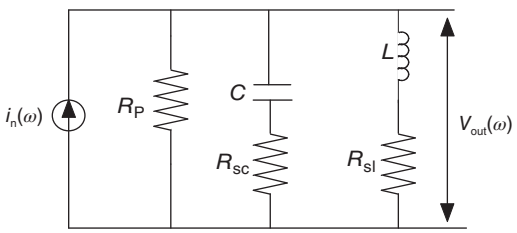


Figure 4-27 Noise response of the RLC resonator.

Noise transfer function of the transistor's flicker noise:

$$\mathrm{NFT}_{i_{\mathrm{fn}}}(\omega_0) = \frac{1}{2}\left[\frac{C_2}{C_1 + C_2}\right]\left[\frac{1}{2\omega_0 Q C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \rightarrow \tag{4-124}$$

Noise transfer function of the collector current shot noise:

$$\mathrm{NFT}_{i_{\mathrm{cn}}}(\omega_0) = \frac{1}{2}\left[\frac{C_1}{C_1 + C_2}\right]\left[\frac{1}{2\omega_0 Q C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right] \rightarrow \tag{4-125}$$

where

$$C_{\mathrm{eff}} = C + \frac{C_1 C_2}{C_1 + C_2} \tag{4-126}$$

$$V_o(\omega_0) = nV_{\mathrm{be}}(\omega_0) \tag{4-127}$$

$\mathrm{NFT}_{\mathrm{in}}(\omega_0)$, $\mathrm{NFT}_{V_{\mathrm{bn}}}(\omega_0)$, $\mathrm{NFT}_{i_{\mathrm{bn}}}(\omega_0)$, and $\mathrm{NFT}_{i_{\mathrm{cn}}}(\omega_0)$ are the noise transfer functions as explained.

The various noise sources of the oscillator circuit whereby the flicker noise current is added to the base current and their noise spectral density is $\frac{K_f I_b^{\mathrm{AF}}}{f_m}$ are as follows:

$[\mathrm{NSD}]_{\mathrm{inr}} = \frac{4KT}{R_P} \rightarrow$ noise spectral density of the thermal noise current from the loss resistance of the resonator
$[\mathrm{NSD}]_{\mathrm{Vbn}} = 4KTr_b \rightarrow$ noise spectral density of the thermal noise voltage from the base resistance
$[\mathrm{NSD}]_{\mathrm{ibn}} = 2qI_b \rightarrow$ noise spectral density of the shot noise current from the base current
$[\mathrm{NSD}]_{\mathrm{ifn}} = \frac{K_f I_b^{\mathrm{AF}}}{f_m} \rightarrow$ Noise spectral density due to 1/*f*-flicker noise
$[\mathrm{NSD}]_{\mathrm{icn}} = 2qI_c \rightarrow$ noise spectral density of the shot noise current from the collector current.

The phase noise contribution now is:

$$\mathrm{PN}(\omega_0 + \Delta\omega) = [\mathrm{NSD}]_{\text{noise-source}}[\mathrm{NFT}_{\text{noise-source}}(\omega_0)]^2 \tag{4-128}$$

$$\mathrm{PN}_{\mathrm{inr}}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}[\mathrm{NF}_{\mathrm{inr}}(\omega_0)]^2 \tag{4-129}$$

$$\mathrm{PN}_{\mathrm{Vbn}}(\omega_0 + \Delta\omega) = 4KTr_b[\mathrm{NF}_{\mathrm{Vbn}}(\omega_0)]^2 \tag{4-130}$$

$$\mathrm{PN}_{\mathrm{ibn}}(\omega_0 + \Delta\omega) = 2qI_B[\mathrm{NF}_{\mathrm{ibn}}(\omega_0)]^2 \tag{4-131}$$

$$\mathrm{PN}_{\mathrm{ifn}}(\omega_0 + \Delta\omega) = \frac{K_f I_b^{\mathrm{AF}}}{f_m}[\mathrm{NF}_{\mathrm{ibn}}(\omega_0)]^2 \tag{4-132}$$

$$\mathrm{PN}_{\mathrm{icn}}(\omega_0 + \Delta\omega) = 2qI_c[\mathrm{NF}_{\mathrm{icn}}(\omega_0)]^2 \tag{4-133}$$

where $\mathrm{PN}(\omega_0 + \Delta\omega)$ is the phase noise at the offset frequency $\Delta\omega$ from the carrier frequency ω_0 and $[\mathrm{NSD}]_{\text{noise-source}}$ is the noise spectral density of the noise sources. The phase noise contribution is

$\mathrm{PN}_{\mathrm{inr}}(\omega_0 + \Delta\omega) = \frac{4KT}{R_P}[\mathrm{NFT}_{\mathrm{inr}}(\omega_0)]^2 = \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase noise contribution from the resonator tank.

$\mathrm{PN}_{\mathrm{Vbn}}(\omega_0 + \Delta\omega) = 4KTr_b[\mathrm{NFT}_{\mathrm{Vbn}}(\omega_0)]^2 = 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase noise contribution from the base resistance.

$\mathrm{PN}_{\mathrm{ibn}}(\omega_0 + \Delta\omega) = 2qI_b[\mathrm{NFT}_{\mathrm{ibn}}(\omega_0)]^2 = 2qI_b\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{\omega_0 Q C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \rightarrow$ phase noise contribution from the base current.

$\mathrm{PN}_{\mathrm{ifn}}(\omega_0+\Delta\omega)=\frac{K_f I_b^{\mathrm{AF}}}{f_m}[\mathrm{NF}_{\mathrm{ibn}}(\omega_0)]^2=\frac{K_f I_b^{\mathrm{AF}}}{f_m}\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the flicker noise of the transistor.

$\mathrm{PN}_{\mathrm{icn}}(\omega_0+\Delta\omega)=2qI_c[\mathrm{NFT}_{\mathrm{icn}}(\omega_0)]^2=2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the collector current.

The total effect of all the four noise sources can be expressed as

$$\mathrm{PN}(\omega_0+\Delta\omega)=[\mathrm{PN}_{\mathrm{inr}}(\omega_0+\omega)]+[\mathrm{PN}_{\mathrm{Vbn}}(\omega_0+\omega)]+[\mathrm{PN}_{\mathrm{ibn}}(\omega_0+\omega)]+[\mathrm{PN}_{\mathrm{icn}}(\omega_0+\omega)] \tag{4-134}$$

$$\mathrm{PN}(\omega_0+\Delta\omega)=\frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2+4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2Q}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$$
$$+\left[2qI_b+\frac{2\pi K_f I_b^{\mathrm{AF}}}{\Delta\omega}\right]\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{2Q\omega_0 C_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2+2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 QC_{\mathrm{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2 \tag{4-135}$$

where

K_f = flicker noise constant
AF = flicker noise exponent

$$C_{\mathrm{eff}}=C+\frac{C_1C_2}{C_1+C_2} \tag{4-136}$$

Note: The effect of the loading of the Q of the resonator is calculated by the noise transfer function multiplied with the noise sources.

The phase noise contribution from the different noise sources for the parallel tuned Colpitts oscillator circuit at $\Delta\omega = 10\,\mathrm{kHz}\,2\pi$ from the oscillator frequency $\omega_0 = 100\,\mathrm{MHz}\,2\pi$ will next be computed. Circuit parameters are as follows:

- Base resistance of transistor rb = 6.14 Ω.
- Parallel loss resistance of the resonator RP = 7.54E11 Ω
- Q of the resonator = 60,000
- Resonator inductance = 15 mH
- Resonator capacitance = 2.7 pF
- Collector current of the transistor Ic = 13 mA
- Base current of the transistor Ib = 130 μA
- Flicker noise exponent AF = 2
- Flicker noise constant Kf = 1E-11
- Feedback factor $n = 6$

Comparing phase noise at 100 Hz and phase noise at 10 kHz,

$\mathrm{PN}_{\mathrm{inr}}(\omega_0+100\,\mathrm{Hz})=-162\,\mathrm{dBc/Hz}$	$\mathrm{PN}_{\mathrm{inr}}(\omega_0+10\,\mathrm{kHz})=-202\,\mathrm{dBc/Hz}$
$\mathrm{PN}_{\mathrm{Vbn}}(\omega_0+100\,\mathrm{Hz})=-176\,\mathrm{dBc/Hz}$	$\mathrm{PN}_{\mathrm{Vbn}}(\omega_0+10\,\mathrm{kHz})=-216\,\mathrm{dBc/Hz}$
$\mathrm{PN}_{(\mathrm{ibn}+\mathrm{ifn})}(\omega_0+100\,\mathrm{Hz})=-140\,\mathrm{dBc/Hz}$	$\mathrm{PN}_{(\mathrm{ibn}+\mathrm{ifn})}(\omega_0+10\,\mathrm{kHz})=-200\,\mathrm{dBc/Hz}$
$\mathrm{PN}_{(\mathrm{icn})}(\omega_0+100\,\mathrm{Hz})=-148\,\mathrm{dBc/Hz}$	$\mathrm{PN}_{(\mathrm{icn})}(\omega_0+10\,\mathrm{kHz})=-189\,\mathrm{dBc/Hz}$

Note: The noise contribution from the resonator at this offset is the same as the flicker noise contribution from the transistor.

It appears that the flicker noise and the noise from the resonator are the limiting factors for the overall phase noise performance of the oscillator circuit.

The dependence of the phase noise performance due to different noise sources present in the oscillator circuits is

$$\mathrm{PN}_{\mathrm{inr}}(\omega_0 + \Delta\omega) \propto \frac{1}{R_P} \tag{4-137}$$

$$\mathrm{PN}_{\mathrm{Vbn}}(\omega_0 + \Delta\omega) \propto = r_b \left\{ \frac{1}{Q} \left[1 + \frac{C_1}{C_2} \right] \right\}^2 \tag{4-138}$$

$$\mathrm{PN}_{\mathrm{ibn}}(\omega_0 + \Delta\omega) \propto I_b \left\{ \frac{1}{QC_{\mathrm{eff}}} \left[\frac{C_2}{C_1 + C_2} \right] \right\}^2 \tag{4-139}$$

$$\mathrm{PN}_{\mathrm{icn}}(\omega_0 + \Delta\omega) \propto = I_c \left\{ \frac{1}{QC_{\mathrm{eff}}} \left[\frac{C_1}{C_1 + C_2} \right] \right\}^2 \tag{4-140}$$

Once the resonator Q is known (parallel loss resistance is fixed), then the only option left is to select a device having a low flicker noise. The base resistance, current, and collector current add little to the performance! Finally, optimization of the phase noise can be done by proper selection of the feedback capacitor under the constraints of the loop gain so that it maintains oscillation.

The value of "n" is defined as $(1 + C_1/C_2)$. Table 4-3 shows the resulting phase noise of a 100 MHz crystal oscillator.

Interesting enough, the far-out noise is not affected, but the close-in noise is. The reason for this is that the larger the C_1 becomes, the more it short-circuits the transistor noise, to the point where the feedback is no longer is large enough for oscillation. There is a limit for how large "n" can be made as one has to consider tolerances in the components and also the temperature-dependence; 7, seems to be a reasonable value, for this particular transistor. The value of n would have to be recalculated for different transistor and frequency of oscillation.

Figure 4-28 illustrates the negative impedance calculation. The capacitance ratio based on an open loop gain of 6 and calculations of Y_{21} (0.225) and the dc (100 mV) offset based on the Bessel function is 6.

The simulation confirms that oscillation occurs at the correct frequency and the phase noise, as shown in Figures 4-29 and 4-30, is attractive.

Design Example of a 1000 MHz CRO

Many applications require a very low-noise microwave oscillator in the 1000 MHz region, and this is best accomplished with a ceramic resonator. An operating Q in the vicinity of 500 is available in this material. An oscillator using an NEC NE68830 transistor has been selected because of its superior flicker noise performance. The Colpitts oscillator uses an 8.2 Ω resistor between the emitter and the capacitive feedback. Rather than take the RF signal at the collector, it is taken from a tap of the emitter inductor. The collector circuit, using PNP transistors, has been designed to set the dc current. The necessary equations for this dc bias are found in [35].

Table 4-3 Phase noise as a function of feedback factor *n*

$n = (1 + C_1/C_2)$	Resulting PN at 100 Hz	Resulting PN at 10 kHz
2	−130 dBc/Hz	−190 dBc/Hz
3	−136 dBc/Hz	−193.4 dBc/Hz
4	−140 dBc/Hz	−193.4 dBc/Hz
5	−142 dBc/Hz	−193.4 dBc/Hz
6	−144 dBc/Hz	−193.4 dBc/Hz
7	−146 dBc/Hz	−193.4 dBc/Hz

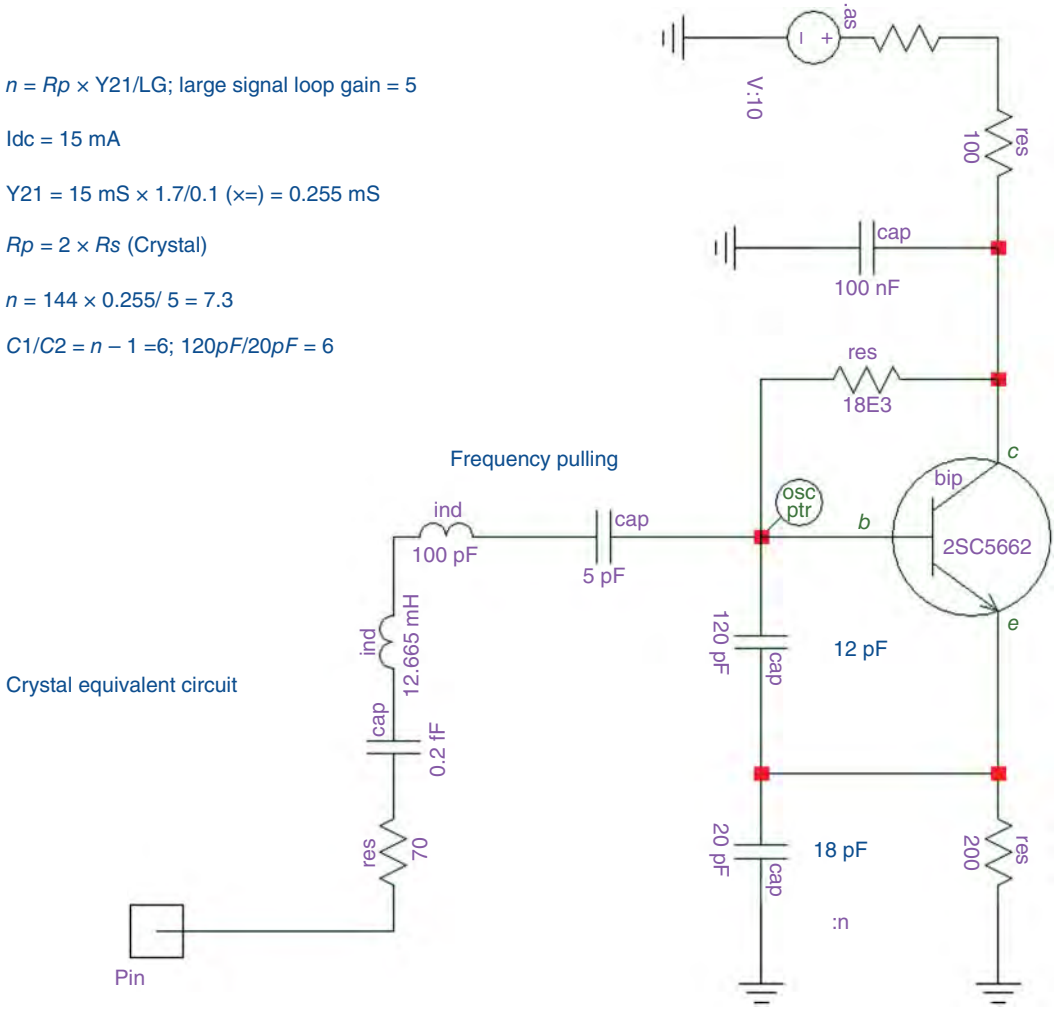


Figure 4-28 Negative impedance calculation.

Class-A common-emitter amplifiers are usually very sensitive to stray impedance in the emitter circuit. Any small inductance in series with the emitter will cause instability; for this reason, the emitter needs to be grounded as directly as possible and bias components in the emitter are generally undesirable. In the schematic in Figure 4-31, Q_1 is the RF amplifier and Q_2 provides its base current required for constant voltage difference across R_c. This constant voltage difference then ensures constant collector current.

Diode D_1 provides some measure of temperature compensation. R_b should be high in order not to affect base impedance, but not so high to cause Q_2 to saturate over temperature and β_1 variation. Neglecting the base current of Q_2, the design equations are

$$I_c = \frac{R_1(A^+ - V_d)}{R_c(R_1 + R_2)} \tag{4-141}$$

$$V_c = A^+ - I_c R_c \tag{4-142}$$

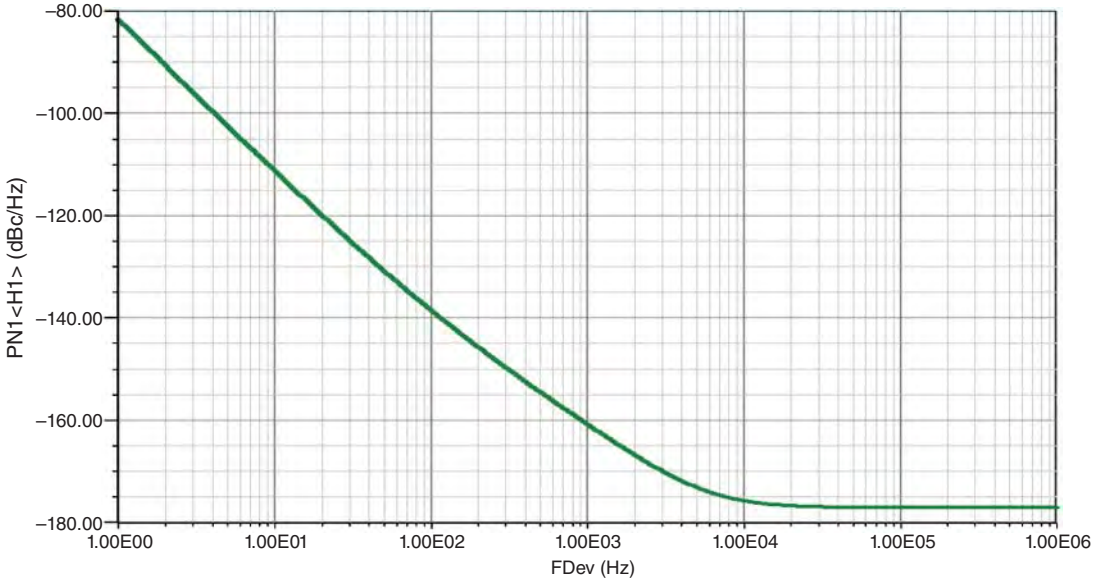


Figure 4-29 Simulated phase noise plot of the circuit in Figure 4-28.

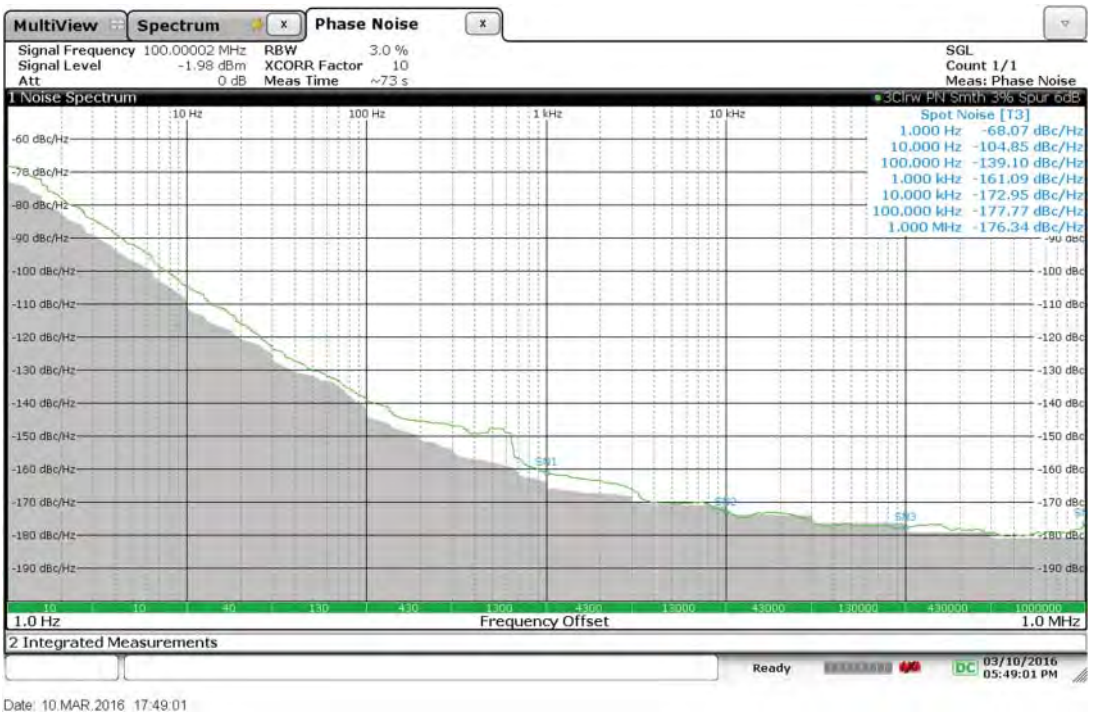


Figure 4-30 Measured phase noise plot of a 100 MHz crystal oscillator.

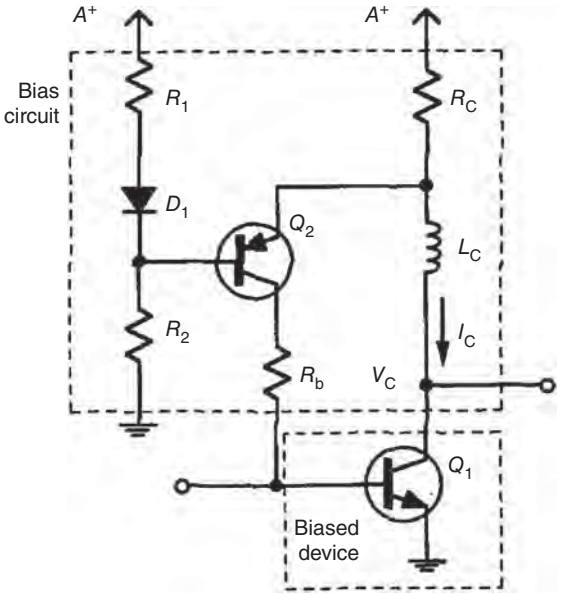


Figure 4-31 Active bias network for a common-emitter RF amplifier stage.

Assuming that we are designing the bias circuit to provide a certain device bias current I_c and collector voltage V_c, select a convenient supply voltage $A^+ > V_c$. The component values are then supplied by the following equations.

$$R_c = \frac{A^+ - V_c}{I_c} \tag{4-143}$$

$$R_1 = \frac{A^+ - V_c}{I_d} \tag{4-144}$$

$$R_2 = \frac{V_c - V_d}{I_d} \tag{4-145}$$

$$R_b < \beta_{\min} \frac{V_c - V_d - 0.2}{I_c} \tag{4-146}$$

where

I_c = desired collector current of Q_1 (A)
V_c = desired collector voltage of Q_1 (V)
V_d = diode, or base–emitter voltage drop, nominally 0.7 (V)
A^+ = chosen supply voltage (V)
R_i = resistor values as shown in Figure 4-30 (Ω)
I_d = bias current through R_1, R_2, and D_1 (A)
$\beta_{\min}$ = minimum beta of Q_1

The bias circuit shown has to be carefully bypassed at both high and low frequencies. There is one inversion from base to collector of Q_1, and another inversion may be introduced by L_c matching components and stray capacitances, resulting in positive feedback around the loop at low frequencies. Low equivalent series resistance (ESR) electrolytic or tantalum capacitors from the collector of Q_2 to ground is usually adequate to ensure stability.

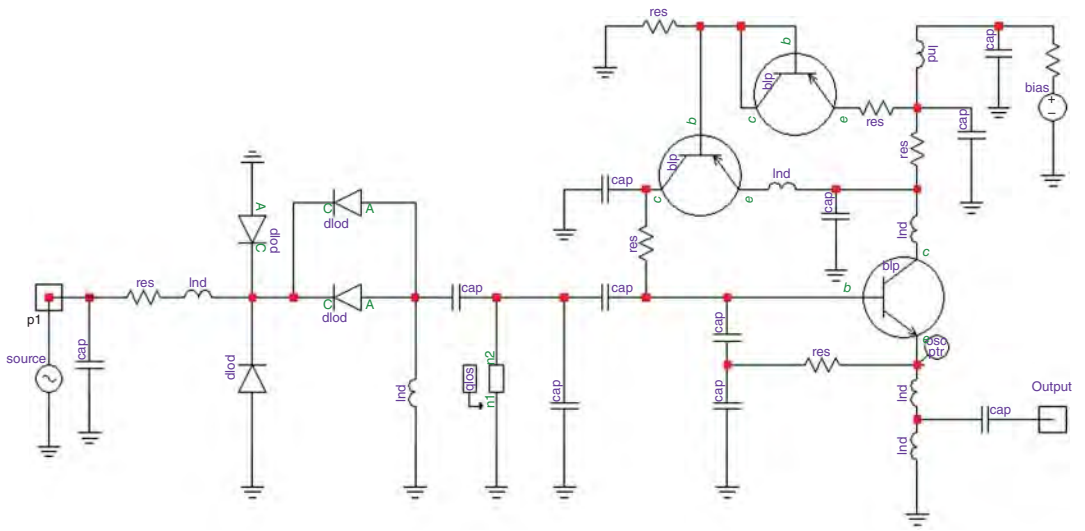


Figure 4-32 1000 MHz ceramic resonator oscillator.

The ceramic resonator is coupled loosely to the transistor with a capacitor of 0.9 pF. The resonator has a parallel capacitor of 0.6 pF, which reduces the manufacturing tolerances of the resonator. The tuning diode assembly, two diodes in parallel, is coupled to the resonator with 0.8 pF. The reason for using two diodes was that there was not one single diode available with the necessary capacitance and Q. Figure 4-32 shows the schematic of the oscillator.

It has been pointed out that the best operating condition will be the case where the most negative resistance occurs at the point of resonance to achieve the best phase noise performance. This is shown in Figure 4-33. The purple-colored curve starting below zero shows the imaginary current that resonates at 1000 MHz, while the green-colored curve shows the negative resistance. The maximum negative peak occurs at exactly 1000 MHz, as it should be.

Figure 4-34 shows the measured phase noise of this oscillator. The measurements were performed with the Aeroflex Euro Test system. At 1 kHz the phase noise is approximately 95 dBc/Hz and at 10 kHz it is approximately 124 dBc/Hz. This is a 30 dB/decade slope, which is triggered by the flicker corner frequency of the transistor. From 10 to 100 kHz, the slope is 20 dB/decade with a phase noise of −145.2 dBc/Hz at 100 kHz. At 1 MHz off the carrier, it is −160 dBc/Hz.

Because of the narrow tuning range and the loose coupling of the tuning diode, the noise contribution of the diode is negligible.

This circuit has been designed using the synthesis procedure and also has been analyzed with the harmonic-balance simulator *Microwave Harmonica* from Ansoft Corporation. Figure 4-35 shows the predicted performance of the phase noise. The actual circuit arrangement is shown in Figure 4-36. The ceramic resonator can be spotted easily.

The parallel tuned circuit shows better phase noise performance, as seen in Figure 4-19, due to the fact that the rate of change of reactance in a parallel tuned circuit is significantly larger than in a simple series tuned oscillator.

4100 MHz Oscillator with Transmission Line Resonators

For less demanding applications, it is possible to design oscillators using transmission line resonators. Their Q depends on the material and implementation of the resonator. Figure 4-37 shows the circuit of the oscillator. While the previous example was a Colpitts parallel resonant circuit, this circuit operates in series resonant mode. The NPN transistor, NE68830, has parasitic inductance in the emitter, base, and collector lines. For the purpose of accurate modeling, TEE and cross-junction models were used, as well as transmission lines where applicable.

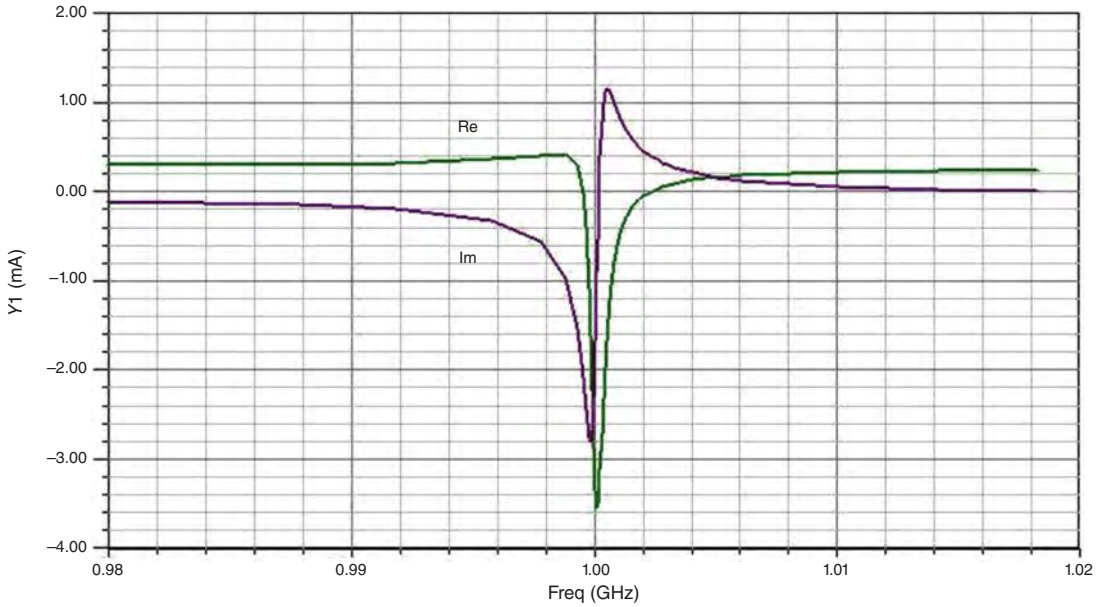


Figure 4-33 Plot of the real and imaginary oscillator currents as a function of frequency.

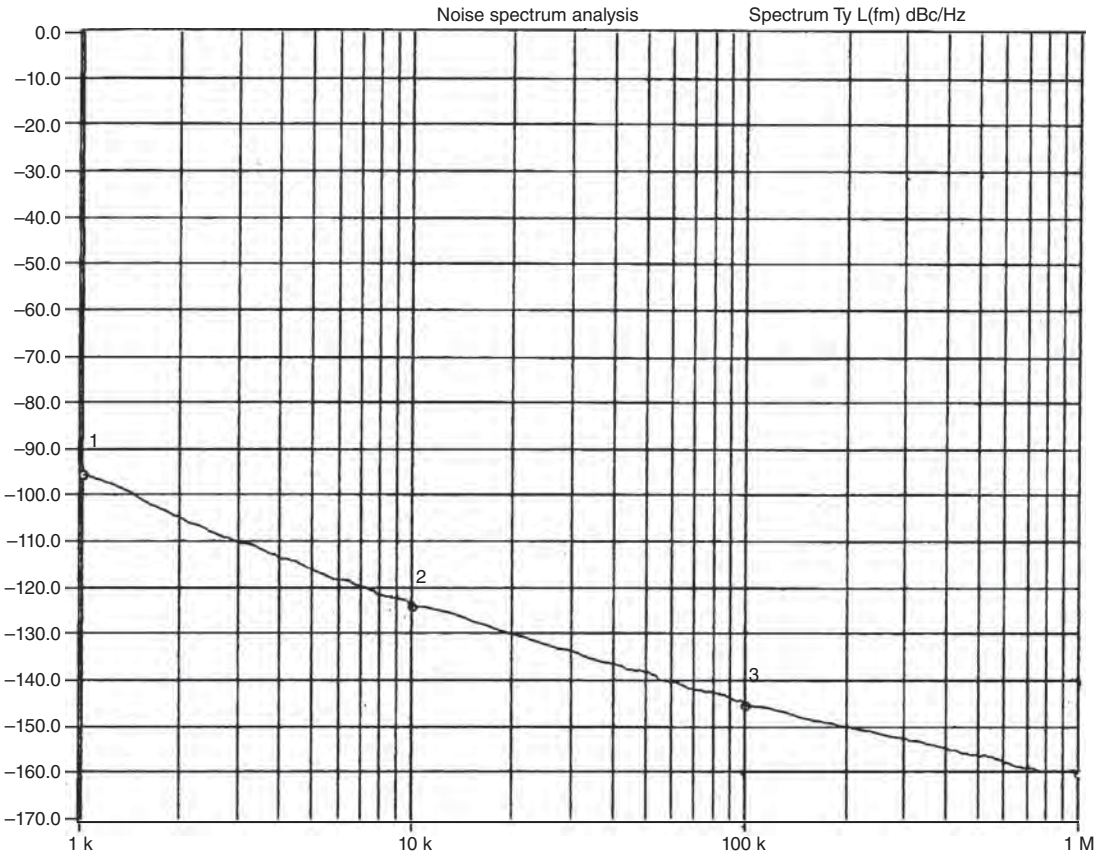
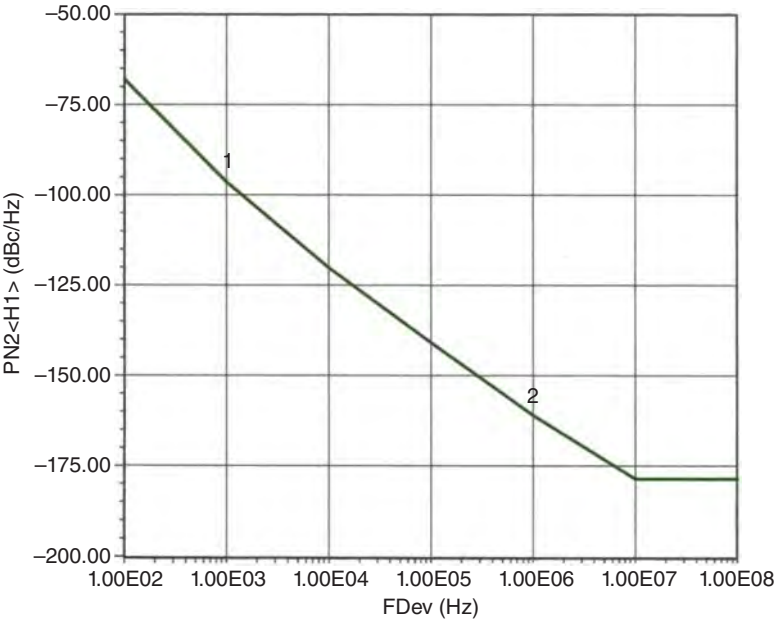


Figure 4-34 Measured phase noise of the 1000 MHz ceramic resonator oscillator.



*X*1 = 1.00E03 Hz *X*2 = 1.00E06 Hz
*Y*1 = –96.30 dBc/Hz *Y*2 = –160.67 dBc/Hz

Figure 4-35 Predicted phase noise of the CRO at 1 GHz shown in Figure 4-33.

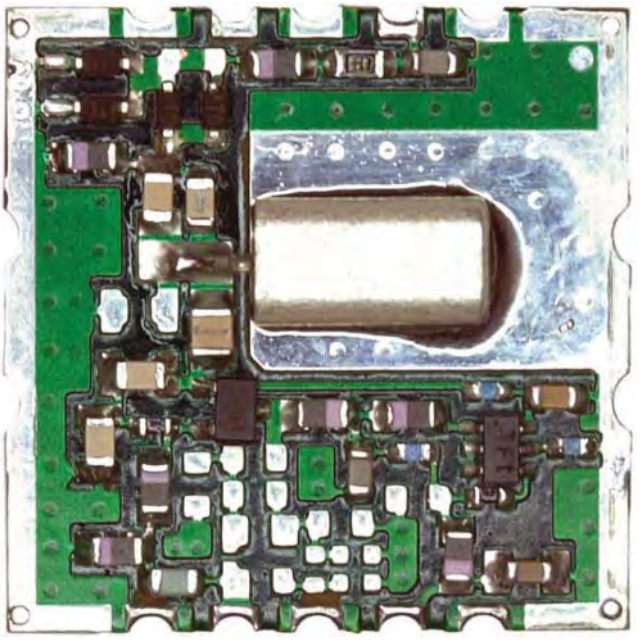


Figure 4-36 Photograph of the 1 GHZ CRO of the schematic shown in Figure 4-32.

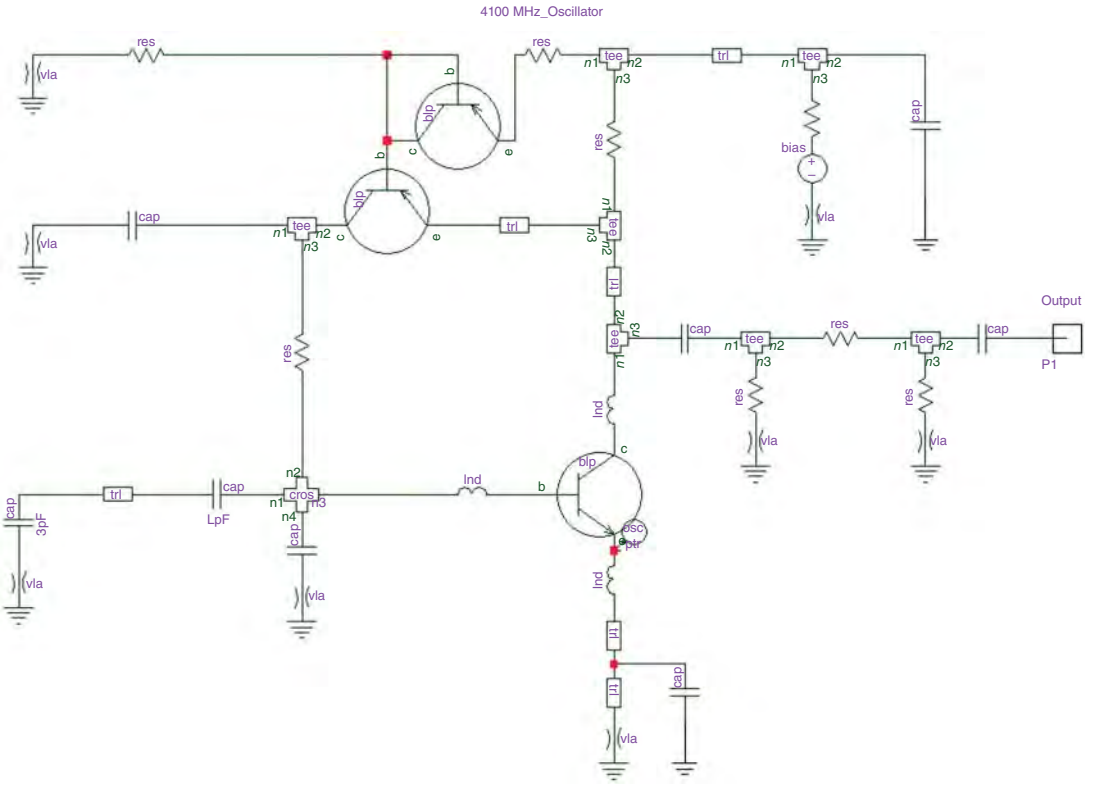


Figure 4-37 Circuit diagram of the 4.1 GHz oscillator.

The dc stabilization circuit uses the same technique as shown in Figure 4-32. This time the RF power is taken from the collector and uses a 10 dB attenuator to minimize frequency pulling. The ground connections for the capacitors are done using via holes. A via hole is the electrical equivalent of a small inductor.

The phase noise of this oscillator was simulated using the values of the synthesis program. Figure 4-38 shows the predicted phase noise.

The output power of this oscillator is 6.8 dBm. This oscillator was built and measured. Figure 4-39 shows the printed circuit board of the oscillator.

Because of the pad-like microstrips, the simulation needs to be done very carefully, and the soldering of the component is also very critical. This frequency range makes the assembly very difficult because it is not high enough for an RFIC and still needs to be done on a printed circuit board. The measured phase noise is shown in Figure 4-40. It agrees well with the predicted phase noise. At 100 kHz the difference is about 3 dB. The same is valid at 10 kHz. At 1 kHz there is a larger difference. The flicker corner frequency of the actual device is different than the simulation.

2000 MHz GaAs FET-Based Oscillator

Low-cost applications are frequently implemented as an RFIC. For further validation, a GaAs FET-based 2000 MHz Colpitts oscillator was designed and built. Figure 4-41 shows the circuit diagram of the oscillator. It uses a combination of transmission lines and rectangular inductors as resonators. The inductor in the middle of the schematic in Figure 4-41, connected to a via hole, is needed as a dc return. If a tuning diode is connected to the capacitor on the left of the schematic in Figure 4-41, then a dc control voltage can be applied, and the

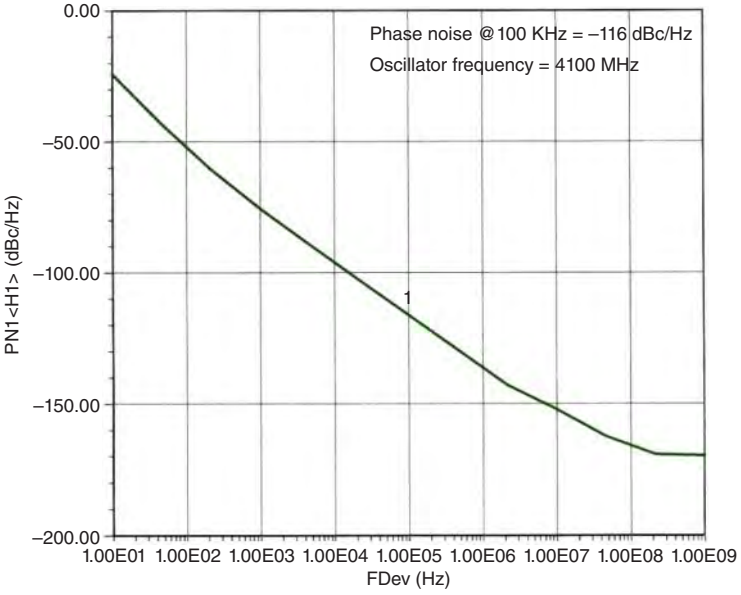


Figure 4-38 Predicted phase noise of the 4.1 GHz oscillator.

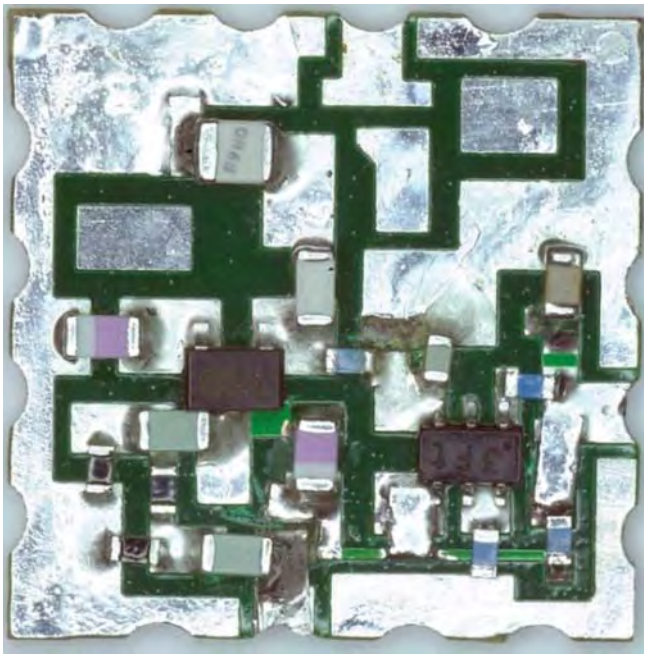


Figure 4-39 Printed circuit board of the 4.1 GHz oscillator shown in Figure 4-38.

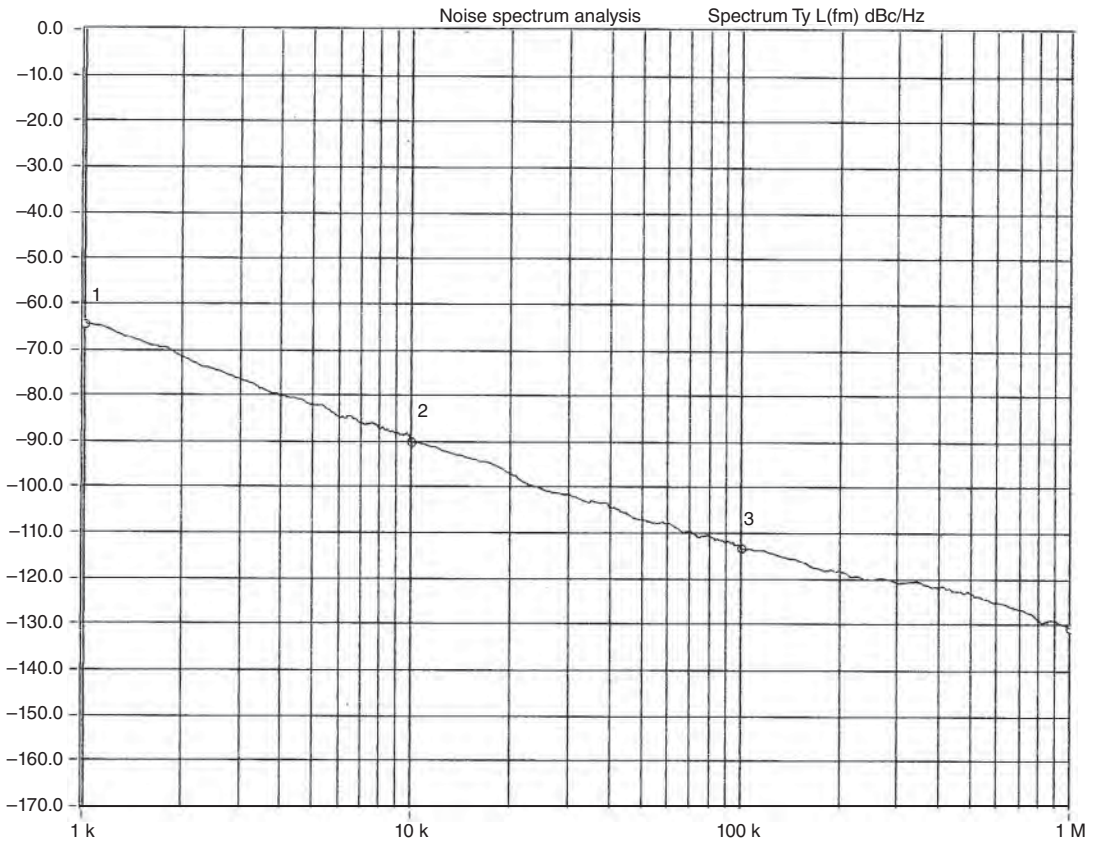


Figure 4-40 Measured phase noise of the 4.1 GHz oscillator.

center inductor becomes an RF choke. The output is taken from the source. An additional external dc decoupling capacitor will be needed because of the dc coupling. The transistor and the circuit were constructed using the TriQuint GaAs Foundry and the transistor was optimized for the dc current. Figure 4-42 shows the predicted phase noise of this oscillator.

The measured values were 100 dBc/Hz at 100 kHz and 120 dBc/Hz at 1 MHz offsets. There is a deviation of about 2 dB compared to simulation.

It is interesting to examine the load line of this oscillator, which is shown in Figure 4-43. This circuit is operated in a fairly linear range.

Figure 4-44 shows the layout of the 2 GHz GaAs FET Oscillator. Its output power is 1.8 dBm.

77 GHz SiGe Oscillator

Millimeter-wave oscillator circuits have been implemented using SiGe bipolar transistors. A considerable amount of data on output power and phase noise regarding these oscillators is found in literature. Therefore, it was interesting to synthesize a 77 GHz oscillator using lossy, lumped elements, which later can be translated into distributed elements, specifically, coplanar waveguides.

Figure 4-45 shows a Colpitts oscillator that is designed around an advanced product of the BFP620 family. It is the typical Colpitts arrangement with a capacitive divider. The resonant circuit consists of a 0.07 pF capacitor and a 100 pH inductor with a Q of 70. Figure 4-46 shows the predicted phase noise at 77 GHz, which agrees well

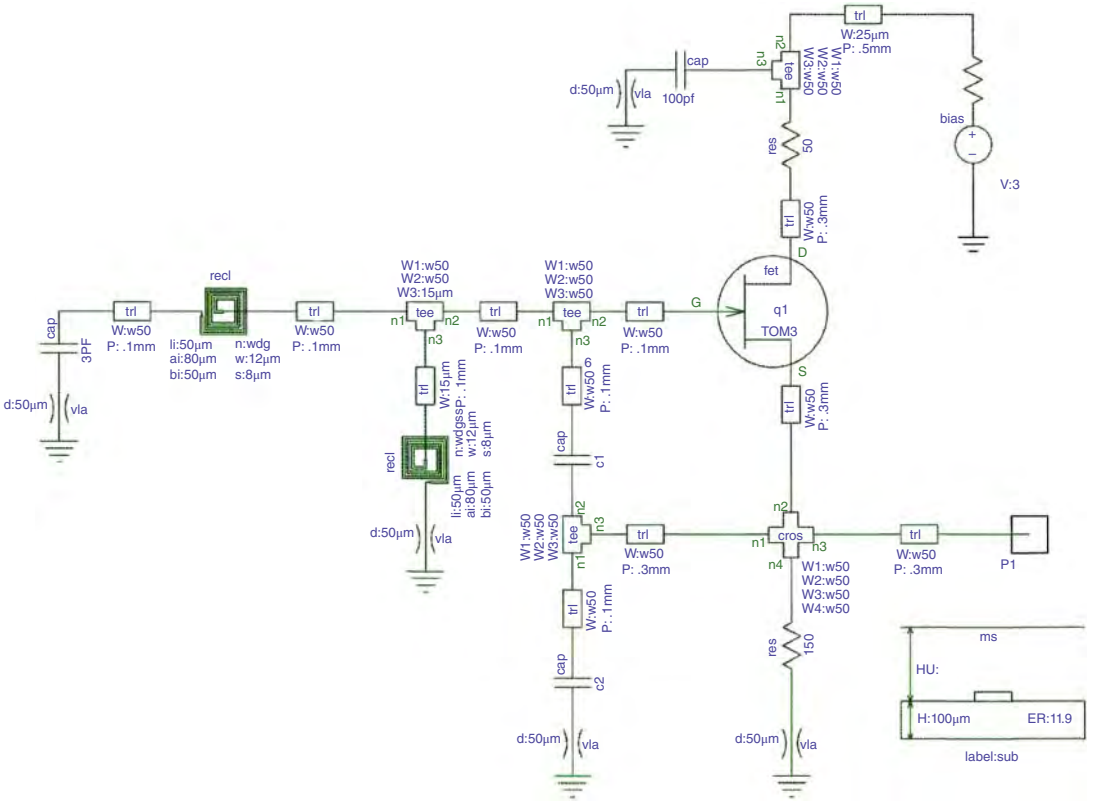
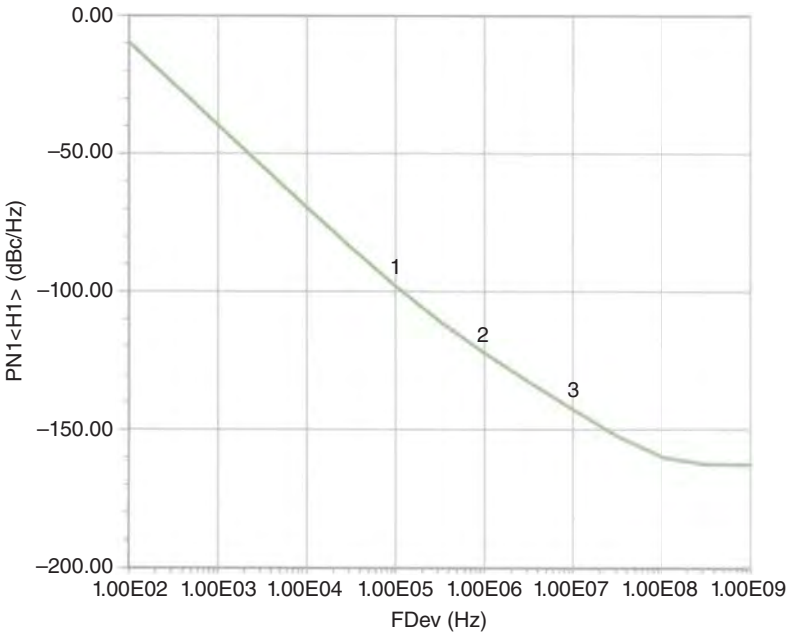


Figure 4-41 Circuit diagram of the 2 GHz GaAs FET oscillator.



*X*1 = 1.00E05 Hz *X*2 = 1.00E06 Hz *X*3 = 1.00E07 Hz
*Y*1 = –98.04 dBc/Hz *Y*2 = –122.22 dBc/Hz *Y*3 = –142.68 dBc/Hz

Figure 4-42 Predicted phase noise of the oscillator shown in Figure 4-41.

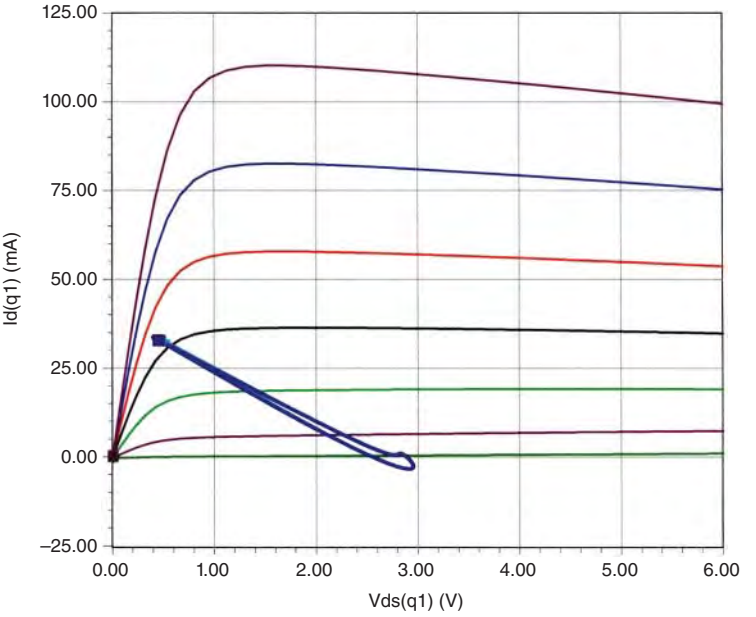


Figure 4-43 Trace of the dc-IV and the load line for the GaAs FET oscillator.

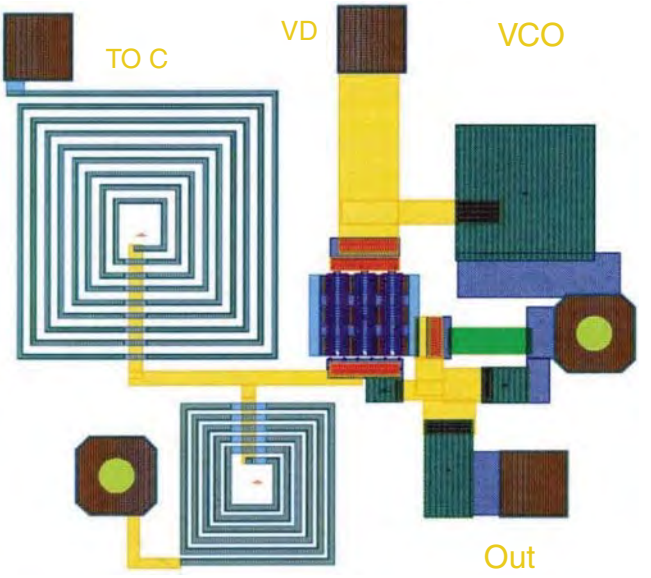


Figure 4-44 Layout of the 2 GHz GaAs FET oscillator.

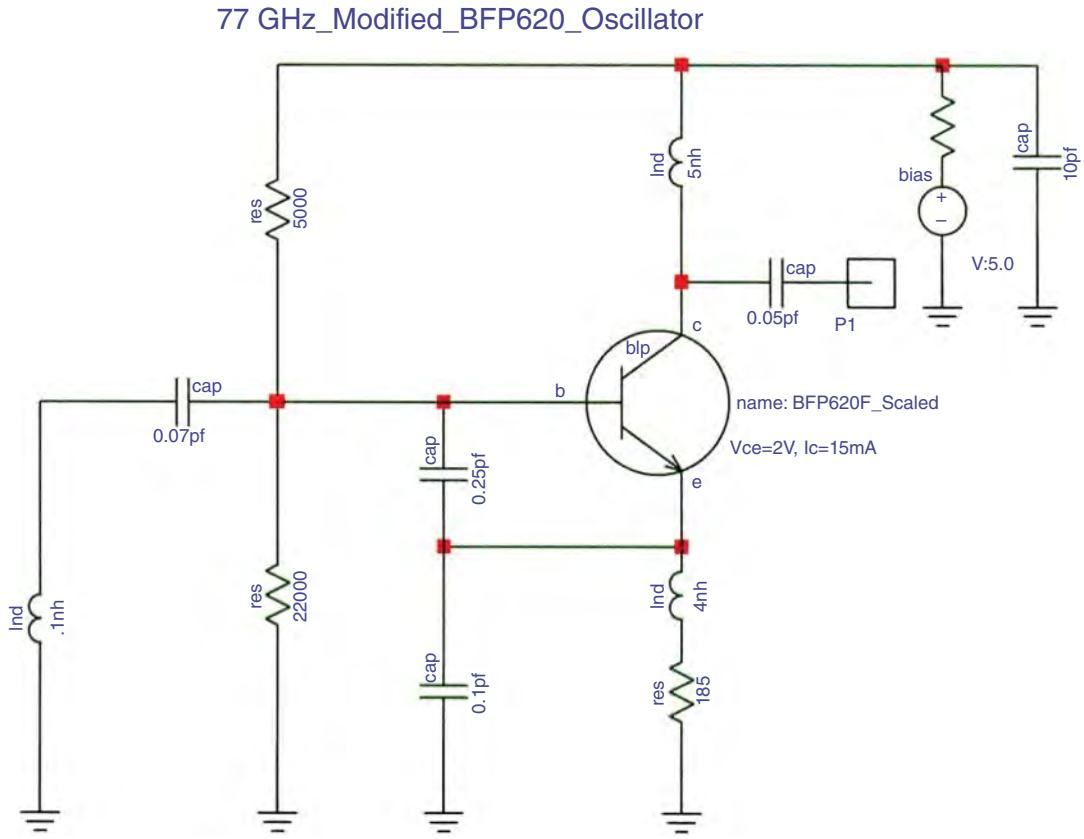
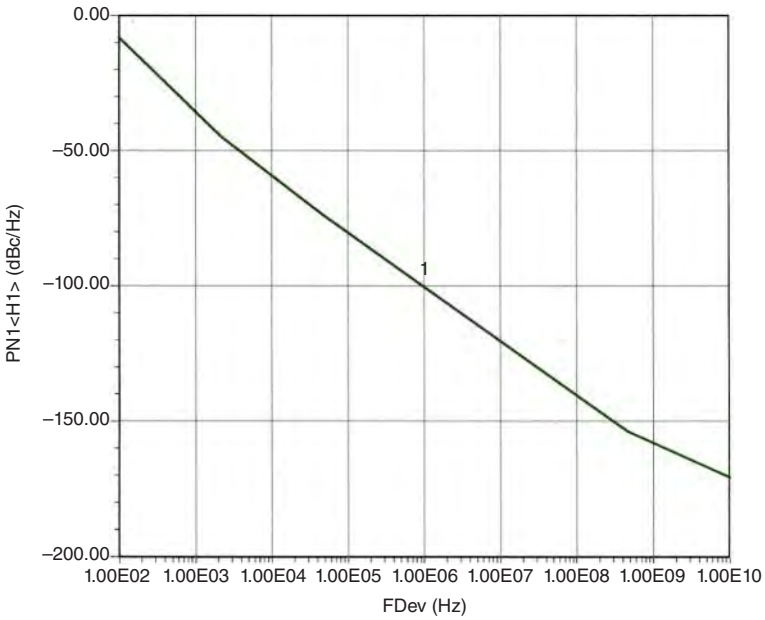


Figure 4-45 77 GHz Colpitts oscillator.



*X*1 = 1.00E06 Hz
*Y*1 = –100.43 dBc/Hz

Figure 4-46 Predicted phase noise of the oscillator shown in Figure 45.

with published data. Here $n = \left(1 + 1\frac{C_1}{C_2}\right) = 3$ (the low Q case as described earlier). The literature shows that such values are obtainable [36–45].

900–1800 MHz Half-Butterfly Resonator-Based Oscillator

This is the example of an oscillator that can only be analyzed, built, and optimized using electromagnetic (EM) tools. The resonator here is a quarter-wave length resonator at 1800 MHz, which gets pulled down by the tuning diodes. Its schematic is shown in Figure 4-47.

For a better understanding, the circuit, which highly depends upon the layout information, is given in Figure 4-48. The resonator is shown on the top right of the layout, a half-butterfly arrangement. The hole on the lower right side is the marking for the ground via.

This was the first attempt to build an EM-based oscillator from where the coupled resonator activity evolved. Figure 4-48 shows the actual built oscillator, and Figure 4-49 shows the achieved phase noise. Given the fact that this is a 1–2 range oscillator (900–1800 MHz), the phase noise compares favorably with other efforts in this frequency range.

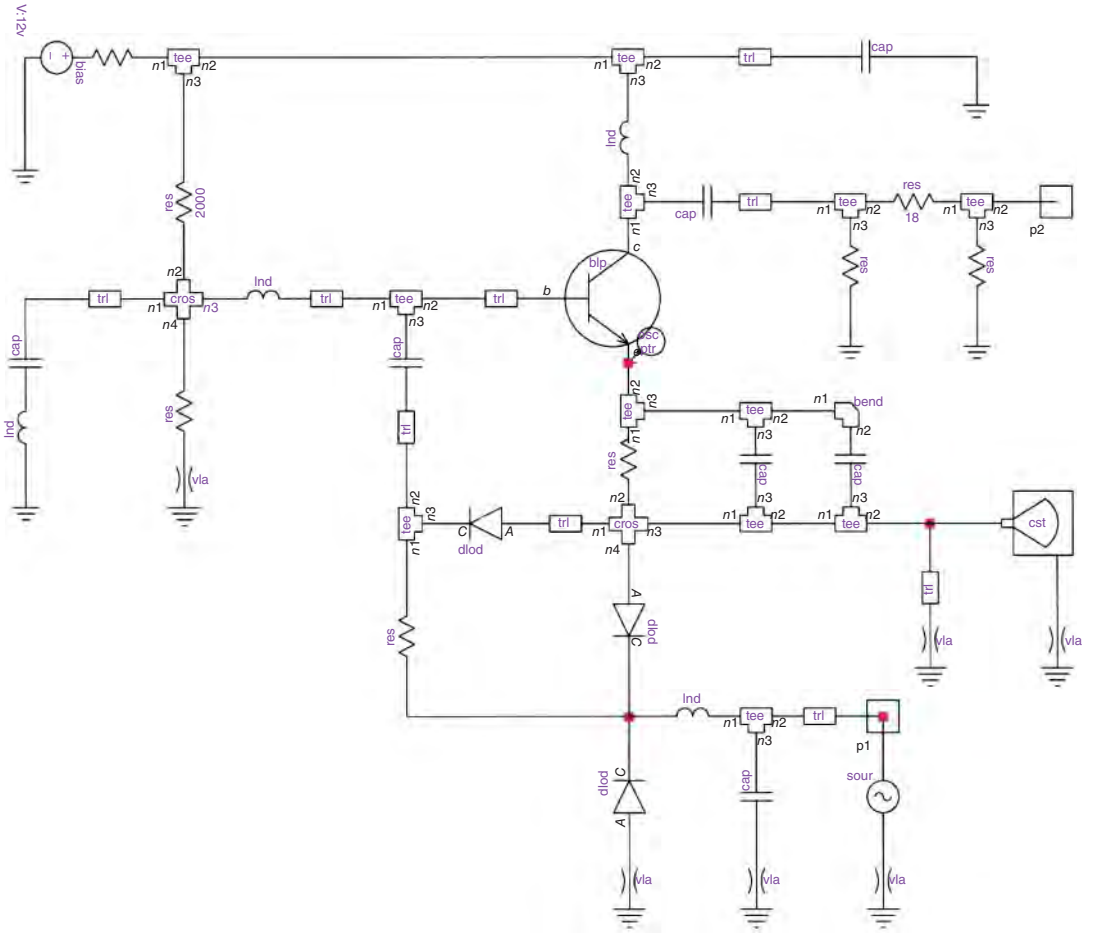


Figure 4-47 Schematic of the oscillator used to demonstrate the multiple-coupled resonator.

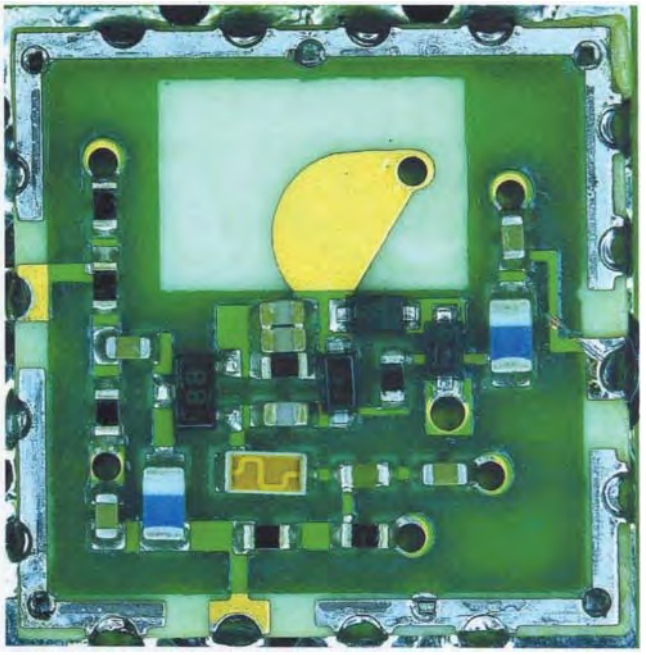


Figure 4-48 Photograph of the 900–1800 MHz VCO.

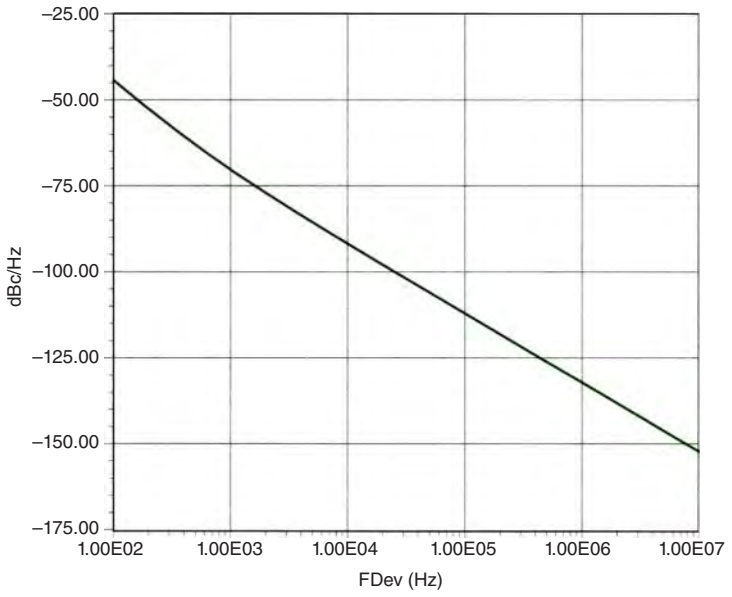


Figure 4-49 Predicted phase noise of the half-butterfly resonator oscillator.

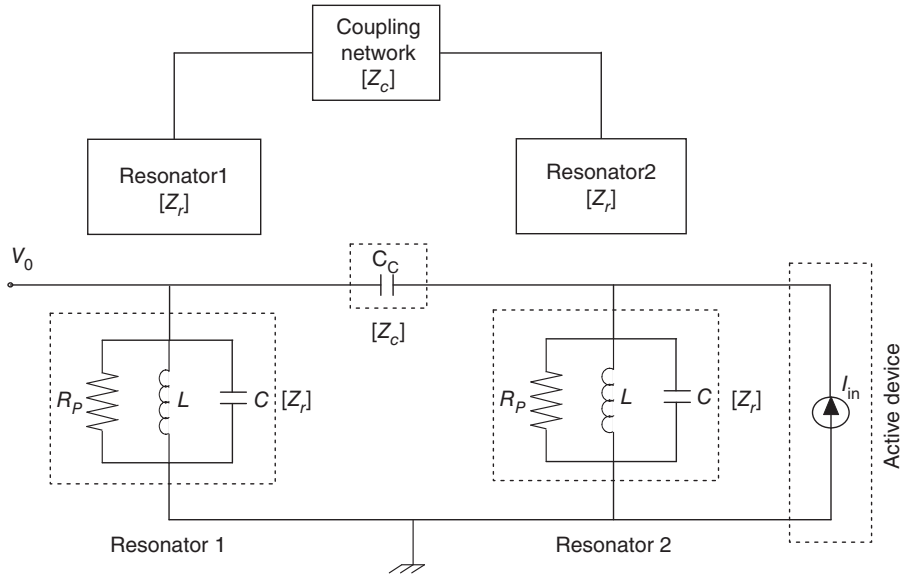


Figure 4-50 Series capacitive coupled resonator.

Coupled Resonator The Q factor of the resonator can be increased by introducing the coupling factor β, which is defined as the ratio of the series coupling capacitor to the resonator capacitor. Figure 4-50 shows two identical resonators with series coupling where Z_r and Z_c are the resonators and the coupling network impedance, respectively.

The effective coupled impedance of the Figure 4-48 is given by

$$Z_{\text{eff}}(\omega) = \left[\frac{V_o}{I_{\text{in}}}\right] = \frac{Z_r(\omega)}{2 + \frac{Z_c(\omega)}{Z_r(\omega)}} = \frac{Z_r^2(\omega)}{Z_c(\omega) + 2Z_r(\omega)} \tag{4-147}$$

where I_{in} is the large-signal current from the active device.

$$Y_{\text{eff}}(\omega) = \frac{1}{Z_{\text{eff}}(\omega)} = \left[\frac{Z_c(\omega)}{Z_r^2(\omega)} + \frac{2}{Z_r(\omega)}\right] = \left[\frac{Y_r^2(\omega)}{Y_c(\omega)} + 2Y_r(\omega\right] \tag{4-148a}$$

For $Z_c(\omega) \gg Z_r(\omega)$, and assuming the Q factor of $Z_r(\omega)$ is sufficiently large, the denominator of Eq. (4-147) may be considered constant over the frequencies within the bandwidth of $Z_r(\omega)$. The coupling admittance is defined by $Y_c(\omega) = j\omega C_c$.

The resonator admittance is given by

$$Y_r(\omega) = \left[\frac{1}{R_P} + \frac{1}{j\omega L} + j\omega C\right] = \left[\frac{j\omega LR_P}{R_P(1 - \omega^2 LC) + j\omega L}\right]^{-1} \tag{4-148b}$$

From (4-148a) and (4-148b) $Y_{\text{eff}}(\omega)$ can be rewritten as

$$Y_{\text{eff}}(\omega) = \left[\frac{2}{R_P} - \frac{2R_P(1 - \omega^2 LC)}{\omega^2 LR_p^2 \beta C}\right] + j\left[\frac{[R_P^2(1 - \omega^2 LC)^2 - \omega^2 L^2]}{\omega^3 R_P^2 L^2 \beta C} - \frac{2R_P(1 - \omega^2 LC)}{R_P \omega L}\right] \tag{4-149}$$

From (4-148b), the phase shift of the coupled resonator is given as

$$\phi = \tan^{-1}\left[\frac{\left(\frac{[R_P^2(1-\omega^2LC)^2-\omega^2L^2]}{\omega^3R_P^2L^2\beta\,C} - \frac{2R_P(1-\omega^2LC)}{R_P\omega\,L}\right)}{\left(\frac{2}{R_P} - \frac{2R_P(1-\omega^2LC)}{\omega^2LR_p^2\beta\,C}\right)}\right] \tag{4-150}$$

At resonance the real part of $Y_{\text{eff}}(\omega)$ is reduced to zero, and the resonance frequency can be derived as

$$\text{Re}[Y_{\text{eff}}(\omega)]_{\omega=\omega_0} = \left[\frac{2}{R_P} - \frac{2R_P(1-\omega^2LC)}{\omega^2LR_p^2\beta\,C}\right]_{\omega=\omega_0} = 0 \Rightarrow \omega_0^2LC(1+\beta) = 1 \tag{4-151}$$

$$[\omega_0]_{\varphi=90°} = \frac{1}{\sqrt{LC(1+\beta)}} \tag{4-152}$$

$$[Y_{\text{eff}}(\omega)]_{\omega=\omega_0} = -j\left[\frac{R_P^2\beta^2C + (1+\beta)L}{\beta(1+\beta)\omega LR_P^2C}\right] \tag{4-153}$$

$$Z_{\text{eff}}(\omega)]_{\omega=\omega_0} = j\left[\frac{\beta(1+\beta)\omega LR_P^2C}{R_P^2\beta^2C + (1+\beta)L}\right] = j\left[\frac{\beta R_P^2\omega C}{\frac{R_P^2\beta^2C}{(1+\beta)L}+1}\right] \Rightarrow j\left[\frac{Q_0\beta R_P}{1+Q^2\beta^2}\right] \tag{4-154}$$

where

$$Q_0 = \omega\,CR_P = \frac{R_P}{\omega\,L}$$

$$\beta = \frac{C_c}{C}$$

From (4-152), the effective quality factor of the coupled resonator is given by [46–48]

$$[Q_{\text{eff-coupled}}(\omega)]_{\omega=\omega_0} = \frac{\omega_0}{2}\left[\frac{\partial\varphi}{\partial\omega}\right] \Rightarrow \frac{2Q_0(1+\beta)}{(1+Q_0^2\beta^2)} \tag{4-155}$$

$$[Q_{\text{eff-coupled}}(\omega_0)]_{\beta\ll1} = \left[\frac{2Q_0(1+\beta)}{(1+Q_0^2\beta^2)}\right]_{\beta\ll1} \approx 2Q_0 \tag{4-156}$$

Weakly coupled resonators ($\beta \ll 1$) will produce high attenuation due the large value of Z_c, so a trade-off between doubling the Q factor and the permissible attenuation is required for the best phase noise performance. For octave-band tunability, the coupling factor β is dynamically adjusted over the tuning range for low-noise performance.

Optimum Phase Noise with Respect to the Loaded Q The amount of loading on a resonator is critical for optimum phase noise in voltage-controlled oscillators (VCOs). A very lightly loaded resonator will have a higher Q factor but will pass less power through it, whereas a heavily loaded resonator will have a very low Q factor but will pass more power through it. From Figure 4-51, the equivalent loading is R_{reso} in parallel with the series combination of $1/g_m$ and R_L, and this will represent the loading factor in the oscillator circuit.

From [5, Eq. (7-26)], the phase noise is given as

$$\mathcal{L}(f_m) = 10\log\left\{\left[1 + \frac{{f_0}^2}{(2f_mQ_L)^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0} + \frac{2kTRK_0^2}{f_m^2}\right\} \tag{4-157}$$

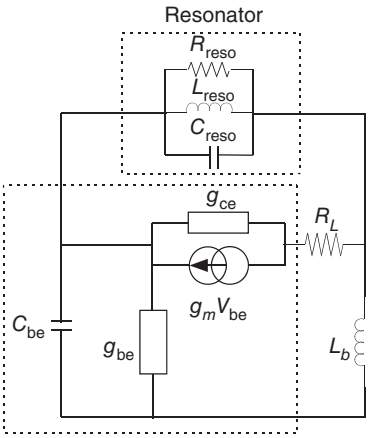


Figure 4-51 Small signal model of the grounded-base oscillator.

$$\mathcal{L}(f_m) = 10\log\left\{\left[1+\frac{{f_0}^2}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^2}{f_m^2}\right\} \tag{4-158}$$

where $m = \frac{Q_L}{Q_0}$.

From [5, Eq. (10-317)], the minimum phase noise can be found by differentiating Eq. (4-158) and equating to zero as $\frac{\partial}{\partial m}[\pounds(f_m)]_{m=m_{opt}} = 0$

$$\frac{d}{dm}\left[10\log\left\{\left[1+\frac{{f_0}^2}{(2f_mQ_0)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_0}+\frac{2kTRK_0^2}{f_m^2}\right\}\right] = 0 \Rightarrow m_{opt} \approx 0.5 \tag{4-159}$$

Figure 4-52 shows the plot of the relative phase noise versus the ratio between loaded and unloaded Q factor of the resonator [5, pp-332].

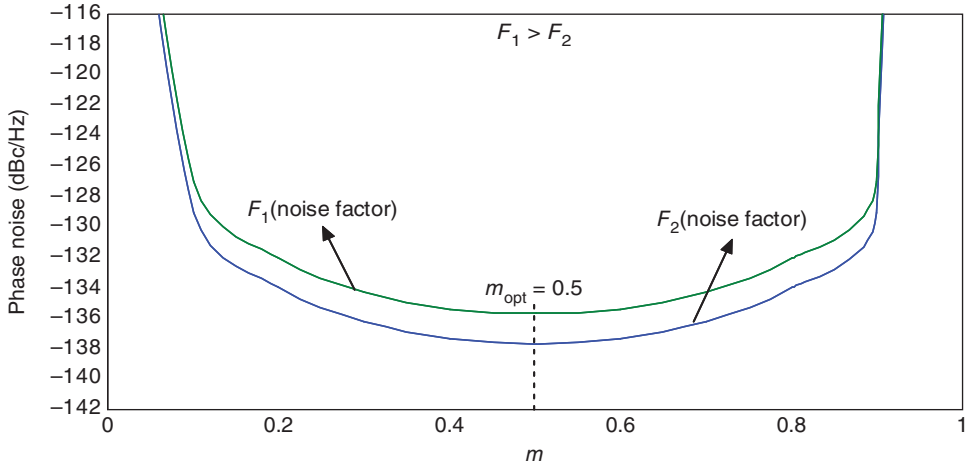


Figure 4-52 Relative phase noise versus the ratio of loaded and unloaded Q of the resonator for noise factor F_1 and F_2, ($F_1 > F_2$) [5].

This implies that for low-noise wideband application, the value of m should be dynamically controlled over the tuning range, and it should lie in the vicinity of m_{opt} for ultra-low phase noise performance over the frequency band [49].

Push–Push Configuration Figure 4-53 shows the two identical oscillator circuits coupled through the arbitrary coupling network under push–push configuration.

The evaluation of pushing factor of the push–push configuration is carried out by considering uncorrelated noise voltage perturbation, Δv_{n1} and Δv_{n2}, associated with the two identical oscillator circuits as shown in Figure 4-53. From [50–52], due to the symmetry of the push–push oscillator topology, two modes (common and differential mode) exist and the corresponding pushing factor is calculated in terms of the common mode (CM) and differential mode (DM) pushing-factor.

The frequency noise spectral density for the push–push topology can be given by

$$\left[\overline{\Delta f_n^2}\right]_{\text{push–push}} = ([\Delta f_n]_{\text{CM}} + [\Delta f_n]_{\text{DM}})^2 \tag{4-160}$$

$$\left[\overline{\Delta f_n^2}\right]_{\text{push–push}} = [K_{\text{PF}}]_{\text{CM}}^2\left[\overline{\Delta v_n^2}\right]_{\text{DM}} + [K_{\text{PF}}]_{\text{DM}}^2\left[\overline{\Delta v_n^2}\right]_{\text{DM}} + 2[K_{\text{PF}}]_{\text{CM}}[K_{\text{PF}}]_{\text{DM}}([\Delta v_n]_{\text{CM}} * [\Delta v_n]_{\text{DM}}) \tag{4-161}$$

where $[K_{\text{PF}}]_{\text{CM}}$ and $[K_{\text{PF}}]_{\text{DM}}$ are common and differential mode pushing factors, and $[\Delta v_n]_{\text{CM}}$ and $[\Delta v_n]_{\text{DM}}$ are the common and differential mode noise perturbations, respectively.

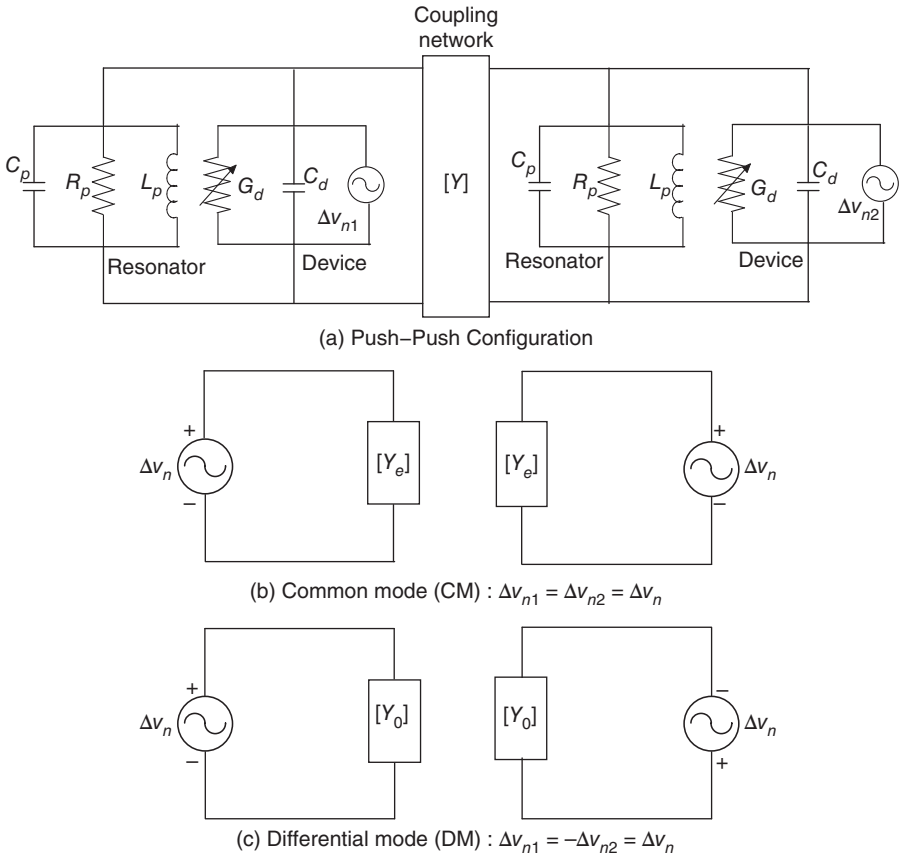


Figure 4-53 Two identical oscillator circuits coupled through the arbitrary coupling network under push–push configuration.

The effect of the differential noise perturbation, due to the symmetry for the push–push topology, gives insignificant variation of the oscillating frequency, so $[K_{PF}]_{DM} \to 0$.

The common mode input noise perturbation of the circuit can be given as

$$\overline{[\Delta v_n^2]}_{CM} = \left[\overline{\frac{\Delta v_{n1} + \Delta v_{n2}}{2}}\right]^2 = \frac{1}{4}\left(\overline{[\Delta v_{n1}^2]} + \overline{[\Delta v_{n2}^2]} + \overline{[\Delta v_{n1} * \Delta v_{n2}]}\right) \tag{4-162}$$

Since the input noise voltage perturbation Δv_{n1} and Δv_{n2} associated with the two identical active devices are uncorrelated to each other, $\overline{[\Delta v_{n1} * \Delta v_{n2}]} = 0$. Considering the active device (transistor) for the two identical oscillator circuits in push–push topology operates under the same working condition, their input noise voltage perturbation can be described by the same statistic and given as $\overline{[\Delta v_{n1}^2]} = \overline{[\Delta v_{n2}^2]}$.

Equation (4-162) can be rewritten as

$$\overline{[\Delta V_n^2]}_{CM} = \left[\overline{\frac{\Delta v_{n1} + \Delta v_{n2}}{2}}\right]^2 = \left[\overline{\frac{[\Delta v_n^2]}{2}}\right] \tag{4-163}$$

From (4-161),

$$\overline{[\Delta f_n^2]}_{push-push} = [K_{PF}]_{CM}^2 \overline{[\Delta v_n^2]}_{CM} = [K_{PF}]_{CM}^2 \left[\overline{\frac{[\Delta v_n^2]}{2}}\right] \tag{4-164}$$

From [5, Eqs. (10-207) and 10-208)], and (4-164),

$$[\mathcal{L}(f_m)]_{push-push\ (f=f_0)} = 20\log\left\{\frac{[\Delta f_n]_{push-push}}{\sqrt{2}f_m}\right\} = -3\text{ dB} + 20\log\left\{\frac{[K_{PF}]_{CM}\Delta v_n}{\sqrt{2}f_m}\right\} \tag{4-165}$$

From (4-165), there is a 3 dB improvement in the phase noise with respect to the individual oscillator oscillating at half the frequency of the push–push frequency, and the analysis agrees with the general equation of the *N*-coupled oscillator [5, Eq. (10-206)].

The improvement of the phase noise of the push–push topology, referring to one individual oscillator that oscillates at fundamental frequency f_0, can be expressed as

$$\frac{[\mathcal{L}\ (f_m)]_{push-push\ (f=f_0)}}{[\mathcal{L}\ (f_m)]_{fundamental\ \left(f=2\frac{f_0}{2}\right)}} = \frac{20\log\left\{\frac{[\Delta f_n]_{push-push\ (f=f_0)}}{\sqrt{2}f_m}\right\}}{20\log\left\{\frac{[\Delta f_n]_{fundamental\ \left(f=2\frac{f_0}{2}\right)}}{\sqrt{2}f_m}\right\}} \tag{4-166}$$

From [5, Eqs. (10-208) and (10-217)],

$$[\mathcal{L}\ (f_m)]_{push-push\ (f=f_0)} = -9\text{ dB} + [\mathcal{L}\ (f_m)]_{fundamental\ \left(f=2\frac{f_0}{2}\right)} \tag{4-167}$$

where $f_0/2$ is the fundamental frequency of the sub-circuit of the oscillator in push–push topology.

From (4-167), push–push topology gives 9 dB improvement in the phase noise compared with the fundamental frequency of the individual oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.

The aforementioned relative noise analysis gives a theoretical basis of the noise prediction as [53]:

- *Fundamental Oscillator*. 12 dB degradation of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency $f_0/2$.
- *Frequency Multiplier/Doubler*. 6 dB degradation of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.
- *Push–Push Topology* ($f = 2f_0/2$). 9 dB improvement of the phase noise with respect to the fundamental oscillator oscillating at f_0, twice the designed oscillating frequency of $f_0/2$.

Validation Figure 4-54 shows the schematic of the push–push oscillator that has two identical oscillators; it consists of two individual oscillators that are oscillating at half the push–push frequency $f_0/2$. The individual oscillator, corresponding to the half-resonator, oscillates at $f_0/2$ (1000 MHz) and is used as a starting point to verify the aforementioned noise analysis with respect to the frequency multiplier and push–push configuration.

Figure 4-55 shows the phase noise plot of the individual oscillator operating at a fundamental frequency of $f_0/2$ (1000 MHz) and f_0 (2000 MHz), working as a frequency doubler (frequency multiplier) at 2000 MHz and a push–push configuration at 2000 MHz.

As discussed above, the phase noise of the fundamental oscillator operating at double the oscillating frequency of 2000 MHz is worsening by 12 dB/octave, with respect to the fundamental oscillator oscillating at a frequency of 1000 MHz.

The simulated graph is based on the unchanged parameters of the active device and the passive components with respect to the two-frequency $f_0/2$ and f_0. It is not an easy task to design the same oscillator operating at $f_0/2$ and f_0 and maintain the same operating parameters of the active device, coupling coefficient, drive level, quality factor, etc.

For the case of the frequency doubler, the phase noise is degraded by 6 dB with respect to the fundamental frequency as shown in Figure 4-55.

The relative improvement of the phase noise of the push–push configuration, with respect to the fundamental frequency of the oscillator composed of push–push topology, is 9 dB. This is shown in Figure 4-55 and agrees with the theoretically predicted result [53].

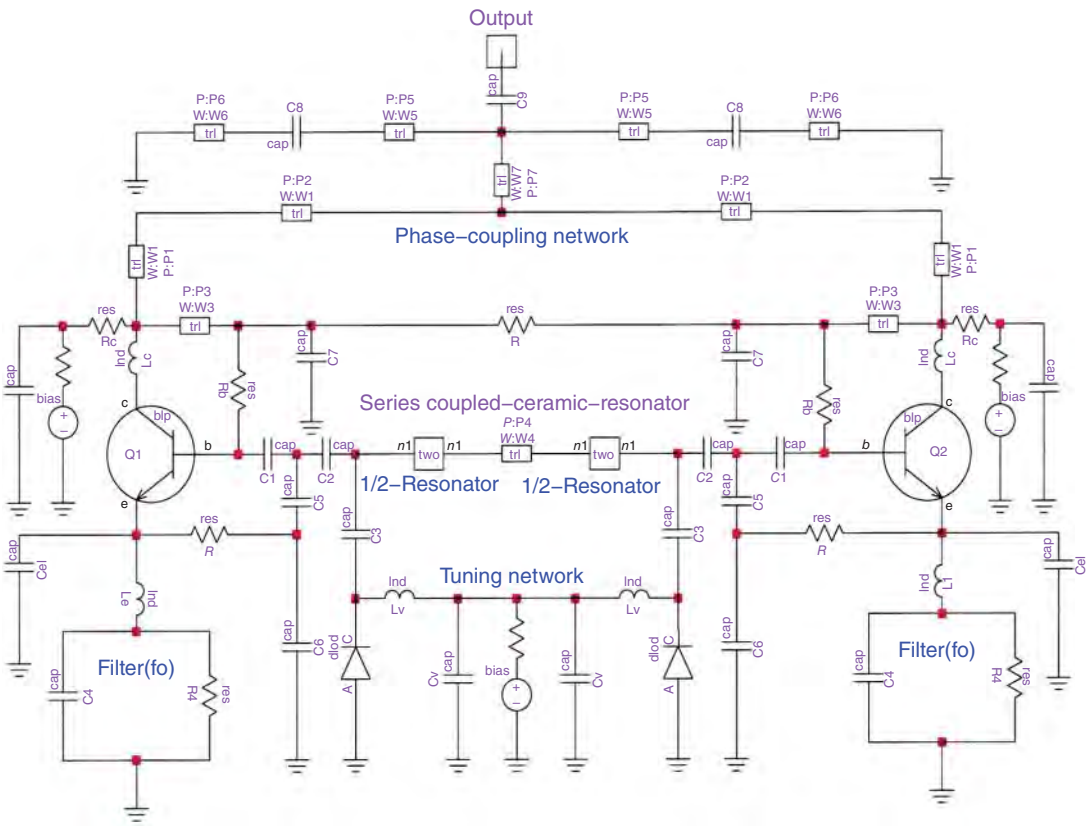


Figure 4-54 Schematic of the push–push oscillator.

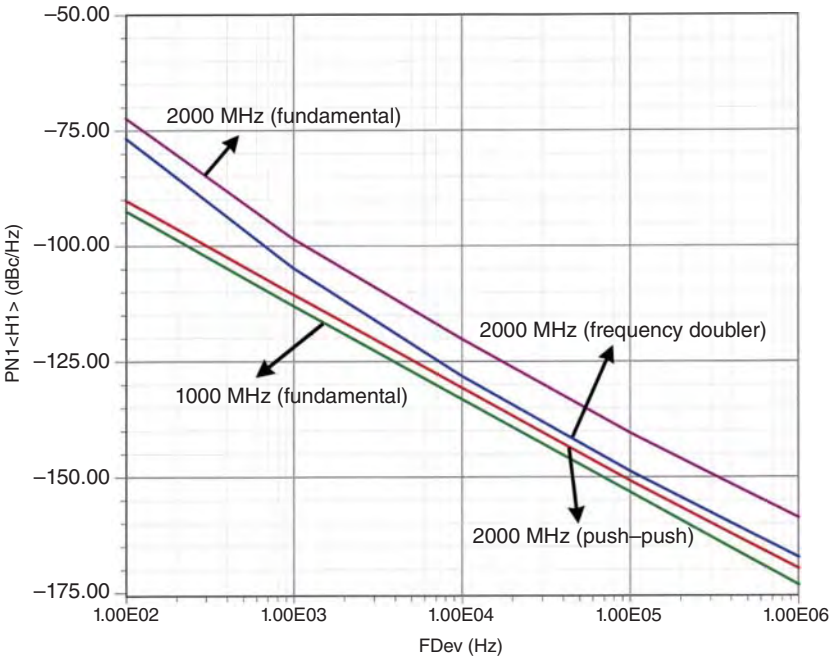


Figure 4-55 Phase noise plot of fundamental oscillator at $f_0/2$, f_0, frequency doubler at f_0, and push–push oscillator at f_0.

Figure 4-56 shows the measured phase noise of a phase-locked loop (PLL) system that uses, Case 1: a reference of 640 MHz surface acoustic wave (SAW) oscillator, shown by the light grey trace and Case 2: 7680 MHz shown by the black trace, using a 1:1 PLL loop against a 7600 MHz signal generator.

If we increase the operating frequencies of these VCOs in a synthesized signal generator, the resulting phase noise is shown in Figure 4-57. Above 6 GHz the output frequency is generated by up-multiplication.

Figure 4-58 shows some typical phase noise values for modern synthesized signal generators over a range of operating frequencies. Note: This applies to LC oscillators and not to yttrium–iron–garnet (YIG) oscillators.

4-2-4 Series Feedback Oscillator[1]

The steady-state oscillation condition for series feedback configuration can be expressed as

$$Z_{\text{out}}(I,\omega) + Z_L(\omega) = 0 \tag{4-168a}$$

$$Z_L(\omega) \to Z_3(\omega) \tag{4-168b}$$

where I is the load current amplitude and w is the resonance frequency. Z_{out} is current and frequency dependent output impedance, whereas Z_L is only a function of frequency.

$$Z_{\text{out}}(I,\omega) = R_{\text{out}}(I,\omega) + jX_{\text{out}}(I,\omega) \tag{4-168c}$$

$$Z_L(\omega) = R_L(\omega) + jX_L(\omega) \tag{4-168d}$$

[1] [5, Appendix A, pp. 384–388]

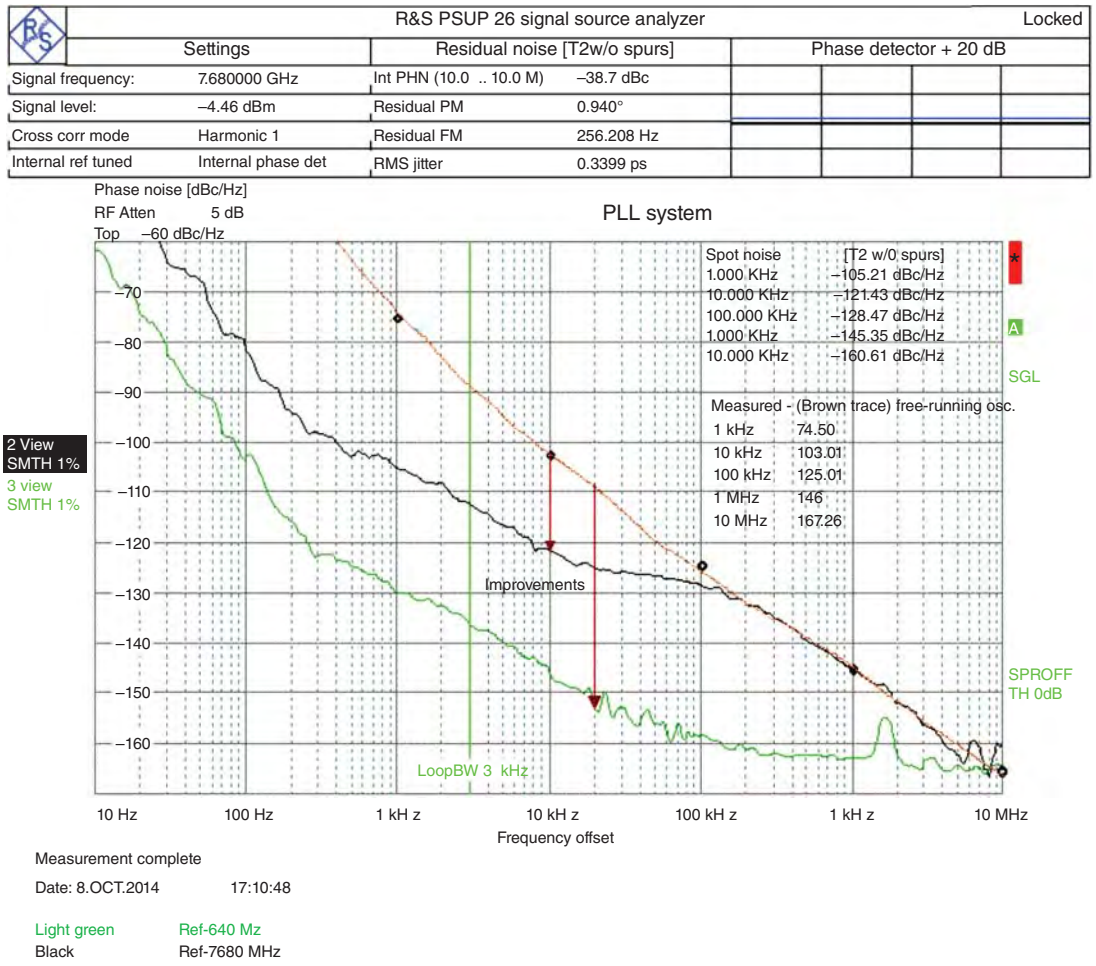


Figure 4-56 Measured phase noise, PLL system.

The expression of output impedance, Z_{out} can be written as

$$Z_{\text{out}} = -Z_3 \Rightarrow [Z_{22} + Z_2] - \frac{[Z_{12} + Z_2][Z_{21} + Z_2]}{[Z_{11} + Z_1 + Z_2]} \tag{4-168e}$$

where $Z_{ij}(i, j = 1, 2)$ is the Z-parameters of the hybrid transistor model and can be written as

$$Z_{i,j} = [R_{ij} + jX_{ij}]_{i,j=1,2} \tag{4-168f}$$

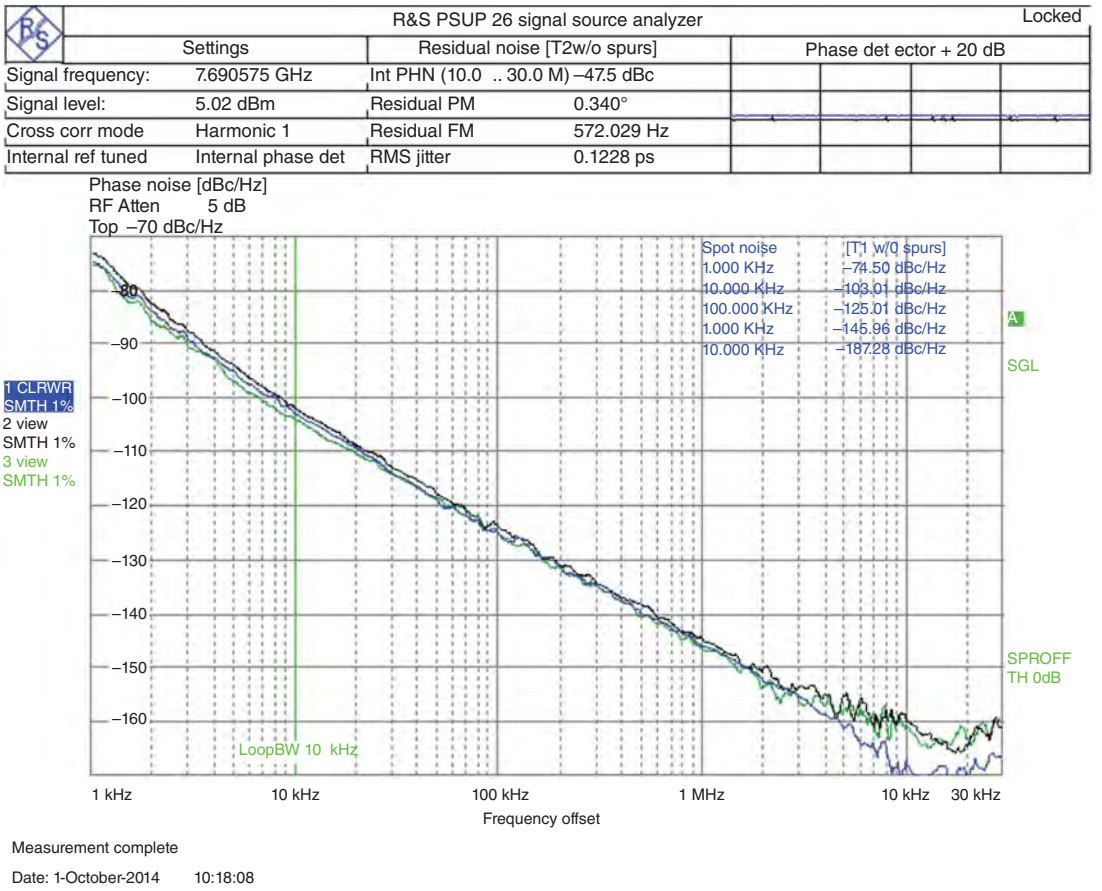


Figure 4-57 Phase noise over 20% tuning range (free-running oscillator).

According to the optimum criterion, the negative real part of the output impedance Z_{out} has to be maximized and the possible optimal values of feedback reactance under which the negative value R_{out} is maximized by setting

$$\frac{\partial \mathrm{Re}[Z_{out}]}{\partial X_1} = 0 \quad \text{and} \quad \frac{\partial \mathrm{Re}[Z_{out}]}{\partial X_2} = 0 \tag{4-168g}$$

$$\Rightarrow \frac{\partial [R_{out}]}{\partial X_1} = 0 \quad \text{and} \quad \frac{\partial [R_{out}]}{\partial X_2} = 0 \tag{4-168h}$$

The optimal values X_1^* and X_2^*, based on the aforementioned condition, can be expressed in terms of a 2-port parameter of the active device (BJT/FET) as

$$X_1^* = -X_{11} + \left[\frac{X_{12} + X_{21}}{2}\right] + \left[\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right]\left[\frac{R_{12} + R_{21}}{2} - R_{11} - R_1\right] \tag{4-168i}$$

$$X_2^* = -\left[\frac{X_{12} + X_{21}}{2}\right] - \left[\frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})}\right] \tag{4-168j}$$

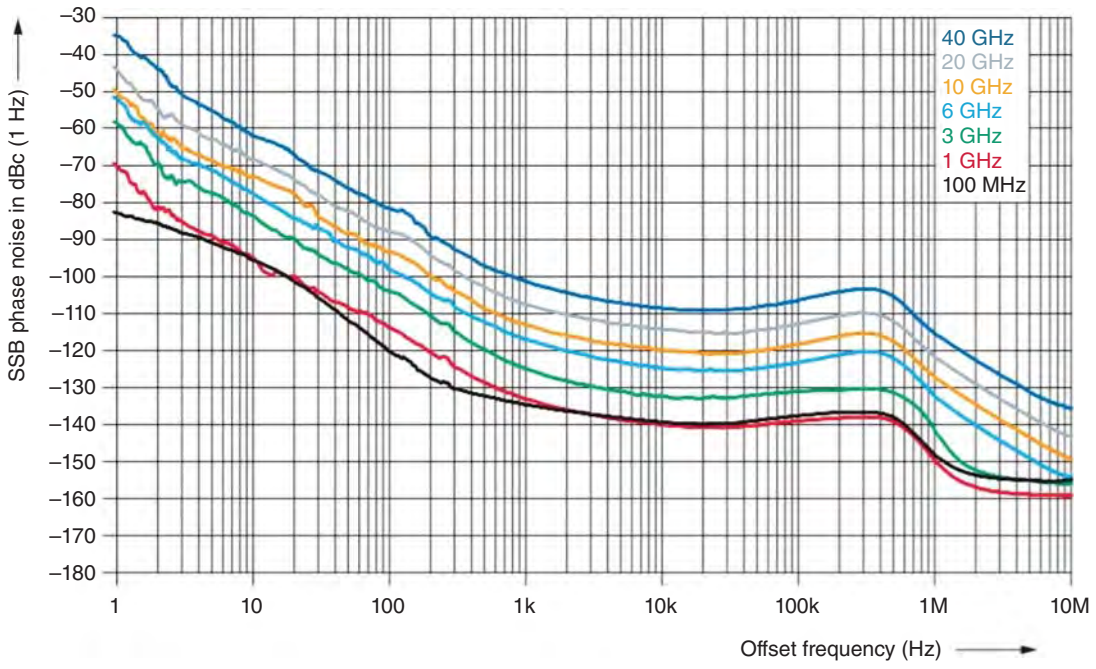


Figure 4-58 Some typical phase noise values for modern synthesized signal generators ranging from 100 MHz to 40 GHz.

By substituting values of X_1^* and X_2^* into aforementioned equation, the optimal real and imaginary parts of the output impedance Z_{out}^* can be expressed as

$$Z_{out}^* = R_{out}^* + X_{out}^* \tag{4-168k}$$

$$(168k) R_{out}^* = R_2 + R_{22} - \left[\frac{(2R_2 + R_{21} + R_{12})^2 + (X_{21} - X_{12})^2}{4(R_{11} + R_2 + R_1)}\right] \tag{4-168l}$$

$$X_{out}^* = X_2^* + X_{22} - \left[\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right][R_{out}^* - R_2 - R_{22}] \tag{4-168m}$$

where

$$X_2^* = -\left[\frac{X_{12} + X_{21}}{2}\right] - \left[\frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})}\right] \tag{4-168n}$$

Thus, in the steady-state operation mode of the oscillator, amplitude and phase balance conditions can be written as

$$R_{out}^* + R_L = 0 \tag{4-168o}$$

$$X_{out}^* + X_L^* = 0 \tag{4-168p}$$

The output power of the oscillator can be expressed in terms of load current and load impedance as

$$P_{out} = \frac{1}{2} I^2 \mathrm{Re}[Z_L] \tag{4-168q}$$

where I and V are the corresponding load current and voltage across the output, respectively.

$$I = \left[\frac{Z_{11} + Z_1 + Z_2}{Z_{22}(Z_{11} + Z_1 + Z_2) - Z_{21}(Z_{12} + Z_2)}\right] V \tag{4-168r}$$

The expression of the phase noise for the series feedback oscillator, following the approach for the Colpitts oscillator, is

$$\left|\overline{\mathrm{L}}\right|_{\mathrm{SSB}} = \left[4KTR + \frac{4qI_c g_m^2(t)}{\omega_0^4 \beta^2 C_{\mathrm{ce}}^2 (C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)^2 + g_m^2 \omega_0^2 (C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)^2}\right] \times \left[\frac{\omega_0^2}{4(\Delta\omega)^2 V_{\mathrm{cc}}^2}\right]\left[\frac{1}{Q_L^2} + \left(1 - \left(\frac{1}{\omega_0^2 L_1}\right)\left(\frac{[(C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2) + C_{\mathrm{ce}}]}{C_{\mathrm{ce}}[(C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)]}\right)\right)^2\right] \tag{4-168s}$$

For large value of Q_1,

$$\left|\overline{\mathrm{L}}\right|_{\mathrm{SSB}} = \left[4KTR + \frac{4qI_c g_m^2(t)}{\omega_0^4 \beta^2 C_{\mathrm{ce}}^2 (C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)^2 + g_m^2 \omega_0^2 (C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)^2}\right] \times \left[\frac{\omega_0^2}{4(\omega)^2 V_{\mathrm{cc}}^2}\right] \frac{1}{\omega_0^4 L_1^2} \left(\frac{[(C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2) + C_{\mathrm{ce}}]}{C_{\mathrm{ce}}[(C_2 + C_{\mathrm{be}} - L_1 C_2 C_{\mathrm{be}} \omega_0^2)]}\right) \tag{4-168t}$$

The important message that can be derived from this calculation is the fact that the parasitics now dominate the design. The negative resistance, which used to be proportional to $1/\omega^2$ now, is $1/\omega^4$. The rule of thumb is to use a large device for lower frequencies and operate it at medium dc currents. This in the millimeter-wave area would be fatal. The large device would have excessive parasitic elements such as inductors and capacitors, and the optimum design is no longer possible since the parasitics would be larger than the values required for optimum performance. These parasitics are the major reason why at millimeter-wave and wide tuning ranges the phase noise is not as good as what a narrowband Colpitts oscillator would provide.

Example Implementation

A 3000 MHz oscillator is designed based on the aforementioned analytical series feedback approach and is also validated with the simulated results. Figure 4-59 shows the series feedback oscillator.

For the oscillation condition, the base-to-ground inductance and the emitter-to-ground capacitance are required. The 12 nH inductor acts a choke. The output is tuned and terminated into 50 Ω.

Large-signal Z-parameters measured data ($I_c = 20$ mA, $V_{\mathrm{ce}} = 2$ V) @ 3000 MHz are given as

$$Z_{11} = R_{11} + jX_{11} = (22.96 + j27.30)\ \Omega \tag{4-169a}$$

$$Z_{21} = R_{21} + jX_{21} = (140 + j670)\ \Omega \tag{4-169b}$$

$$Z_{12} = R_{12} + jX_{12} = (2.72 + j4.99)\ \Omega \tag{4-169c}$$

$$Z_{22} = R_{22} + jX_{22} = (46.04 + j21.45)\ \Omega \tag{4-169d}$$

$$X_1^* = -X_{11} + \left[\frac{X_{12} + X_{21}}{2}\right] + \left[\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right] \left[\frac{R_{12} + R_{21}}{2} - R_{11} - R_1\right] \tag{4-169e}$$

$$X_1^* = 319.9654\ \Omega \Rightarrow L_1 = 16.9\ \mathrm{nH} \tag{4-169f}$$

$$X_2^* = -\left[\frac{X_{12} + X_{21}}{2}\right] - \left[\frac{(R_{21} - R_{12})(2R_2 + R_{12} + R_{21})}{2(X_{21} - X_{12})}\right] \tag{4-169g}$$

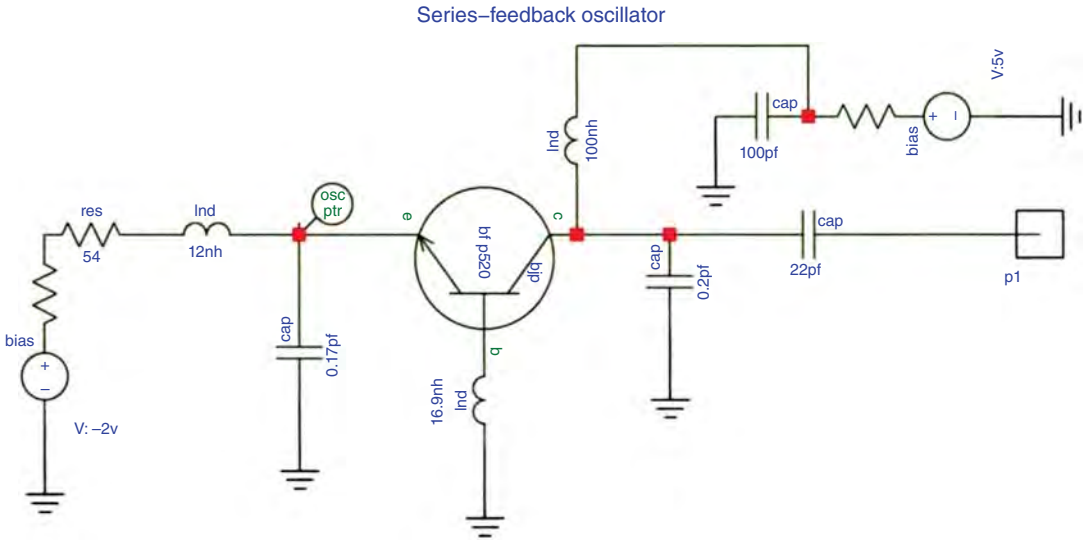


Figure 4-59 Series feedback oscillator.

$$X_2^* = -311.67084 \Rightarrow C_2 = 0.17\ \text{pF} \tag{4-169h}$$

$$X_{\text{out}}^* = X_2^* + X_{22} - \left[\frac{R_{21} - R_{12}}{X_{21} - X_{12}}\right][R_{\text{out}}^* - R_2 - R_{22}] \tag{4-169i}$$

$$X_{\text{out}}^* = -259.31176 \Rightarrow C_3 = 0.2\ \text{pF} \tag{4-169j}$$

The simulated response of the oscillator circuit, having resonance at 2980 MHz or 1% error, is a good starting value for tuning and optimization for optimum phase noise and output power. The best phase noise at a given power output is basically dependent upon the ratio and absolute value of the feedback capacitor, which in turn depends upon the optimum drive-level. The detailed analysis for designing the best phase noise, based on a unified approach, is discussed in the next section. Figure 4-60 shows the real and imaginary currents for oscillating conditions for optimum output power. In this case, the operating Q is very low, as can be seen from the shallow curve at which the imaginary current crosses the zero line, while the real current is still negative. To optimize this circuit for phase noise, the imaginary curve should go through the zero line at the point of steepest ascent, while maintaining a negative real current. The low Q resonator guarantees that the most output power is available, and the resonator is heavily loaded.

Calculated phase noise using the Modified Leeson equation [54, pg. 302, eq (7.25)],

$$L_i := 10 \log\left[\left(1 + \frac{(fo)^2}{(2\,fm_1\,Q_L)^2\left(1 - \frac{Q_L}{Q_O}\right)^2}\right) \cdot \left(1 + \frac{fc}{0.25(fm_1)^{1.5}}\right) \cdot \frac{FkT}{2Psav} + \frac{2\,kTRKo^2}{(fm_i)^2}\right] \tag{4-170}$$

A practical oscillator design is documented in Figures 4-61a–4-61d.

4-2-5 2400 MHz MOSFET-Based Push–Pull Oscillator

Wireless applications are extremely cost sensitive, and when implemented as an RFIC, they are designed using silicon technology. Most mixers in RFICs are built on the principle of differential amplifiers (Gilbert cell) and require a phase and out-of-phase signal (symmetrical drive). For these symmetrical requirements, this is best achieved

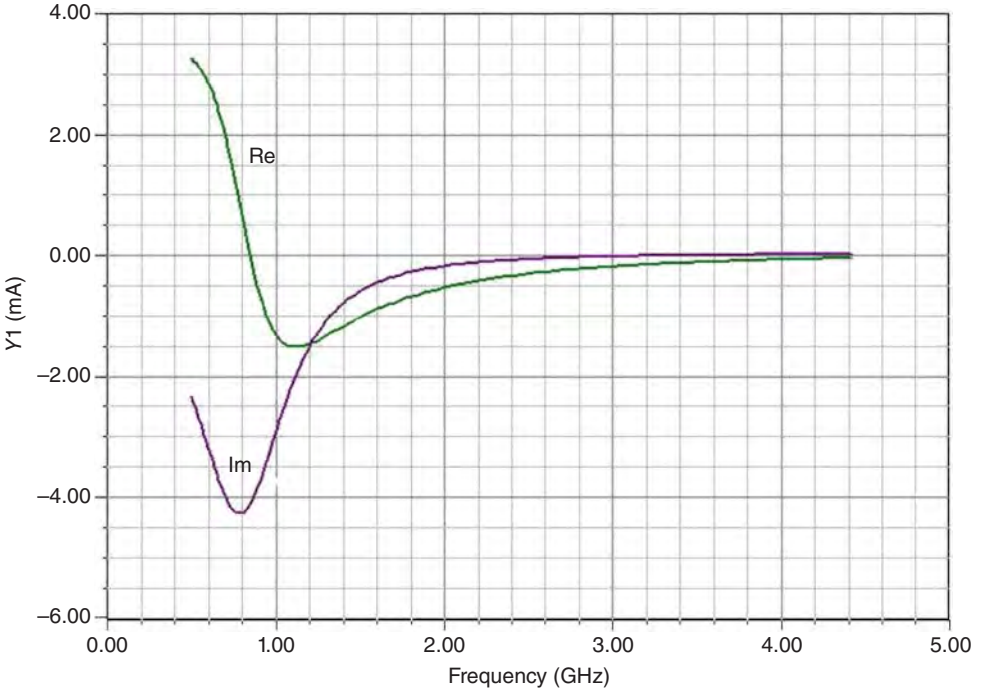


Figure 4-60 The real and imaginary currents of the 3 GHz series-type oscillator. The very shallow curve should be noted.

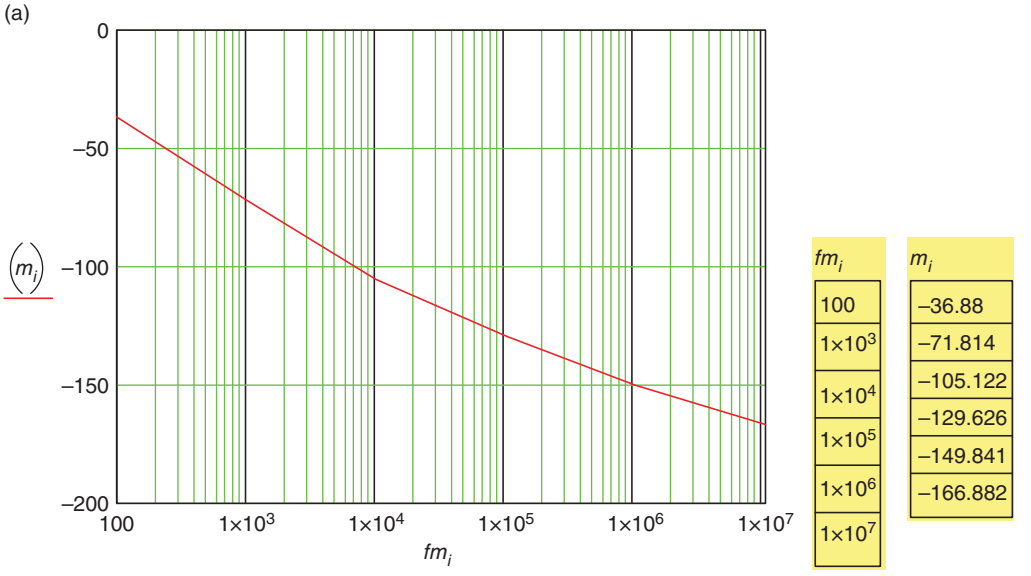


Figure 4-61a Practical example—design of a 10 GHz YIG oscillator using Eq. (4-170).

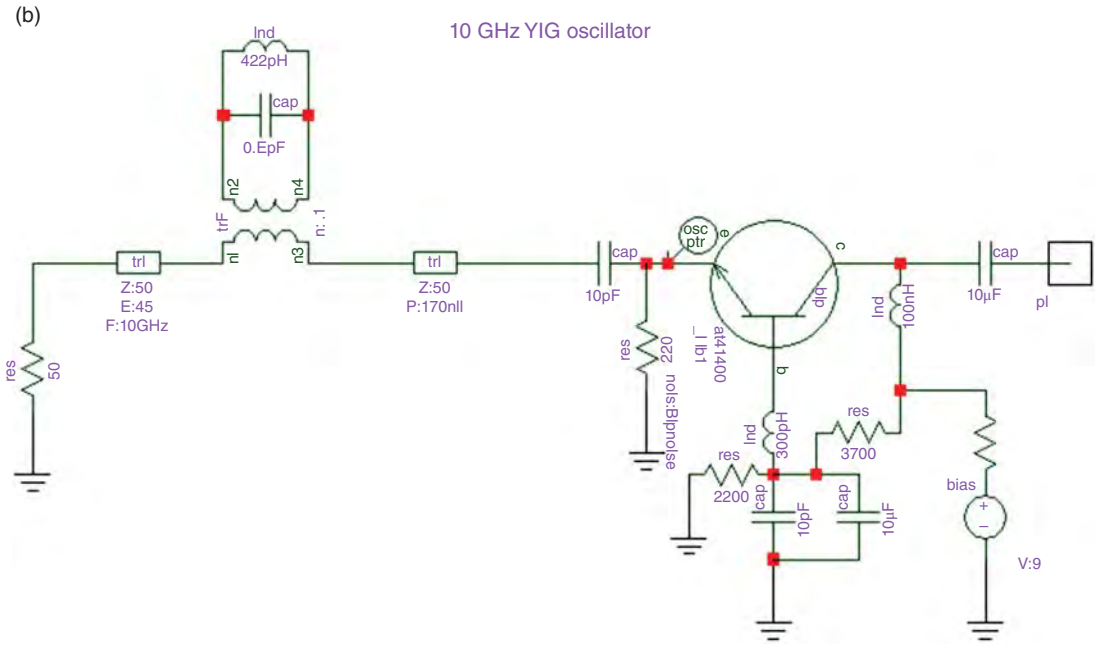


Figure 4-61b Schematic of the proposed 10 GHz YIG oscillator.

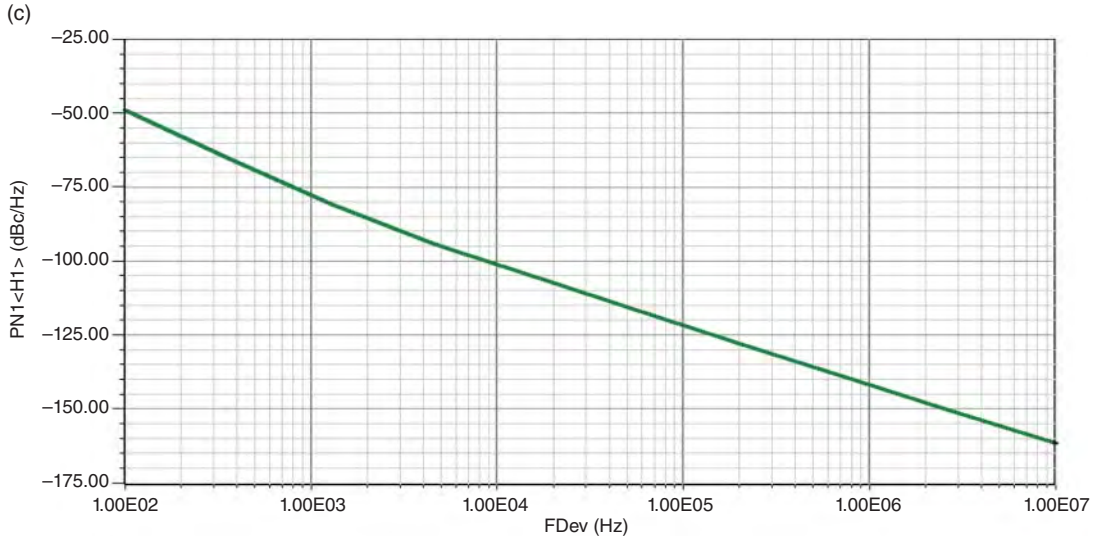


Figure 4-61c Simulated phase noise of the YIG oscillator in Figure 4-61a.

(d)

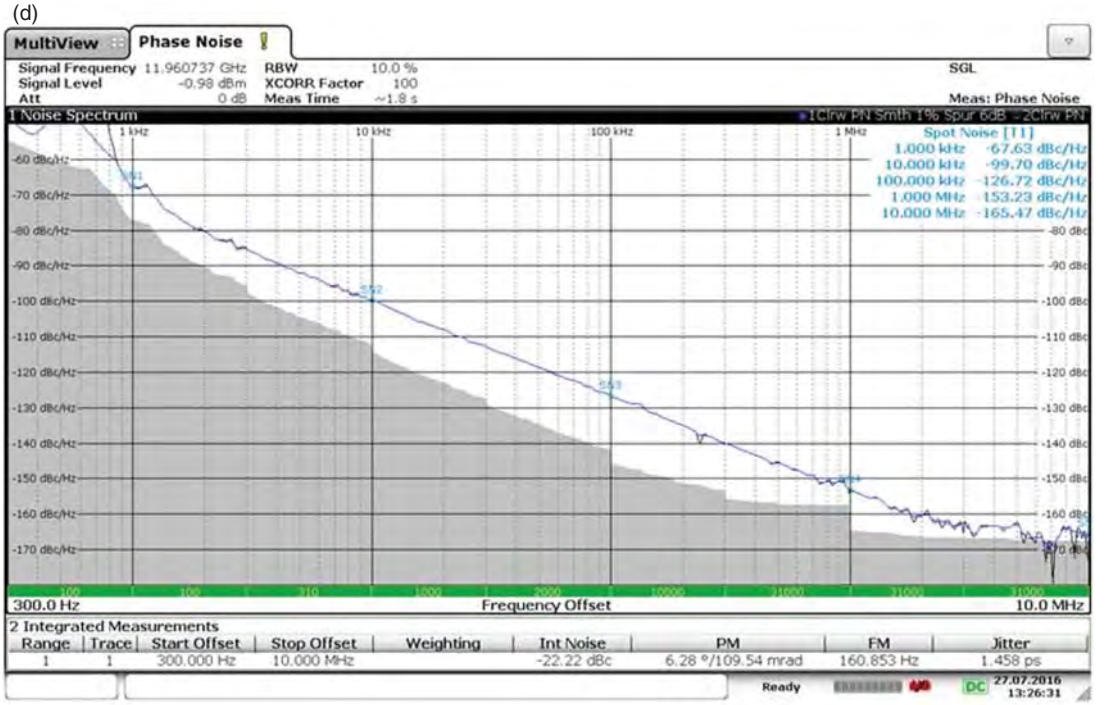


Figure 4-61d Measured phase noise of 12 GHz YIG oscillator using the design method shown earlier.

using a push–pull technology with two outputs. The design choices are SiGe transistors or BiCMOS transistors. The submicron devices in 0.35 micron technology and smaller are ideally suited for this frequency application. The 0.25 and smaller technology is more costly but does not provide a significant advantage. As will be seen, the critical phase noise is determined by the Q of the inductor and other elements of the resonator and by the flicker noise from the device.

Figure 4-62 shows the circuit of the 2400 MHz integrated CMOS oscillator 0.35 µm in cross-coupled (push–pull) configuration [55–73].

The circuit earlier uses a cross-coupled CMOS-NMOS pair as an oscillator. The advantage compared with an all NMOS structure is that it generates a large symmetrical signal swing and balances out the pull-up and pull-down signals, resulting in a better noise. This type of topology rejects the common mode noise and substrate noise.

Figure 4-63 shows the starting condition, which requires a negative resistance and a cancellation of the reactances at the frequency of oscillation. The currents shown in Figure 4-63 indicate that this condition is met.

It is important to notice that the condition of zero reactance does not quite occur at the point of most negative current. Since the circuit is totally symmetrical, only the condition $C_1 = C_2$ can be met. C_1 and C_2 refer to the gate source capacitance of the field-effect transistors. As outlined previously, this is not necessarily the best condition for phase noise.

Figures 4-64 and 4-65 show the predicted phase and RF output power, including harmonic contents.

Design Equations

Figure 4-66 shows a cross-coupled PMOS and a cross-coupled NMOS pair using CMOS devices. According to the literature, PMOS transistors offer lower $1/f$ and thermal noise while NMOS transistors exhibit a higher f_T and a higher transconductance for the same operating point.

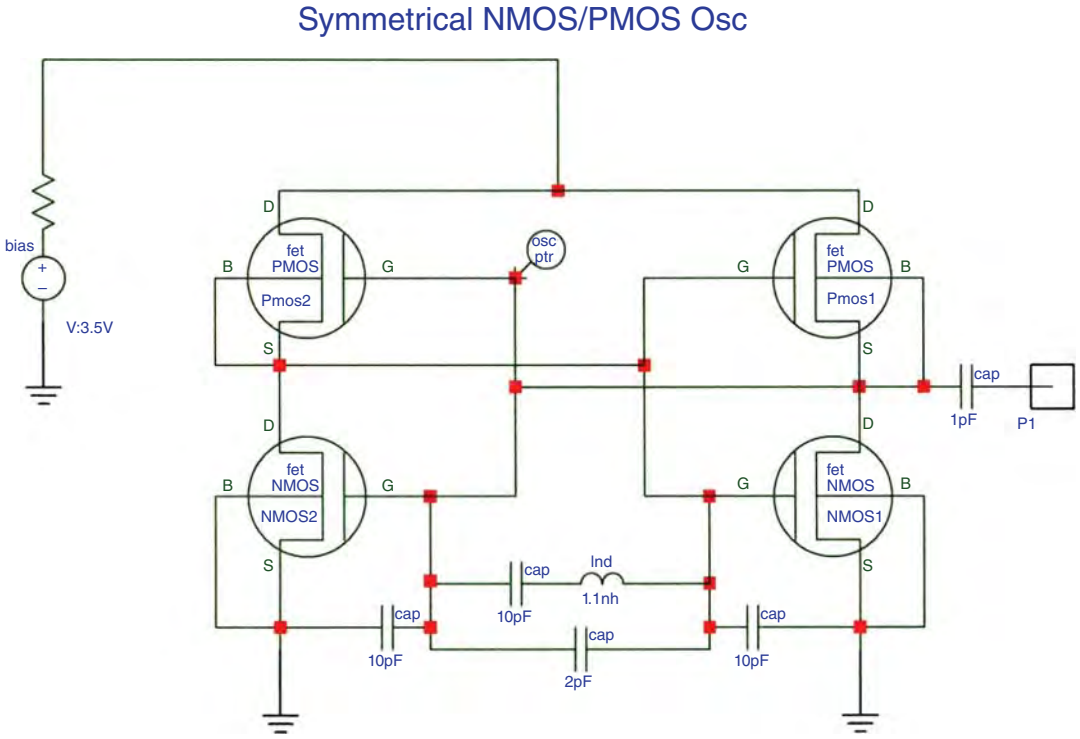


Figure 4-62 Circuit of the 2400 MHz integrated CMOS oscillator.

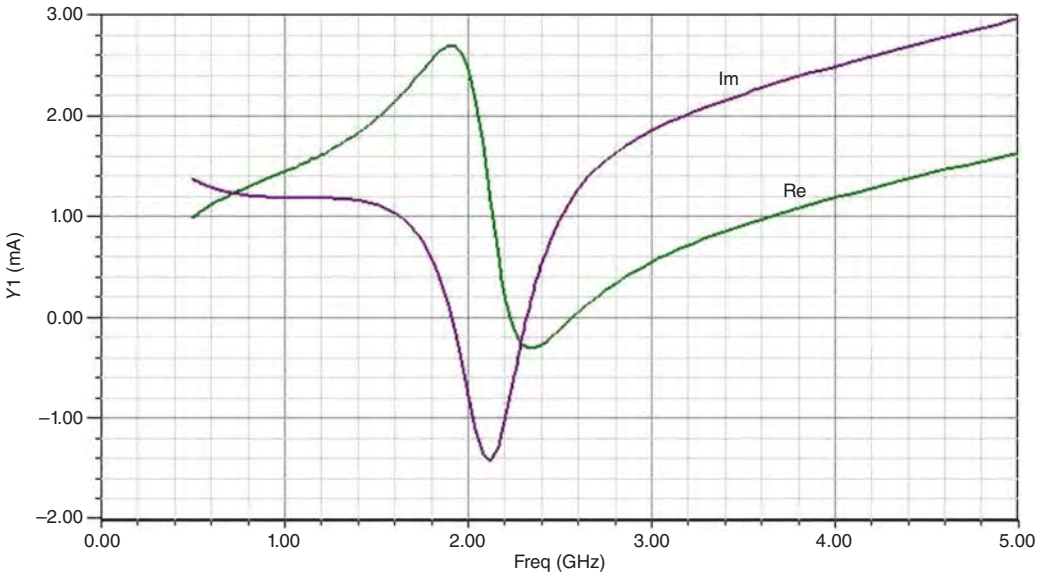


Figure 4-63 The real and imaginary currents that cause the negative resistance for oscillation.

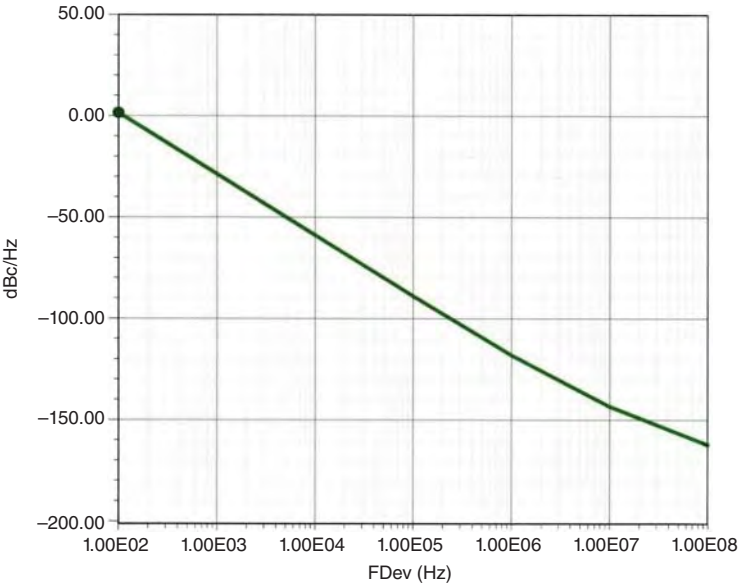


Figure 4-64 Predicted phase noise of the 2400 MHz MOSFET oscillator.

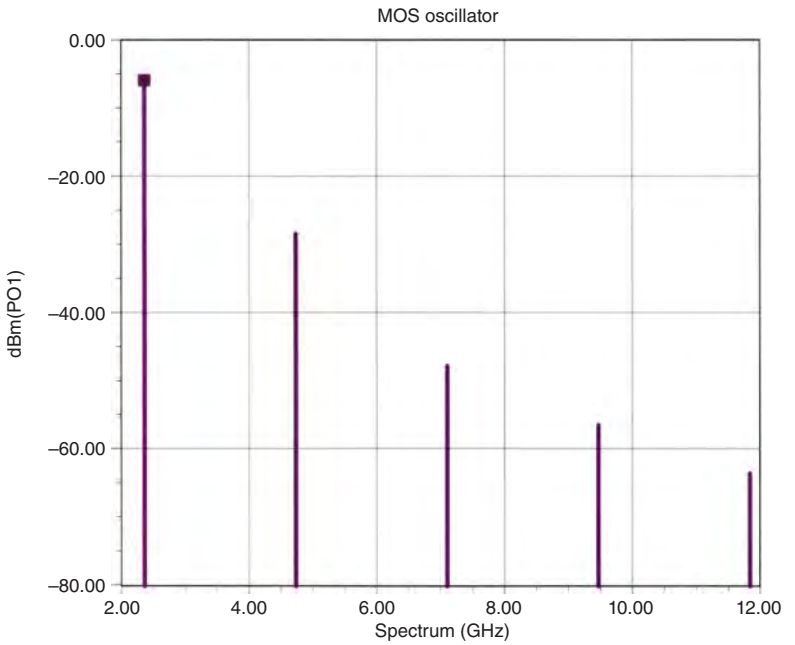


Figure 4-65 Predicted output spectrum of the 2400 MOSFET oscillator.

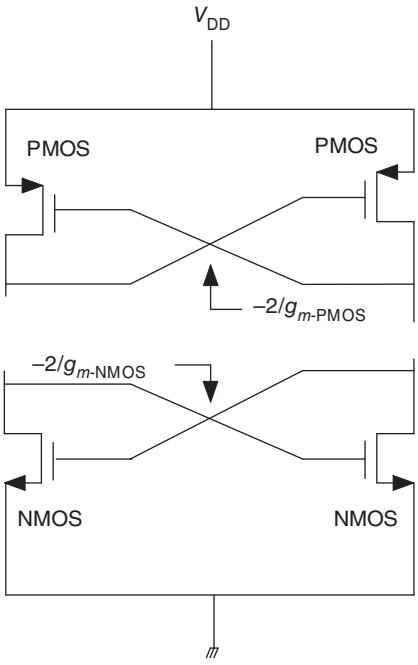


Figure 4-66 Determining the transconductance of the differential circuit of the cross-coupled PMOS and NMOS pair.

The total transconductance is

$$[g_m]_{\text{large-signal}} = -\frac{[g_m]_{\text{PMOS}} + [g_m]_{\text{NMOS}}}{2} \tag{4-171a}$$

$$[g_m]_{\text{large-signal}} = \frac{\partial I_{\text{ds}}}{\partial V_{\text{gs}}} \tag{4-171b}$$

$$[g_m]_{\text{NMOS}} = \sqrt{2I_{\text{ds}}\mu_{\text{nmos}}C_{\text{ox-nmos}}\left[\frac{w}{L}\right]_{\text{nmos}}} \tag{4-172}$$

$$[g_m]_{\text{PMOS}} = \sqrt{2I_{\text{ds}}\mu_{\text{pmos}}C_{\text{ox-nmos}}\left[\frac{w}{L}\right]_{\text{pmos}}} \tag{4-173}$$

$$\frac{\partial I_{\text{ds}}}{\partial V_{\text{gs}}} = K_p\frac{w}{L}(V_{\text{gs}} - V_{\text{th}}) \tag{4-174}$$

$$[g_m]_{\text{large-signal}} = \sqrt{\frac{2wK_pI_{\text{ds}}}{L}} \tag{4-175}$$

where

K_p = transconductance parameter
μ_{pmos} = carrier mobility of the PMOS device
μ_{nmos} = carrier mobility of the NMOS device
C_{ox} = unit capacitance of the gate oxide

The transconductance parameter is defined as

$$K_p = \mu\, C_{\text{ox}} \tag{4-176}$$

where μ is the carrier mobility and C_{ox} is the unit capacitance of the gate oxide.

The unit capacitance of the gate oxide is given as

$$C_{\text{ox}} = \varepsilon_{\text{ox}} \left[\frac{w_i l_i}{t_{\text{ox}}}\right] \tag{4-177}$$

where

ε_{ox} = permittivity of the oxide
t_{ox} = thickness of the oxide layer between spiral and substrate
w_i = width of the spiral line
l_i = length of the spiral line.

The drain current is

$$I_{\text{ds}} = \frac{1}{2}\left[K_p \frac{w}{L}(V_{\text{gs}} - V_{\text{th}})^2\right] \tag{4-178}$$

$$I_{\text{ds}} = \frac{g_m}{2}(V_{\text{gs}} - V_{\text{th}}) \tag{4-179}$$

where $(V_{\text{gs}} - V_{\text{th}})$ is defined as

$$(V_{\text{gs}} - V_{\text{th}}) = \sqrt{\frac{2I_{\text{ds}}L}{K_p w}} \tag{4-180}$$

The size of the device determines the transconductance of the transistor, and the large-signal transconductance needs to be large enough to sustain oscillation and compensate the losses of the resonator.

The expression of the ratio of the channel width (gate) and channel length (gate) is

$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_p I_{\text{ds}}} \rightarrow \frac{(g_m)^2}{2K_p I_{\text{ds}}} \tag{4-181}$$

where w is the width of the channel (gate) and L is the length of the channel (gate) of the device.

Figure 4-67a,b shows the equivalent cross-coupled oscillator resonant circuit and the corresponding equivalent resistances at resonance condition.

The total equivalent parallel resistor at resonance frequency is

$$R_T = \frac{2R_P}{2 - R_P(g_{m\text{-NMOS}} + g_{m\text{-PMOS}})} \tag{4-182}$$

$$Q_L = \frac{R_P}{\omega L} \tag{4-183}$$

where $g_{m\text{-NMOS}}$ and $g_{m\text{-PMOS}}$ are the corresponding large-signal transconductances of the NMOS and PMOS device, respectively.

For a symmetrical output signal, the large-signal transconductance of the NMOS and PMOS transistors have to be ideally equal as $g_{m\text{-NMOS}} = g_{m\text{-PMOS}} = g_m$ and the equivalent resistance at resonance condition is

$$R_T = \frac{1}{\left[\frac{1}{R_P} - g_m\right]} \tag{4-184}$$

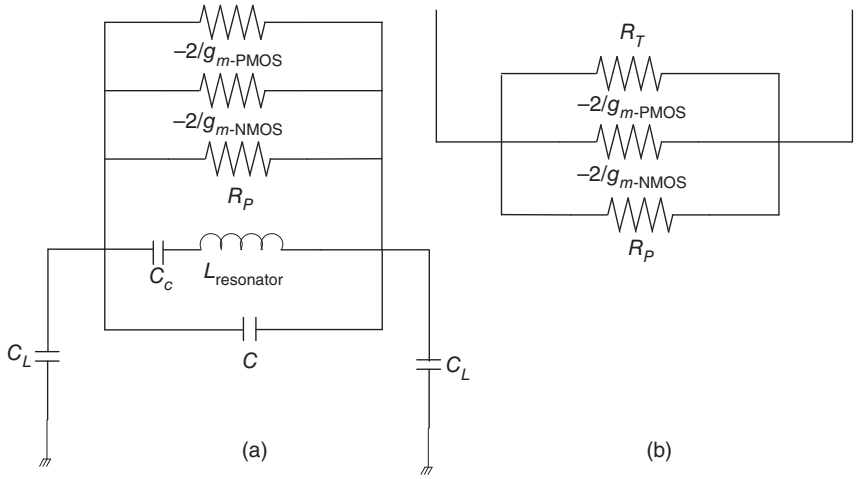


Figure 4-67 (A) The equivalent cross-coupled oscillator resonator circuit. (B) The equivalent resistances at resonance condition.

The differential negative resistance generated by the cross-coupled NMOS and PMOS transistors-pair compensates the parallel loss resistance R_P of the resonator circuit.

For the start-up condition and guaranteed sustained oscillation condition, the value of R_T must be negative and

$$R_T = \frac{1}{\left[\frac{1}{R_P} - g_m\right]} < 0 \Rightarrow g_m > \frac{1}{R_P} \tag{4-185}$$

From the loop gain criteria using a stability factor of 2 (loop gain = 2), the gain is adjusted to 1 by self-adjusting the conducting angle of the circuit), the start-up condition is

$$\frac{g_m}{SG_p} \rightarrow 2 \tag{4-186}$$

where

$$G_P = \frac{1}{R_P} \tag{4-187}$$

S = stability factor
R_P = equivalent parallel loss resistance of the resonator

Design Calculations

The equivalent parallel loss resistance of the resonator is given as

$$R_P = (1 + Q^2)R_S \Rightarrow 101R_S \quad \text{for } (Q = 10) \tag{4-188}$$

where R_S is series loss-resistance.

$$[R_P]_{f=2400\text{ MHz}} = Q\omega L_{\text{ind}} = 190\,\Omega \tag{4-189}$$

where:

$$Q = 10$$
$$L_{\text{ind}} = 1.1\ \text{nH}$$
$$G_P = \frac{1}{R_P} \Rightarrow 6.577\ \text{mS}$$

The large-signal transconductance is given by

$$[g_m]_{\text{large-signal}} = \sqrt{\frac{2wK_pI_{\text{ds}}}{L}} = \sqrt{\frac{2^*(250\text{E-}6)^*(35.6\text{E-}6)^*(14.8\text{E-}3)}{0.35\text{E-}6}} = 27.435\ \text{mS} \tag{4-190}$$

The width of the CMOS is given as

$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_pI_{\text{ds}}} \rightarrow \frac{(g_m)^2}{2K_pI_{\text{ds}}} \tag{4-191}$$
$$\frac{w}{L} = \frac{(2SG_P)^2}{2K_pI_{\text{ds}}} = 714.3\ \mu\text{m} \tag{4-192}$$

for $L = 0.35\ \mu\text{m}$, $w = 250\ \mu\text{m}$.
where

K_p = 35.6E−6
I_{ds} = 14.8 mA
G_p = 6.577 mS
S = 2

The frequency of the oscillation is given as

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{resonator-tank}}C_{\text{resonator-tank}}}} \tag{4-193}$$
$$C_{\text{resonator-tank}} = \frac{1}{2}[C_{\text{NMOS}} + C_{\text{PMOS}} + C_L + C] \tag{4-194}$$

where

$$C_{\text{NMOS}} = 4C_{\text{gd-nmos}} + C_{\text{gs-nmos}} + C_{\text{db-nmos}} \tag{4-195}$$

$$C_{\text{PMOS}} = 4C_{\text{gd-pmos}} + C_{\text{gs-pmos}} + C_{\text{db-pmos}} \tag{4-196}$$

For the cross-coupled configuration $C_{\text{NMOS-Pair}}$ is the series combination of the two C_{NMOS} and is given as

$$C_{\text{NMOS-Pair}} = 2C_{\text{gd-nmos}} + \frac{1}{2}C_{\text{gs-nmos}} + \frac{1}{2}C_{\text{db-nmos}} \tag{4-197}$$

Similarly, $C_{\text{PMOS-Pair}}$ is the series combination of the two C_{PMOS} and is given as

$$C_{\text{PMOS-Pair}} = 2C_{\text{gd-pmos}} + \frac{1}{2}C_{\text{gs-pmos}} + \frac{1}{2}C_{\text{db-pmos}} \tag{4-198}$$

The capacitance of the resonator is given as

$$C_{\text{resonator-tank}} = \frac{1}{2}[C_{\text{NMOS}} + C_{\text{PMOS}} + C_L + C] \tag{4-199}$$

where

C_L = 10 pF (load capacitance)
C = ½ resonator-parallel capacitance

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{resonator-tank}}C_{\text{resonator-tank}}}} = \frac{1}{2\pi\sqrt{1.1E-9{*}3.3E-12}} = 2400\,\text{MHz} \tag{4-200}$$

where $L_{\text{resonator-tank}} = 1.1$ nH and $C_{\text{resonator-tank}} = 3.3$ pF.

Phase Noise

The phase noise of CMOS oscillators has been subject to endless discussions. The main contributors still are the resonant circuit with a low Q and the flicker frequency contribution from the device. We take the following equations and adapt them to the CMOS device.

$\text{PN}_{\text{inr}}(\omega_0+\omega) = \frac{4KT}{R_P}[\text{NFT}_{\text{inr}}(\omega_0)]^2 = \frac{4KT}{R_P}\left\{\frac{1}{2}\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the resonator.

$\text{PN}_{\text{Vbn}}(\omega_0+\omega) = 4KTr_b[\text{NFT}_{\text{Vbn}}(\omega_0)]^2 = 4KTr_b\left\{\frac{1}{2}\left[\frac{C_1+C_2}{C_2}\right]\left[\frac{1}{2jQ_0}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the gate resistance.

$\text{PN}_{\text{ibn}}(\omega_0+\omega) = 2qI_b[\text{NFT}_{\text{ibn}}(\omega_0)]^2 = 2qI_b\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the gate current.

$\text{PN}_{\text{ibn}}(\omega_0+\omega) = \frac{K_f I_b^{\text{AF}}}{f_m}[\text{NF}_{\text{ibn}}(\omega_0)]^2 = \frac{K_f I_b^{\text{AF}}}{\Delta\omega}\left\{\frac{1}{2}\left[\frac{C_2}{C_1+C_2}\right]\left[\frac{1}{j2\omega_0 Q_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the flicker noise of the transistor.

$\text{PN}_{\text{icn}}(\omega_0+\omega) = 2qI_c[\text{NFT}_{\text{icn}}(\omega_0)]^2 = 2qI_c\left\{\frac{1}{2}\left[\frac{C_1}{C_1+C_2}\right]\left[\frac{1}{2\omega_0 C_{\text{eff}}}\right]\left[\frac{\omega_0}{\Delta\omega}\right]\right\}^2$ → phase noise contribution from the drain current.

The following values were used:

$R_p = 190\,\Omega$
$f_0 = 2.4$ GHz
$L = 1.1$ nH
$C_{\text{O}} = 2$ pF
$C_1 = C_2 = 0.2$ pF
$n = 2$
$I_g = 100\,\mu$A
$I_d = 14$ mA
AF = 2
KF = 5E−5
q = 1.6E−19
$T = 290°$ K

and the following contributions were obtained at 1 MHz offset:

PN1 = −117.78 dBc/Hz
PN2 = −146.37 dBc/Hz
PN3 = −123.4 dBc/Hz
PN4 = −140.9 dBc/Hz

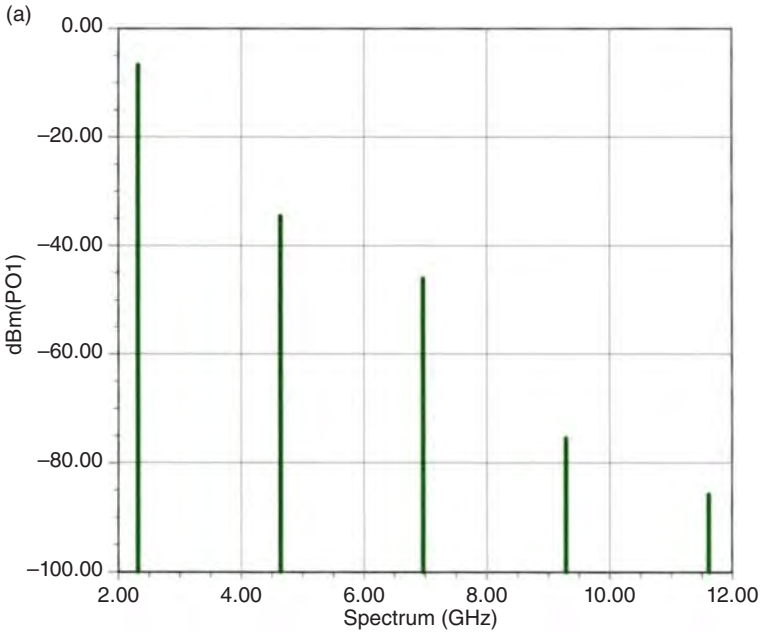


Figure 4-68a The predicted output spectrum of the CMOS oscillator.

These calculations show that the phase noise contribution from the tuned circuit dominates and sets the value at −117.78 dBc/Hz.

The circuit was analyzed using Microwave Harmonica/Ansoft Designer, using a lossy circuit with a Q_0 of 10 and using the SPICE-type parameters which were obtained from the manufacturer.

The output power measured single-ended was −7 dBm. Figure 4-68a shows the simulated output power and harmonic contents. The accuracy of the prediction is within 1 dB.

Figure 4-68b shows the predicted phase noise from Designer and the phase noise prediction from the set of equations shown earlier. It should be pointed out that close-in the flicker noise contribution dominates, in the medium range, the resonator Q dominates, and for high currents, the drain current adds significant noise.

Figure 4-68d shows photograph of a Motorola CMOS based oscillator, which was used in some part of the radios.

This approach has shown a very good agreement between the simulations and calculations as demonstrated. The publications that cover this topic have analyzed various other contributions, both from the transistor and the tuning mechanism. When FETs are used as varactors, the average Q is in the vicinity of 30, which means that the low-Q inductor still is responsible for the overall phase noise. The three areas of improvement are the power supply voltage, the Q, and the device selection. So far, the power supply voltage has not been addressed. However, latest designs operating at 1.5 V show a poorer noise performance. Their distinct trade-offs and the application dictate if such degradation is allowable.

1/f Noise

The electrical properties of surfaces or boundary layers are influenced energetically by states, which are subject to statistical fluctuations and, therefore, lead to the flicker noise or 1/*f* noise for the current flow. 1/*f* noise is observable at low frequencies and generally decreases with increasing frequency *f* according to the 1/*f* law until it is covered by frequency independent mechanisms, like thermal noise or shot noise. An example case follows.

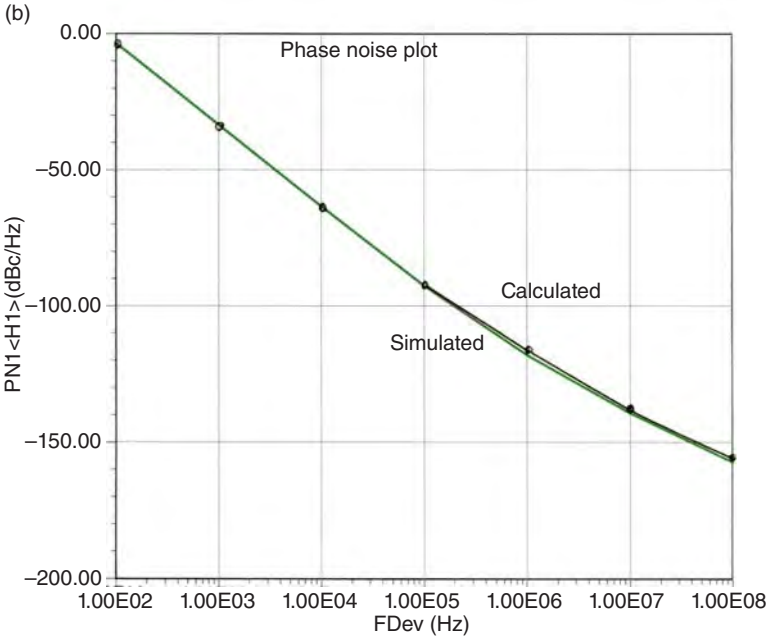


Figure 4-68b The predicted phase noise from Ansoft Designer.

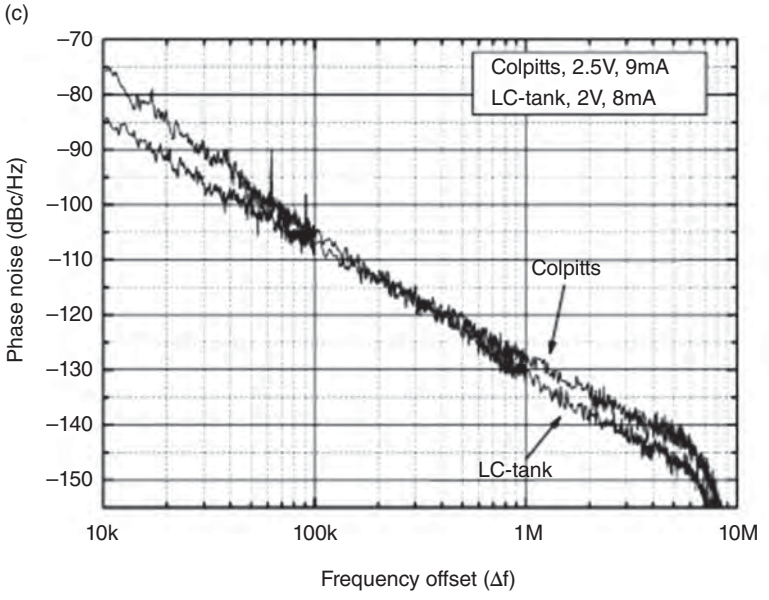


Figure 4-68c Measured phase noise of a CMOS LC and Colpitts oscillator at 2.9 Ghz [74].

(d)

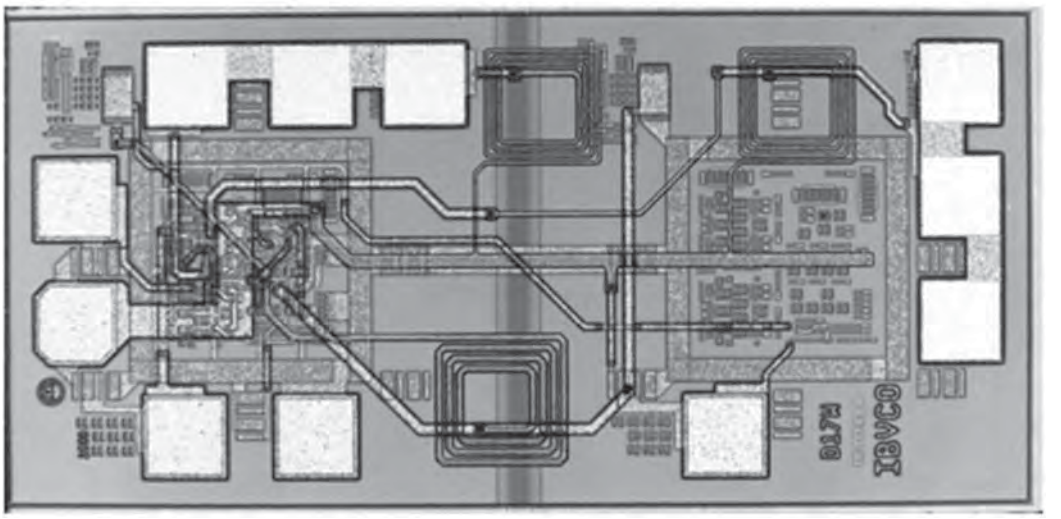


Figure 4-68d Photograph of a Motorola CMOS based oscillator. Courtesy Motorola, David Lovelace.

The noise for a conducting diode is bias-dependent and is expressed in terms of AF and KF.

$$\langle i_{\mathrm{Dn}}^2 \rangle_{\mathrm{AC}} = 2qI_{\mathrm{dc}}B + \mathrm{KF}\frac{I_{\mathrm{dc}}^{\mathrm{AF}}}{f}B$$

The AF is generally in range of 1–3 (a dimensionless quantity) and is a bias-dependent curve fitting term, typically 2.

The KF value ranges from 10^{-12} to 10^{-6} and defines the flicker corner frequency [75].

One of the important characteristics for device evaluation and selection is $1/f$ noise, which is a function of the active device characteristics and a major contributor to phase noise, especially in applications such as VCOs [5, 20]. In an oscillator, $1/f$ noise that is present in transistors at low frequencies is up-converted and added to the phase noise around the carrier signal. Hence, proper characterization of $1/f$ noise and its effects on phase noise are important topics. In addition, $1/f$ noise is not solely an active device phenomenon. Passive devices such as carbon resistors, quartz resonators, SAW devices, and ceramic capacitors are among devices that show presence of this phenomenon when used as part of low-noise electronic systems. Generally, $1/f$ noise is present in most physical systems and many electronic components [19, 22, 23].

Flicker noise in BJTs is also known as $1/f$ noise because of the $1/f$ slope characteristics of the noise spectra. This noise is caused mainly by traps associated with contamination and crystal defects in the emitter–base depletion layer. These traps capture and release carriers in a random fashion. The time constants associated with the process produce a noise signal at low frequencies. The flicker noise spectral density is given by

$$S(f)df = (KF)IB^{AF}df/Fc \tag{4-201}$$

where:

KF = flicker noise constant
AF = flicker noise exponent
IB = dc base current
Fc = flicker noise corner frequency

The measured flicker corner frequency, F_{meas}, is determined by noting the intersection of the 1/*f* noise spectrum and the white noise spectrum. This intersection is where the measured flicker noise power and the white noise power are equal. To determine F_{bn}, the intrinsic base flicker noise corner requires solving the following equation [20, 21].

$$F_{bn} = F_{meas}[1 + 1/\beta + 2V_{th}G_{in}/IB] \tag{4-202}$$

where

F_{bn} = intrinsic base flicker noise corner
F_{meas} = measured flicker corner
β = collector–base current gain
V_{th} = thermal voltage = kT/q
G_{in} = external input conductance
IB = dc base biasing current

The equation for the intrinsic base flicker corner modifies the measured flicker corner to account for the input conductance, base current, and dc current gain of the device. The formula for F_{bn} is valid provided the measured output noise characteristics are dominated by the base flicker and base shot noise sources.

Changing the *KF* and *AF* factors affects the phase noise, as can be seen from the plots in Figure 4-69.

Y-intercept of the 1/*f* spectra increases proportionally to *KF*. The *Y*-intercept of the 1/*f* spectra decreases more rapidly with increase in AF (see Figure 4-70). The following discussion of the tuning diodes results in a noise contribution similar to this flicker mechanism.

AM-to-PM Conversion from Tuning Diodes

Figure 4-71 shows a parallel-tuned circuit that is connected to the oscillator discussed earlier. The frequency change is obtained by applying a positive voltage to the + terminal. The parallel capacitor is replaced by the two tuning diodes. Here we will show the influence of the tuning diodes in the VCOs; the resulting phase noise generated by tuning diodes is shown in Figure 4-72.

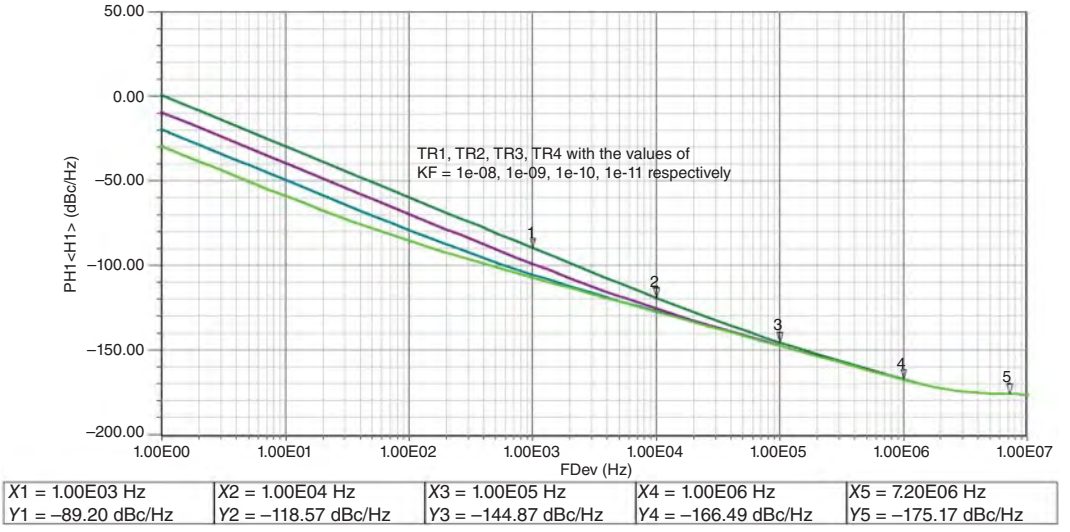


Figure 4-69 Effect of *KF* factor on phase noise.

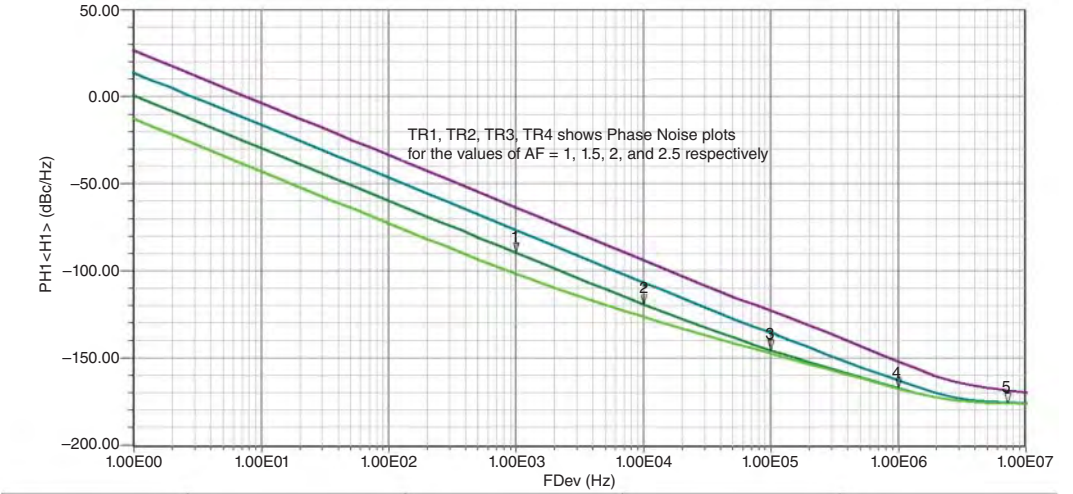


Figure 4-70 Effect of *AF* factor on phase noise.

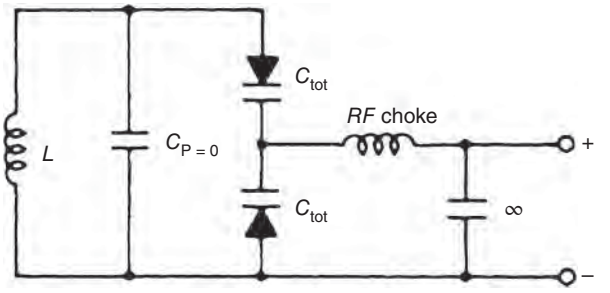


Figure 4-71 Parallel-tuned circuit with tuning diodes.

It is possible to define an equivalent noise R_{aeq} that, inserted in Nyquist's Johnson noise equation,

$$V_n = \sqrt{4kT_oR\Delta f} \tag{4-203}$$

where $kT_o = 4.2 \times 10^{-21}$ at about 300 K, R is the equivalent noise resistor, and Δf is the bandwidth, determines an open-circuit noise voltage across the tuning diode. Practical values of R_{aeq} for carefully selected tuning diodes are in the vicinity of 200 Ω to 50 kΩ. If we now determine the noise voltage, $V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 10{,}000}$, the resulting voltage value is $1.296 \times 10^{-8} V\sqrt{\text{Hz}}$.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o, resulting in the rms frequency deviation

$$(\Delta f_{\text{rms}}) = K_o \times (1.296 \times 10^{-8}\text{V}) \text{ in 1-Hz bandwidth} \tag{4-204}$$

To translate this into an equivalent peak phase deviation,

$$\theta_d = \frac{K_o\sqrt{2}}{f_m}(1.296 \times 10^{-8}) \text{ rad in 1-Hz bandwidth} \tag{4-205}$$

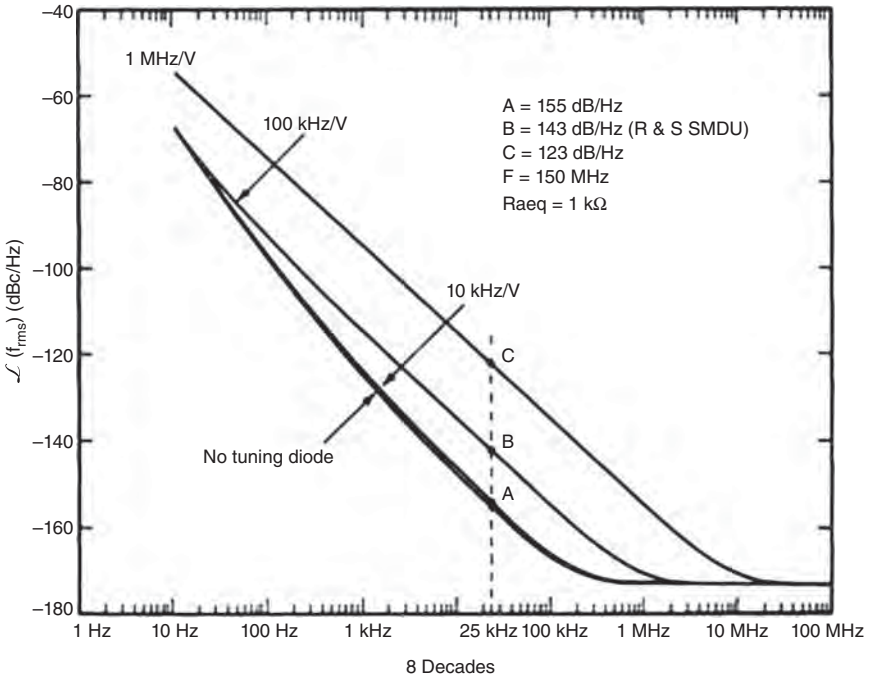


Figure 4-72 Influence of tuning diode on phase noise.

or for a typical oscillator gain of 100 kHz/V,

$$\theta_d = \frac{0.00183}{f_m} \text{ rad in 1-Hz bandwidth} \tag{4-206}$$

For $f_m = 25$ kHz (typical spacing for adjacent-channel measurements for FM mobile radios), the $\theta_c = 7.32 \times 10^{-8}$. This can be converted now into the single sideband (SSB) signal-to-noise ratio:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -149 \text{ dBc/Hz} \tag{4-207}$$

For the typical oscillator gain of 10 MHz/V found in wireless applications, the resulting phase noise will be 20 dB worse [10 log(10 MHz ÷ 100 kHz). However, the best tuning diodes, like the BB104, have an R_n of 200 Ω instead of 10 kΩ, which again changes the picture. Therefore, with $kT_o = 4.2 \times 10^{-21}$ the resulting noise voltage will be

$$V_n = \sqrt{4 \times 4.2 \times 10^{-21} \times 200} = 1.833 \times 10^{-9} \text{ V}\sqrt{\text{Hz}} \tag{4-208}$$

The equivalent peak phase deviation for a gain of 10 MHz/V in a 1-Hz bandwidth is then

$$\theta_d = \frac{1 \times 10^7\sqrt{2}}{f_m}(1.833 \times 10^{-9}) \text{ rad} \tag{4-209}$$

or

$$\theta_d = \frac{0.026}{f_m} \text{ rad in 1-Hz bandwidth} \tag{4-210}$$

with $f_m = 25\,\text{kHz}$, $\theta_c = 1.04 \times 10^{-6}$. Expressing this as phase noise:

$$\mathcal{L}(f_m) = 20\log_{10}\frac{\theta_c}{2} = -126\,\text{dBc/Hz} \tag{4-211}$$

Figure 4-71 shows the influence of the tuning diode on the phase noise. For the purpose of discussion, the equivalent noise resistance is assumed 1 kΩ, and three sensitivity curves are shown. For a tuning sensitivity of more than 100 kHz/V, the varactor noise dominates. As the tuning sensitivity increases, the influence of the oscillator noise itself disappears.

4-2-6 Oscillators for IC Applications

The ADF4356 as an example has an integrated VCO core, typically 4 VCOs with a fundamental output frequency ranging from 3400 to 6800 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allow the user to generate RF output frequencies as low as 53.125 MHz. The oscillator internally uses a large number of CMOS switches to obtain a coarse frequency selection combined with tuning diodes. A block diagram is given in Figure 4-73.

Figure 4-74 documents open-loop and closed loop phase noise measurements.

The phase noise seems to be limited to a noise of −155 dBc/Hz at the VCO frequency and limited to −160+ dBc/Hz at about 50 MHz.

Using the familiar equation

$$\mathcal{L} = 10\log\left\{\left[1 + \frac{fo^2}{(2\cdot fm\cdot Ql)^2\cdot\left(1-\frac{Ql}{Qo}\right)^2}\right]\cdot\left(1+\frac{fc}{fm}\right)\cdot\frac{(F\cdot kT)}{2\cdot Po\omega} + \frac{2\cdot kT\cdot R\cdot ko^2}{fm^2}, 10\right\}$$

And some parameter fitting, we obtain a similar plot (see Figure 4-75). Of course, the Q of the resonator is "not award winning"!

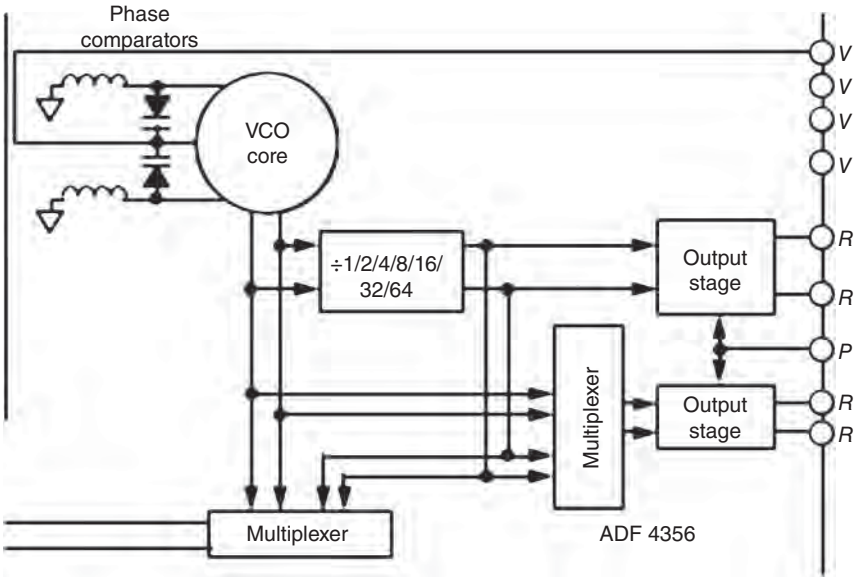


Figure 4-73 IC oscillator block diagram.

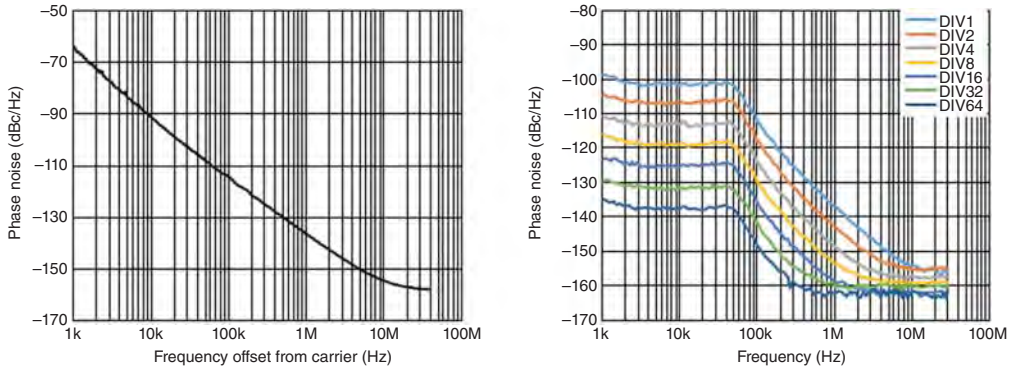


Figure 4-74 (a) Open-loop VCO phase noise, 3.4 GHz. (b) Closed-loop phase noise, fundamental VCO, and dividers; VCO = 3.4 GHz, bandwidth = 40 kHz.

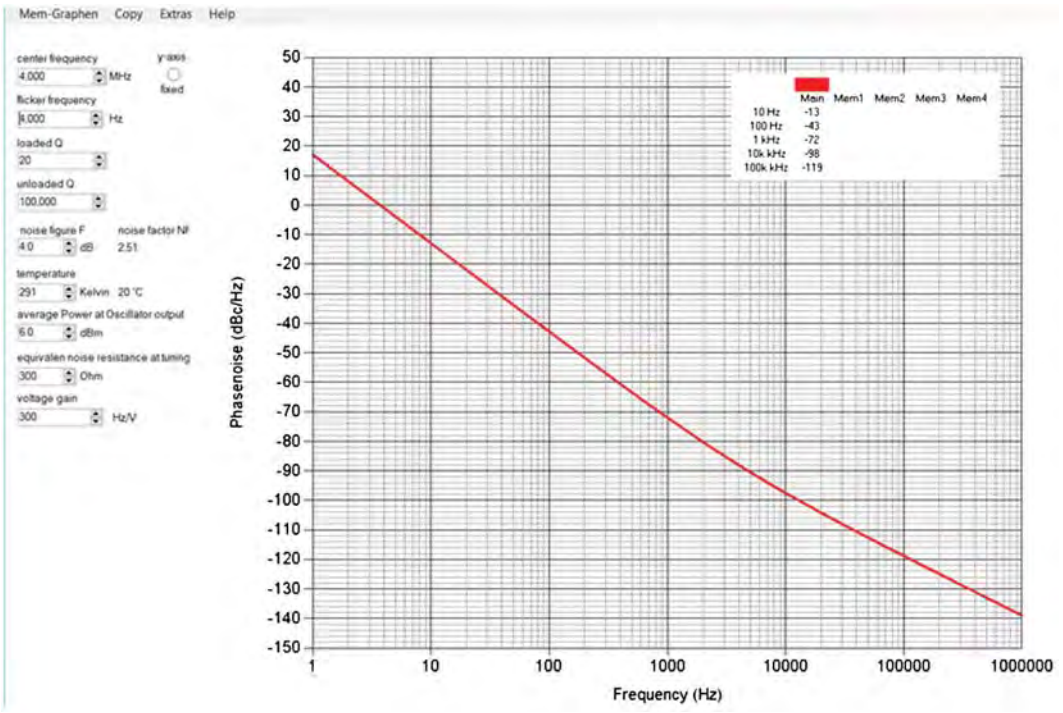


Figure 4-75 Phase noise as a function of frequency.

4-2-7 Noise in Semiconductors and Circuits

Microwave applications generally use bipolar transistors and following are their noise contributions [3, 5, 6, 9, 21, 75]:

- Johnson noise and Planck's radiation noise.
- Johnson noise (thermal noise) is due to the movement of molecules in solid-state devices called Brown's molecular movements. It is expressed as

$$v_n^2 = 4kT_0RB\,(\text{emf})\ \left(\text{V}^2/\text{Hz}\right)$$

The power can thus be written as

$$\text{noise power} = \frac{v_n^2}{R} = 4kT_0B\,(\text{W/Hz})$$

$$\text{for } B = 1\text{ Hz, noise power} = 4kT_0$$

$$T = 290\text{K and } k - \text{Boltzmann}'\text{s const.} = 1.38 \times 10^{-23}$$

$$\text{by Thevenin, noise power} = 1.38 \times 10^{-23} \times 290 = 4 \times 10^{-21}\text{ W}$$

$$L(\omega) = 10.\log\left(\frac{v_n^2/R}{1\text{ dBm}}\right) = -173.97\text{ dBm or about} - 174\text{ dBm}$$

In order to reduce this noise, the only option is to lower the temperature, since noise power is directly proportional to temperature. The Johnson noise sets the theoretical noise floor.

- The available noise power does not depend on the value of the resistor but it is a function of temperature T. The noise temperature can thus be used as a quantity to describe the noise behavior of a general lossy one-port network. For high frequencies and/or low temperature, a quantum mechanical correction factor has to be incorporated for the validation of equations. This correction term results from Planck's radiation law, which applies to blackbody radiation.

$$P_{\text{av}} = kT \cdot \Delta f$$

$$P_{\text{av}} = kT\Delta f \cdot p(f,T); \quad \text{with } p(f,T) = \left[\frac{hf}{kT}\Big/\left(e^{\left(\frac{hf}{kT}\right)} - 1\right)\right]$$

$$\text{where } h = 6.626 \cdot 10^{-34} J/s, \text{ Planck}'\text{s constant}$$

- *Schottky/Shot Noise*. The Schottky noise occurs in conducting PN junctions (semiconductor devices) where electrons are freely moving. The root mean square (RMS) noise current is given by

$$\overline{i_n^2} = 2 \times q \times I_{\text{dc}}; P = i_n^2 \times Z$$

where q is the charge of the electron, P is the noise power, and I_{dc} is the dc bias current. Z is the termination load (can be complex).

Since the origin of this noise generated is totally different, they are independent of each other.

- *Flicker Noise*. The electrical properties of surfaces or boundary layers are influenced energetically by states, which are subject to statistical fluctuations and therefore, lead to the flicker noise or 1/*f* noise for the current flow. 1/*f* noise is observable at low frequencies and generally decreases with increasing frequency *f* according to the 1/*f*-law until it is covered by frequency independent mechanisms, like thermal noise or shot noise. As an example, the noise for a conducting diode is bias-dependent and is expressed in terms of *AF* and *KF*.

$$\langle i_{Dn}^2 \rangle_{\text{AC}} = 2qI_{\text{DC}}B + \text{KF}\frac{I_{\text{DC}}^{\text{AF}}}{f}B$$

The AF is generally in range of 1–3 (a dimensionless quantity) and is a bias-dependent curve fitting term, typically 2. The *KF* value is ranging from 1E^{-12} to 1E^{-6} and defines the flicker corner frequency.

- *Transit Time and Recombination Noise*. When the transit time of the carriers crossing the potential barrier is comparable with the periodic signal, some carriers diffuse back and this causes noise. This is typically seen in the collector area of NPN transistor. The electron and hole movements are responsible for this noise. The physics for this noise has not been fully established.

- *Avalanche Noise*. When a reverse bias is applied to semiconductor junction, the normally small depletion region expands rapidly. The free holes and electrons then collide with the atoms in depletion region, thus ionizing them and produce spiked current called the avalanche current. The spectral density of avalanche noise is mostly flat. At higher frequencies the junction capacitor with lead inductance acts as a low-pass filter (LPF). Zener diodes are used as voltage reference sources and the avalanche noise needs to be reduced by large value bypass capacitors.

4-2-8 Summary

With a systematic approach to the Colpitts oscillator, this chapter provides information for an optimized design and the resulting phase noise performance. Starting with the explanation about the Colpitts oscillator, invented in 1918, we have discussed a linear analysis based the on *Y*-parameters, followed by *S*-parameter approach, which is applicable to practically all oscillators and then move into the important time-domain analysis. This allows a very reliable design, where the simulated, calculated, and measured results agree well. This detailed analysis gives a thorough insight into the design approach and results of a Colpitts oscillator. Finally, the noise contribution of the tuning diodes is added. The interested reader, having access to CAD tools, can run some experiments by varying the component values.

At this point we would also like to thank our reviewers for their valuable suggestions to optimize this chapter.

4-3 USE OF TUNING DIODES

In order to tune the oscillator within the required range, so-called tuning diodes are used. These diodes are often called varactors or voltage sensitive diodes. By way of approximation, we can use the equation

$$C = \frac{K}{(V_R + V_D)^n} \tag{4-212}$$

wherein all constants and all parameters determined by the manufacturing process are contained in K. The exponent is a measure of the slope of the capacitance/voltage characteristic and is 0.5 for alloyed diodes, 0.33 for single diffused diodes, and (on average) 0.75 for tuner diodes with a hyper abrupt PN junction [54, 76]. Figure 4-76 shows the capacitance/voltage characteristics of an alloyed, a diffused, and a tuner diode.

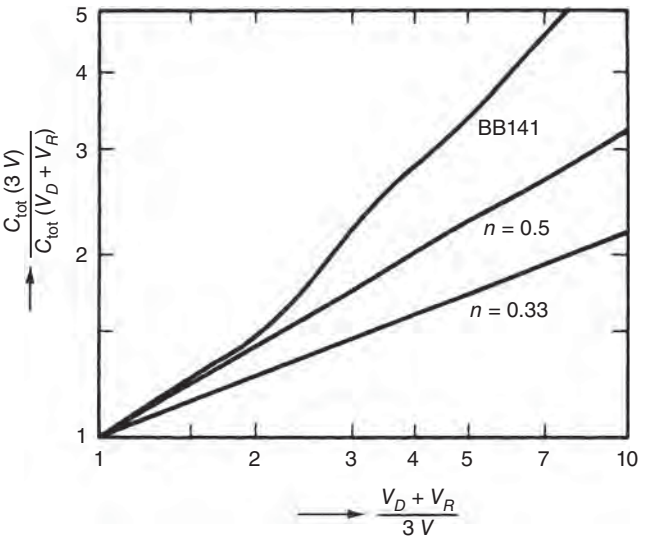


Figure 4-76 Capacitance/voltage characteristic for an alloyed capacitance diode ($n = 0.33$), a diffused capacitance diode ($n = 0.5$), and a wide-range tuner diode (BB141).

Table 4-4 Example tuning diode devices

Capacitance	MV209	BB105	MVAM125
At $V_R = 1$ V, C_{tot}	40 pF	18 pF	500 pF
At $V_R = 25$ V, C_{tot}	6 pF	2 pF	33 pF
Useful capacitance ratio, $C_{tot}(1\text{ V})/C_{tot}(25\text{ V})$	6	9	15

An equation was subsequently developed that, although purely formal, describes the practical characteristic better than Eq. (4-212):

$$C = C_0\left(\frac{A}{A + V_R}\right)^m \tag{4-213}$$

wherein C_0 is the capacitance at $V_R = 0$, and A is a constant whose dimension is a volt. The exponent m is much less dependent on voltage than the exponent n in Eq. (4-212).

The operating range of a capacitance diode or its useful capacitance ratio

$$\frac{C_{max}}{C_{min}} = \frac{C_{tot}(V_{Rmin})}{C_{tot}(V_{Rmax})} \tag{4-214}$$

is limited by the fact that the diode must not be driven by the alternating voltage superimposed on the tuning voltage either into the forward mode or the breakdown mode. Otherwise, rectification would take place, which would shift the bias of the diode and considerably affect its figure of merit.

There are several manufacturers of tuning diodes, including Motorola, Siemens, and Philips. Table 4-4 contains information for three typical tuning diodes as they might be considered useful for our applications.

4-3-1 Diode Tuned Resonant Circuits

Tuner Diode in Parallel Resonant Circuit

Figures 4-77–4-79 illustrate three basic circuits for the tuning of parallel resonant circuits by means of capacitance diodes. In the circuit diagram of Figure 4-77, the tuning voltage is applied to the tuner diode via the tank coil and the bias resistor R_B. Series-connected to the tuner diode is the series capacitor C_S, which completes the circuit for the alternating current but isolates the cathode of the tuner diode from the coil and thus from the negative terminal of the tuning voltage. Moreover, a fixed parallel capacitance C_P is provided. The decoupling capacitor preceding the bias resistor is large enough to be disregarded in the following discussion. Since for high frequency purposes the biasing resistor is connected in parallel with the series capacitor, it is transformed into the circuit as an additional equivalent shunt resistance R_c. We have the equation

$$R_c = R_B\left(1 + \frac{C_S}{C_{tot}}\right)^2 \tag{4-215}$$

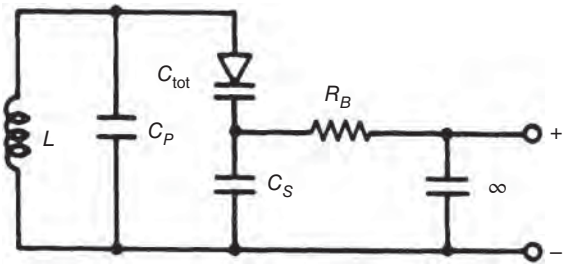


Figure 4-77 Parallel resonant circuit with tuner diode and bias resistor parallel to the series capacitor.

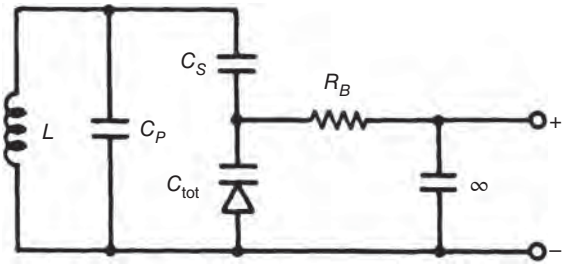


Figure 4-78 Parallel resonant circuit with tuner diode and bias resistor parallel to the diode.

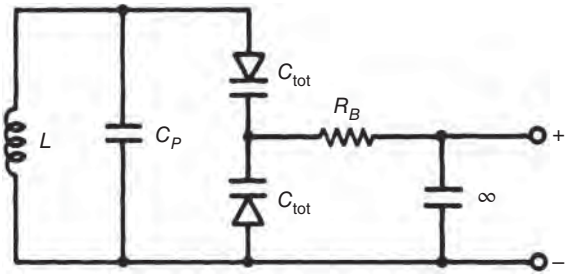


Figure 4-79 Parallel resonant circuit with two tuner diodes.

If in this equation the diode capacitance is replaced by the resonant circuit frequency ω, we obtain

$$R_c = R_B\left(\frac{\omega^2 LC_S}{1-\omega^2 LC_P}\right)^2 \tag{4-216}$$

The resistive loss R_c, caused by the bias resistor R_B, is seen to be highly frequency dependent, and this may result in the bandwidth of the tuned circuit being dependent on frequency if the capacitance of the series capacitor C_S is not chosen sufficiently high.

Figure 4-78 shows that the tuning voltage can also be applied directly and in parallel to the tuner diode. For the parallel loss resistance transformed into the circuit, we have the expression

$$R_c = R_B\left(1+\frac{C_{tot}}{C_S}\right)^2 \tag{4-217}$$

and

$$R_c = R_B\left[\frac{\omega^2 LC_S}{\omega^2 L(C_S+C_P)-1}\right]^2 \tag{4-218}$$

The influence of the bias resistor R_B in this case is larger than in the circuit of Figure 4-77, provided that

$$C_S^2 > C_S(C_{tot}+C_P)+C_{tot}C_P$$

This is usually the case because the largest possible capacitance will be preferred for the series capacitor C_S, and the smallest for the shunt capacitance C_P. The circuit of Figure 4-77 is therefore normally preferred to that of Figure 4-78. An exception would be the case in which the resonant circuit is meant to be additionally damped by means of the bias resistor at higher frequencies.

In the circuit of Figure 4-79, the resonant circuit is tuned by two tuner diodes, which are connected in parallel via the coil for tuning purposes, but series-connected in opposition for high frequency signals. This arrangement has the advantage that the capacitance shift caused by the ac modulation takes effect in opposite directions in these diodes and therefore cancels itself. The bias resistor R_B, which applies the tuning voltage to the tuner diodes, is transformed into the circuit at a constant ratio throughout the whole tuning range. Given two identical, loss-free tuner diodes, we obtain the expression

$$R_c = 4R_B \tag{4-219}$$

Capacitances Connected in Parallel or in Series with the Tuner Diode

Figures 4-77 and 4-78 show that a capacitor is usually in series with the tuner diode, in order to close the circuit for alternating current and, at the same time, to isolate one terminal of the tuner diode from the rest of the circuit with respect to direct current, so as to enable the tuning voltage to be applied to the diode. If possible, the value of the series capacitor C_S will be chosen such that the effective capacitance variation is not restricted. However, in some cases—for example, in the oscillator circuit of receivers whose intermediate frequency is on the order of magnitude of the reception frequency—this is not possible, and the influence of the series capacitance will then have to be taken into account. By connecting the capacitor C_S, assumed to be loss-free, in series with the diode capacitance C_{tot}, the tuning capacitance is reduced to the value

$$C^* = C_{\text{tot}} \frac{1}{1 + C_{\text{tot}}/C_S} \tag{4-220}$$

The Q-factor of the effective tuning capacitance, taking into account the Q-factor of the tuner diode, increases to

$$Q^* = Q\left(1 + \frac{C_{\text{tot}}}{C_S}\right) \tag{4-221}$$

The useful capacitance ratio is reduced to the value

$$\frac{C^*_{\text{max}}}{C^*_{\text{min}}} = \frac{C_{\text{max}}}{C_{\text{min}}} \frac{1 + C_{\text{min}}/C_S}{1 + C_{\text{max}}/C_S} \tag{4-222}$$

wherein C_{max} and C_{min} are the maximum and minimum capacitances of the tuner diode.

On the other hand, the advantage is gained that, due to capacitive potential division, the amplitude of the alternating voltage applied to the tuner diode is reduced to

$$\hat{v}^* = \hat{v} \frac{1}{1 + C_{\text{tot}}/C} \tag{4-223}$$

so that the lower value of the tuning voltage can be smaller, and this results in a higher maximum capacitance C_{max} of the tuner diode and a higher useful capacitance ratio. The influence exerted by the series capacitor, then, can actually be kept lower than Eq. (4-221) would suggest.

The parallel capacitance C_P that appears in Figures 4-77–4-79 is always present, since wiring capacitances are inevitable and every coil has its self-capacitance. By treating the capacitance C_P, assumed to be loss-free, as a shunt capacitance, the total tuning capacitance rises in value and, if C_S is assumed to be large enough to be disregarded, we obtain

$$C^* = C_{\text{tot}}\left(1 + \frac{C_P}{C_{\text{tot}}}\right) \tag{4-224}$$

The Q-factor of the effective tuning capacitance, derived from the Q-factor of the tuner diode, is

$$Q^* = Q\left(1 + \frac{C_P}{C_{\text{tot}}}\right) \tag{4-225}$$

or, in other words, it rises with the magnitude of the parallel capacitance. The useful capacitance ratio is reduced:

$$\frac{C^*_{\max}}{C^*_{\min}} = \frac{C_{\max}}{C_{\min}} \frac{1 + C_P/C_{\max}}{1 + C_P/C_{\min}} \tag{4-226}$$

In view of the fact that even a comparatively small shunt capacitance reduces the capacitance ratio considerably, it is necessary to ensure low wiring and coil capacitances in the layout stage.

Tuning Range The frequency range over which a parallel resonant circuit (according to Figure 4-77) can be tuned by means of the tuner diode depends on the useful capacitance ratio of the diode and on the parallel and series capacitances present in the circuit. The ratio is

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{1 + \frac{C_{\max}}{C_P(1+C_{\max}/C_S)}}{1 + \frac{C_{\max}}{C_P(C_{\max}/C_{\min}+C_{\max}/C_S)}}} \tag{4-227}$$

In many cases the series capacitor can be chosen large enough for its effect to be negligible. In that case, Eq. (4-69) is simplified as follows:

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{1 + C_{\max}/C_P}{1 + C_{\min}/C_P}} \tag{4-228}$$

From this equation, the diagram shown in Figure 4-80 is computed. With the aid of this diagram, the tuning diode parameters required for tuning a resonant circuit over a stipulated frequency range (i.e., the maximum capacitance and the capacitance ratio) can be determined. Whenever the series capacitance C_S cannot be disregarded, the effective capacitance ratio is reduced according to Eq. (4-222).

When several tuned circuits are used on the same frequency, diodes have to be selected for perfect tracking.

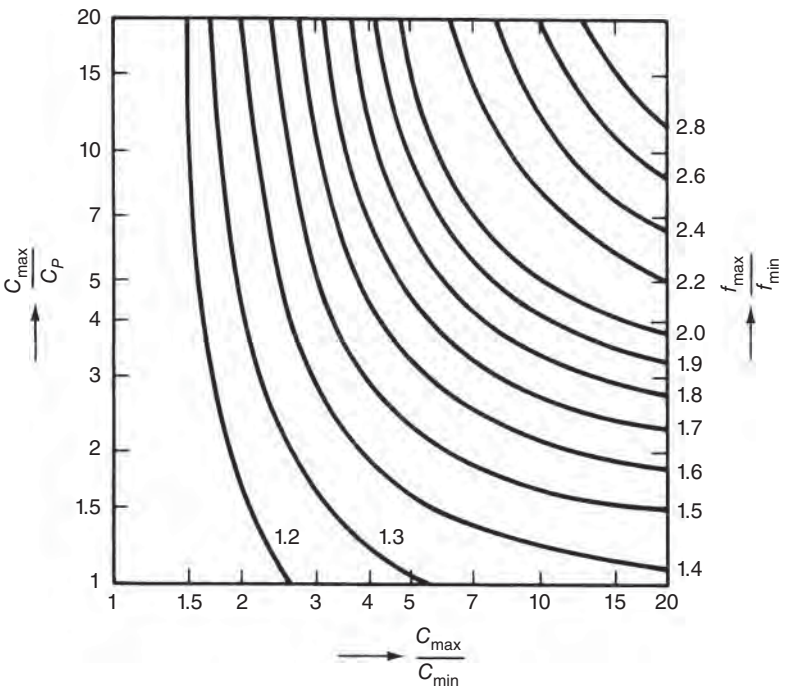


Figure 4-80 Diagram for determining the capacitance ratio and maximum capacitance.

4-3-2 Practical Circuits

After so much theory, it may be nice to take a look at some practical circuits, such as the one shown in Figure 4-81. This oscillator is being used in the Rohde & Schwarz ESN/ESVN40 field strength meter and in the HF1030 receiver produced by Cubic Communications, San Diego. This circuit combines all the various techniques shown previously. A single diode is being used for fine-tuning a narrow range of less than 1 MHz; coarse tuning is achieved with the antiparallel diodes.

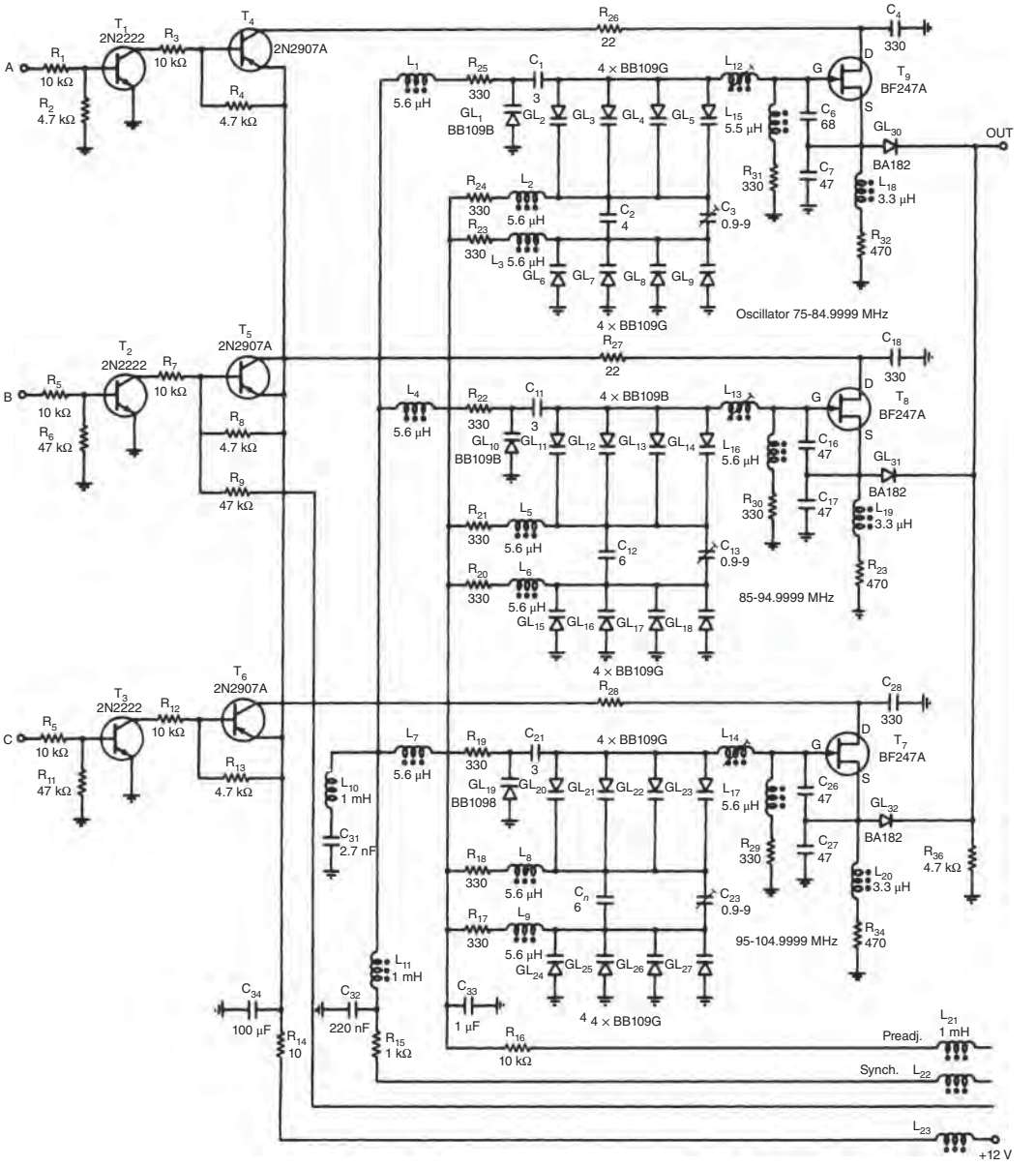


Figure 4-81 Oscillator and switching section of the Rohde & Schwarz ESH2/ESH3 test receiver.

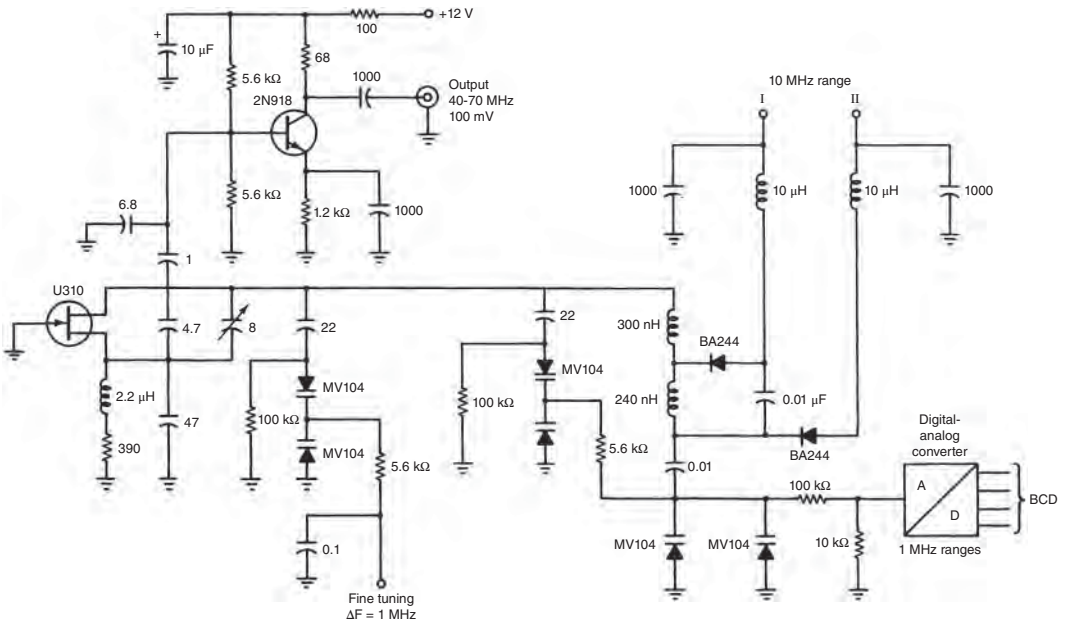


Figure 4-82 A 40–70 MHz VCO with two coarse-steering ranges and fine-tuning range of 1 MHz.

Several unusual properties of this circuit are apparent:

- The fine tuning is achieved with a tuning diode that has a much larger capacitance than that of the coupling capacitor to the circuit. The advantage of this technique is that the fixed capacitor and the tuning diode form a voltage divider whereby the voltage across the tuning diode decreases as the capacitance increases. For larger values of the capacitance of the tuning diode, the Q changes and the gain K_0 increases. Because of the voltage division, the noise contribution and loading effect of the diode are reduced.
- In the coarse-tuning circuit, several tuning diodes are used in parallel. The advantage of this circuit is a change in LC ratio by using a higher C and storing more energy in the tuned circuit. There are no high-Q diodes available with such large capacitance values, and therefore preference is given to using several diodes in parallel rather than one tuning diode with a large capacitance, normally used only for AM tuner circuits.

We have mentioned previously that, despite this, the coarse-tuning circuit will introduce noise outside the loop bandwidth, where it cannot be corrected. It is therefore preferable to incorporate switching diodes for segmenting ranges at the expense of switching current drain.

Figure 4-82 shows a circuit using a combined technique of tuning diodes for fine- and medium-resolution tuning and coarse tuning with switching diodes. The physics and technique of using switching diodes are explained in the next section.

4-4 USE OF DIODE SWITCHES

The diode switches described here differ somewhat from the switching diodes used in computer and pulse technology. In normal diodes, the signal itself triggers the switching operation—current does or does not pass through the switching diode in dependence on the signal level. Diode switches allow an alternating current to be switched on or off by application of a direct voltage or a direct current. The diode switches BA243, BA244, and the later

version BA238 by ITT or the Motorola MPN 3401 series were developed especially for such a purpose. However, diodes can also be employed to advantage for switching audio signals.

4-4-1 Diode Switches for Electronic Band Selection

The advantages of the electronic tuning of VHF/UHF circuits become fully effective only when band selection also takes place electronically and no longer by means of mechanically operated switching contacts that are subject to wear and contamination. Figure 4-83 shows an example of the use of diode switches.

Diode switches are preferable to mechanical switches because of their higher reliability and virtually unlimited life. Since the diode switches BA243 and BA244 permit range switching without mechanical contacts, and since they can be controlled in a similar way as capacitance diodes by the application of a direct current, there are many applications for these devices in remote control receivers. Their use obviates the need for mechanical links between the front-panel control and the tuned circuit to be switched, allowing a VHF/UHF circuit to be located in the most favorable place with regard to electrical or thermal influence, giving the designer more freedom in front-panel layout. Moreover, because the tuner is no longer subject to mechanical stress, its chassis may be injection-molded from a plastic material, which can be plated for screening purposes. All this makes for small, more compact tuners and results in considerable savings in production.

Let us take a look at three oscillators that are designed around switching diodes. Figure 4-84 shows an oscillator that is used in the Rohde & Schwarz EK070 shortwave receiver and that presets the value of the frequency within a few hundred kHz off the final frequency. The fine tuning then is accomplished by the use of varactor diodes or tuning diodes.

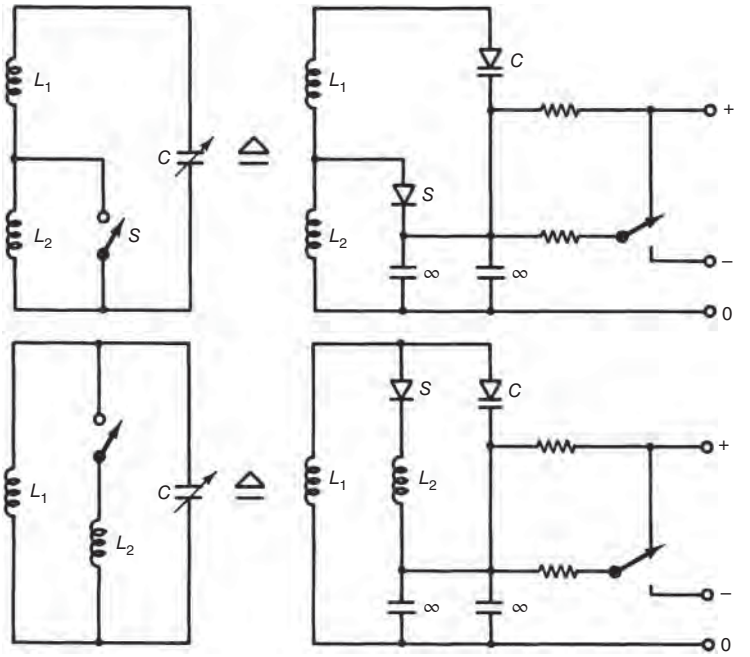


Figure 4-83 Comparison of mechanically and electronically tuned and switched resonant circuits.

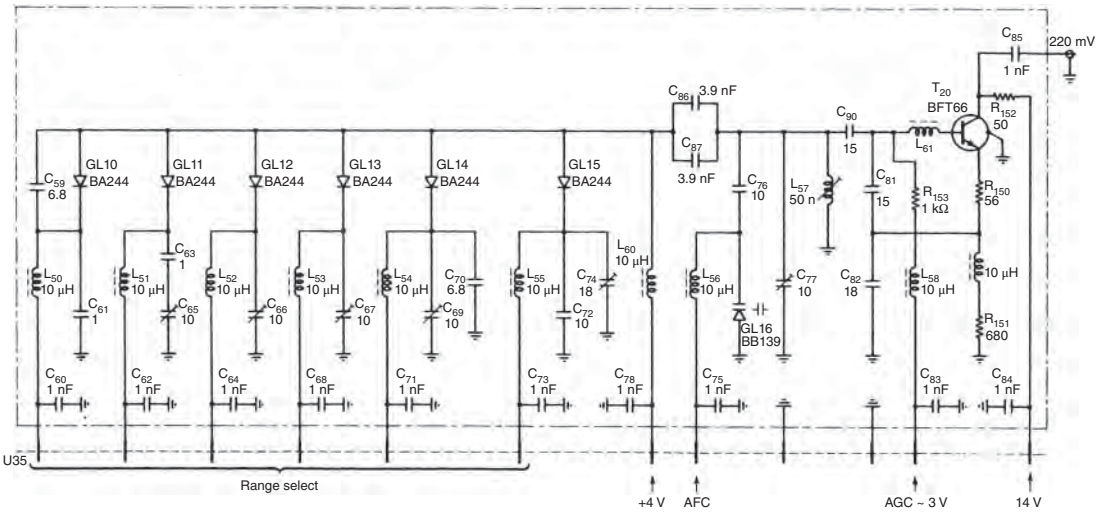


Figure 4-84 Schematic of the VCD from the Rohde & Schwarz EK070 receiver.

The advantage of using one oscillator for the entire frequency range lies in the fact that the switching speed is not slowed by the settling time of an oscillator circuit being activated and showing the familiar initial drift phenomena.

The gain of the oscillator K_o now changes due to the parallel capacitance switched into the tuning diodes, and the loop therefore requires some gain adjustments.

While the aforementioned circuit uses external AGC, which is frequently used with bipolar transistors, Figure 4-85 shows a similar circuit operating from 42 to 72 MHz using field-effect transistors and switching diodes.

Those previously shown circuits switch capacitors rather than inductors. Figure 4-86 shows a circuit that is being used in the HP signal generator type 8962. High-Q inductors are being switched in and out rather than capacitors, thereby avoiding the gain variation of the oscillator to a large degree.

This oscillator also uses a differential amplifier feedback circuit, and the advantage of this circuit is that the signal-to-noise ratio is further improved. Details on differential limiter low-noise design can be found in the literature [77].

4-4-2 Use of Diodes for Frequency Multiplication

So far, we have been dealing with free-running oscillators that are being locked to a reference with the PLL. We mentioned earlier that some synthesizer simplification is possible when using a heterodyne technique. The auxiliary frequency for this heterodyne action can be obtained from the frequency standard by multiplication. There are a number of ways in which to obtain harmonic outputs, and probably the best one is the highest frequency of operation and the use of special diodes, such as step recovery diodes or snap-off diodes. This application would lead us into microwave techniques, which are beyond the scope of this book. Figure 4-87 shows a schematic of a 100–1700 MHz frequency multiplier. More information about frequency multiplication is found in the bibliography at the end of this chapter.

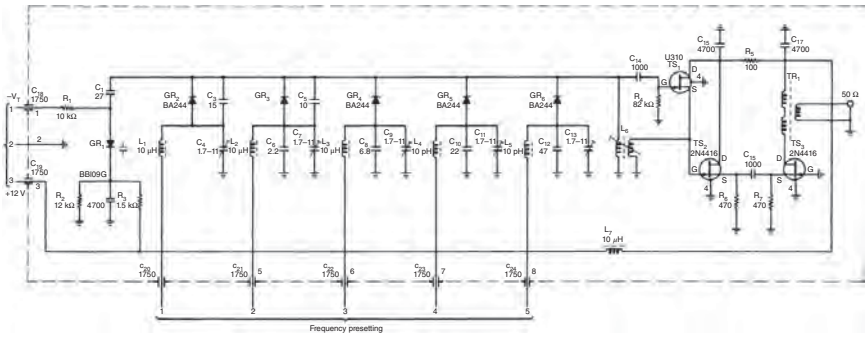


Figure 4-85 VCO operating from 42 to 72 MHz with coarse tuning by switching diodes and high-isolation output stage.

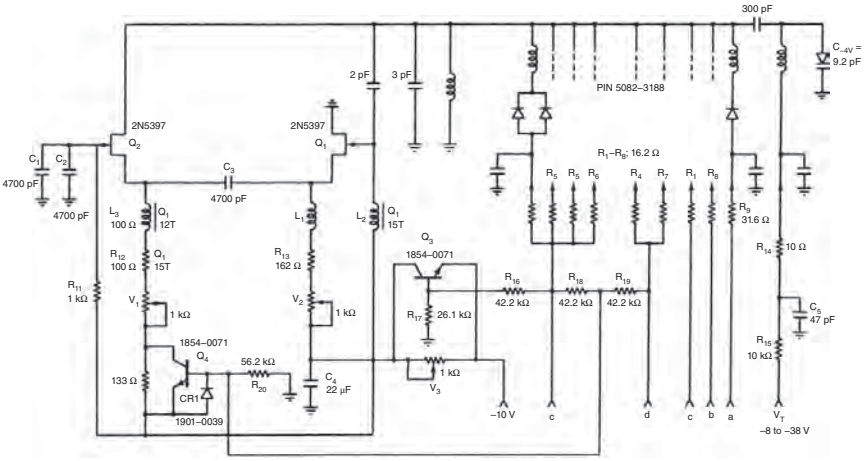


Figure 4-86 Schematic of the HP8662A VCD operating from 260 to 520 MHz.

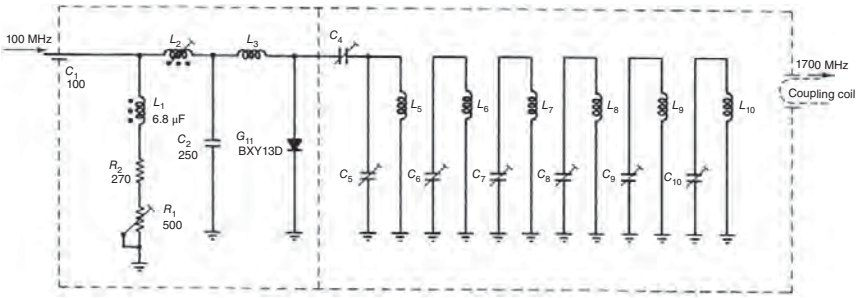


Figure 4-87 A 100–170 MHz frequency multiplier.

4-5 REFERENCE FREQUENCY STANDARDS

Frequency standards are the heart of the synthesizer, as they control the accuracy of the frequency (if we are dealing with a coherent synthesizer) and, within the loop bandwidth, the noise sideband performance of the synthesizer. There are several frequency standards available, and basically, they can be put into three categories:

- Cesium frequency standards
- Rubidium frequency standards
- Crystal oscillators

While it must be noted that at least one manufacturer in the United States is selling a commercial hydrogen maser [78], the maser has not achieved widespread usage. Cesium frequency standards are used as primary standards where extremely accurate stability is needed for long periods of time. Crystal oscillators are currently the most popular choice for reference standards in frequency synthesizers. The short-term stability and noise floor of the crystal oscillator are typically equal to or better than the rubidium standard, and considerably better than the cesium standard. Depending on a number of factors, such as price, performance, size, and power, we find frequency standards ranging from simple crystal oscillators to very high-stability double-oven crystal oscillators to ultrastable cesium beam standards.

4-5-1 Specifying Oscillators

Although it is fairly simple to design a crystal oscillator that has moderate stability, it is not a trivial task to design a high-stability oscillator with low noise. Consequently, it is generally more economical to purchase oscillators for use in synthesizers. This section provides guidelines for specifying crystal oscillators. Specifying the proper parameters (and, perhaps as important from a cost standpoint, not specifying unnecessary parameters) is an important matter. Developing a proper specification is most important when specifying custom oscillators. The following items can be considered as a guideline when specifying oscillators. Generally, not every parameter listed in the following text needs to be, or should be, specified. Rather, the parameters can be used as a checklist when developing a specification.

1.0 *Scope*. This is a general description of the type of oscillator, whether it be a TCXO, OCXO, DCXO, rubidium, or cesium.
2.0 *Reference Documents*. Any reference documents such as test methods or military specifications are listed here. Such examples might be MIL-0-55310 [5] (which is an excellent reference for specifying crystal oscillators).
3.0 *Electrical Requirements*.
3.1 *Nominal Frequency*.
3.2 *Frequency Stability*. This is considered over operating temperature range.
3.3 *Aging*. This should be specified on a per day, per month, or per year basis. Depending on the test method, it is possible to obtain greatly different aging results for the same oscillator.
3.4 *Power Supply Voltages and Tolerances*.
3.5 *Frequency Change*. This results from power supply variations.
3.6 *Power Supply Currents or Power*. Note that the peak heater current as well as steady-state currents should be specified.
3.7 *Output Power and Signal Type*. If a sine wave is desired, the power into 50 Ω is normally specified. If digital output is desired, the type (TTL, CMOS, etc.), duty cycle, and fanout should be specified.
3.8 *Load Stability*. This is normally specified as the amount of frequency change allowed when the load VSWR is varied over some range, say, 2:1.
3.9 *Phase Noise and/or Allan Variance*. If the application requires operation during vibration, the phase noise in vibration should be specified as well.
3.10 *Electrical or Mechanical Tuning Range*. Sufficient tuning must be allowed to accommodate for anticipated frequency aging.
3.11 *Acceleration Sensitivity*. This is a specification of the frequency change due to acceleration. It is often specified in terms of a two-G tipover test, where the oscillator is physically turned over and the resulting frequency change measured. The units are most commonly specified in terms of parts per G.

3.12 *Magnetic Field Sensitivity*. The sensitivity to magnetic fields can be specified in terms of spurious signals induced by a time-varying field.

3.13 *Radiation Hardness*. Since the frequency of an oscillator may change significantly upon exposure to radiation, it is important to specify this parameter for applications where exposure to radiation may be encountered, such as a space environment.

4.0 *Environmental Requirements*. This section includes factors such as operating temperature range, shock, vibration, and any other factors as necessary.

5.0 *Quality Assurance Requirements*. Any special screening, parts, or other quality assurance requirements should be specified. Since these requirements can add considerable cost to the unit, proper specification of these requirements is essential to maintaining reasonable costs with good performance.

4-5-2 Typical Examples of Crystal Oscillator Specifications

As in all design work, the optimal crystal oscillator design depends on the particular application. For instance, there are trade-offs that can be made between long-term aging and short-term stability, and between the noise floor and close-in noise.

Table 4-5 shows the phase noise for various frequency sources, while Table 4-6 shows typical specifications for an ovenized crystal oscillator of moderately high stability. This oscillator does not represent the state of the art but is representative for good-quality commercial oscillators. It employs a third overtone AT crystal in a Colpitts

Table 4-5 Frequency stability of various frequency standards (Rohde & Schwarz)

Offset from signal f (Hz)	Cesium XSC	Rubidium XSRM	Quartz XSD2
10^{-2}	−30	−62	
10^{-1}	−50	−80	
10^{0}	−85	−105	−90
10^{1}	−125	−132	−120
10^{2}	−140	−140	−140
10^{3}	−144	−145	−157
10^{4}	−150	−150	−160

Table 4-6 Partial specification for a moderately high-performance commercial-grade oscillator (Ovenaire 49-5-2)

Parameter	Value
Center frequency	10 MHz
Aging	$\pm(5\text{–}10)^{-10}$/day
Allan variance (1 s)	3×10^{-11}
Temperature range	0 to +60 °C
Ambient stability	$\pm 3 \times 10^{-9}$
Supply voltage	+20 V_{dc}, ±5%
Warm-up power	9 W
Warm-up time	20 min
Steady-state power at 25 °C	2.2 W
Voltage stability	$\pm(5 \times 10)^{-10}$
Phase noise at offset of	
10 Hz	−120 dBc
100 Hz	−140 dBc
1000 Hz	−145 dBc
10,000 Hz	−145 dBc

Table 4-7 Typical specifications for a moderately high-performance commercial-grade TCXO (McCoy electronics)

Parameter	Value
Center frequency	10 MHz
Temperature range	−45 to +85 °C
Ambient stability	±8 ppm
Supply voltage	+12 V_{dc}
Supply power	200 mW max
Output	+7 dBm into 50 Ω
Aging	0.3 ppm/year max
Phase noise at offset of	
10 Hz	−90 dBc
100 Hz	−120 dBc
1000 Hz	−145 dBc
10,000 Hz	−160 dBc

oscillator. The entire assembly is hermetically sealed. Table 4-7 shows typical specifications for a precision analog TCXO. Note that the floor of the TCXO is much better, but close-in noise performance is not as good. In general, the floor of TCXOs can be almost as good as high-stability ovenized oscillators, but the close-in phase noise and short-term stability are very poor relative to an oven. This is because the need to pull the oscillator frequency of a TCXO mandates a low resonator Q relative to an ovenized oscillator.

The TCXO uses a 3.333-MHz fundamental crystal that is multiplied to the output frequency. This approach produces better aging and compensation. A 10-MHz monolithic crystal filter is used to reduce subharmonics to −70 dBc and lower the noise floor to less than −160 dBc. This is achieved with a crystal power dissipation of approximately 50 μW.

By using digital compensation rather than analog compensation, the ambient stability can be reduced to less than ±0.1 ppm [79, 80]. If the frequency is later adjusted for aging, however, the compensation may be altered [81, 82]. Considering these and other subtle effects such as hysteresis in the frequency/temperature characteristics of the crystal, it is very difficult to make a digitally compensated oscillator that is stable and repeatable to better than ±0.05 ppm under all conditions. CXOs also often have a noise spur in the output spectrum at the clock rate of the temperature correction circuitry, although the new techniques of digital compensation may eliminate this problem [83].

If it is expected that the frequency will be adjusted to correct for aging, the customer would be wise to measure the frequency stability over temperature at extremes of the frequency adjust trimmer, and while varying temperature from cold to hot and hot to cold. It is generally found that the compensation varies considerably [82]. Figure 4-88

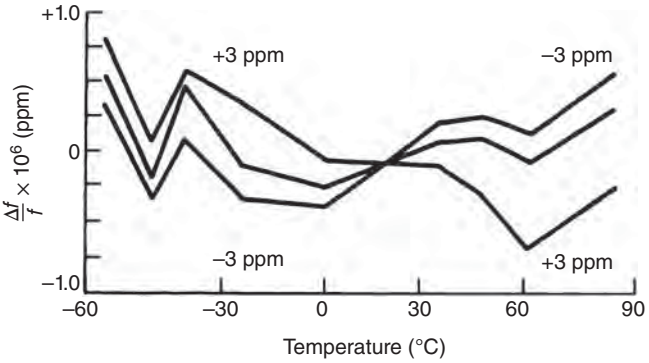


Figure 4-88 Effect of varying frequency adjustment on ambient stability of a typical TCXO. The frequency scale is normalized so that all curves intersect at +25 °C.

Double oven controlled 5MHz crystal oscillator

Features
- High stability vs. temperature: up to $\pm 5 \times 10^{-11}$
- Very low aging upto $\pm 5 \times 10^{-9}$/year
- Low sensitivity to rapid temperature changes
- Sinewave output
- +12V

Typical temperature stability –20 to +70° C $<\pm 1 \times 10^{-10}$

Offset frequency	Phase noise in dBc/Hz (typical)
1 Hz	–105
10 Hz	–130
100 Hz	–145
1 Hz	–150
10 Hz	–155

Figure 4-89 Specifications for double oven controlled 5 MHz crystal oscillator. Performance based on published data from Morion Inc.

100 MHz oven controlled crystal oscillator

Features
- Low phase noise: <–140 dBc/Hz @ 10 KHz<–180 dBc/Hz @ 100 KHz
- Low G–sensitivity: <1E–9/G (typ), option to <2E–10/G
- Standard frequencies: 60,80, 100, 120, and 122.76 MHz
- High stability vs, temperature: up to $\pm 5 \times 10^{-8}$
- Small package: 25×25×10.3 mm
- Sinewave output
- Power supply: 5 V or 12 V

Typical temperature stability –20 to +70° C $<\pm 5 \times 10^{-8}$

Offset frequency	Phase noise in dBc/Hz (typical)
1 Hz	–75
10 Hz	–107
100 Hz	–140
1 kHz	–165
10 kHz	–176
100 kHz	–178

Figure 4-90 Specifications for 100 MHz oven controlled crystal oscillator. Performance based on published data from Morion Inc.

shows the frequency stability of a typical TCXO as the frequency is varied ±3 ppm to compensate for aging. It must be noted though that the new compensation techniques mentioned earlier may allow DCXOs consistently to maintain a stability of around ±0.05 ppm [83], while maintaining good short-term stability.

Typical performance data is given in Figures 4-89 and 4-90.

4-6 MIXER APPLICATIONS

In multiloop synthesizers, the heterodyne principle is used, and various frequencies are combined with mixers. For frequency synthesizer applications, only double-balanced mixers should be used. They fall into the following

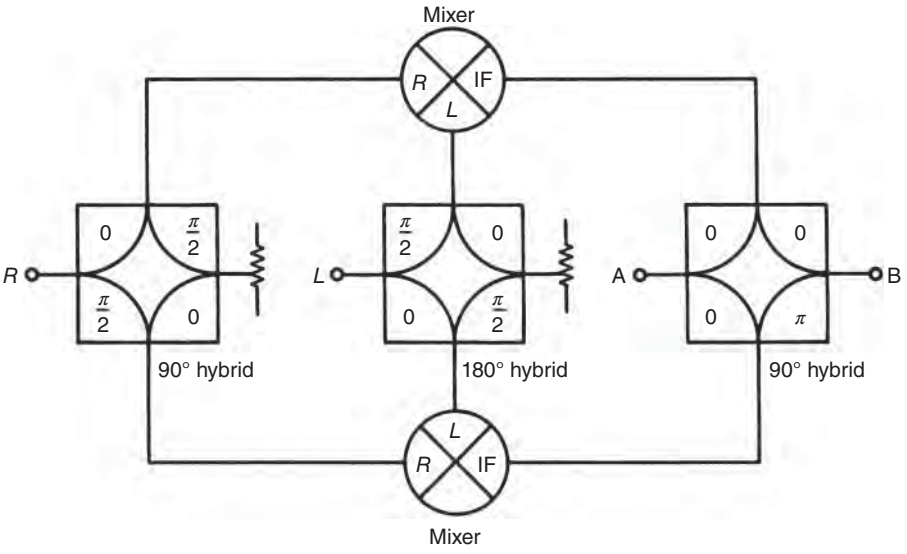


Figure 4-91 Single-sideband mixer.

categories and are considered a component. Active mixers typically do not show enough suppression of unwanted frequencies as can be obtained in passive double-balanced mixers.

- *Single-Sideband Mixer*. A single-sideband mixer is capable of delivering an IF output composed of one sideband only. Figure 4-91 shows a combination that provides the upper sideband at port A and the lower sideband at port B.
- *Image-Rejection Mixers*. An LO frequency of 75 MHz and a desired RF frequency of 25 MHz would produce an IF difference frequency of 50 MHz. Similarly, an image frequency of 125 MHz at the mixer RF port would produce the same 50-MHz difference frequency. The image-rejection mixer shown in Figure 4-92 produces a desired IF difference frequency at port C while rejecting difference frequencies from RF signals, which are greater than the LO frequency.
- *Termination-Insensitive Mixers*. While the phrase "termination insensitive" is somewhat misleading, a combination as shown in Figure 4-93 results in a mixer design that allows a fairly high VSWR at the output without third-order intermodulation distortion being much affected by port mismatches.

Double-balanced mixers are manufactured by several companies. Some specialize in high-performance mixers at very high costs, others in large-volume inexpensive devices. It is advisable to contact the manufacturer before deciding on a particular mixer, as technology changes and new mixer combinations are being introduced. Most manufacturers supply detailed application reports and information about their mixers. Therefore, these details do not have to be covered here.

Table 4-8 is of interest as it shows the typical spurious response of a high-level double-balanced mixer and information about unwanted products to be gathered.

Important: Make absolutely sure that the mixer sees a 50 Ω resistive load; this is achieved either by diplexer, resistive padding, or the use of feedback amplifiers that have 50 Ω input impedance or grounded gate FET amplifiers using devices such as the CP643.

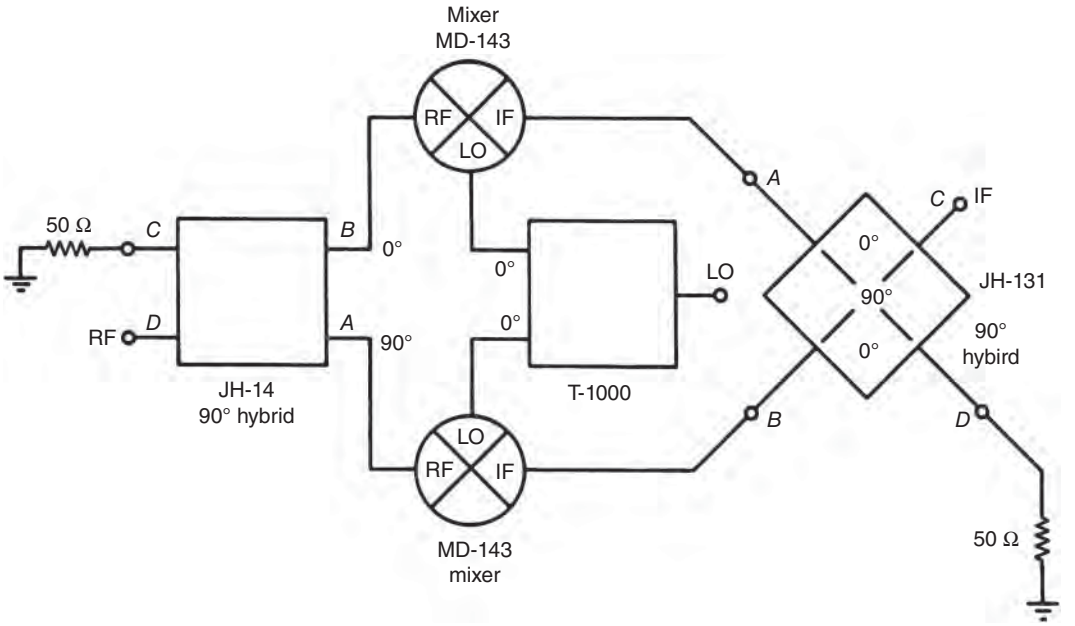


Figure 4-92 Image-rejection mixer.

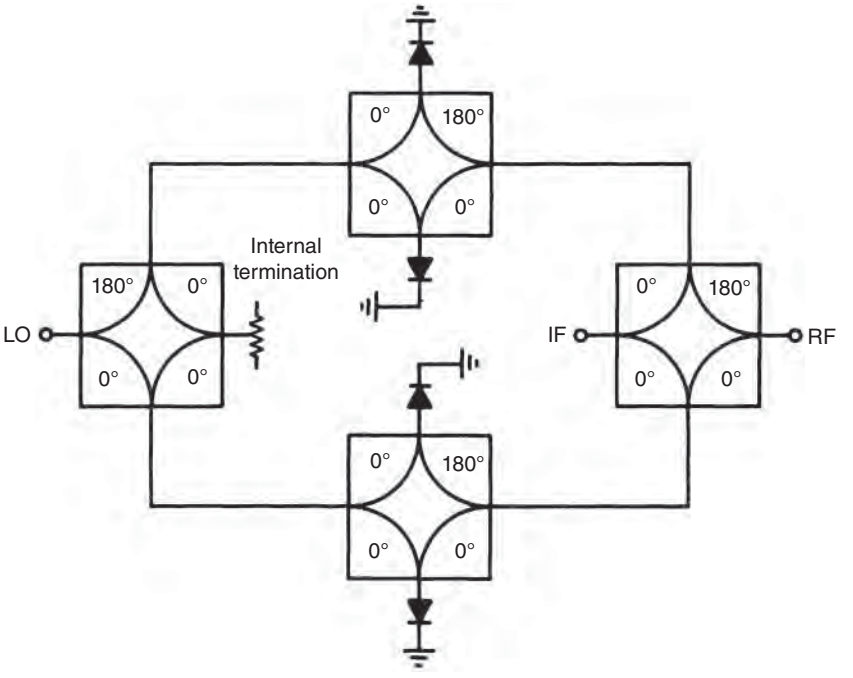


Figure 4-93 Termination-insensitive mixer.

Table 4-8 Typical spurious response of a high-level double-balanced mixer

	Harmonics of f_{RF}								
$8f_{RF}$	100	100	100	100	100	100	100	100	100
$7f_{RF}$	100	97	102	95	100	100	100	90	100
$6f_{RF}$	100	92	97	95	100	100	95	100	100
$5f_{RF}$	90	84	86	72	92	70	95	70	92
$4f_{RF}$	90	84	97	86	97	90	100	90	92
$3f_{RF}$	75	63	66	72	72	58	86	58	80
$2f_{RF}$	70	72	72	70	82	62	75	75	100
$1f_{RF}$	60	0	35	15	37	37	45	40	50
		60	60	70	72	72	62	70	70
		$1f_{LO}$	$2f_{LO}$	$3f_{LO}$	$4f_{LO}$	$5f_{LO}$	$6f_{LO}$	$7f_{LO}$	$8f_{LO}$

Notes:
RF harmonic referenced to RF input signal; LO harmonic referenced to LO input signal.
Spurious responses caused by internal harmonic generation and mixing of the input signals are shown. The mixing products are referenced in dB below the desired $f_{LO} \pm f_{RF}$ output or 0 level at f_{IF}. This performance can typically be attained with f_{LO} and f_{RP} at approximately 100 MHz, f_{LO} at +17 dBm, and f_{RP} at −0 dBm using broadband resistive terminations at all ports.

4-7 PHASE/FREQUENCY COMPARATORS

In Chapter 1 we looked at the phase-locked loop as the fundamental building block of any synthesizer that uses its principle, and we decided to use two classifications—analog and digital loops. The main criterion was the phase/frequency comparator. The phase/frequency comparator can be divided into two types:

- Phase detectors
- Phase/frequency comparators

This means that the phase comparator has limited means to compare two signals and accepts only phase, not frequency, information. In this case, particular measures have to be taken to pull the VCO into the locking range. The phase comparators require special locking help, and we dealt with this previously. Here, we are analyzing only the performance.

The phase detectors we will treat are the diode ring, the exclusive-OR gate, and the sample/hold comparator. The digital phase/frequency comparator (the exclusive-OR gate, because of the waveforms, is a digital device, and the sample/hold comparator, because of its special signal processing, can also be considered in this category) comes in several versions. Here our main interest will be in the tri-state or sequential phase/frequency comparator.

4-7-1 Diode Rings

The diode ring is normally driven with two signals with sinusoidal waveform and also is some sort of a mixer. Here it will suffice to derive the gain characteristic K_θ of the device. If the input signal is $\theta_i = A_i \sin \omega_0 t$, and the reference signal is $\theta_r = A_r \sin(\omega_0 t + \phi)$, where ϕ is the phase difference between the two signals, the output signal θ_e is

$$\theta_e = \theta_i \theta_r = \frac{A_i A_r}{2} K \cos \phi - \frac{A_i A_r}{2} K \cos(2\omega_0 t + \phi) \tag{4-229}$$

where K is the mixer gain. One of the primary functions of the LPF is to eliminate the second harmonic term before it reaches the VCO. The second harmonic will be assumed to be filtered out and only the first term will be considered, so

$$\theta_e = \frac{A_i A_r}{2} K \cos \phi \tag{4-230}$$

when the error signal is zero, $\phi = \pi/2$. Thus, the error signal is proportional to phase differences from 90°. For small changes in phase $\Delta\phi$,

$$\theta_e \simeq \frac{\pi}{2} + \Delta\phi = \frac{A_i A_r}{2} K \left[\cos\left(\frac{\pi}{2} + \Delta\phi\right)\right]$$
$$= \frac{A_i A_r}{2} K \sin \Delta\phi \tag{4-231}$$

For a small phase perturbation $\Delta\phi$,

$$\theta_e \simeq \frac{A_i A_r K}{2} \Delta\phi \tag{4-232}$$

Since the phase detector output was assumed to be

$$\theta_e = K_\theta(\theta_i - \theta_o) \tag{4-233}$$

The phase detector scale factor K_θ is given by

$$K_\theta = \frac{A_i A_r K}{2} \tag{4-234}$$

The phase detector scale factor K_θ depends on the input signal amplitudes; the device can be considered linear only for constant-amplitude input signals and for small deviations in phase. For larger deviations in phase,

$$\theta_e = K_\theta \sin \Delta\phi \tag{4-235}$$

which describes a nonlinear relation between θ_e and ϕ.

In frequency synthesizers, the reference is typically generated from a reference oscillator and is lower than the VCO frequency, which is divided by a programmable divider. Both signals are therefore square waves rather than sine waves, and theoretically, a diode ring can be driven from those two signals.

A drawback is that the output voltage of the diode ring is very small, about several hundred millivolts at most, and a postamplifier is required, which is bound to generate noise. Some modification of this analog circuit is possible to increase the voltage.

Figure 4-94 shows a phase detector circuit used in the frequency synthesizer of the Rohde & Schwarz EK47 shortwave receiver. This balanced mixer arrangement has a limited capture range but supplies enough output voltage and therefore does not require an additional amplifier. There are several possible combinations of this circuit, and because it is not a double-balanced mixer, some harmonics may be at the output, and care has to be taken to avoid having any unwanted spikes on the control line.

4-7-2 Exclusive ORs

The exclusive-OR gate is, to a certain degree, the equivalent of a balanced mixer. However, there are certain restrictions. Let us take a look at several waveform combinations. Figure 4-95 shows the case where two waveforms of equal frequency and different phase are applied and the resulting output from the exclusive-OR gate. If the reference and the VCO waveform have the same duty cycle, the output of the phase/frequency discriminator is clearly defined. In the case of a phase shift of $\pi/2$, the output results in a square wave of twice the frequency, with a duty cycle of 50%. If the waveforms do not have the same duty cycle, things become more complicated. If the VCO frequency is divided by a programmable counter, the pulses from the programmable divider are fairly narrow and thus the duty cycle becomes very small. It is therefore possible, because of the unsymmetrical form of the waveform, that the output voltage is the same for two different phase errors, depending on the duty cycle. To avoid difficulties, it is necessary to add an additional stage that acts as a pulse stretcher, and this pulse stretcher will make the waveform approximately symmetrical.

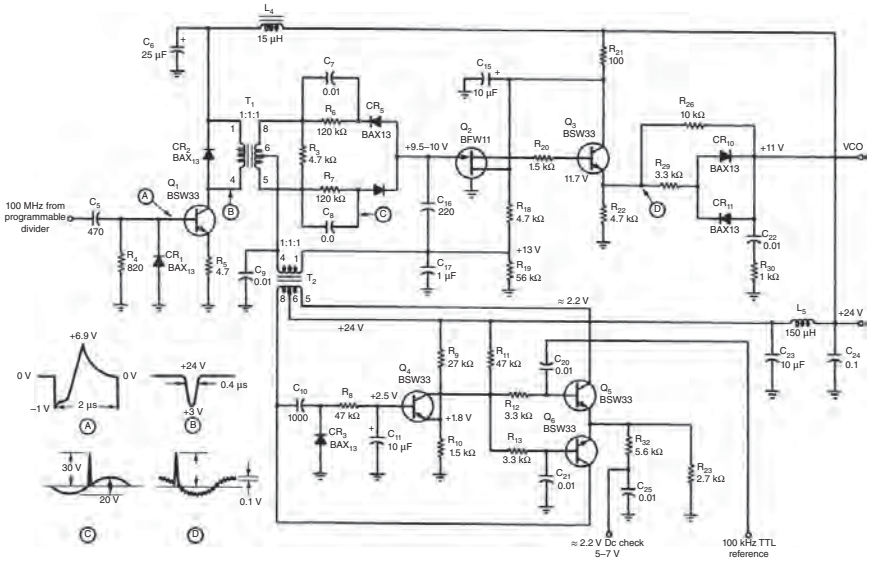


Figure 4-94 Phase detector circuit and loop filter for the Rohde & Schwarz EK47 receiver.

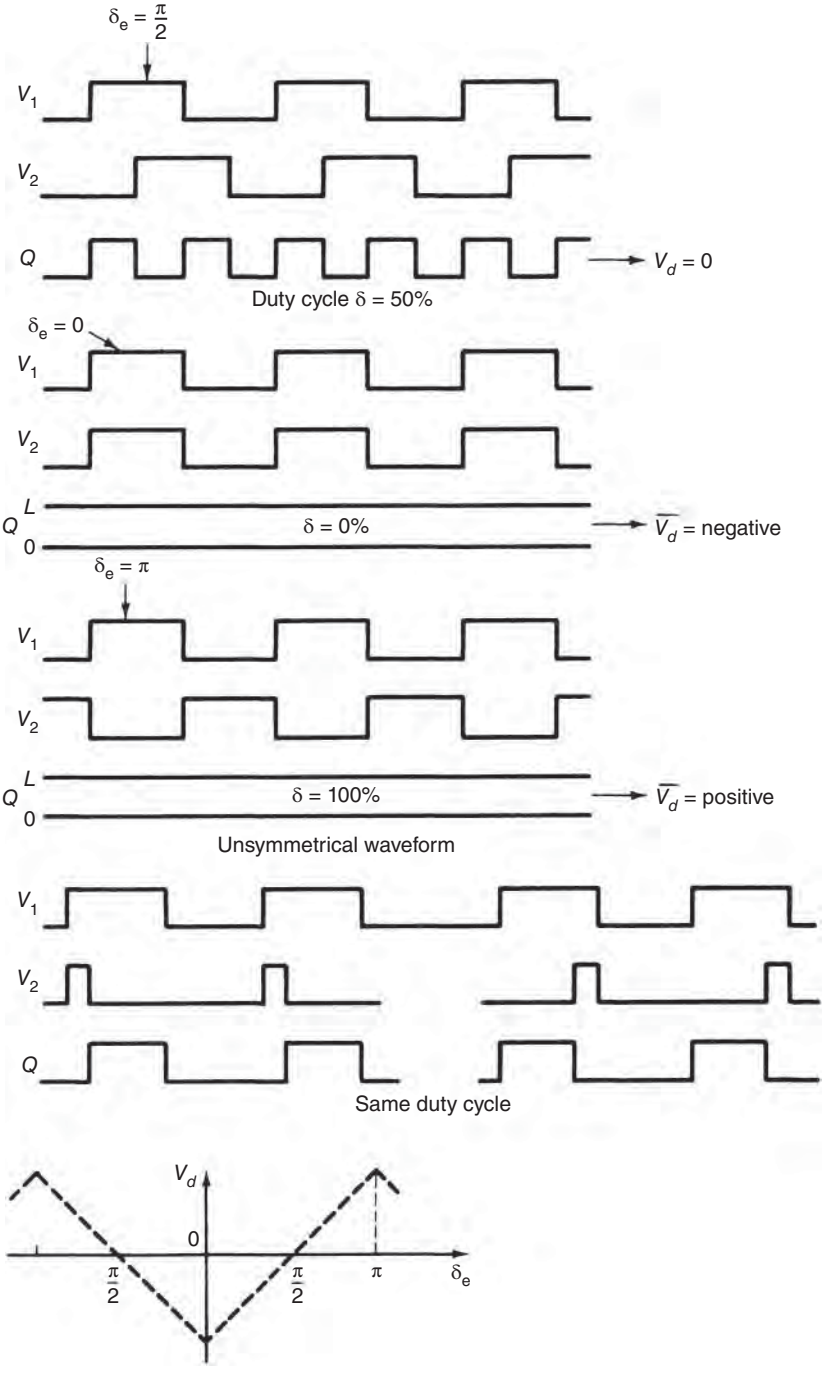


Figure 4-95 Performance of the exclusive-OR phase detector relative to different waveforms at the input.

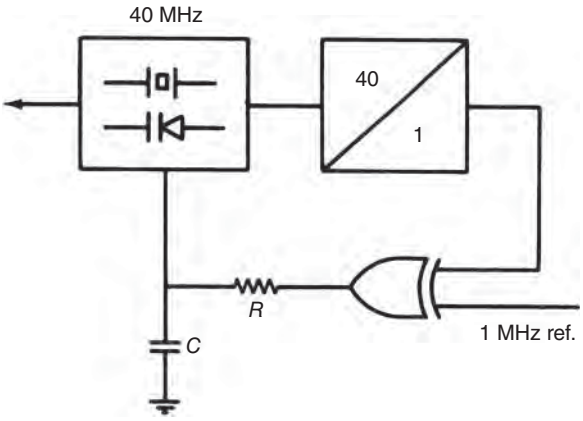


Figure 4-96 Block diagram of a 40-MHz single-loop synthesizer using an exclusive-OR gate as phase detector.

The exclusive-OR gate phase/frequency discriminator should really be used only in cases where the reference and VCO frequency are fairly high and very close together. Figure 4-96 shows a typical application where the exclusive-OR gate is recommended. A 40-MHz crystal oscillator is divided down by 10 and by 4 and provides 1 MHz of output. The reference oscillator is divided down to 1 MHz. Since the crystal oscillator at most will be 1 or 2 kHz off the reference frequency, it is well within the capture range of the exclusive-OR gate, and if both duty cycles are equal and 50%, the circuit can be made stable with a fairly simple RC LPF. This is a type 1 second-order phase-locked loop and will follow the equations in Chapter 1. As the loop bandwidth can be made as narrow as 10 Hz, it will probably compensate only for temperature drift and aging of the crystal relative to the frequency standard.

Example Implementation

Let us assume that we have a crystal that can be pulled 2 kHz with 10 V, and that our phase detector operates from 0 to 5 V. The product $K = K_0K_\theta/N$ then equals 100 Hz. The 3-dB bandwidth of this simple synthesizer without any loop filter added would result in a loop bandwidth of 100 Hz. An additional filter would be required to reduce the loop bandwidth down to 10 Hz. In Chapter 1 we learned that there is a beat frequency generated at the output of the phase detector, and the 10 Hz LPF will attenuate the output voltage at the beat frequency.

Let us assume that our initial condition is that the 40 MHz crystal is aligned to be within 1 Hz of final frequency and that the loop is closed. For most receivers, a proportionally controlled crystal oscillator is used that has a warm-up time of 1 or 2 min for the internal standard to reach final frequency. As a result, the initial offset at the output can be 2000 or 200 Hz at the phase/frequency comparator. In this case, our formula for the pull-in range applies,

$$T_p = \frac{\Delta\omega_0^2}{2\zeta\omega_n^3} \tag{4-236}$$

and we will insert the values

$$\Delta\omega = 2000 \times 2\pi$$

$$\zeta = 0.7$$

$$\omega_n = 10 \times 2\pi$$

or

$$T_p = \frac{2000}{1.4\pi} = 454 \text{ s}$$

However, as the final error after 1 min or 90 s approaches 1 Hz, the pull-in time T_p becomes 4.49 ms.

Most oven-controlled frequency standards have a type 2 second-order servo control system, and therefore the frequency of the frequency standard will go through the desired value and become higher, and then it will settle at the final frequency. Because of this, the frequency standard, so to speak, sweeps the 40 MHz crystal, and therefore the locking is made much faster than 454 s, even under the assumption that the initial frequency error was 2000 Hz because of aging or drift.

4-7-3 Sample/Hold Detectors

Phase detection can also be accomplished with a linear time-varying switch that is closed periodically. Mathematically, the switch can be described as a pulse modulator, as shown in Figure 4-97. If the operation of the sampling switch is periodic, that is, if the sampler closes for a short interval P at instants $T = 0, T, 2T, \ldots, nT$, the sampling is uniform. The waveshapes of the input and output signals of a uniform rate sampling device are shown in Figure 4-98.

The output can be considered to be

$$\theta_e(t) = \theta_i(t)\theta r(t) \tag{4-237}$$

where $\theta_r(t)$ can be assumed to be a periodic train of constant-amplitude pulses of amplitude A_r, width p, and period T. Since $\theta_r(t)$ is periodic, it can be expanded in a Fourier series as

$$\theta_r(t) = \sum_{n=0}^{\infty} C_n \cos n\omega_0 t \tag{4-238}$$

where

$$\begin{aligned} C_n &= \frac{2}{T}\int_{-P/2}^{P/2} \frac{A_r}{2}\cos n\omega_0 t \; dt \\ &= 2\frac{A_r}{T}\left[\left(\sin\frac{n\omega_0 P}{2}\right) - \frac{1}{n\omega_0}\right] \qquad (n \neq 0) \rightarrow \frac{A_r}{T}P \qquad (n \approx 0) \end{aligned} \tag{4-239}$$

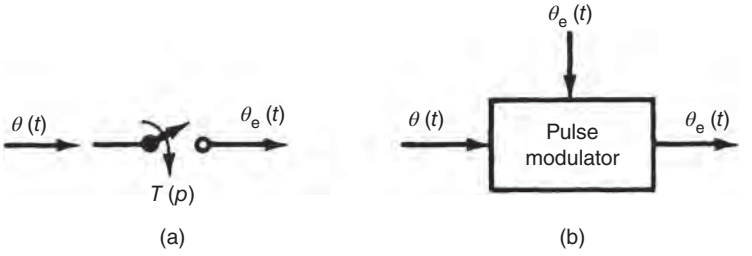


Figure 4-97 Switch shown as a pulse modulator.

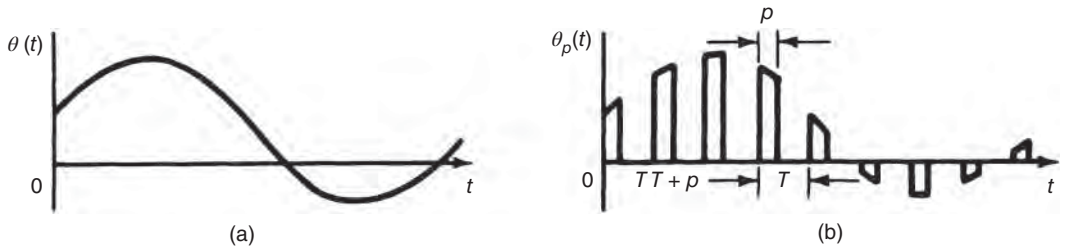


Figure 4-98 Input and output waveforms of a uniform sampling device.

Thus,

$$\theta_r(t) = \frac{A_r}{T}P + \sum_{n=1}^{\infty} 2\frac{A_r}{T}\sin\frac{n\omega_0 P/2}{n\omega_0}\cos\, n\omega_0 t \tag{4-240}$$

If the input signal is a sine wave,

$$\theta_i(t) = A_i[\sin(\omega_i t + \theta_i)] \tag{4-241}$$

then

$$\begin{aligned}\theta_e(t) &= \theta_r(t)\theta_i(t)\\ &= \frac{A_i A_r}{T}\left\{P\sin(\omega_i t + \theta) + \sum_{n=1}^{\infty}\sin\frac{n\omega_0 P/2}{n\omega_0}\right.\\ &\quad\left.\times[\sin(n\omega_0 + \omega_i)t + \theta_i] + \sin(\omega_i t + \theta_i - n\omega_0 t)\right\}\end{aligned} \tag{4-242}$$

when the loop is in lock ($\omega_i = \omega_0$). The dc term is

$$\theta_e(t)_{\text{dc}} = \frac{A_i A_r}{T}\sin\frac{\omega_0 P/2}{\omega_0}(-\sin\theta_i) \tag{4-243}$$

For small θ_i, the error signal is proportional to the phase difference θ_i. Therefore, the linear time-varying switch is able to serve as a phase detector. It differs from the mixer in that the dc output is zero when $\sin\theta_i = 0$, that is, when the oscillator and reference signal are in phase. The mixer type of phase detector is nulled when the two signals are in phase quadrature. Also, when the loop is in lock ($\omega_i = \omega_0$), the mixer output contains a dc term and the second harmonic, whereas the sampled output contains a dc term plus all harmonics of the input frequency. Therefore, the LPF requirements for the sampling type of phase detector are more stringent than those for the sinusoidal mixer.

Fortunately, there are filters that can easily be implemented for the sampling PD. The most commonly used is the zero-order data hold (ZODH) or "boxcar generator." The ZODH is a device that converts the pulse of width P to constant-amplitude pulses of width T, as shown in Figure 4-99.

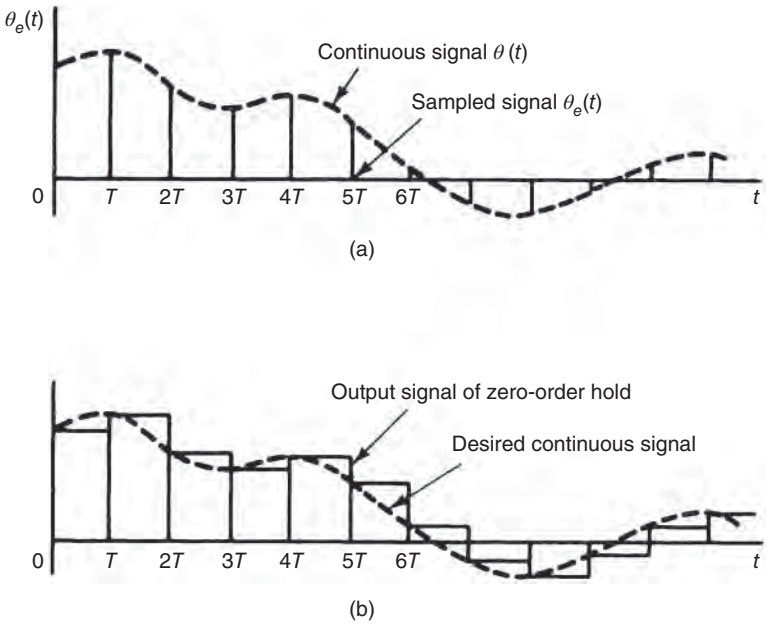


Figure 4-99 Zero-order data hold filter.

The output of the ZODH $\theta_0(t)$ between the sampling instants t_i and t_{i+1} is

$$\theta_0(t) = \theta_e(t_i)[u(t) - u(t_i)] \tag{4-244}$$

where $\theta_e(t)$ is the value of $\theta_e(t)$ at the sampling time t_i. Although the exact analysis of the finite-pulse-width sampler and ZODH combination is complex, the frequency response can be approximated closely if the sampling process is replaced by an "ideal sampler" whose output is a train of impulses. That is, the sampled signal $\theta^*(t)$ is a train of amplitude-modulated impulses

$$\theta^*(t) = \theta_i(t)\delta_T(t) \tag{4-245}$$

where $\delta_T(t)$ is a unit impulse train of period T:

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT) \tag{4-246}$$

where $\delta(t - nT)$ represents an impulse of unit area occurring at time $t = nT$. Since $\delta_T(t)$ is periodic, it can be expressed by the Fourier series

$$\delta_T(t) = \sum_{n=-\infty}^{\infty} C_n e^{-j\,n\,\omega_0 t} \tag{4-247}$$

where

$$\omega_0 = \frac{2\pi}{T} \tag{4-248}$$

The constants C_n are determined from

$$C_n = \frac{1}{T}\int_{-T/2}^{T/2} \delta_T(t) e^{-j\,n\,\omega_0\,t} dt = \frac{1}{T} \tag{4-249}$$

That is, the frequency spectrum of impulse train of period T contains a dc term plus the fundamental frequency and all harmonics, all with an amplitude of $1/T$.

$$\delta_T(t) = \frac{1}{T}\sum_{n=-\infty}^{\infty} e^{jn\omega_0 t} \quad \omega = \frac{2\pi}{T} \tag{4-250}$$

and since

$$e^{j\,n\,\omega_0\,t} + e^{-j\,n\,\omega_0\,t} = 2\cos n\omega_0 t \tag{4-251}$$

$$\delta_T(t) = \frac{1}{T} + \frac{2}{T}\sum_{n=1}^{\infty} \cos n\omega_0 t \tag{4-252}$$

Therefore, Eq. (4-121) can be written

$$\theta^*(t) = \theta_i(t)\frac{1}{T} + \frac{2}{T}\sum_{n=1}^{\infty} \cos n\omega_0 t \tag{4-253}$$

If the input $\theta_i(t)$ is a sine wave $\theta_i(t)_i = A_i \sin(\omega_t t + \theta_i)$,

$$\theta^*(t) = \frac{A_i}{T}\left[\sin(\omega_i t + \theta_i) + 2\sum_{n=1}^{\infty} \cos n\omega_0\, t \sin(\omega_i t + \theta_i)\right] \tag{4-254}$$

This equation is similar to the result obtained in Eq. (4-242) for the more realistic finite-pulse-width model of the sampler. The difference is that for the finite-pulse-width model, the harmonics are attenuated by the factor

$$\frac{\sin(n\omega_0 P/2)}{n\omega_0}$$

With the impulse sampler, all harmonics are of amplitude $2/T$.

The impulse response of the ZODH is

$$u(t) - u(t-T) = \frac{1 - e^{-sT}}{s} \tag{4-255}$$

and the ZODH frequency response is

$$\frac{1 - e^{-j\omega T/2}}{j\omega} = \frac{2}{T} e^{-j\omega T/2} \frac{e^{j\omega T/2} - e^{-j\omega T/2}}{j\omega T/2} \tag{4-256}$$

$$G_z(j\omega) = \frac{2}{T} e^{-j\omega T/2} \frac{\sin(\omega T/2)}{\omega T/2} \tag{4-257}$$

which is a digital LPF with a linear phase response, as illustrated in Figure 4-100. An important feature of this filter is that it has zero gain at the sampling frequency and at all harmonics thereof. As Eq. (4-242) or (4-254) shows, when the input and sampling frequencies are equal, the output of the sampler contains a dc term and all harmonics of the sampling frequency. Since the ZODH has zero gain at these frequencies, the unwanted harmonics are completely removed by the filter. This is one of the primary reasons for the widespread application of samplers in phase-locked loops. The ZODH has a phase lag that increases linearly with frequency. This negative phase shift can seriously degrade loop stability.

Whenever the only frequency-sensitive components in the PLL are the VCO and the sampler plus ZODH, the loop stability and frequency response are readily analyzed. When the loop is in frequency lock, the system can be represented as shown in the block diagram of Figure 4-101. The open-loop transfer function is

$$G(j\omega) = \frac{2}{T} \frac{K_v e^{-j\omega T/2}}{j\omega} \frac{\sin(\omega T/2)}{\omega T/2} \tag{4-258}$$

At the crossover frequency ω_c, the open-loop phase shift is

$$\phi = -\frac{\pi}{2} - \frac{\omega_c T}{2} \tag{4-259}$$

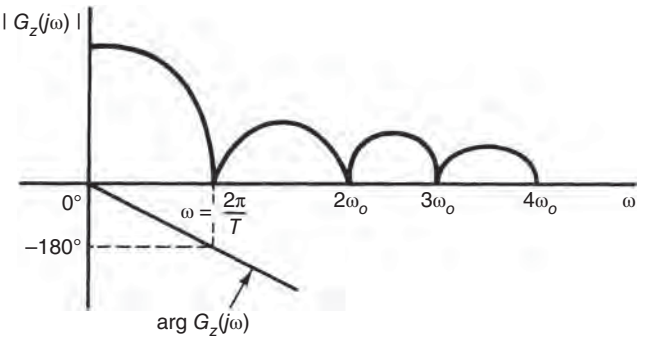


Figure 4-100 Transfer characteristic of the ZODH filter.

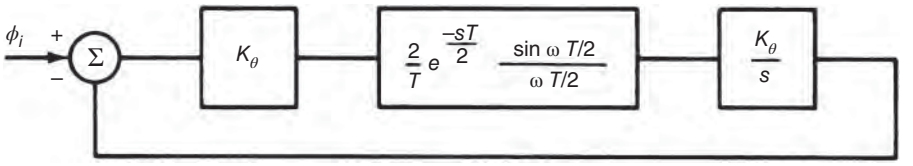


Figure 4-101 Block diagram of a PLL with a sample/hold comparator.

and the phase margin is

$$\phi_m = \pi + \phi = \frac{\pi}{2} - \frac{\omega_c T}{2} \tag{4-260}$$

Since the magnitude of the open-loop gain at ω_c is unity,

$$K_v \frac{\sin(\omega_c T/2)}{(\omega_c T/2)^2} = 1 \tag{4-261}$$

or

$$\begin{aligned} K_v &= \frac{(\omega_c T/2)^2}{\sin(\omega_c T/2)} = 1 \\ &= \frac{(\pi/2 - \phi_m)^2}{\sin(\pi/2 - \phi_m)} \end{aligned} \tag{4-262}$$

Equation (4-262) describes the relation between phase margin ϕ_m and loop gain K_v. The plot of K_v as a function of ϕ_m given in Figure 4-102 shows that for each value of ϕ_m, there is a single value of K_v. For a $K_v = (\pi/2)^2$, the phase margin is 0°. As K_v is decreased, the phase margin increases and reaches 90° for $K_v = 0$.

The effect on loop performance of changes in the sampling rate T can be determined in the same manner. Since at the crossover frequency ω_c the magnitude of the open-loop gain is unity,

$$K_v \frac{\sin(\omega_c T/2)}{(\omega_c T/2)^2} = 1 \tag{4-263}$$

If K_v remains constant and the sampling rate T is changed, ω_c must change such that $\omega_c T =$ constant. That is, if the sampling rate is decreased (T increases), the crossover frequency must decrease so that $\omega_c T$ remains constant. Therefore, changing the sampling rate of the system has no effect on the system phase margin or system stability; it affects only the loop bandwidth.

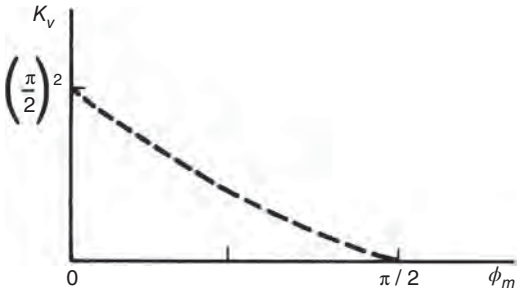


Figure 4-102 Plot of K_v as a function of ϕ_m.

Example Implementation

Calculate the value of K_v required for a 45° phase margin in a PLL whose open-loop transfer function is given by Eq. (4-258).

Solution. In order to have a 45° phase margin, the phase lag of the sample/hold comparator must be 45° at the crossover frequency. Therefore,

$$\frac{\omega_c T}{2} = \frac{\pi}{4} \tag{4-263}$$

and the crossover frequency must be

$$\omega_c = \frac{\pi}{2T} \tag{4-264}$$

Since the magnitude of the open-loop gain is unity at the crossover frequency, K_v is determined from

$$K_v \frac{\sin(\pi/4)}{(\pi/4)^2} = 1 \tag{4-265}$$

or

$$K_v \left(\frac{\pi}{4}\right)^2 \sqrt{2} \tag{4-266}$$

The sample/hold comparator, however, has a somewhat limited frequency range. In frequency synthesizer applications, it is not very likely that it will be used below a few hundred hertz, and the upper limit is determined by the speed of the following circuit and the crosstalk. Crosstalk depends on the isolation of the CMOS switch.

Let us take a look at a practical circuit using the sample/hold comparator. It is typically used in a cascaded form, which means that there are two samplers. The reason for this is the fact that one gets better reference suppression. Figure 4-103 shows a dual sample/hold comparator with the additional filtering circuits. The 10 kHz output from the divider, depending on the division ratio, is 200–500 ns wide, and a special circuit acts as a pulse stretcher to increase the width of these pulses to 2 μs.

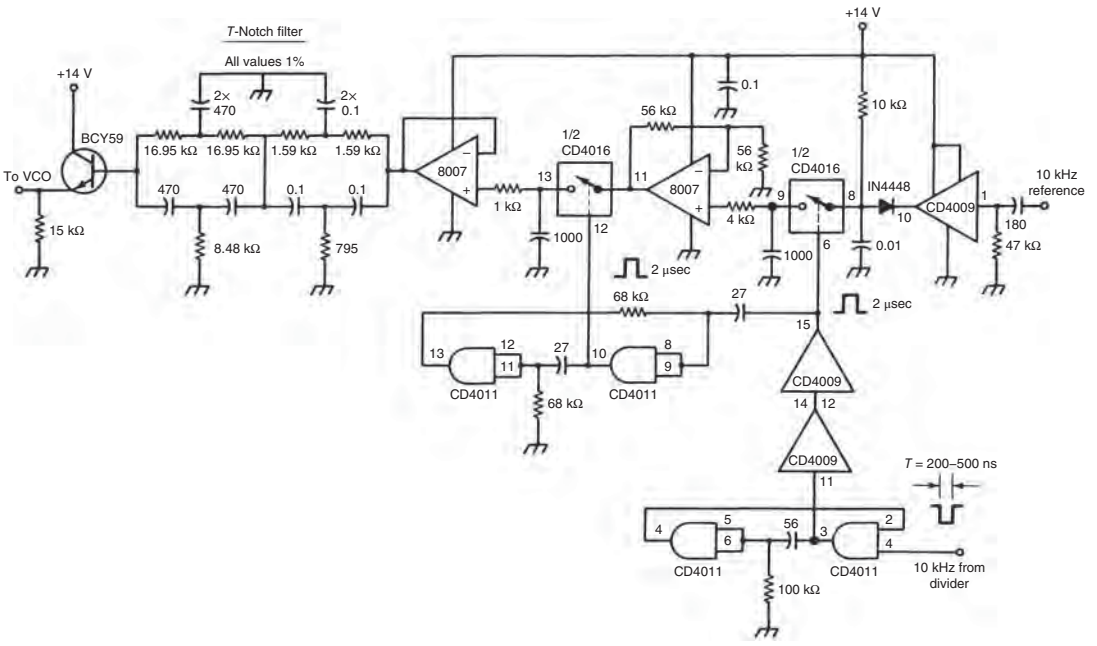


Figure 4-103 Dual sample/hold comparator with additional filtering.

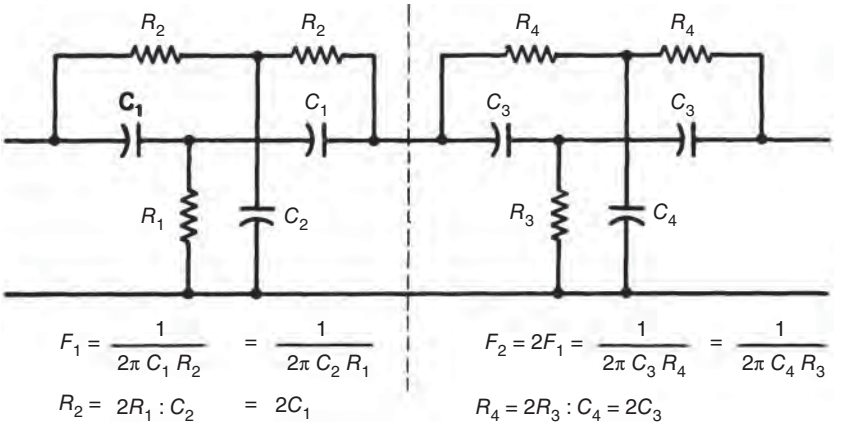


Figure 4-104 T-notch filter with design equations.

The two CD4009s decouple the circuit. Two CD4016s are being used as CMOS switches. The first CD4009 generates the ramp, and the two 8007 operational amplifiers again provide the necessary decoupling and high input impedances.

In the output of the second 8007, we have a *T-notch filter*, which is a minimal phase shift filter with about 40 dB of suppression of the reference. In this particular circuit two T-notch filters are being used to suppress the fundamental and first harmonic frequency. Later in this chapter it will be shown that at times the active second-order LPF is a good replacement for the T-notch filter because it attenuates all harmonics rather than two discrete frequencies and requires fewer low-tolerance components.

Figure 4-104 shows the T-notch filter with the design formulas.

The highest recommended frequency of operation for the phase/frequency comparator is approximately 5 kHz. At frequencies above this, the CMOS switches are not fast enough. The high impedance and parasitic capacitance produce crosstalk, and only 60 dB of attenuation is possible.

While sample/hold comparators will typically operate from 12 to 24 V, the minimum crosstalk voltage that determines the resolution and the reference suppression is about 10 μV. The attenuation possible with the sample/hold comparator is therefore about 110 dB. This is a highly theoretical value and in practice depends on the relationship of reference frequency and desired cutoff frequency. In many cases, the loop bandwidth is set to one-half of the reference frequency, and then delays and stray effects become very critical.

4-7-4 Edge-Triggered JK Master/Slave Flip-Flops

The fundamental idea of the sequential phase comparator we will be dealing with is that there are two outputs available, one to charge and one to discharge a capacitor. Output 1 then is high if the signal 1 frequency is greater than the signal 2 frequency; or if the two frequencies are equal, if signal 1 leads signal 2 in phase. Output 2 is high if the frequency of signal 2 is greater than that of signal 1, or if the signal frequencies are the same and signal 2 leads signal 1 in phase.

Figure 4-105 shows the minimum configuration to build such a phase comparator. It can be operated from -2π to $+2\pi$, and an active amplifier is recommended as a charge pump. The Q output of the JK master/slave flip-flop is set to 1 by the negative edge of the signal 1, while the negative edge of the signal 2 resets it to zero. Therefore, the output Q is the complement of Q. The output voltage $\overline{V}$ is defined as the weighted duty cycle of Q and $\overline{Q}$. This means that a positive contribution is made when $Q = 1$ and a negative contribution (discharge) is made when $Q = 0$. The averaging and filtering of the unwanted ac component are done by the following integrator. The integrator circuit then is called a *charge pump*, as the loop capacitor is being charged and discharged depending on whether Q is high or low.

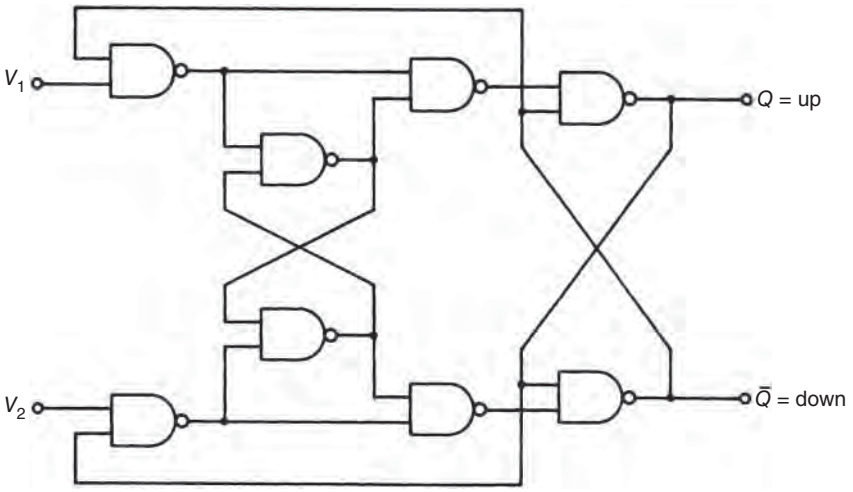


Figure 4-105 Edge-triggered JK master/slave flip-flop.

If the system using the JK flip-flop is not in lock and there is a large difference between frequencies Fl and F2 at the input, the output is not going to be zero but will be positive or negative relative to one-half the supply voltage. This is an advantage and indicates that this system is frequency sensitive. We therefore call it a *phase/frequency comparator* because of its capability to detect both phase and frequency offsets. In its locking performance and pull-in performance, it is similar to the exclusive-OR gate.

For better understanding, let us look at a few cases where the system is in lock. It should be noted that whereas the exclusive-OR gate was sensitive to the duty cycle of the input signals, the JK flip-flop responds only to the edges, and therefore the phase/frequency comparator can be used for unsymmetrical waveforms. Let us assume first that the input signals 1 and 2 have the same frequency. Figure 4-106 shows what happens if the phase error is about 0, π, and 2π. In those cases, the duty cycle at the output is about 0%, 50%, or 100%, respectively. The narrow output pulses may cause spikes on the power supply line and lines in the vicinity, and certain precautions have to be taken to filter them.

The output voltage $\overline{V}$ is the average of the signal Q and is a linear function of the phase error.

Now let us take a look at several cases where the system is not in lock. Figure 4-107 shows the case where frequency 1 is substantially higher than frequency 2.

As a result, the output duty cycle is close to 100%, and the VCO frequency is being pulled up to higher frequencies. If the frequency at input 2 is much higher than that at input 1, the opposite is true. This proves that this device is sensitive to frequency changes.

In cases where both frequencies are about the same, as shown in Figure 4-108, the crossover area is not clearly defined. The first picture shows the case where frequency 2 is 10% higher than frequency 1, and the duty cycle is changing periodically between 0% and 100%. Therefore, the ac voltages look like a sawtooth, with a rate equal to the difference of both frequencies. The same holds true if the two inputs are reversed. In the case where both frequencies are identical, the JK flip-flop behaves the same way as an exclusive-OR gate. From this discussion it can be concluded that, while this phase/frequency comparator was included to explain how it works, it is not a very desirable device because of the uncertainty of its behavior close to lock.

4-7-5 Digital Tri-State Comparators

The digital tri-state phase/frequency comparator is probably the most universally used and most important next to the sample/hold comparator. Although the ring and exclusive-OR gate have some applications, the tri-state phase/frequency comparator can be used widely. Even in cases where a sample/hold comparator theoretically could be used, it may be inferior as far as reference attenuation or noise is concerned, but it is generally well behaved.

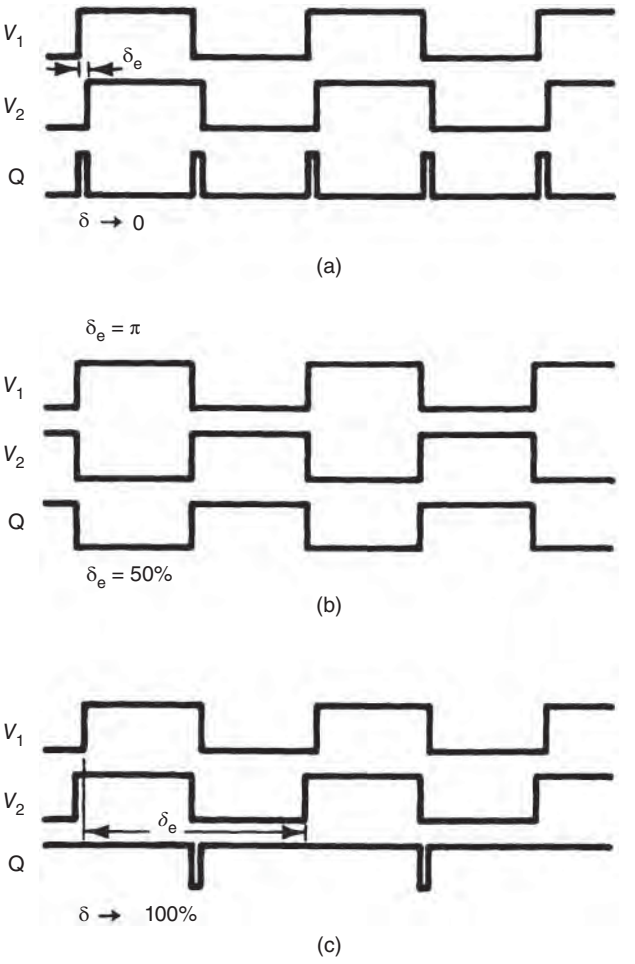


Figure 4-106 Performance of the JK phase/frequency comparator for different input signals.

Unfortunately, the tri-state system is complex and shows a number of unusual phenomena. Such a digital tri-state comparator is shown in Figure 4-109 using two *D* flip-flops and a NAND gate. The Q_2 output signal is filtered with the LPF. The operation of this logic circuit is readily analyzed using the state transition diagram shown in Figure 4-110. The *D* flip-flop outputs go high on the leading edge of their respective clock inputs and remain high until they are reset. The rest signal occurs when both inputs are high. When both signals are in phase and of the same frequency, both outputs will remain low, and no signal will be applied to the operational amplifier. When the two signal frequencies are the same, the dc output voltage transfer characteristic will be as shown in Figure 4-111. If the two signal frequencies are not the same, the output voltage will depend on both the relative frequency difference and the phase difference.

The timing diagram of Figure 4-112 illustrates the case in which $f_2 = 3f_1$. In part (a) of the figure, the leading edge of f_1 occurs just after that of f_2, so that Q_2 is high 50% of the time, and the average value of the PD output is 50%. In part (b) of the figure, the leading edge of f_1 occurs just before that of f_2, so Q_2 is high almost all the time and the average output voltage is approximately *V*. The output voltage averaged over all phase differences is then 67% for $f_2 = 3f_1$. In general, it can be said that the average output (averaged over all phase differences) is given by

$$V_{\text{ave}} = 1 - \frac{f_1}{f_2} V \tag{4-267}$$

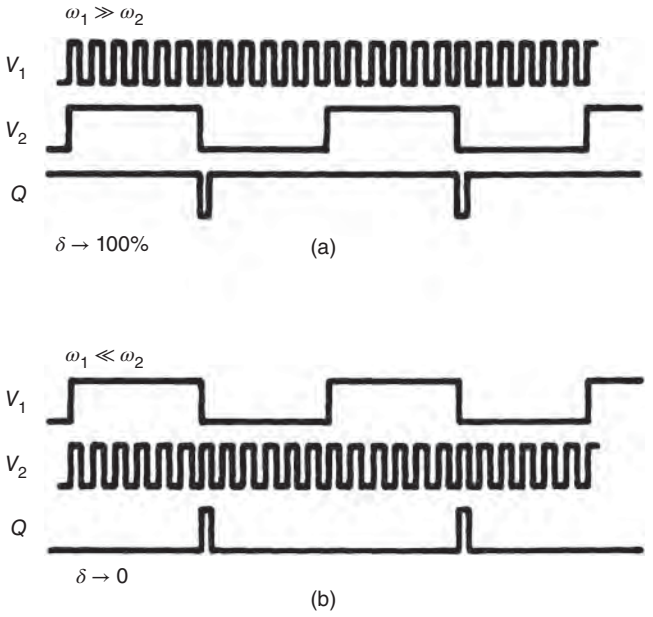


Figure 4-107 Phase detector output for two input frequencies that are substantially different.

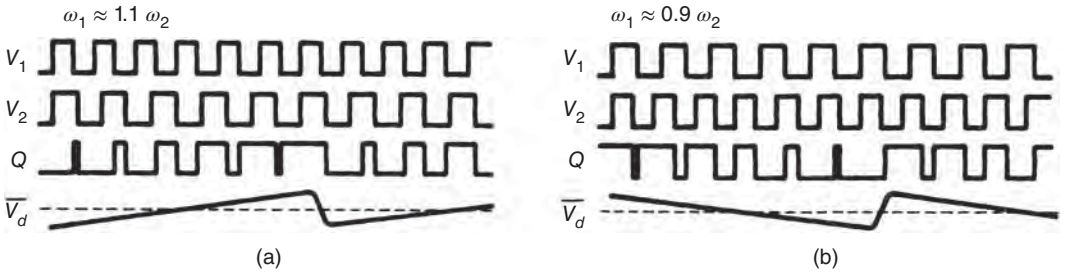


Figure 4-108 Performance of the phase detector for small frequency errors.

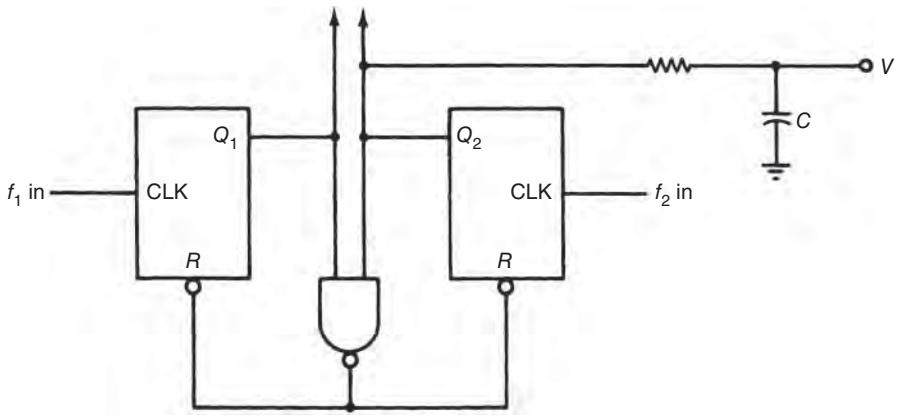


Figure 4-109 Phase detector with two *D* flip-flops and an NAND gate. This type of phase detector will be called a tri-state comparator.

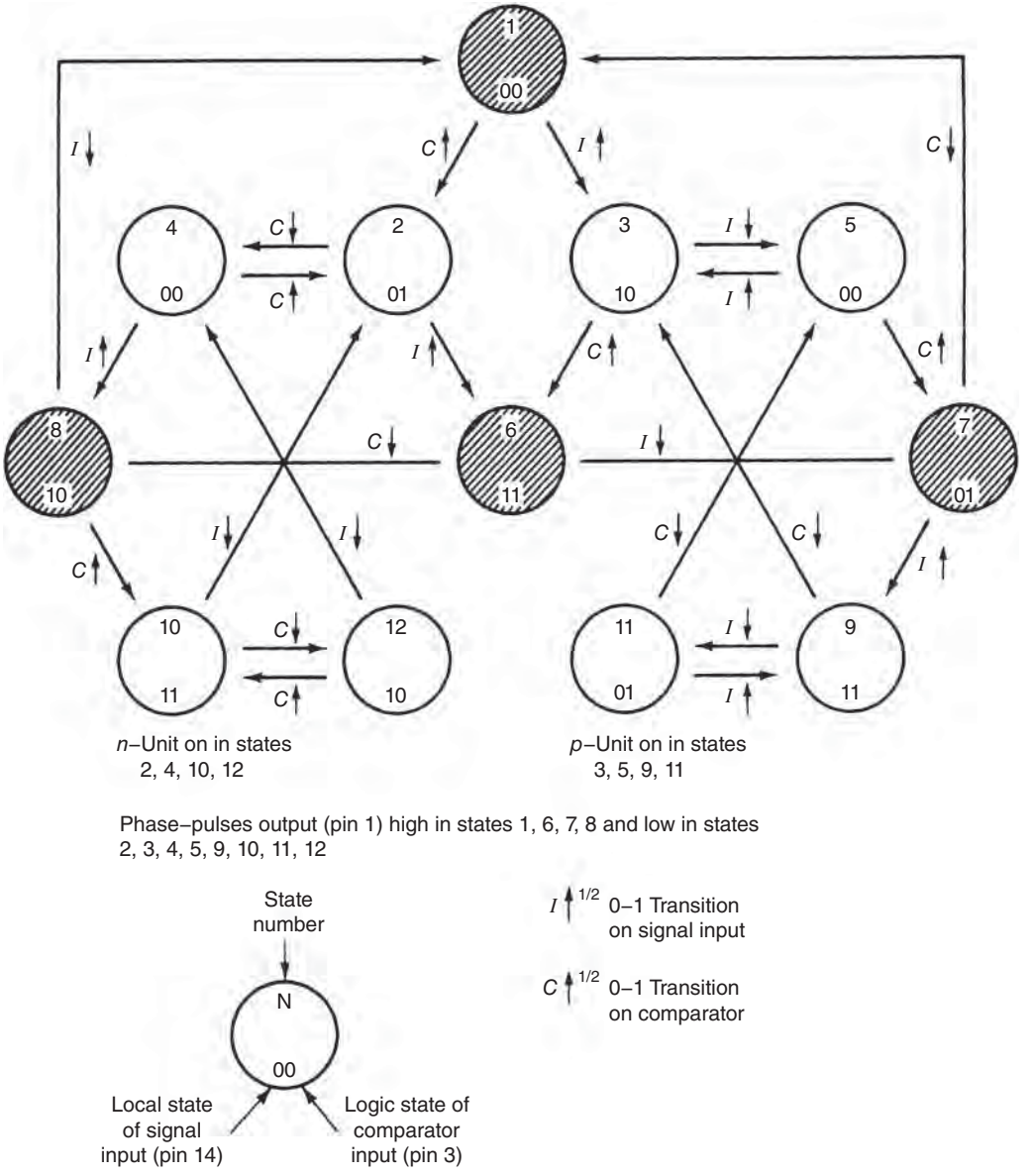


Figure 4-110 Logic diagram of the tri-state detector.

provided that f_2 is greater than f_1. This expression is plotted in Figure 4-113 together with the cases in which f_1 is greater than f_2.

The digital network used in this realization is only one of a large number of logic circuits that could be used. Many IC manufacturers produce a quad-*D* circuit, which functions much like the dual *D* flip-flop; the main difference is that when the frequency of one signal is more than twice that of the other signal, the corresponding output will be high all of the time. Therefore, a larger voltage is applied to the VCO and the loop response is faster. An example of a quad-*D* circuit is shown in Figure 4-114.

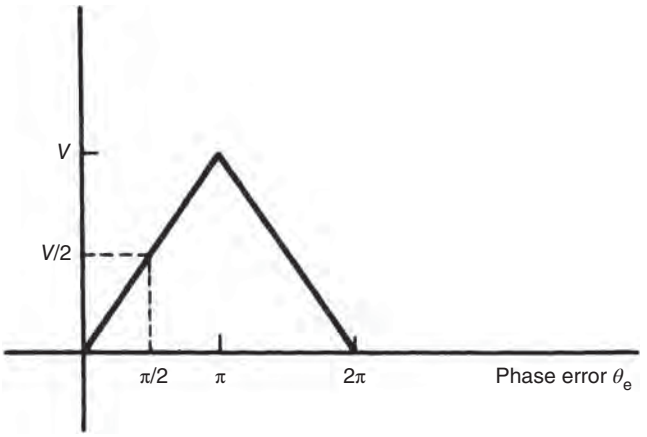


Figure 4-111 Transfer characteristic of the tri-state phase/frequency comparator.

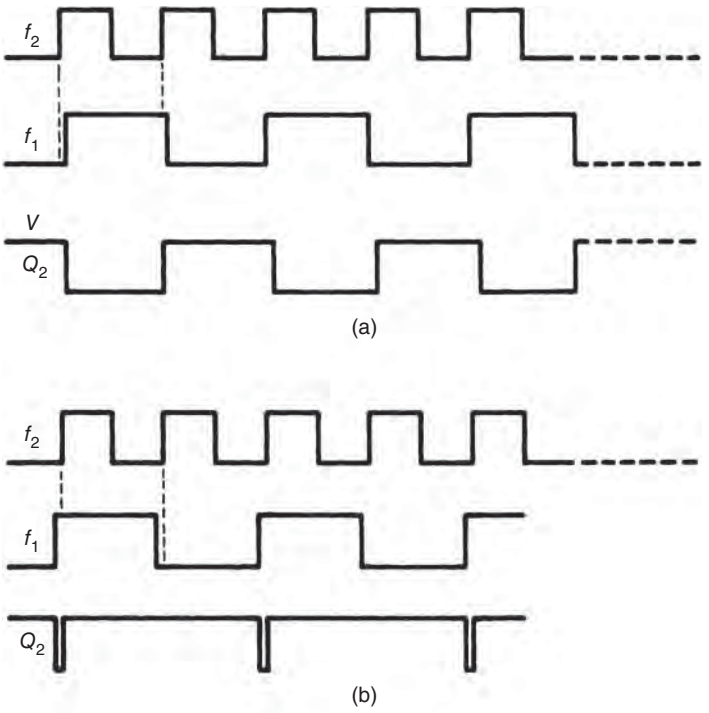


Figure 4-112 Output waveforms of the tri-state frequency comparators for different input frequencies.

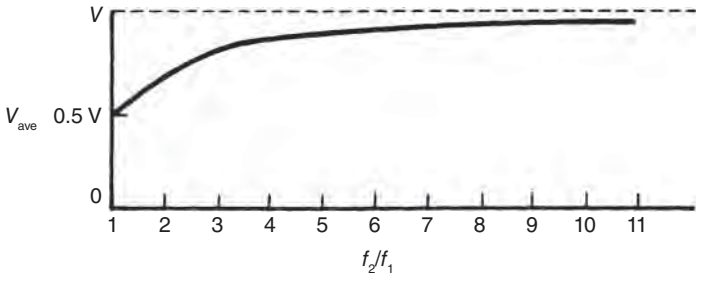


Figure 4-113 Average output voltage as a function of frequency ratio.

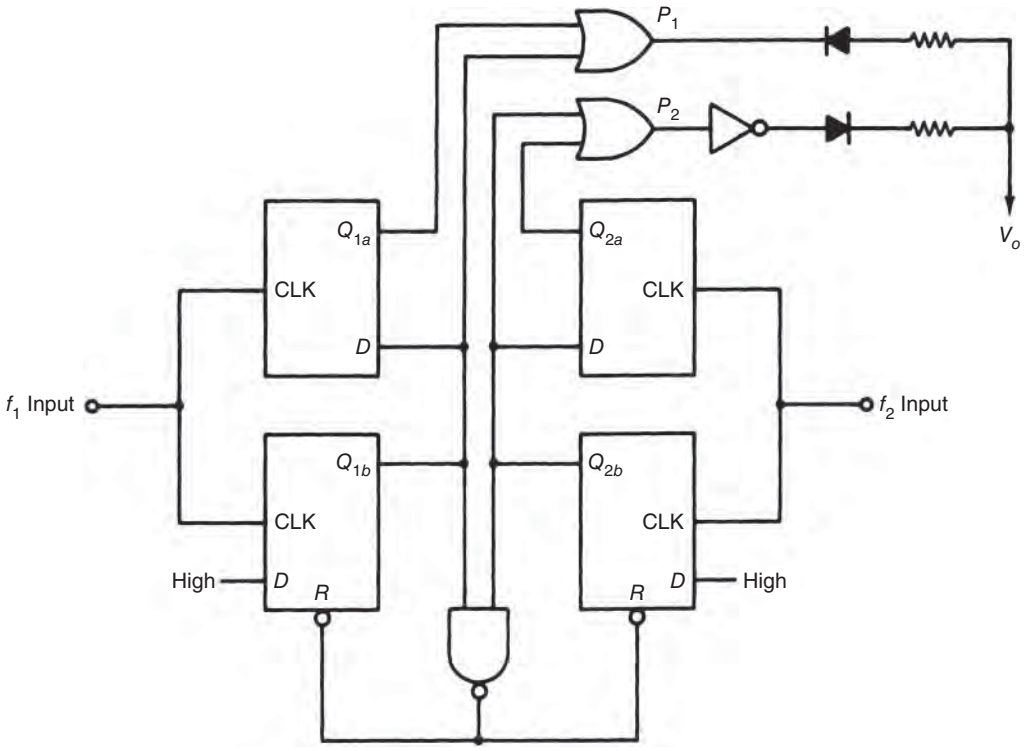


Figure 4-114 Example of a quad-*D* circuit.

The CD4046 PLL IC, a popular digital tri-state phase/frequency comparator, is shown in Figure 4-115. It contains an additional phase comparator, an exclusive-OR gate that can be used as a lock indicator. In addition, two field-effect transistors are used to sum the two outputs. A slightly faster version in transistor–transistor logic (TTL) techniques is the Motorola MC4044.

The fastest version in emitter-coupled logic (ECL) is the MC12040, also made by Motorola, shown in Figure 4-116. Sometimes it is convenient to build the phase/frequency comparator in discrete technique to add additional features. Figure 4-117 shows an example.

This particular tri-state phase/frequency comparator has a peculiarity that was first mentioned by Egan and Clark [84]. When actually building a phase-locked loop with this phase/frequency comparator or the CD4046 type by going through the normal mathematical design routine, it will become apparent that the expected performance and the actual results are not the same, notably:

- The reference suppression will be better than expected.
- The phase error or tracking will be worse than expected.
- The phase margin will differ, and the system may not lock despite the fact that the calculation is correct.

The reason for this is due to two effects:

(1) The flip-flops are not absolutely alike, and as a result of this, the output in the crossover region is not zero.
(2) If there is very little or no correction voltage required, the gain of the phase detector will drop substantially.

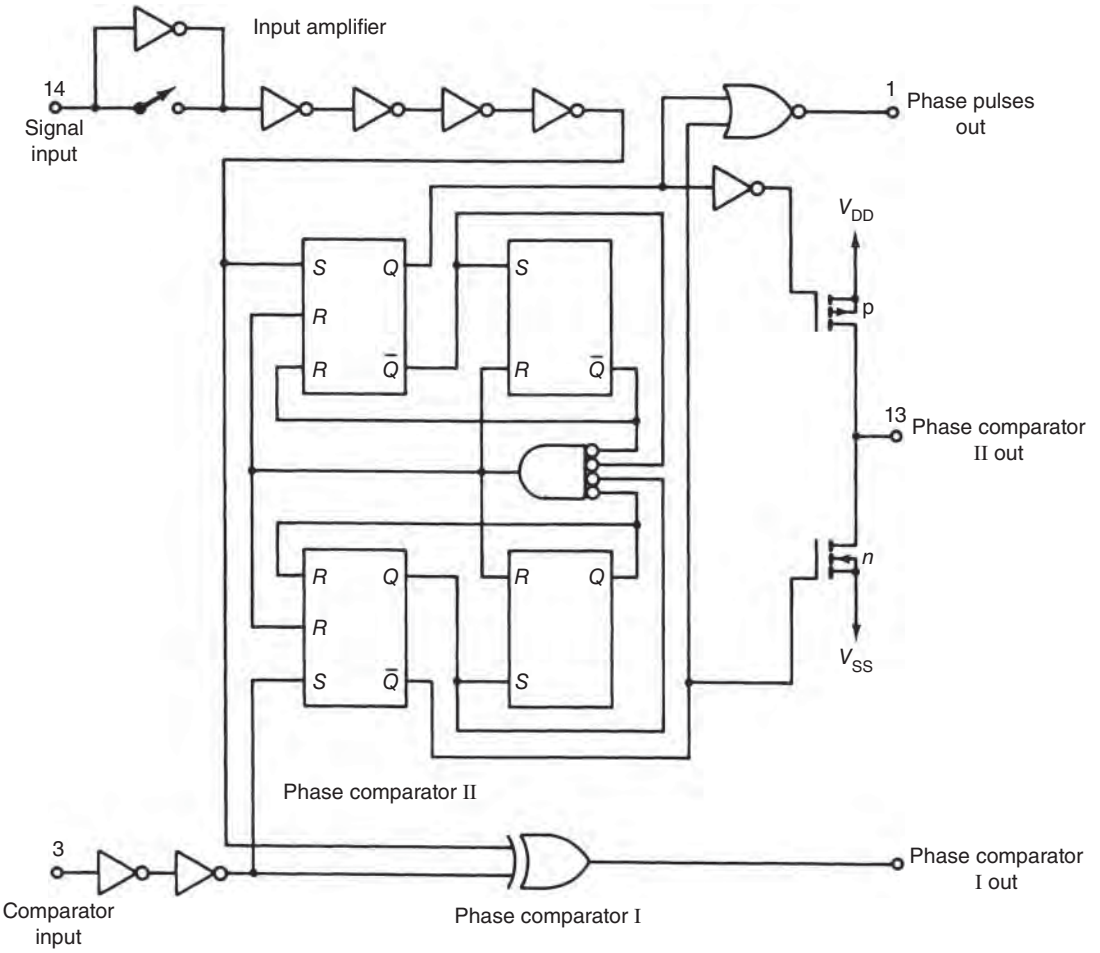


Figure 4-115 Block diagram of CD4046 phase/frequency comparator.

Let us assume the ideal situation where the output of the phase/frequency comparator feeding the charge pump does not have to correct any error, the system is drift free, and there are no leakage currents. The holding capacitor of the charge pump would maintain constant voltage, and, as there is no drift, no correction voltage is necessary.

The flip-flops, however, introduce a certain amount of jitter, and a certain amount of jitter is also introduced by the frequency dividers, both the reference divider and the programmable divider. This jitter results in an uncertainty regarding the zero crossings, and extremely narrow pulses will appear at the output of the summation amplifier used in the CD4046.

Under the ideal assumption that there are no corrections required and those pulses would not exist, the reference suppression would be infinite, as there is no output and, therefore, the reference suppression, disregarding the effect of the loop filter, depends only on how well this condition is met.

The change of gain seems somewhat surprising, but as we think of it, if there is no correction and no update, there is also no gain. It is impossible to meet this condition, which is fortunate, but with regard to the temperature stability and aging effect of some devices, we may have some difficulties as far as predicting the actual performance.

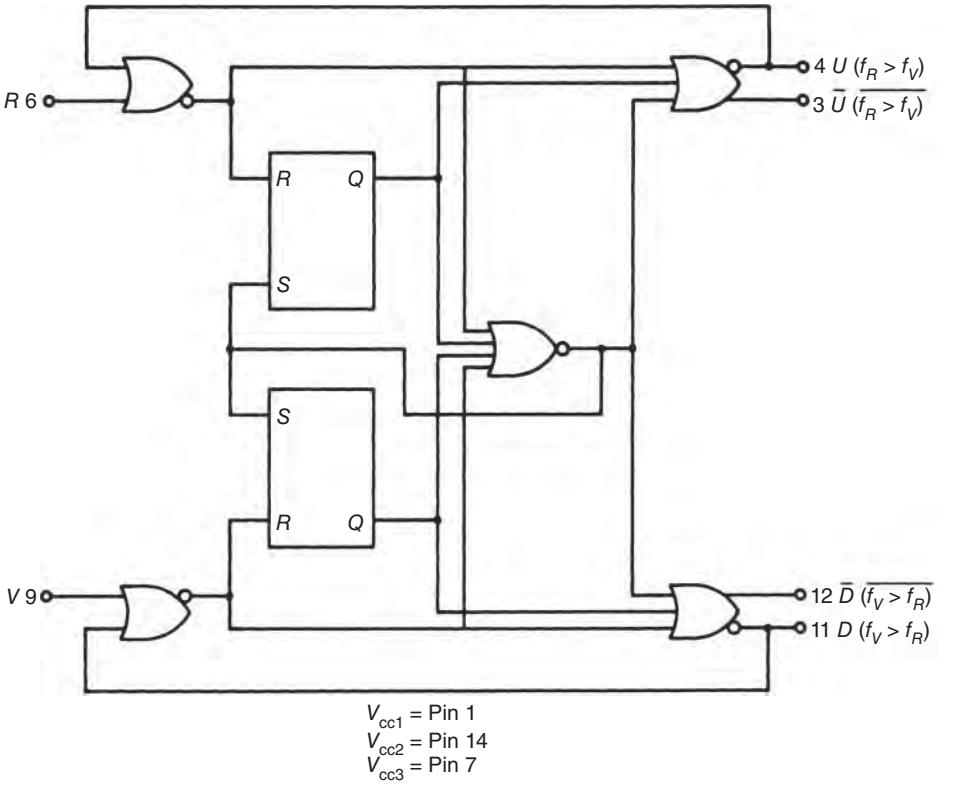


Figure 4-116 Block diagram of Motorola MC12040 phase/frequency comparator.

There are several remedies to this problem. A simple version is to introduce a controlled amount of leakage. While the electrolytic capacitor required in the charge pump will have a leakage current, it is better to use a leakage current that is independent of temperature and aging. This can be accomplished by putting a 1-MΩ resistor from the output of the CD4046 to ground. The phase/frequency comparator then has to deliver an output current, and this output current is determined by a resistor that can be independent of temperature and other effects. As a result of this, the duty cycle of the output pulses of the phase/frequency comparator will change and the pulses will become wider. As these pulses contain more energy, the reference suppression will suffer.

It is theoretically possible to put one side of the 1 MΩ resistor, instead of to ground, to the wiper of a potentiometer and set the voltage in such a manner that this offset is compensated, but again, because the phase will shift theoretically, one has to adjust the potentiometer according to the actual phase error. This is not a very convenient arrangement.

A somewhat better method was proposed by Fairchild, but the hardware was never realized. It was proposed to insert a gate in one of the output arms of the phase/frequency comparator, before the signal is fed to the summation amplifier, and a periodic current disturbance is introduced. This disturbance has the same rate as the reference frequency and is of extremely small duration, so that the output contains only fairly high harmonics of reference, which is easily filtered as it contains very little energy. This periodic disturbance offsets the output of the phase/frequency comparator and therefore has an effect similar to that of a leakage resistor. The advantage of this method, however,

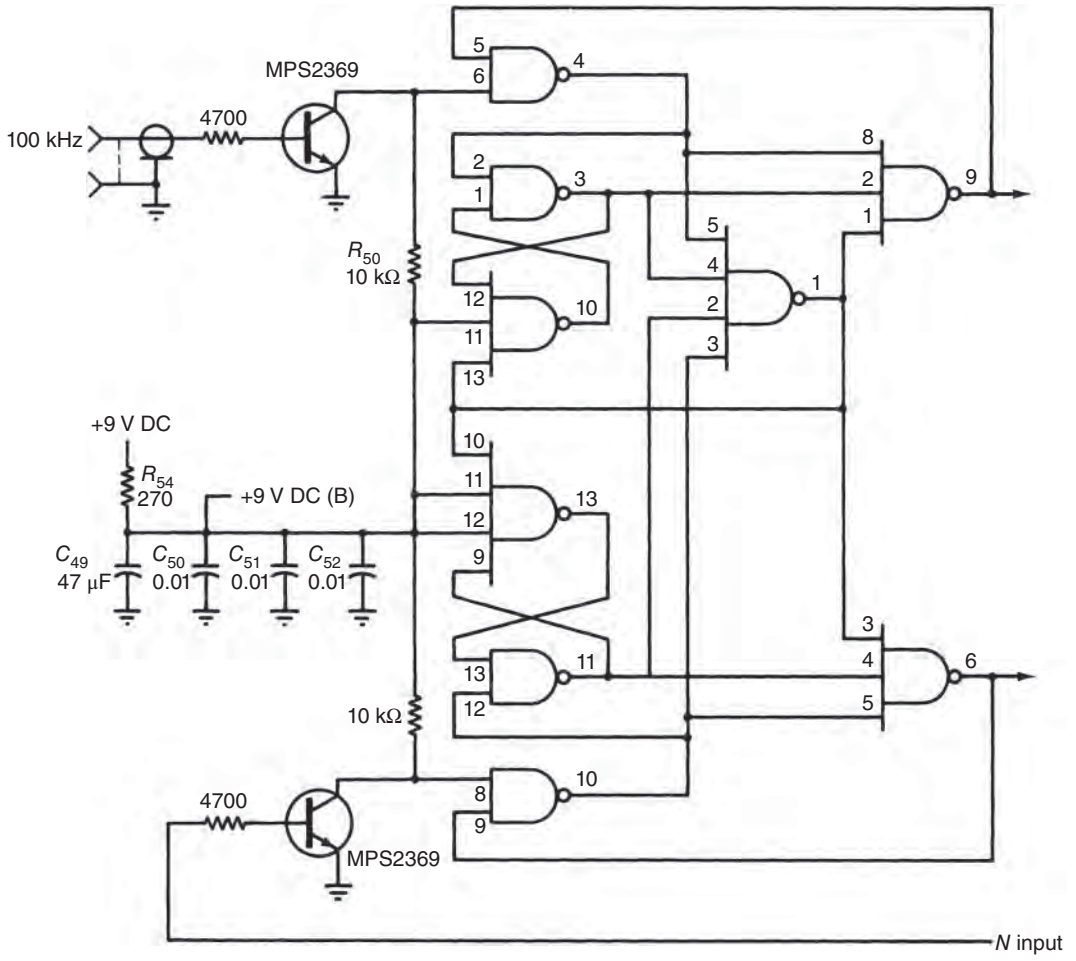


Figure 4-117 Possible version of tri-state phase/frequency comparator.

is that this is done at a fairly high frequency and does not introduce low-frequency noise generated by the 1 MΩ resistor.

Figure 4-118 shows the circuit that accomplishes this, and Figure 4-119 shows the effect on the output pulses. The charge pump output exhibits a short negative-going pulse followed immediately by a short positive-going pulse. This can also be called an antibacklash feature, and it prevents operating in the dead zone. This zone is not really a dead zone because of the leakage currents in the tuning diode. The duration and proximity of these pulses are such that they cause no net change to the charge of the integrator. Figure 4-120 shows the response of a phase/frequency detector near loop lock, including the dead zone; this may not be true for ECL.

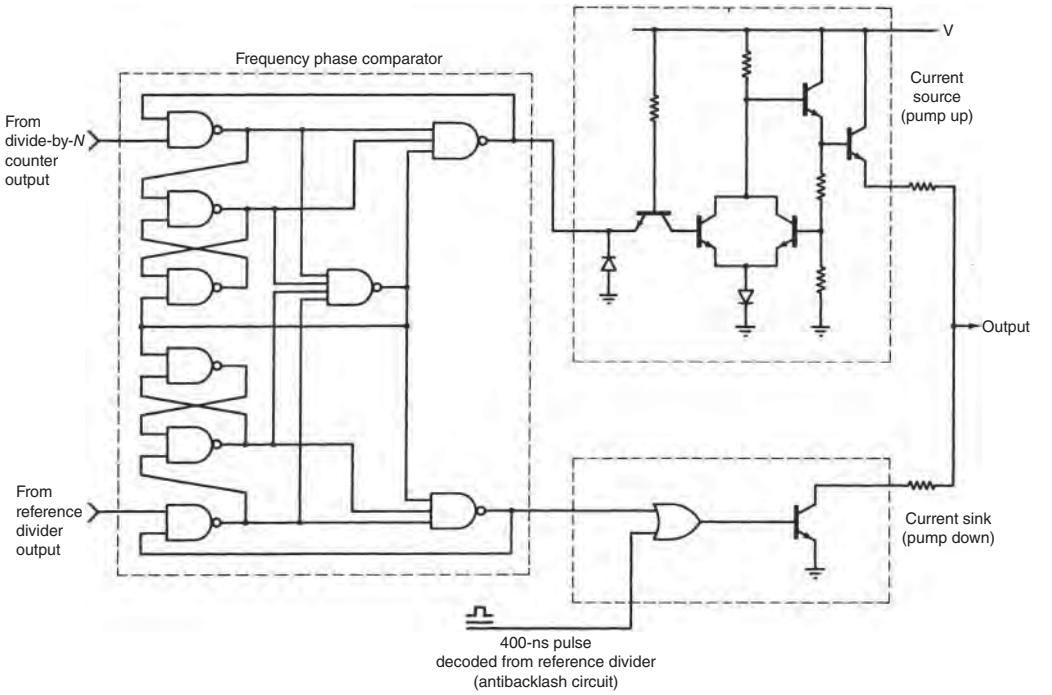


Figure 4-118 Tri-state detector with antibacklash circuit included.

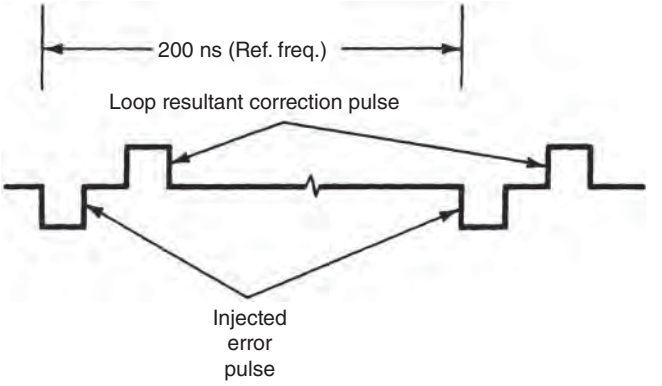


Figure 4-119 Output of frequency/phase detector with antibacklash circuit.

4-8 WIDEBAND HIGH-GAIN AMPLIFIERS

4-8-1 Summation Amplifiers

Depending on the application, we have two types of high-gain amplifiers that require a fairly high bandwidth.

(1) Operational amplifiers for the loop filter.
(2) Wideband amplifiers that either act as isolation amplifiers or transform sine-wave voltages into square-wave voltages (differential limiters), or power amplifiers that raise the output level of a synthesizer. Although they belong in the category of isolation amplifiers, they also require some different considerations.

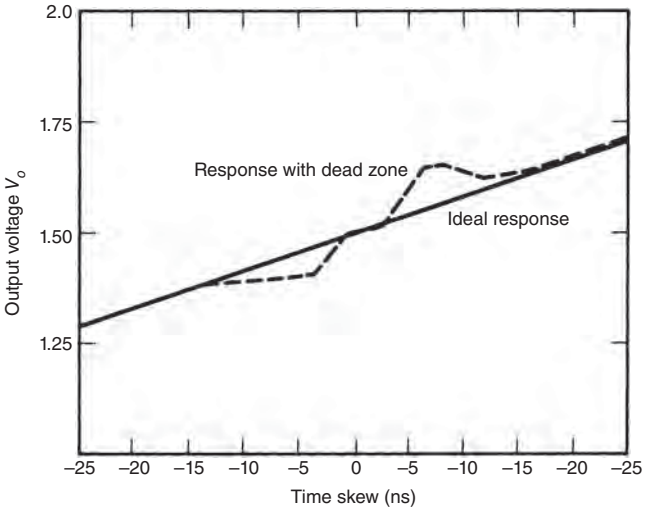


Figure 4-120 Response of frequency/phase detector near loop lock resulting in a dead zone.

Let us start with the operational amplifiers required for the loop filters. Although we will be dealing with loop filters, specifically active loop filters, in great detail, we should touch on the requirement for operational amplifiers. As in some cases the reference frequency will be as high as several megahertz, in order to maintain a wide loop bandwidth, the operational amplifier has to be able to track the frequencies involved. The slew rate of the operational amplifier, which determines how many volts per microsecond the operational amplifier can follow, is one figure of merit that has to be taken into consideration, and it is interesting that most operational amplifiers that do not have fixed internal frequency compensation are fairly poor in slew rate. In addition, the more familiar cutoff frequency of the operational amplifier indicates the 3 dB drop in gain in the open-loop configuration. The open-loop configuration, however, is not used, as the loop filter will reduce the passband, and there are only a few cases in which the input frequency would come close to the cutoff frequency of the operational amplifier. As operational amplifiers are introduced very frequently, it is somewhat dangerous to indicate a particular type. However, it was found that the CA3160 is a good choice for low frequencies (CA3130, CA3100).

The tri-state phase/frequency comparator has two outputs that are being fed together in a circuit that we call a summation amplifier. The high and low pulses generated by the digital portion are being fed simultaneously to two ports, and the amplifier then has to combine the two pulses into a single output. The simplest way of accomplishing this it to take an operational amplifier in which the two inputs are connected to the inverting and noninverting input and the biasing is provided with identical resistors to avoid any offset problems. Many application reports, such as the Motorola MC145156, recommend this circuit.

The drawback is that, as the pulses become faster in frequency, the operational amplifier will be unable to follow, and a discrete amplifier has to be built. There are several choices for discrete loop amplifiers, whose main purposes are as follows:

(1) To be able to follow the input pulses up to several hundred kilohertz or even several megahertz (good choices include the CA3100, 9906, and 9909).
(2) To have very little or no dc drift.
(3) To not introduce any significant noise.
(4) To be as symmetrical as possible and therefore to avoid any leakage of reference at the output.
(5) To avoid a dead zone (the dead zone was mentioned previously).

Figure 4-121 shows a dc amplifier that takes the two outputs from the phase/frequency comparator type 4044, made by Motorola, and then operates into the loop filter. This is a fairly complex arrangement, and Figure 4-122

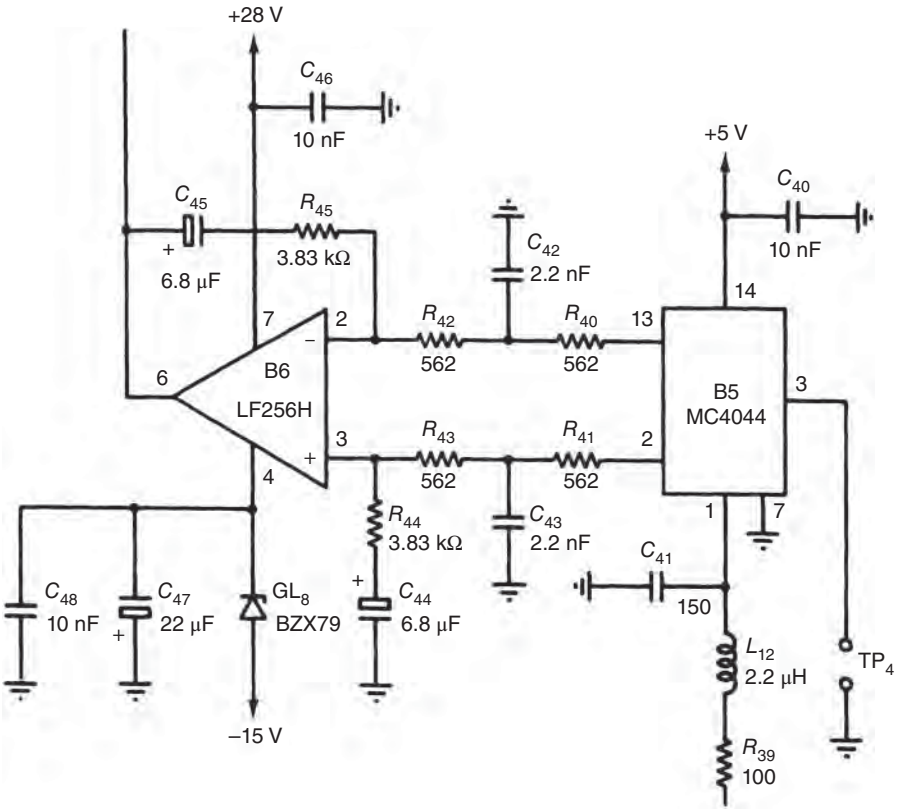


Figure 4-121 Schematic of the phase/frequency comparator MC4344 and an active loop filter using both inverting and noninverting input for stabilization. The first RC network is for transient suppression.

shows a circuit with basically the same performance that operates from an ECL phase/frequency comparator, which by definition has less dc output voltage. Figure 4-123 shows a phase/frequency comparator with the discrete operational amplifier containing several diodes for temperature compensation, as well as voltage shifts.

When analyzing operational amplifiers, it becomes apparent that those having very little output saturation voltage (i.e., CMOS outputs) cannot tolerate a high supply voltage. The discrete amplifier can be operated up to 30–40 V.

It was indicated, however, that most tuning diodes become noisy, and the operating voltage should be restricted to less than 30 V. In addition, when using such a high voltage, one will find that the voltage gain of the diode becomes so small that the loop gain has to be adjusted to avoid sluggish performance at the top of the band.

Several combinations of these circuits are possible, and depending on the transistors or new integrated circuits, these loop amplifiers may change from time to time. The additional dc gain has to be taken into consideration as the simple amplifier that is used in monolithic devices, such as the CD4046, has unity gain, and the more complex circuits, such as those earlier, have gain that can be adjusted by selecting component values. In the case of the temperature-compensated amplifier, the two resistors in series with the emitters determine the open-loop gain. In order to provide sufficient frequency response, very fast switching transistors should be used and matched where possible.

We will now take a look at RF applications, the first one being the requirement to drive frequency dividers from a sine-wave source.

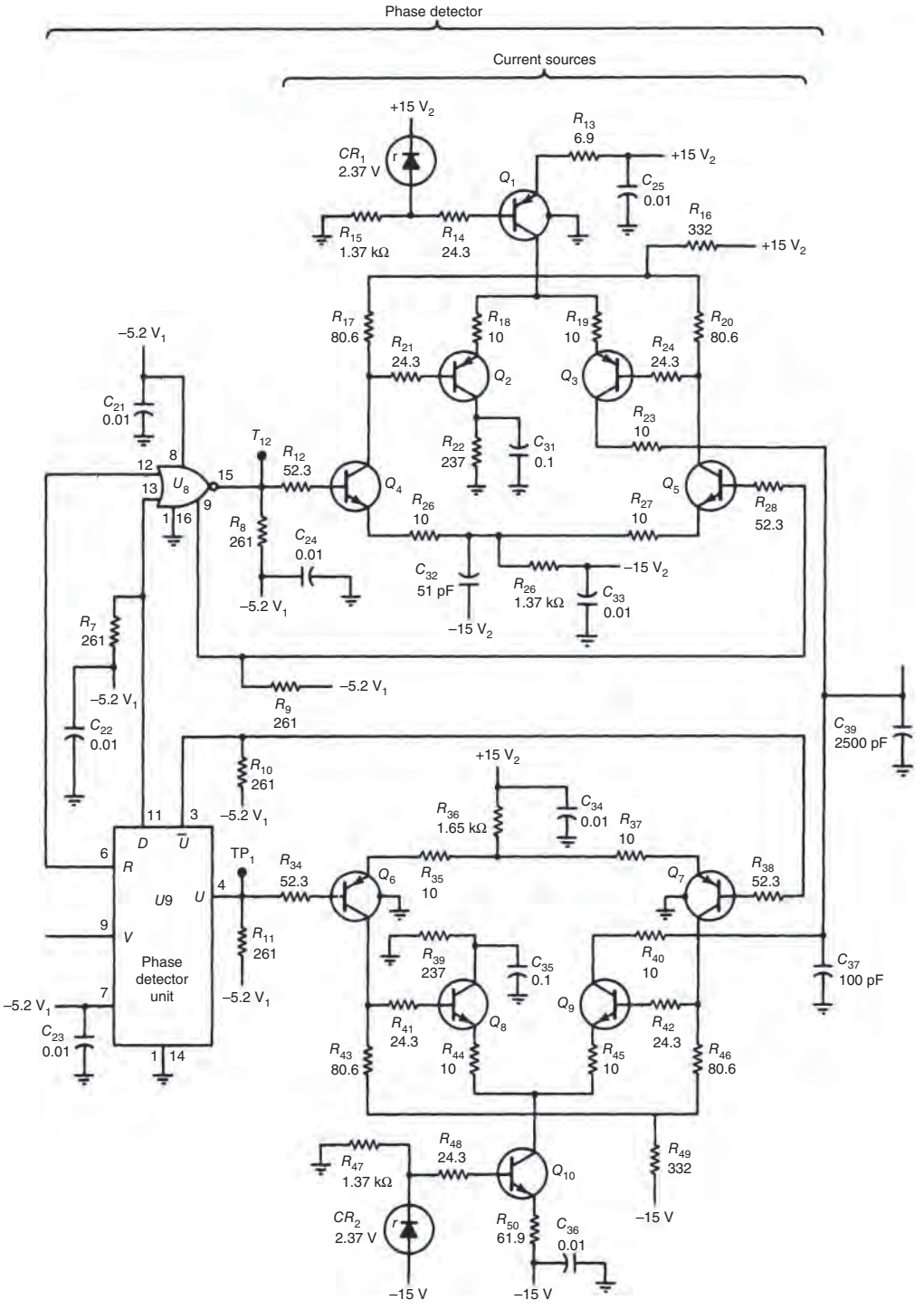


Figure 4-122 Phase/frequency comparator and discrete summation amplifier for low-noise operation. The loop filter is not shown.

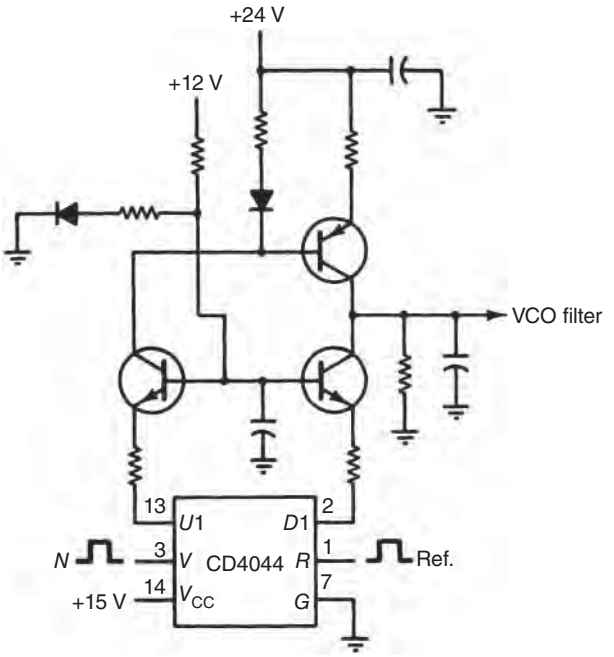


Figure 4-123 Discrete summation amplifier recommended for use with the CD4044 up to 1 MHz.

4-8-2 Differential Limiters

The easiest way to convert a sine wave into a square wave is to use an integrated circuit called a *line receiver*. A line receiver is an amplifier, practically always a differential limiter, which converts a sine wave into an ECL- to TTL-compatible waveform. Integrated TTL line receivers are relatively slow (about 5 MHz or so), and it is common practice to build a discrete line receiver using two PNP transistors, as shown in Figure 4-124. The gain of such a device depends on the ratio of collector resistor to emitter differential resistance (RD = 28 mV/I_e). For a current of 5 mA, this RD is about 5 Ω, and if a 500 Ω collector resistor is used, the gain is 100 or 40 dB. Depending on the collector resistor and the collector voltage, these devices can be made to work for ECL, TTL, or 12 V CMOS logic. The differential limiter should be made as fast as possible, which means that the rise time and fall time should be extremely short. It is important to minimize hysteresis or zero-crossing errors. It has been shown several times that if a poorly designed differential limiter follows a low-noise frequency standard, the introduction of noise by the slow limiter determines the system's noise rather than the crystal oscillator. Modern integrated circuits, such as the Plessey swallow counters, can be driven with sine-wave inputs and have open collector outputs. The open collector outputs allow the use of the necessary resistor and voltage from the power supply to adapt to the following circuits, and therefore no line receivers are required. The line receivers are absolutely necessary for TTL and CMOS logic.

In most cases, however, we do not want to limit the output, but rather isolate output from input without distorting the transferred waveform output of a required output power, so that reverse feedback and isolation have to be considered. These isolation amplifiers are described next.

4-8-3 Isolation Amplifiers

The output from the VCO is fed into an amplifier that has to drive the frequency divider chain, and an additional output provides the desired frequency $N \times f_{\text{ref}}$.

There are several ways to accomplish this task. Obviously, it is important to use a low-noise amplifier, which suggests the use of a dual-gate MOSFET amplifier, which, driven by the VCO, is excellent for low noise and high

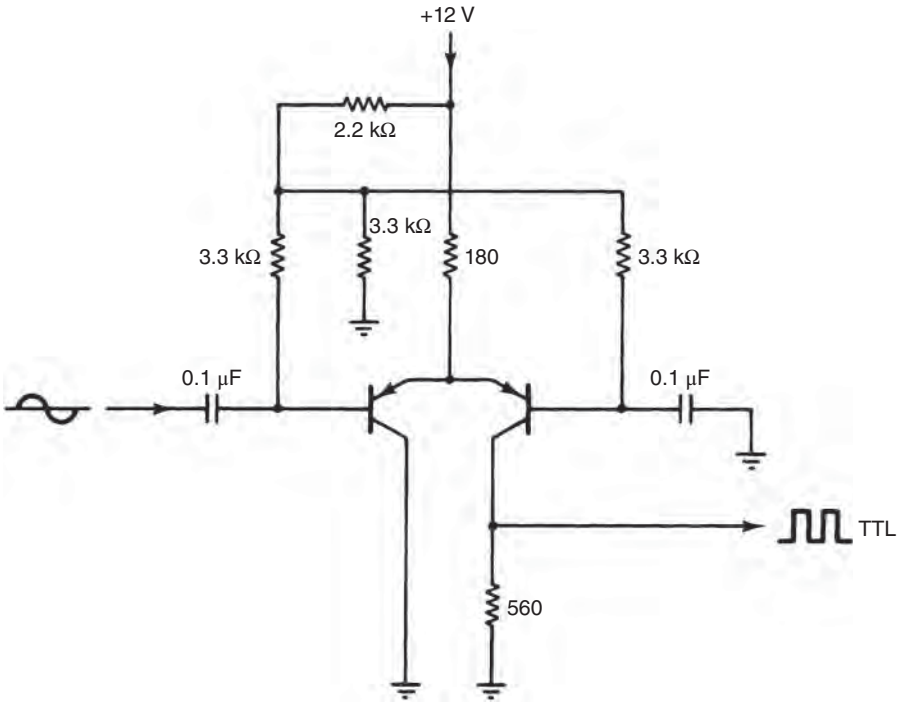


Figure 4-124 Schematic of a differential amplifier operating up to 10 MHz.

reverse isolation. Because of the high-impedance nature of these devices, they will work well only in conjunction with an impedance transformation circuit as shown in Figure 4-125. In the frequency range 30–120 MHz, this circuit has enough reverse isolation (at least 60 dB) and is capable of driving stages such as high-level mixers requiring +23 dBm of drive. For wider frequency ranges, Figure 4-126 shows a multistage amplifier that will meet this requirement.

Another solution is offered in Figure 4-127. It shows the combination of a discrete transistor type 2N5179 driving a power splitter, sometimes called a *hybrid coupler*, and a wideband monolithic amplifier type 733, which is manufactured by several companies, including Motorola and Fairchild.

The 2N5179 transistor has a very low reverse feedback, and the hybrid coupler is capable of up to 40 dB isolation. Although in many cases designers use two different amplifiers, the use of a hybrid coupler should be preferred, as it is a passive device with no power consumption and a long life expectancy.

The 733 amplifier is a unique device that allows programming internal gain. By setting the appropriate bypass capacitor, different gain can be chosen, and this amplifier can even be used in a linear mode exhibiting good intermodulation distortion.

As it is an internal push–pull configuration, the use of balanced output terminals is recommended. Several monolithic amplifiers are available as isolation stages, and amplifiers such as the CA3028 or similar can be used in a differential mode and AGC can be applied.

We previously learned that the proper termination of the mixer is absolutely essential. The feedback amplifier shown in Figure 4-128 will provide extremely low noise and perfect matching. This is an example of several feedback amplifiers that can be constructed, and this combination seems to be the best. It is based on Patent No. 3891934 issued to David Norton. This type of lossless feedback amplifier consists of a three-winding transformer connected to a common-base transistor in such a manner as to provide gain and impedance matching.

This circuit can be analyzed under the simplifying assumptions that the common-base transistor has a zero input impedance, an infinite output impedance, and unity current gain, while the transformer is considered to be

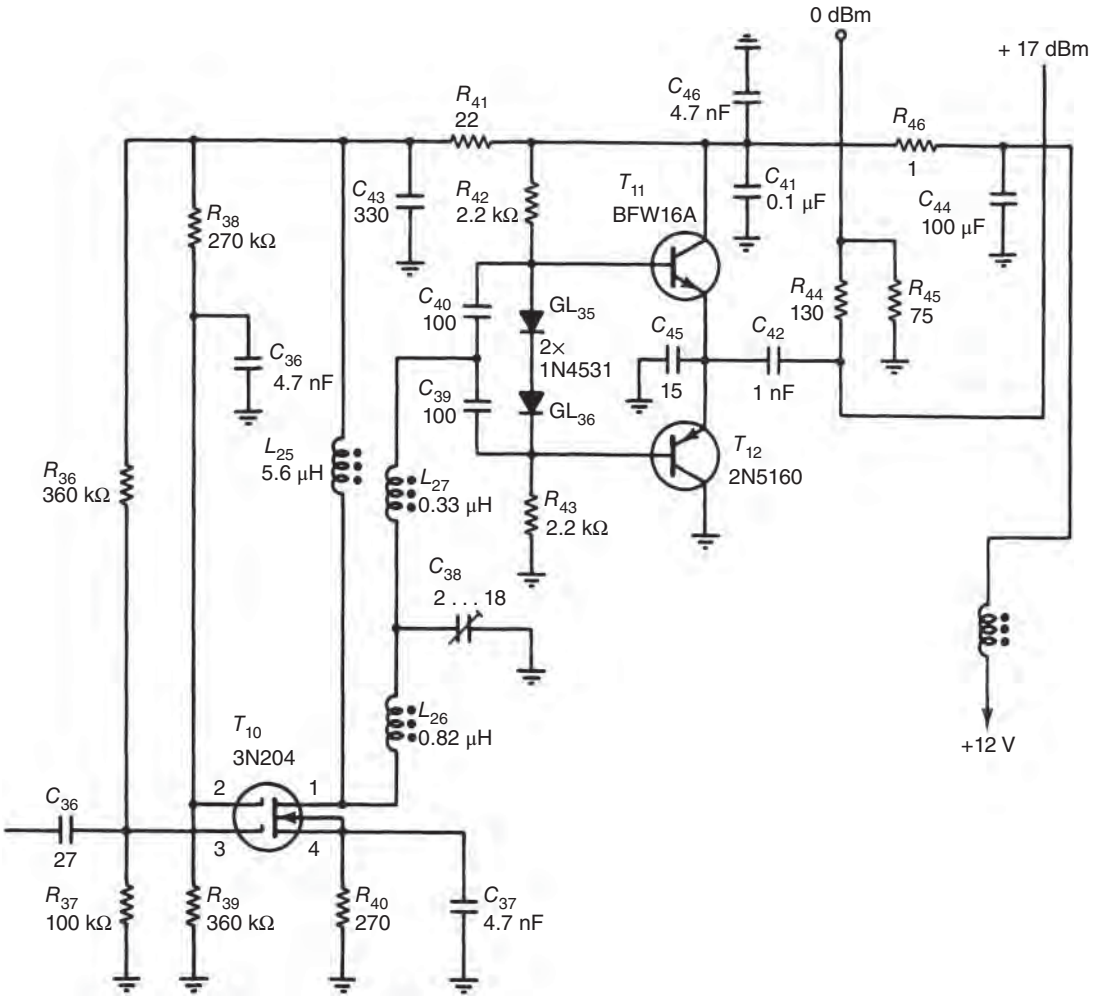


Figure 4-125 High-power output stage with isolation amplifier delivering about +17 dBm. The circuit works well up to 100 MHz.

ideal. With these assumptions it can easily be shown that a two-way impedance match to Z_o will be obtained if the transformer turns ratio is chosen such that $n = m^2 - m - 1$.

With this choice, the power gain is m^2, the load impedance presented to the collector is $(n + m)\ Z_o$, and the source impedance presented to the emitter is $2Z_o$. Turn ratios for m equal to 2, 3, and 4 yield gains of 6, 9.5, and 12 dB and load impedances of 3, 8, and $15Z_o$, respectively.

It is seen that, similar to a conventional common-base amplifier, the gain of the stage is determined by the ratio of the load impedance, Z_l, to the input impedance, Z_{in}. In this case the gain is given by $Z_l/Z_{in} + 1$, whereas it is just Z_l/Z_{in} in the conventional configuration. The significant difference is that the transformer-coupled device provides a two-way impedance match, which is obtained by coupling the load impedance to the input, and the source impedance to the output by transformer action.

The dynamic range considerations for this device are similar to those of the directional coupler circuit, but with some important differences. First, the operation of the circuit depends on the completely mismatched conditions presented by the transistor to the circuit (i.e., the emitter presents a short circuit and the collector an open circuit). Hence, there is no requirement to introduce resistive elements for impedance matching as in the directional coupler

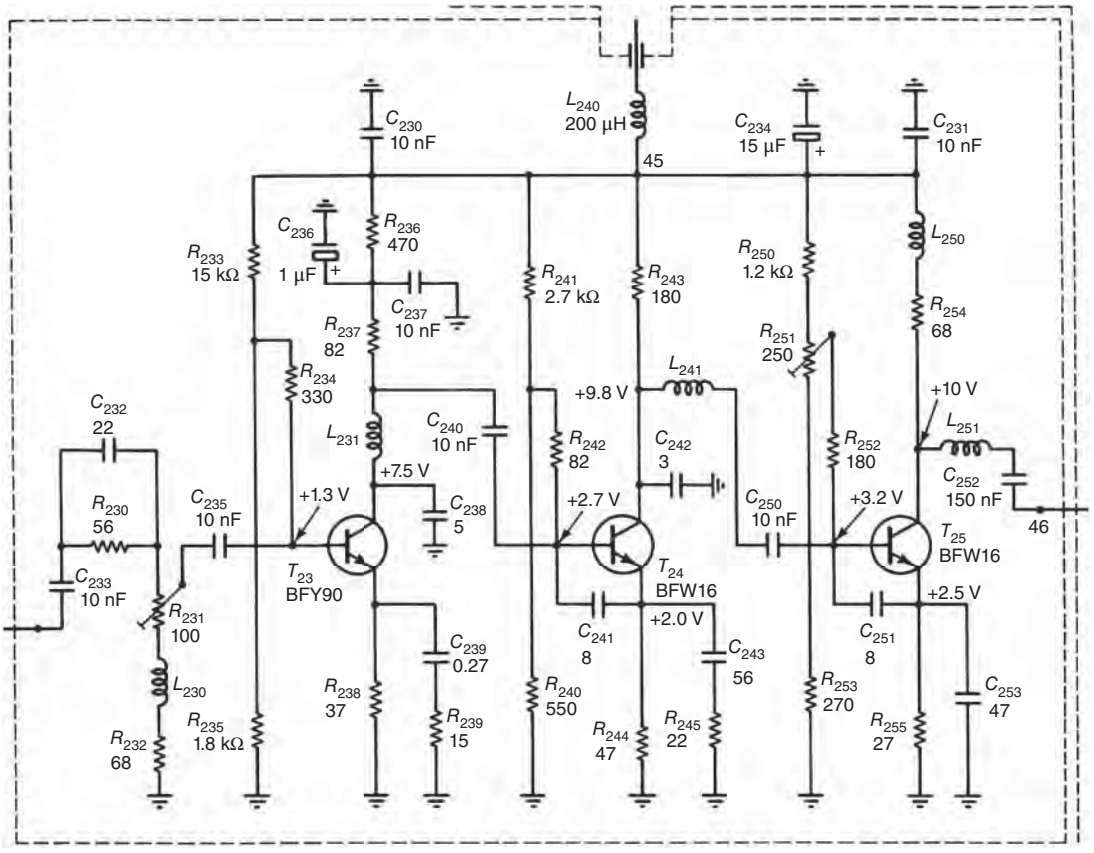


Figure 4-126 Wideband amplifier from 100 kHz to 600 MHz.

circuit. Therefore, a noise figure advantage is obtained with this circuit. Second, the source impedance of $2Z_o$ presented to the emitter tends to give optimum noise figure performance with low collector currents, which also favors lower noise figures. Finally, in spite of the small currents involved, relatively large output powers can be provided because of the high load impedance, which goes along with the higher-gain versions.

The main disadvantage of the circuit is that the high load impedance tends to limit the bandwidth. Nevertheless, sufficient bandwidth can be achieved to provide broadband IF gain with noise figures competitive with those that could be obtained previously only in very narrowband units.

As this is a very convenient circuit, let us look at the actual working design shown in Figure 4-129. Both transistors are made by Siemens.

The antiparallel diodes at the input can be omitted. The core material used in the transformers depends on the frequency range. Siemens ferrite material type B62152-A8-X17, U17 for frequencies from 100 MHz up and K30 material for frequencies below, should be used.

Figure 4-130 shows the winding arrangement for the transformer. This amplifier has the following characteristics:

- Power gain 19 dB.
- Noise figure 1.35, equivalent to 1.3 dB.
- Third-order intercept point 14 dBm at the input or 33 dBm at the output.
- 1-dB compression +18 dBm.

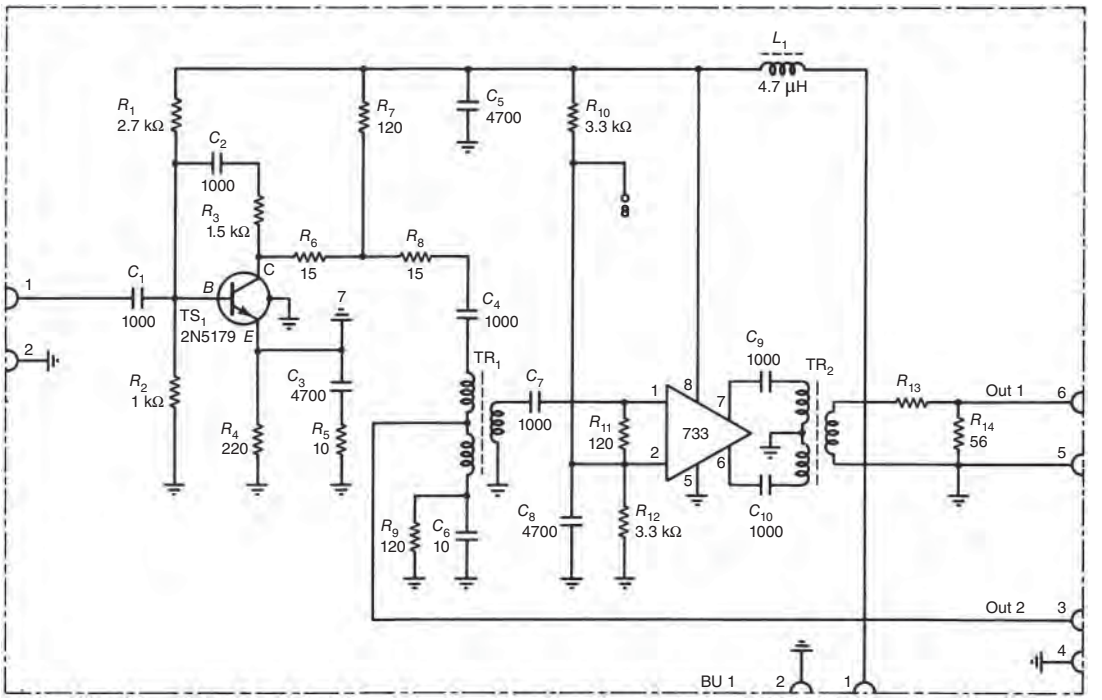


Figure 4-127 Wideband amplifier with two outputs and high reverse isolation operating up to 100 MHz. TR1 is a 3 dB coupler.

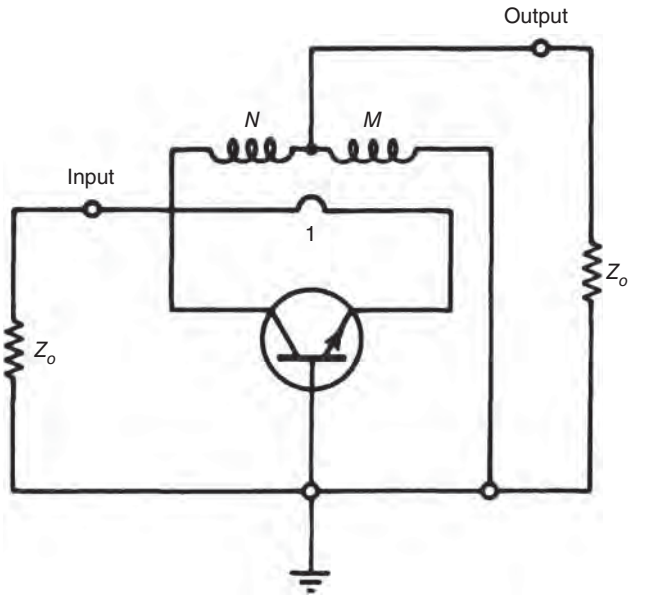


Figure 4-128 Feedback amplifier using the noiseless feedback technique.

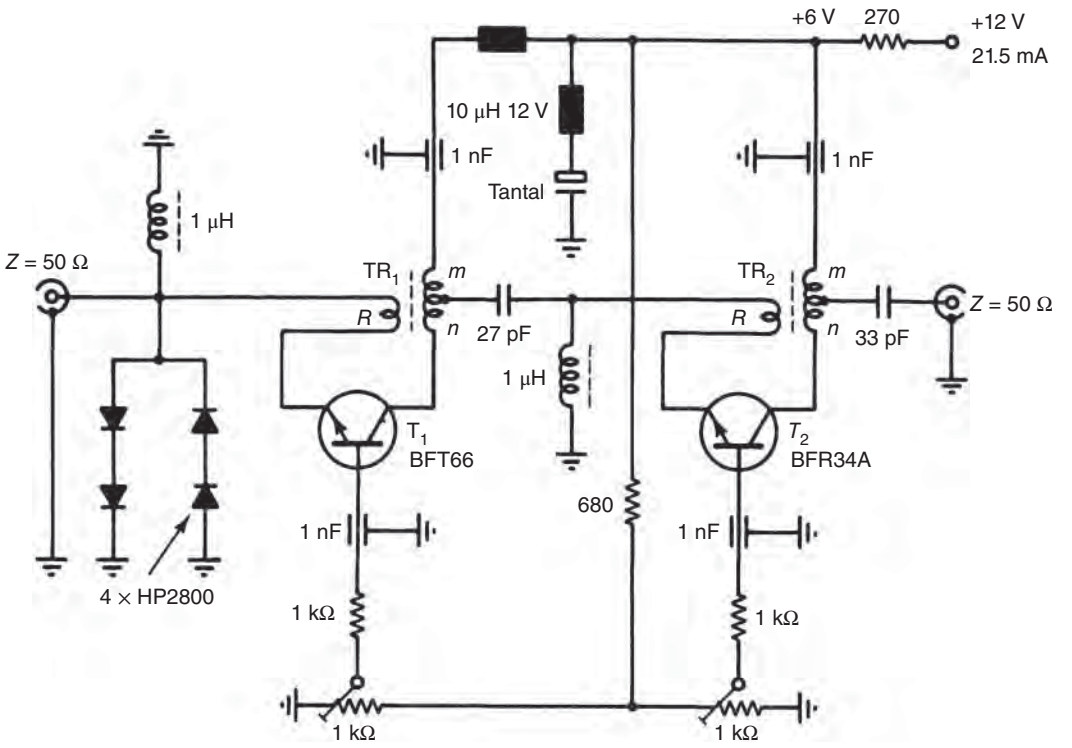


Figure 4-129 Two-stage ultra-low-noise high dynamic amplifier.

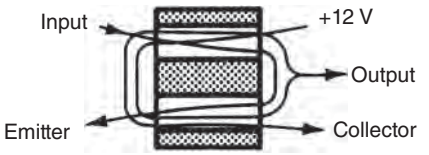


Figure 4-130 Details on the transformer for schematic of Figure 4-129.

- Input impedance $50 \pm 2\,\Omega$.
- Bandwidth 70–570 MHz (can be made to work at lower frequencies with the higher-permeability core).
- Dynamic range 102 dB determined from the fact that two signals, separated in frequency of 3.17 mV at the input of the amplifier, result in two intermodulation-distortion products of 25.4 nV. The noise figure of 1.3 dB at 2.4 kHz bandwidth results in the same noise voltage of 25.4 nV. If the noise floor of −138.8 dBm equivalent to the 25.4 nV is subtracted from the −36.96 dBm or the 3.17 mV, which generates the two intermodulation-distortion products, the difference is approximately 102 dB.
- Power supply 12 V, 21 mA.

4-8-4 Example Implementations

An example MOS-FET amplifier is shown in Figure 4-131. Predicted performance is charted in Figure 4-132. The 4 GHz gain is about 8 dB, the noise figure is 0.9 dB, and $S_{11} = -10$ dB.

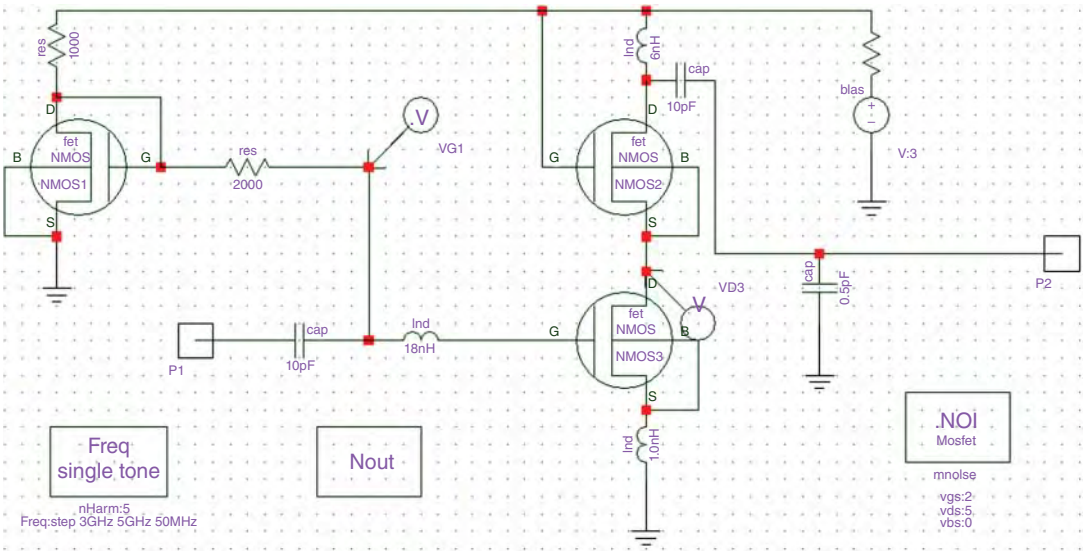


Figure 4-131 Example MOS-FET amplifier.

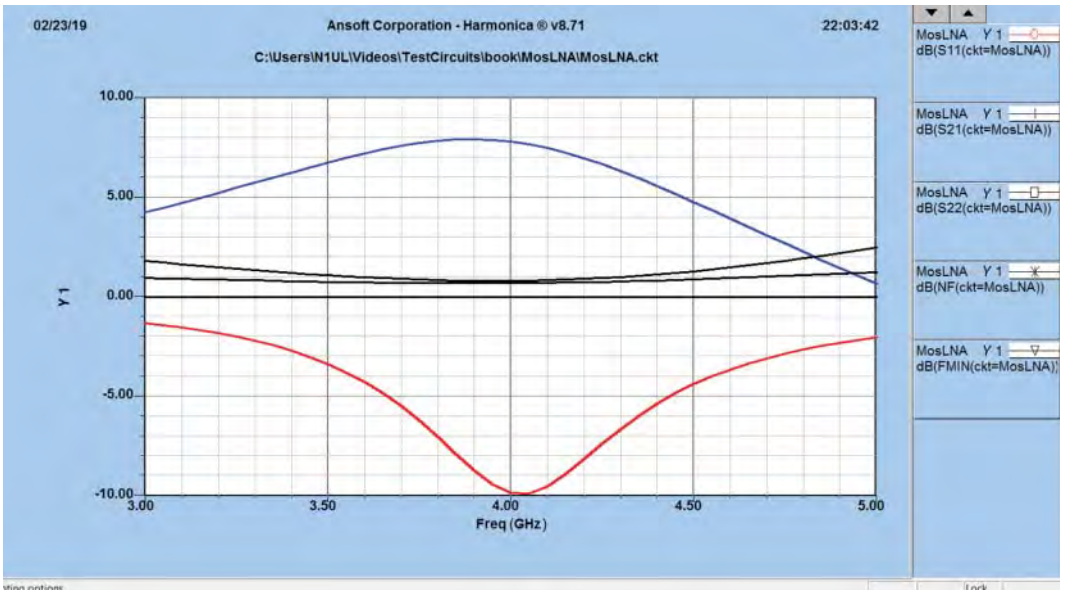


Figure 4-132 Performance of the MOS-FET amplifier.

For most modern generators a wideband medium gain amplifier is needed that also has a low IMP product. A distributed amplifier is a good solution. Figure 4-133 shows the schematic diagram of an example implementation. Predicted performance is charted in Figure 4-134a–Figure 4-13d.

Advanced technologies have provided implementers with a wide array of amplifier features and choices for various applications. The TriQuint TGA2216 is an example of a modern high frequency power

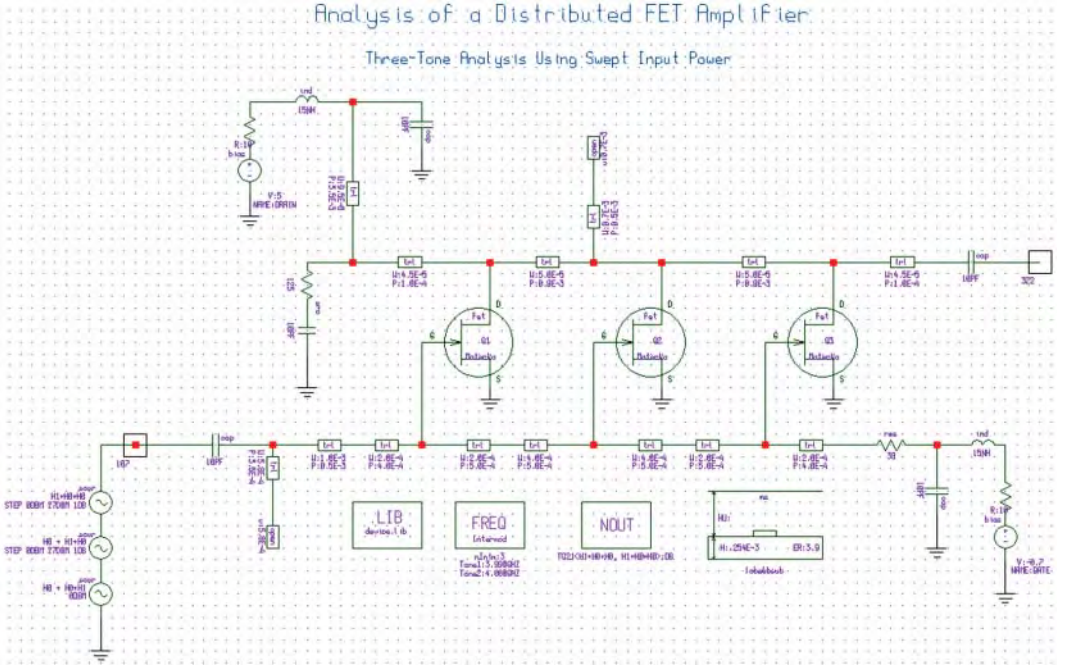


Figure 4-133 Distributed FET amplifier.

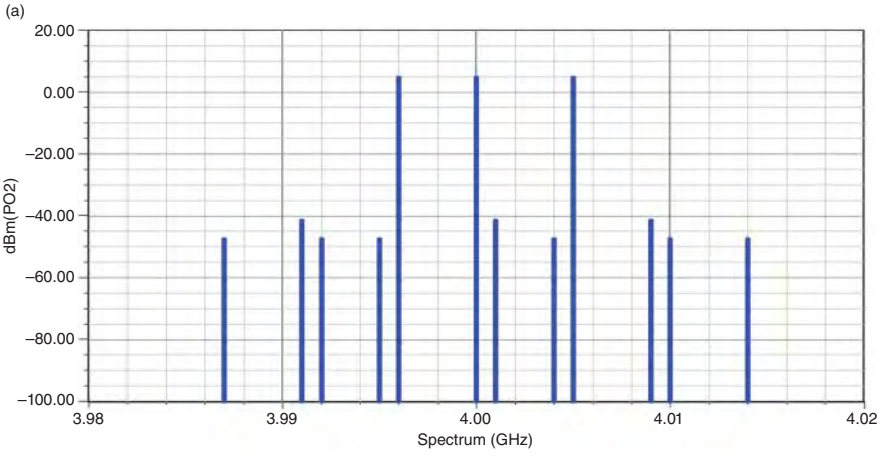


Figure 4-134a Three tone output spectrum.

amplifier.[2] The TGA2216 is a wideband cascode amplifier fabricated on a 0.25 µm GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 48 V operation. The TGA2216 operates from 0.1 to 3.0 GHz and provides up to 12 W of saturated output power with 14 dB of large-signal gain and greater than 40% power-added efficiency. The broadband performance supports both

[2]This section is based on: "Triquint TGGA2216, 0.1 – 3.0 GHz 12 W GaN Power Amplifier," Rev. A, Triquint, Hillsboro, OR, 2015.

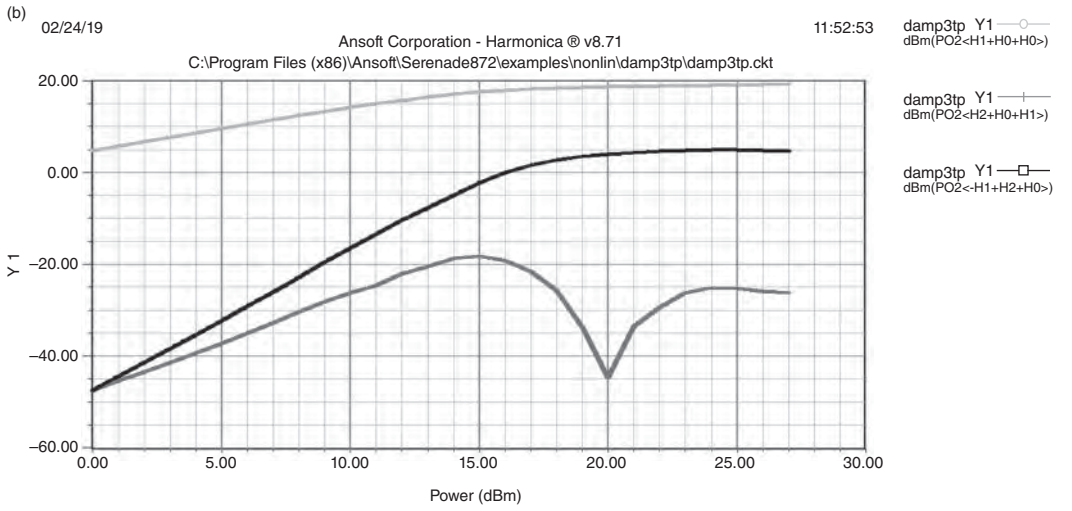


Figure 4-134b The light grey trace represents the output signal, the dark grey trace is the third order signal, and the black trace is the fifth-order signal product.

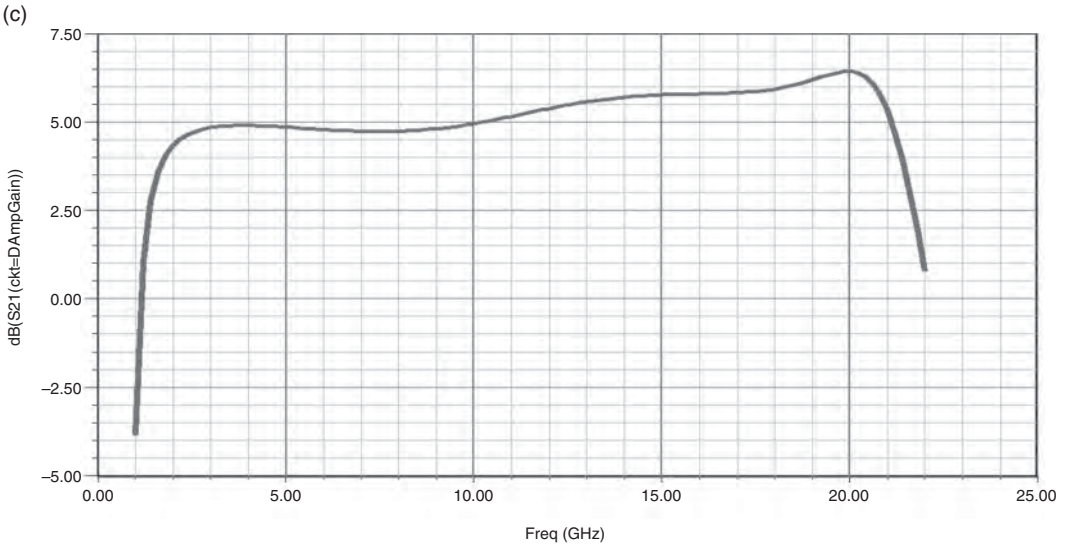


Figure 4-134c Frequency response of the 3-stage distributed amplifier.

radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2216 is fully matched to 50 Ω at both RF ports allowing for simple system integration. dc blocks are required on both RF ports and the drain voltage must be injected through an off-chip bias-tee on the RF output port. An example application of the TGA2216 is shown in Figure 4-135.

Plots of typical performance of the TGA2216 are documented in Figure 4-136.

A physical implementation of the power amplifier is shown in Figure 4-137.

(d)

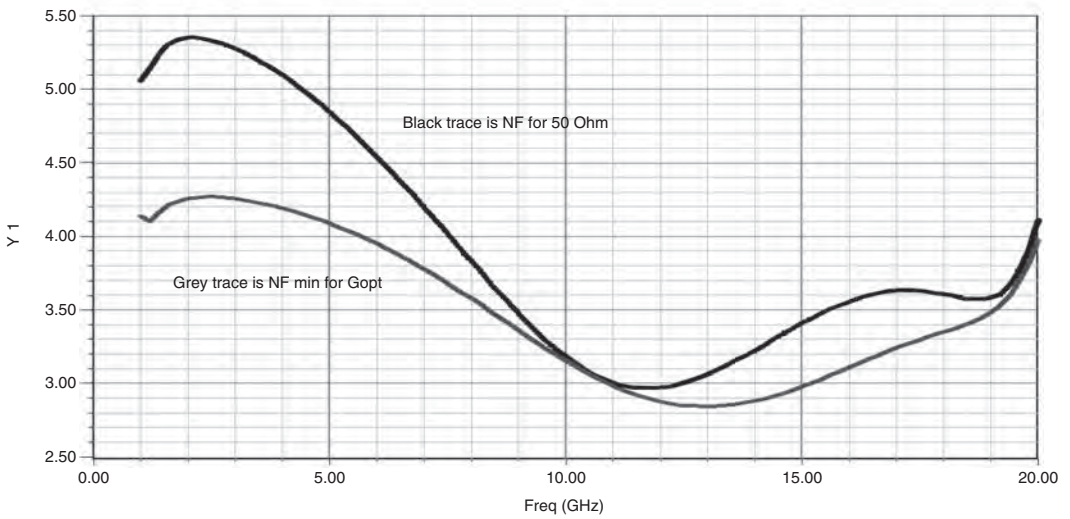


Figure 4-134d The black trace is the 50 Ω noise figure, and the dark grey trace is the minimum noise figure of the 3 stage distributed amplifier.

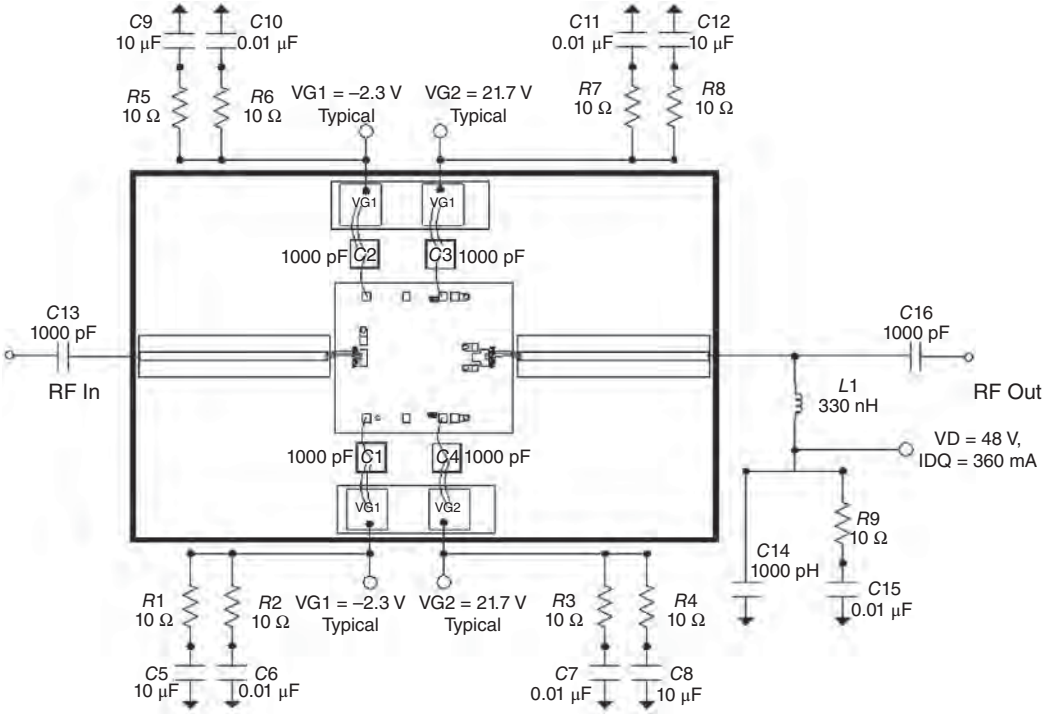


Figure 4-135 Application example of the TGA2216. (*Courtesy of TriQuint*.)

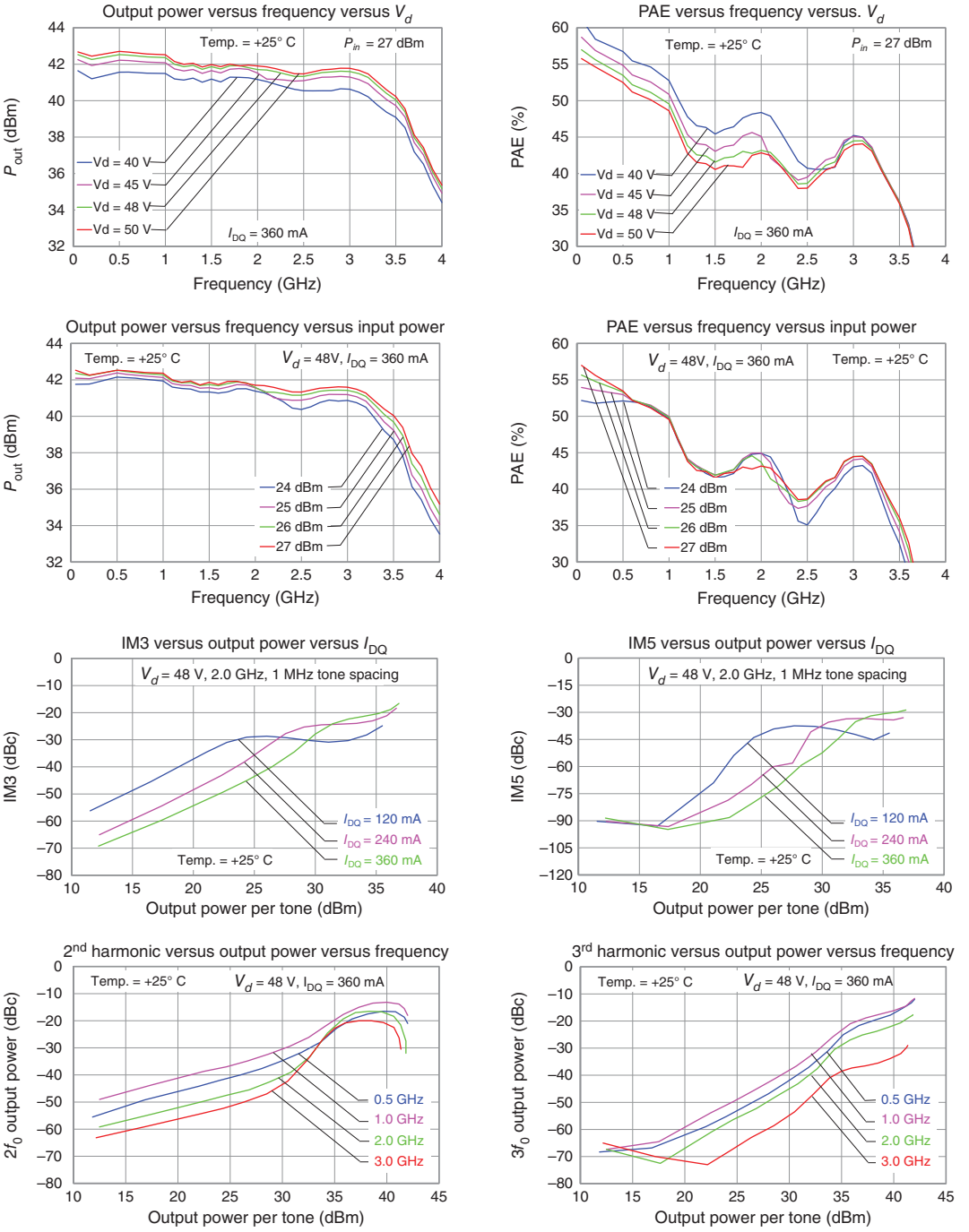


Figure 4-136 Selected performance characteristics of the TGA2216. (*Courtesy of TriQuint*.)

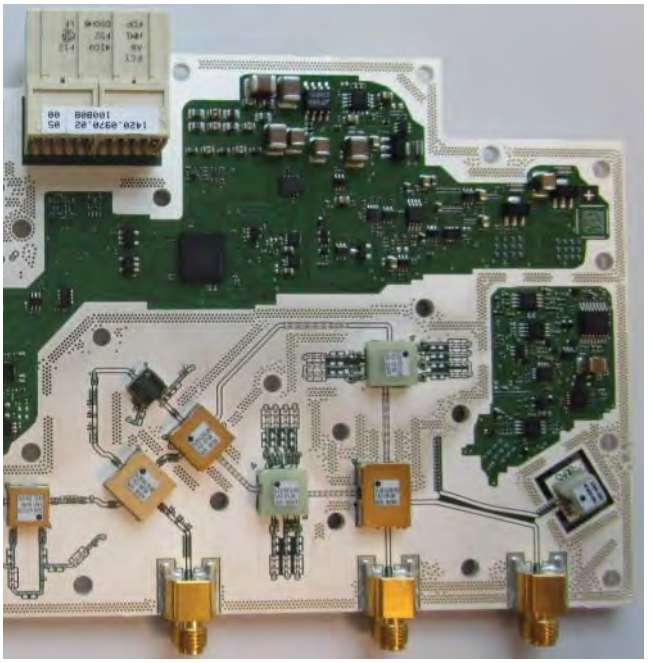


Figure 4-137 Photograph of the R&S 40 GHz SMA power amplifier.

4-9 PROGRAMMABLE DIVIDERS

4-9-1 Asynchronous Counters

In frequency synthesizers, the VCO is operating at a much higher frequency than the reference. There are two ways to provide information for the phase/frequency comparator.

(1) The use of harmonic sampling. Here, the reference generates extremely narrow high harmonic contents, pulses that are being fed together with the VCO frequency to the phase detector. In addition, a coarse steering circuit pretunes the oscillator so that the oscillator frequency is very close to the required harmonic of the comb generator.

(2) The input frequency is divided to the reference frequency. The same is correct for the reference frequency, as the reference oscillator may be much higher than the desired reference frequency or step size. In most cases, the reference frequency is at 5 or 10 MHz, sometimes even as high as 100 MHz, while the comparison frequency applied to the phase/frequency comparator may lie between 1 MHz and 1 kHz.

The reference divider for most cases requires only a simple asynchronous counter, whereas the programmable divider chain requires synchronous and resettable counters.

While the simplest counter or divider is a flip-flop dividing by 2, modern design uses dividers of high integration. Originally, the dividers were built in RTL logic, then TTL logic, then Schottky clamped, and then CMOS integrated circuits were developed.

In parallel, the ECL technology was expanded up in frequency, and we now have dividers that operate well above 1000 MHz. Power consumption of these devices naturally is very high, while the CMOS technology was developed to reduce power consumption. TTL devices are probably the least expensive but very noisy, and we will find that most synthesizers go from ECL to CMOS directly, avoiding TTL as much as possible. The more

advanced frequency dividers have the ECL to TTL or CMOS translators built in. TTL circuitry is probably used only to support the dual-modulus counters, as you will see later.

The following types of counters are typically offered in CMOS:

(1) Seven-stage ripple counter.
(2) Decade counter/divider.
(3) Presettable divide-by-*N* counter.
(4) Decade counter (asynchronous clear).
(5) Decade counter (synchronous clear).
(6) 4-bit presettable up/down-counter.
(7) BCD up/down-counter.
(8) Programmable divide-by-*N* 4-bit counter (BCD).
(9) 12-bit binary counter.
(10) 14-bit binary counter.
(11) Octal counter/divider.
(12) 4-bit binary counter (asynchronous clear).
(13) 4-bit binary counter (synchronous clear).
(14) Binary up/down-counter.
(15) Programmable divide-by-*N* 4-bit counter (binary).
(16) Dual BCD up-counter.
(17) Dual binary up-counter.
(18) Dual programmable BCD/binary counter.
(19) Three-digit BCD counter.
(20) Real-time five-decade counter.
(21) Industrial time-base generator.

Similar dividers are available in ECL and TTL. Special devices in ECL are bi/quinary counters and swallow counters.

Figure 4-138 shows a speed/power characteristic of major logic lines. It is apparent that CMOS is indicated only in quiescent dissipation. The reason for this is the fact that the power consumption is a function of actual input frequency. Depending on the particular device and the manufacturing process, it is very possible that TTL dividers at 10 MHz require less power than a similar CMOS device. However, the additional interface circuit may justify the use of CMOS rather than involving three different logic families.

The simplest divider is a flip-flop. The flip-flop divides by 2, and input frequency ranges up to 2300 MHz are handled. Several of these flip-flops can be cascaded, and the drawback of this circuit is the resulting division $N = 2^n$, where n is the number of stages. The figures referred to below show configurations where flip-flops are being cascaded to provide dividers with random division rates. This is accomplished by feedback loops.

A typical application of this technique is used in the familiar 7490 divide-by-10 counter, which is an asynchronous decade counter. Figure 4-139 shows the internal arrangement. It consists of four master/slave flip-flops. The asynchronous dividers are slow, as the input signal triggers the first flip-flop, which then triggers the second flip-flop, and so on. In the synchronous divider, the clock is fed to all the clock inputs simultaneously, and, therefore, the delay is avoided.

4-9-2 Programmable Synchronous Up-/Down-Counters

In frequency synthesizers, asynchronous dividers have very little application, while synchronous dividers are of greater importance. In this section we deal with synchronous dividers and a special version of them, presettable dividers, as the synthesizer requires that the division rate be selective rather than hard-wired. Figure 4-140 shows synchronous counters consisting of several flip-flops with the according waveforms.

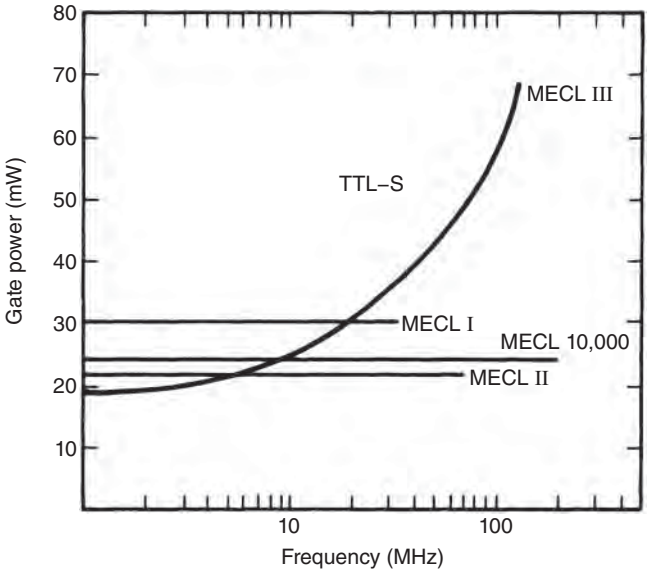


Figure 4-138 Power consumption of different divider technologies as a function of frequency.

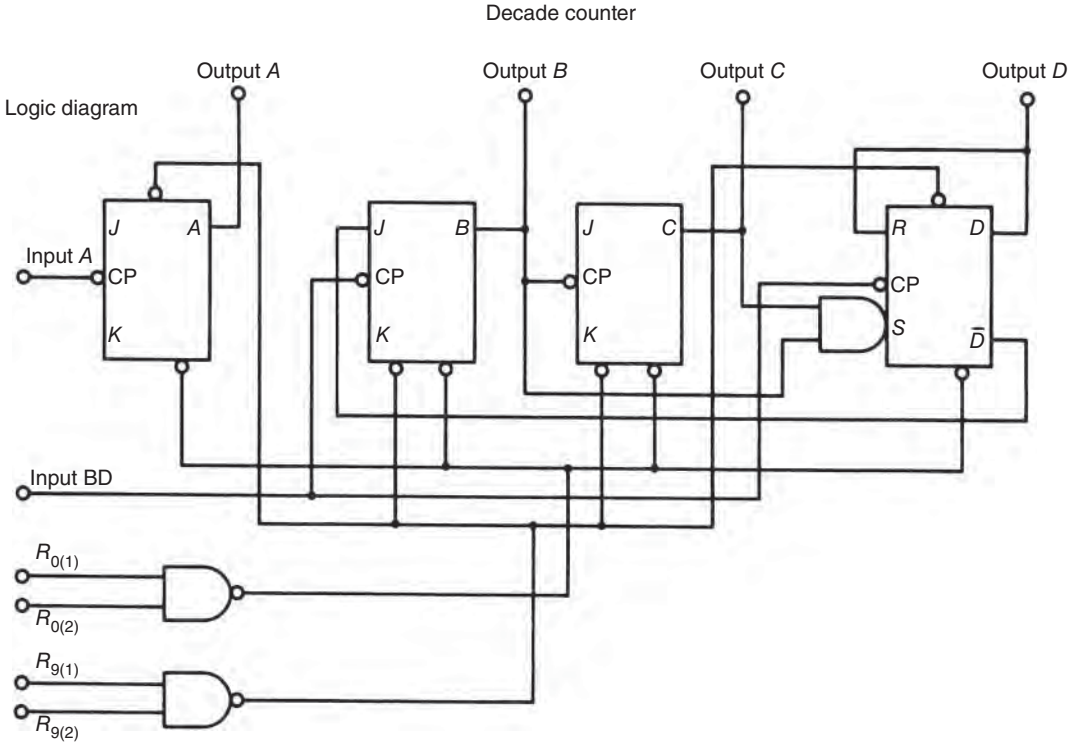


Figure 4-139 Schematic of the 7490 divide-by-10 counter.

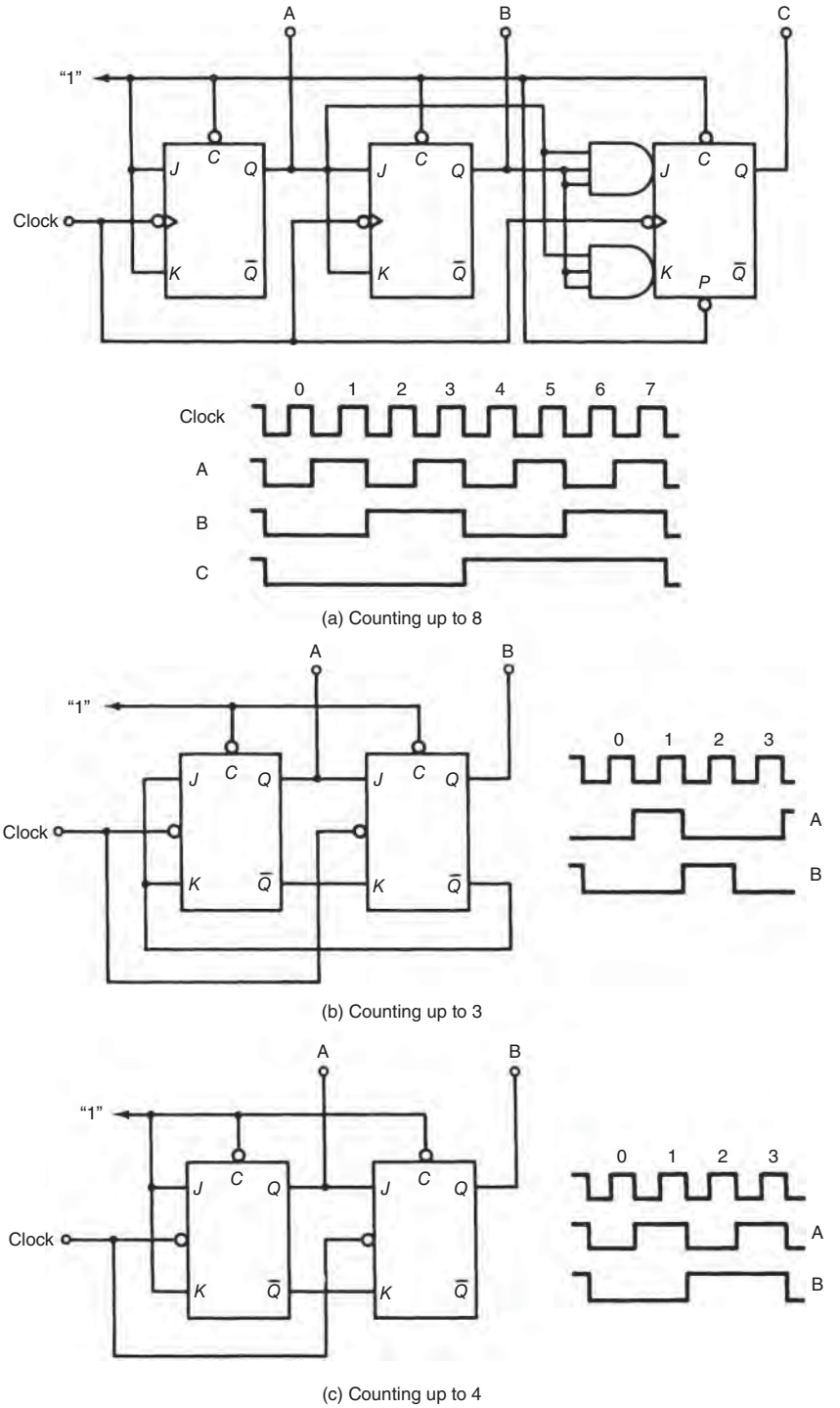
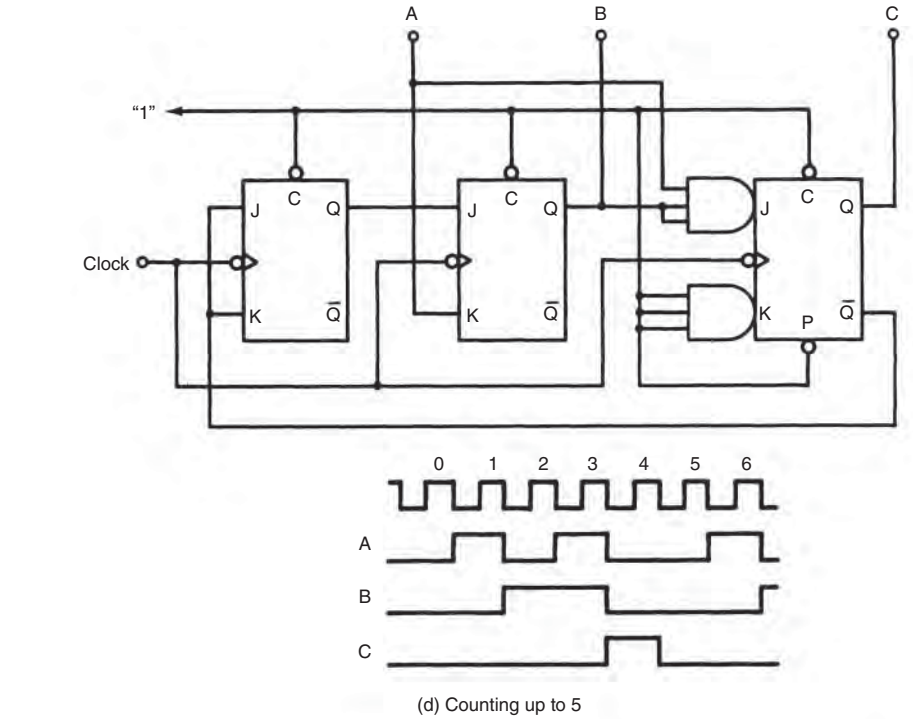
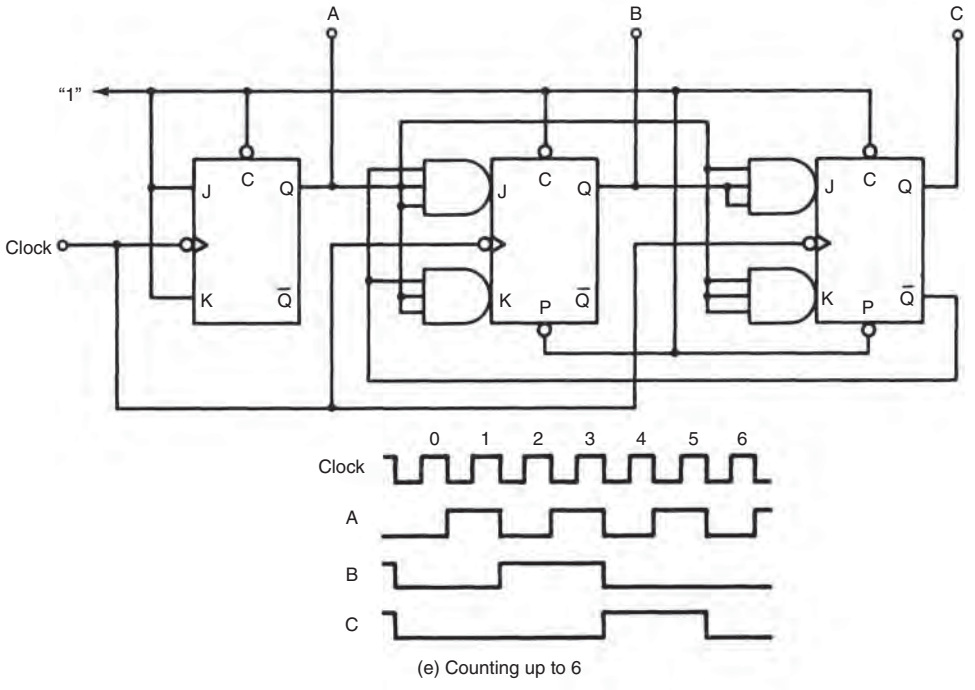


Figure 4-140 Synchronous counters.

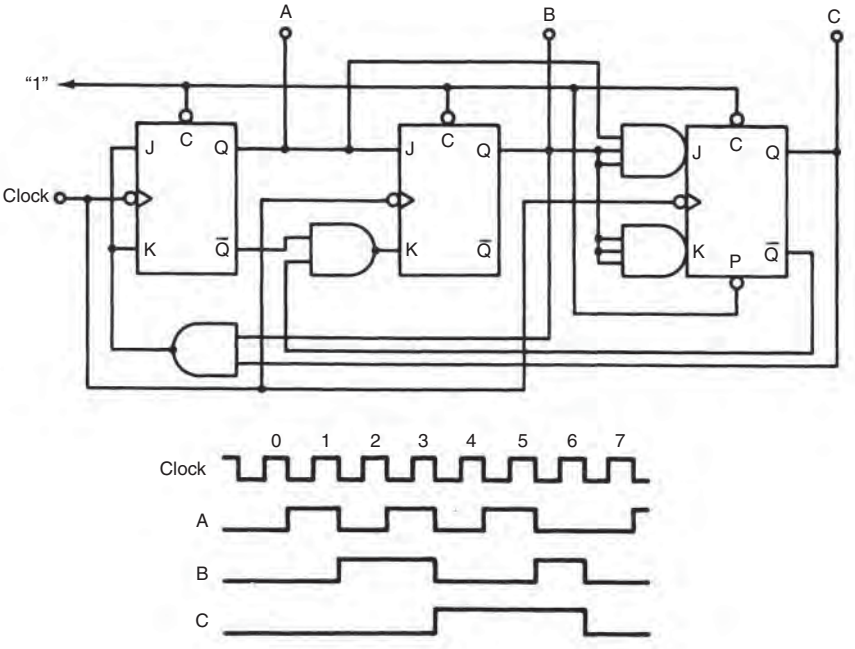


(d) Counting up to 5

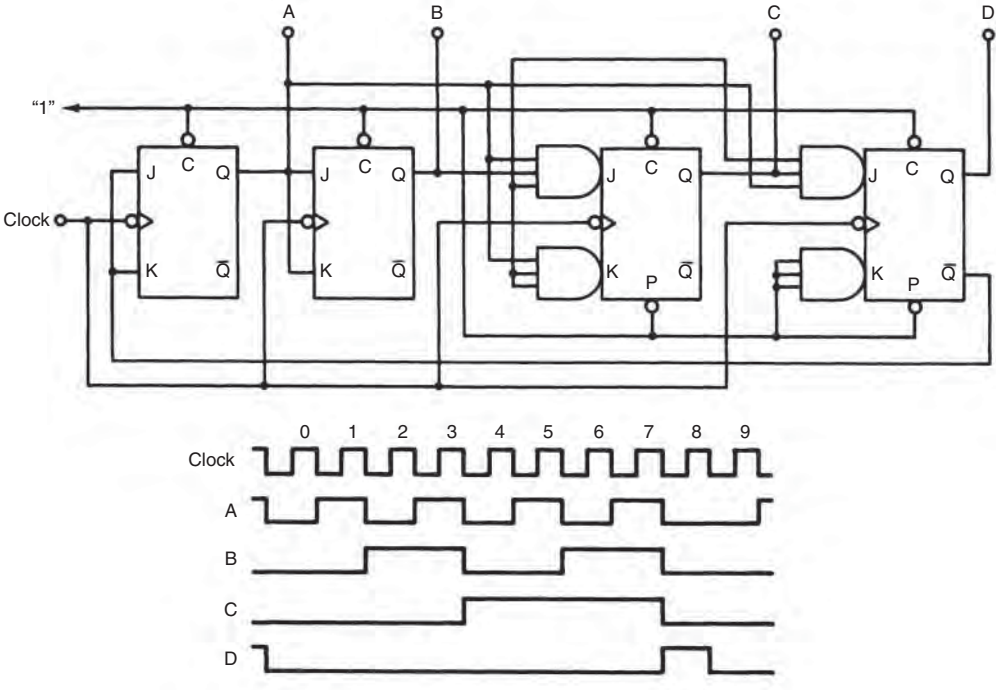


(e) Counting up to 6

Figure 4-140 (*Continued*)

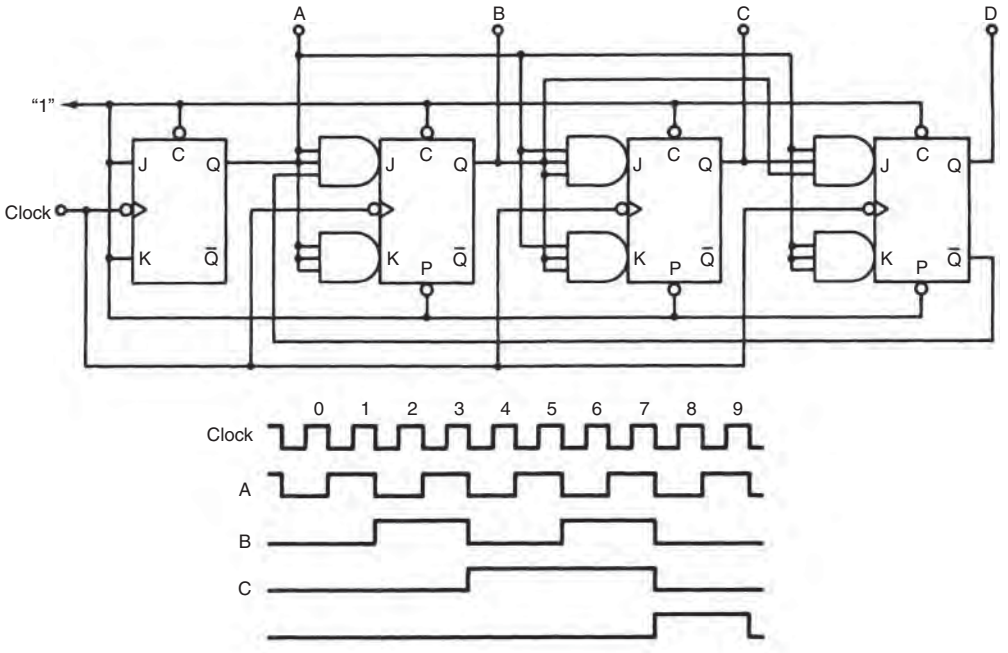


(f) Counting up to 7

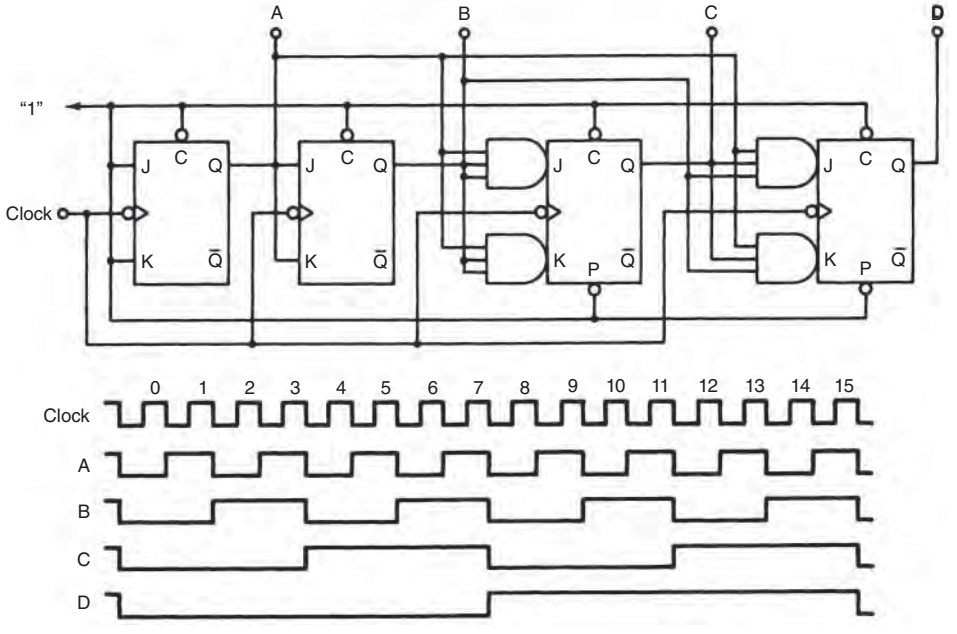


(g) Counting up to 9

Figure 4-140 (*Continued*)



(h) Counting up to 10



(i) Counting up to16

Figure 4-140 (*Continued*)

8	4	2	1	Decimal value
O	O	O	O	0
O	O	O	L	1
O	O	L	O	2
O	O	L	L	3
O	L	O	O	4
O	L	O	L	5
O	L	L	O	6
O	L	L	L	7
L	O	O	O	8
L	O	O	L	9

(j) Truth table to convert 1248 BCD to decimal

	2	4	2	1
Clock	D	C	B	A
0	O	O	O	O
1	O	O	O	L
2	O	O	L	O
3	O	O	L	L
4	O	L	O	O
5	L	O	L	L
6	L	L	O	O
7	L	L	O	L
8	L	L	L	O
9	L	L	L	L

(k) Synchronous 1248 BCD counter

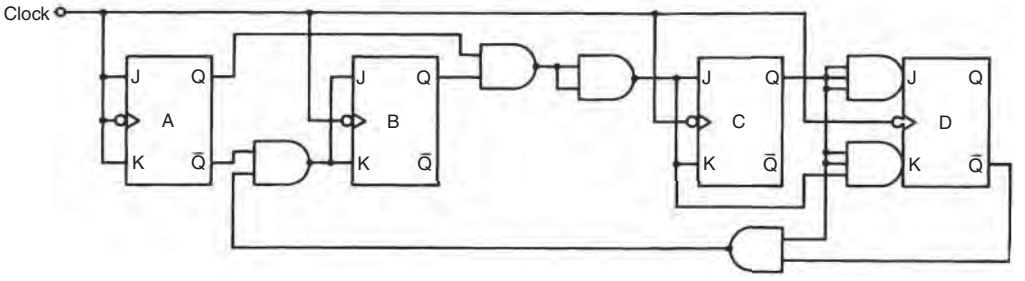


Figure 4-140 (*Continued*)

Several applications require up-/down-counters. The reason for this is that for programmed division ratio, the decoding of the circuit becomes easy. The series 74192/74193 counters provide this facility.

Both the 74192 and 74193 are synchronous reversible (up/down) counters with four master/slave flip-flop stages. Inputs include the separate up/down count, load preset, overriding clear, and individual preset data input to each stage. The 74192 BCD counter is capable of counting either up from zero to BCD nine or down from BCD nine to zero. The 74193 is a four-stage binary counter operating in exactly the same manner, except that it can count up to binary fifteen from zero and down from binary fifteen to zero.

The state of the counter outputs depends on the number of count (clock) input pulses received on either the count-up or count-down input. The counter is advanced to its next appropriate state on the positive transitions of the count pulses, while the unused count input is held high. To count in the up direction, the count-up input is pulsed, and to count down, the count-down input is pulsed. The count direction is changed by taking both count inputs high before entering the count signal on the other count input.

In addition to changing the counter state in the normal counting mode, when the counter outputs respond to the incoming pulses, the counter state can easily be taken to any desired state within its range. This is achieved using the fully presettable facilities of the counter. The desired new count state is entered in parallel on the preset data inputs, and the load preset input is taken low, enabling the preset data to be presented to the outputs. The signals on the outputs then agree with those on the preset data inputs independent of any further clock information received while the load preset input is low. This preset state is stored in the counter when the load preset input goes high. Further count input pulses then clock the counter to its next appropriate state.

To reset all outputs to zero, the clear input is taken high. The overriding clear is independent of load and count inputs.

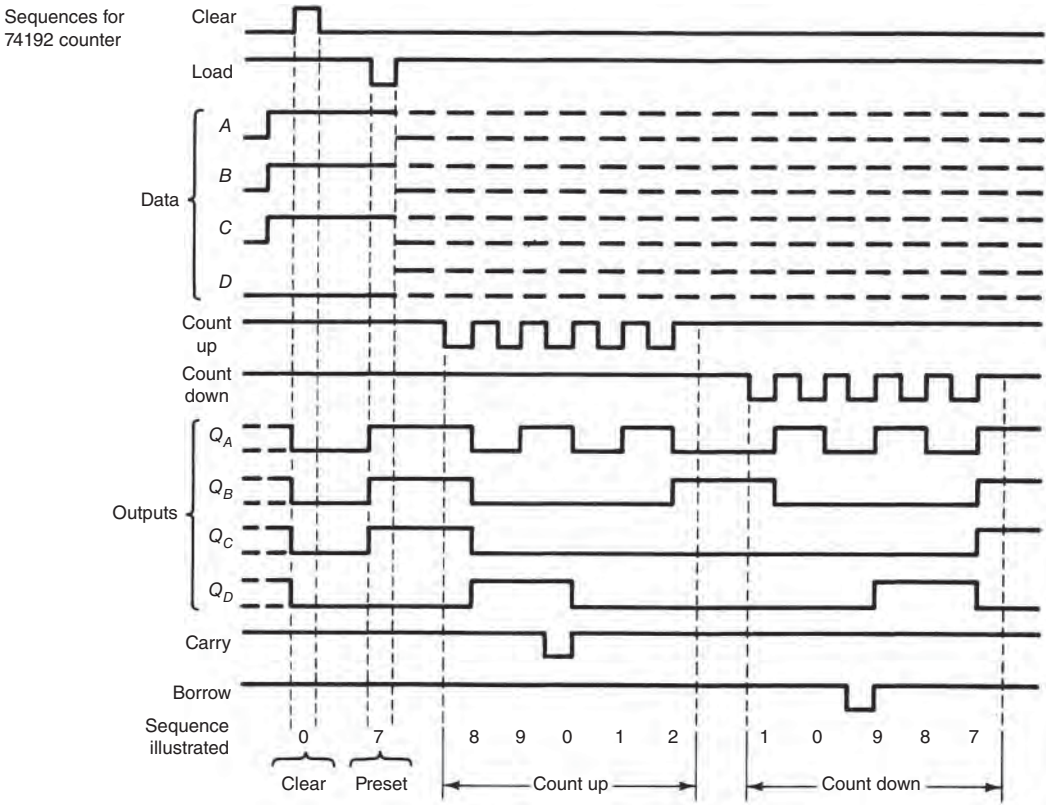
These counters can be cascaded without additional logic. When the counter overflows, the carry output produces a pulse of width equal to that of the count-up input pulse. Similarly, the borrow output pulse width equals that of the count-down input pulse when the counter underflows.

All inputs have input clamping diodes to reduce line termination effects and outputs are of standard 74 series configuration.

Typical clear, load, and count sequences for the 74192 Decade Counter

Illustrated below is the following sequence:

1. Clear all outputs to zero.
2. Preset to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



Notes:
1. Clear overrides all other inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

Figure 4-141 Timing table to the 74192 decade counter.

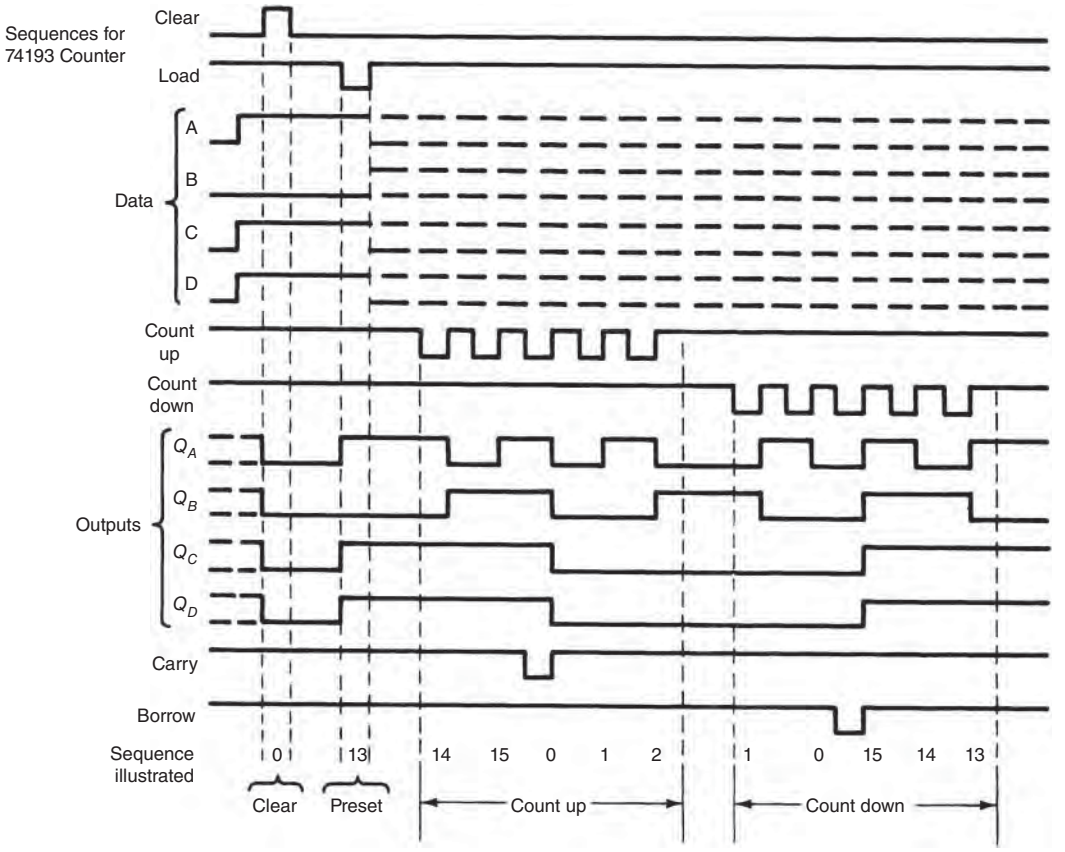
Figure 4-141 shows the various signals in the clear, load, and count sequences for the 74192. Figure 4-142 shows the same for the 74193. Figure 4-143 is a logic diagram for the 74192 and Figure 4-144 is a logic diagram for the 74193.

The 7496 is a similar powerful divider that provides:

- Preset parallel input.
- Parallel or serial input.
- Parallel and serial output.
- Buffered clear, clock, and serial inputs.
- Serial to parallel/parallel to serial converter capability.

Typical clear, load, and count sequences for the 74192 Binary Counter
Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.



Notes:

1. Clear overrides all other inputs.
2. When counting up, count-down input must be high, when counting down, count-up input must be high.

Figure 4-142 Timing table for the 74193 binary counter.

Figure 4-145 shows the block diagram. The 7496 consists of five RS master/slave flip-flops connected to form a 5-bit shift register. The clock, clear, and serial inputs are buffered by four inverters. The preset inputs A to E are connected to the flip-flop preset inputs via five two-input NAND gates. The second input of each gate is connected to the common preset input, which when at logical 1 enables all preset inputs. A logical 1 on these inputs sets the flip-flops to the logical 1 state. A logical 1 on the clear input sets all flip-flops to the logical 0 state simultaneously. Right shift in the register occurs on the positive edge of the clock pulse. The serial input data must be present prior to the clock edge. All inputs have clamping diodes and outputs are standard 74 series configuration. The registers may be cascaded to provide any length of register.

There are basically two forms of parallel input shift registers: the preset parallel input type such as the 7494 and 7496 and the clocked parallel input type such as the 7495.

The inputs of the preset type are connected to the flip-flop preset inputs via appropriate gating. The application of a logical 1 voltage to the input sets the flip-flop to logical 1 state, but the application of a logical 0 voltage then has no effect. To set flip-flops to logical 0 state, the clear input must be used.

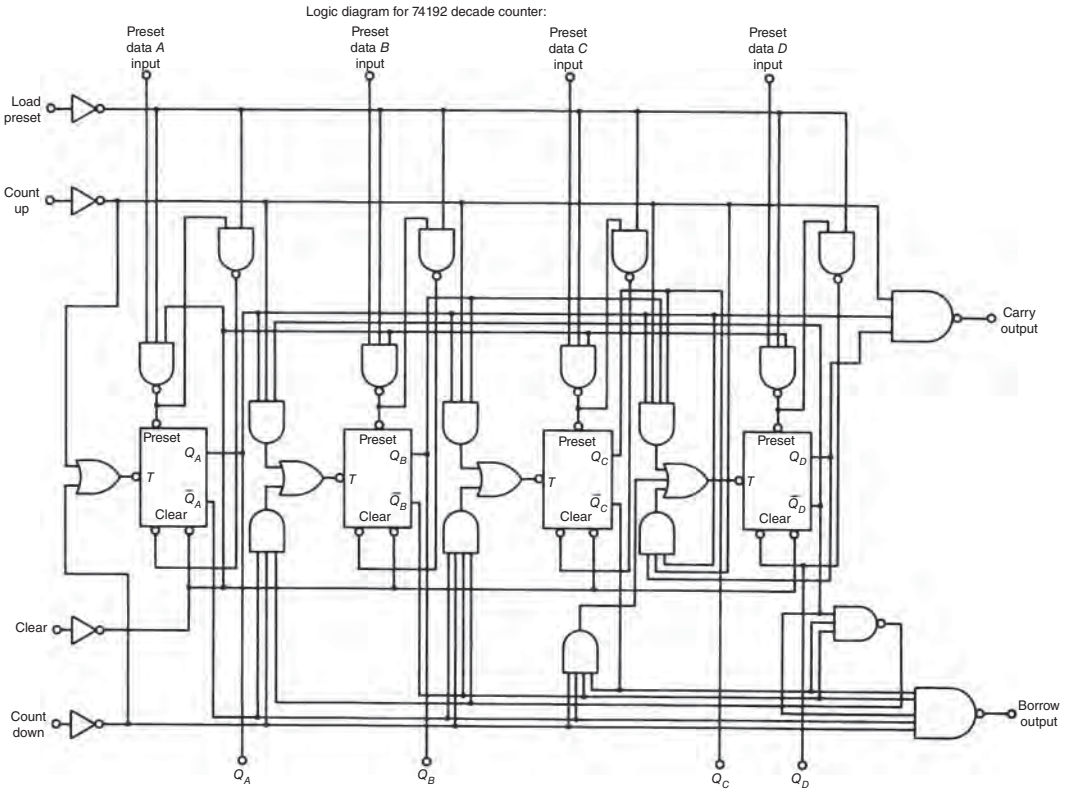


Figure 4-143 Logic diagram for the 74192 decade counter.

The inputs of the clocked type are connected to the RS flip-flop inputs via appropriate gating. The application of a logical 1 voltage at the input prior to clocking sets the flip-flops to a logical 1 state. Similarly, the application of a logical 0 voltage at the input sets the flip-flops to a logical 0 state. Hence, the clocked parallel register is most suitable for applications where the parallel data are applied for a predetermined time, as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrive randomly or are present for a very short time, as can be the case in some types of analog-to-digital conversion systems.

The various counters mentioned earlier, available in CMOS and TTL, are spin-offs that may be advantageous for certain applications. It is important to consult the data books of the various manufacturers to determine which divider is the best for a particular application. What this means is that the divider that has the highest flexibility may also be the most expensive, and in some cases, not all capabilities are required simultaneously. In order to select the right device, a price/performance analysis has to be done. As a result of price/performance analysis, as we have mentioned earlier, choosing CMOS devices and avoiding TTL may be the most judicious choice.

Although these divider changes have to remain programmable, the simultaneous availability of parallel and serial loading may not be a requirement. In some designs, however, serial loading may ease the concept; microprocessor applications, for instance, will make the design much easier and require fewer wires if serial loading is used.

Several modern integrated circuits are offered that have all the required dividers on one chip. This may be a convenience for a particular design, but only in cases where the integrated circuit is specifically designed for the application will the integrated circuit have sufficient flexibility. Generally, there is a trade-off between high integration and flexibility. As the number of available pins on the integrated circuit and decoding format limits the number of different tasks, some particular design efforts may require the use of discrete integrated circuits rather than LSI circuits.

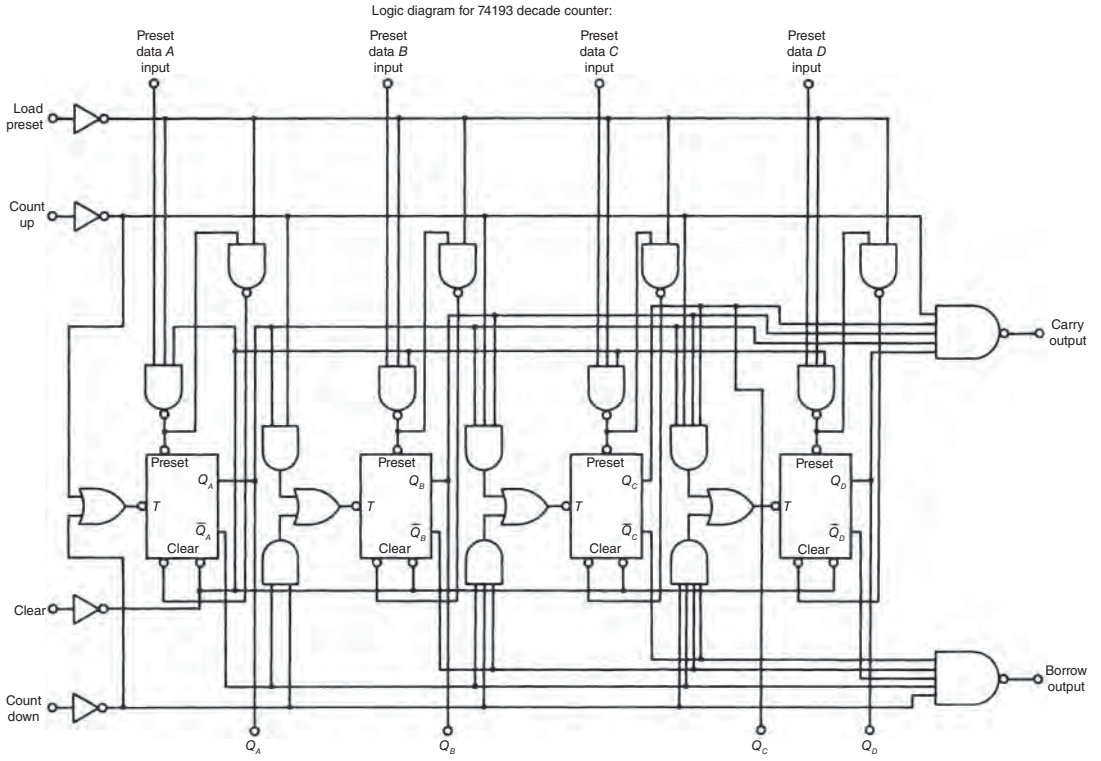


Figure 4-144 Logic diagram for the 74193 binary counter.

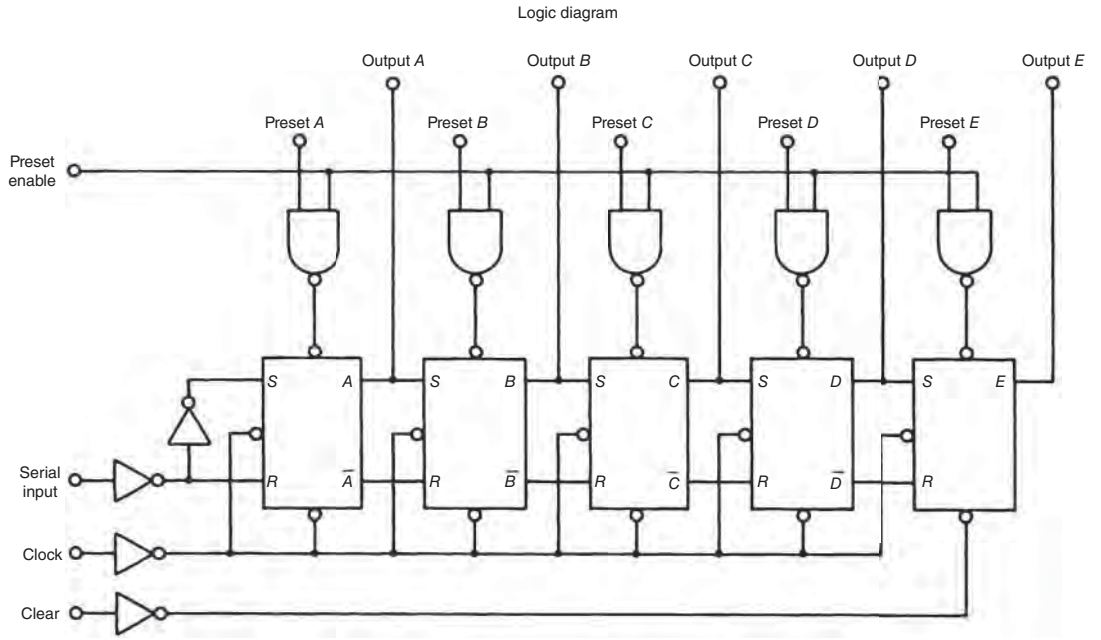


Figure 4-145 Block diagram of the 7496 counter.

4-9-3 Advanced Implementation Example

The ADF4371, a PLL chip with highly integrated circuitry and considerable flexibility, is a good example of the progress in RF IC technology. The following pages provide some of the relevant pieces of the datasheet. Analog Devices have some very impressive products in this realm, even with doublers incorporated. As time goes on this class of ICs is certain to be further developed.

ANALOG DEVICES

Microwave Wideband Synthesizer with Integrated VCO

Data Sheet

ADF4371

FEATURES

- RF output frequency range: 62.5 MHz to 32,000 MHz
- Fractional-N synthesizer and Integer N synthesizer
- High resolution 39-bit fractional modulus
- Typical spurious PFD: −90 dBc
- Integrated rms jitter: 38 fs (1 kHz to 100 MHz)
- Normalized phase noise floor: −234 dBc/Hz
- PFD operation to 250 MHz
- Reference frequency operation to 600 MHz
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
- 62.5 MHz to 8,000 MHz output at RF8x and RFAUX8x
- 8,000 MHz to 16,000 MHz output at RF16x
- 16,000 MHz to 32,000 MHz output at RF32x
- Lock time approximately 3 ms with automatic calibration
- Lock time <30 µs with autocalibration bypassed
- Analog and digital power supplies: 3.3 V
- VCO power supply: 3.3 V and 5 V
- RF output mute function
- 7mm × 7mm, 48-terminal LGA package

APPLICATIONS

- Wireless infrastructure (multicarrier global system for mobile communication (MC-GSM), 5 G)
- Test equipment and instrumentation
- Clock generation
- Aerospace and defense

GENERAL DESCRIPTION

The ADF4371 allows implementation of fractional-N or Integer N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. The wideband microwave voltage controlled oscillator (VCO) design allows frequencies from 62.5 MHz to 32 GHz to be generated.

The ADF4371 has an integrated VCO with a fundamental output frequency ranging from 4000 MHz to 8000 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allows the user to generate radio frequency (RF) output frequencies as low as 62.5 MHz at RF8x. A frequency multiplier at RF16x generates from 8 GHz to 16 GHz. A frequency quadrupler generates frequencies from 16 GHz to 32 GHz at RF32x. RFAUX8x duplicates the frequency range of RF8x or permits direct access to the VCO output. To suppress the unwanted products of frequency multiplication, a harmonic filter exists between the multipliers and the output stages of RF16x and RF32x.

Control of all on-chip registers is through a 3-wire interface. The ADF4371 operates with analog and digital power supplies ranging from 3.15 V to 3.45 V, and 5 V for the VCO power supply. The ADF4371 also contains hardware and software power-down modes.

FUNCTIONAL BLOCK DIAGRAM

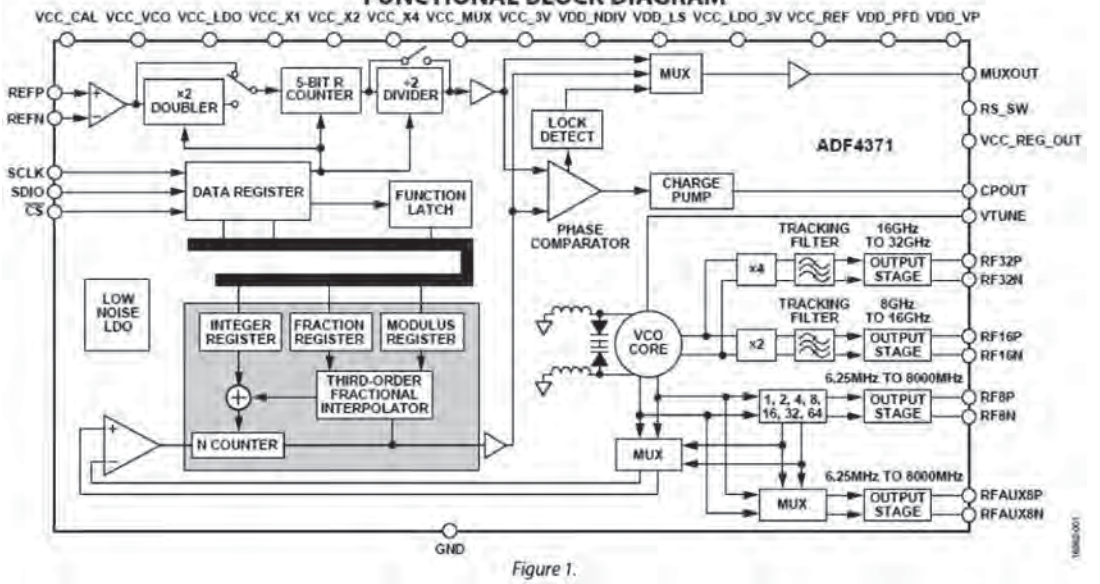


Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

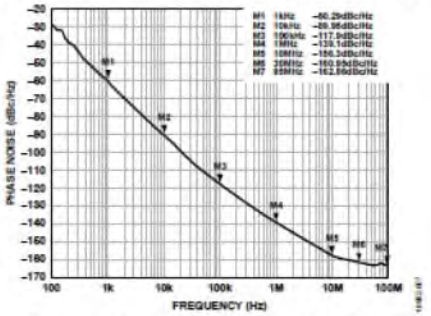


Figure 7. Open-Loop VCO Phase Noise, 4.0 GHz, VCC_VCO = 5 V

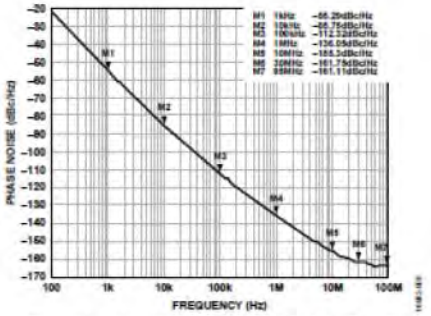


Figure 8. Open-Loop VCO Phase Noise, 5.7 GHz, VCC_VCO = 5 V

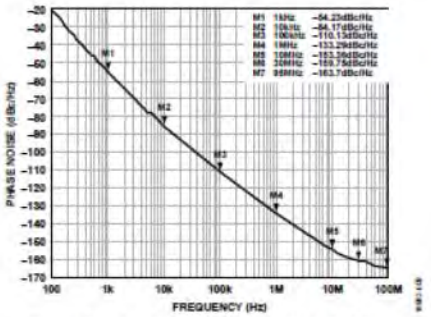


Figure 9. Open-Loop VCO Phase Noise, 8.0 GHz, VCC_VCO = 5 V

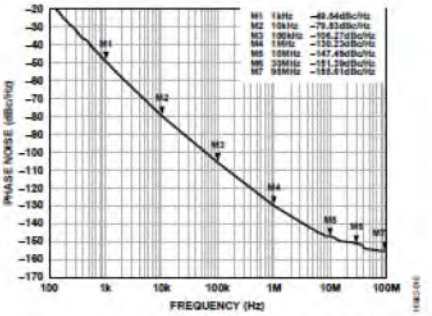


Figure 10. Open-Loop VCO Phase Noise at RF16x Output, 11.4 GHz, VCC_VCO = 5 V

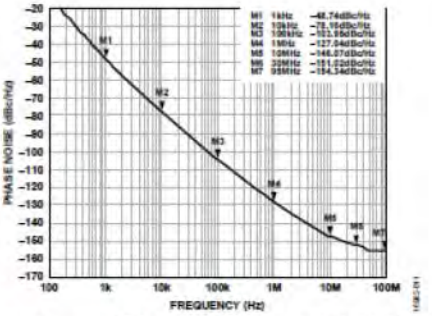


Figure 11. Open-Loop VCO Phase Noise at RF16x Output, 16.0 GHz, VCC_VCO = 5 V

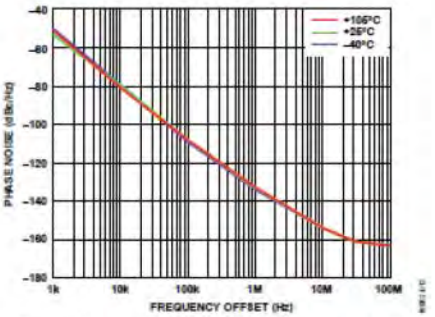


Figure 12. Open-Loop VCO Phase Noise over Temperature, 8.0 GHz, VCC_VCO = 5 V

4-9-4 Swallow Counters/Dual-Modulus Counters

To extend the frequency range, *swallow counters* can be used—often referred to as two- or dual-modulus prescalers. Figure 4-146 shows the block diagram of such a device. The three flip-flops are wired in such a manner that by changing the decoding, the division ratio can be changed between a division ratio of 2, 5, 6, 10, 11, or 12. The Motorola MC12012 shown in the figure can be used for this. There are several ways to interface these dual-modulus prescalers, which we prefer to refer to as swallow counters. What actually happens is that out of a chain of pulses, one or two pulses are being swallowed; but let us first take a look at how the system works.

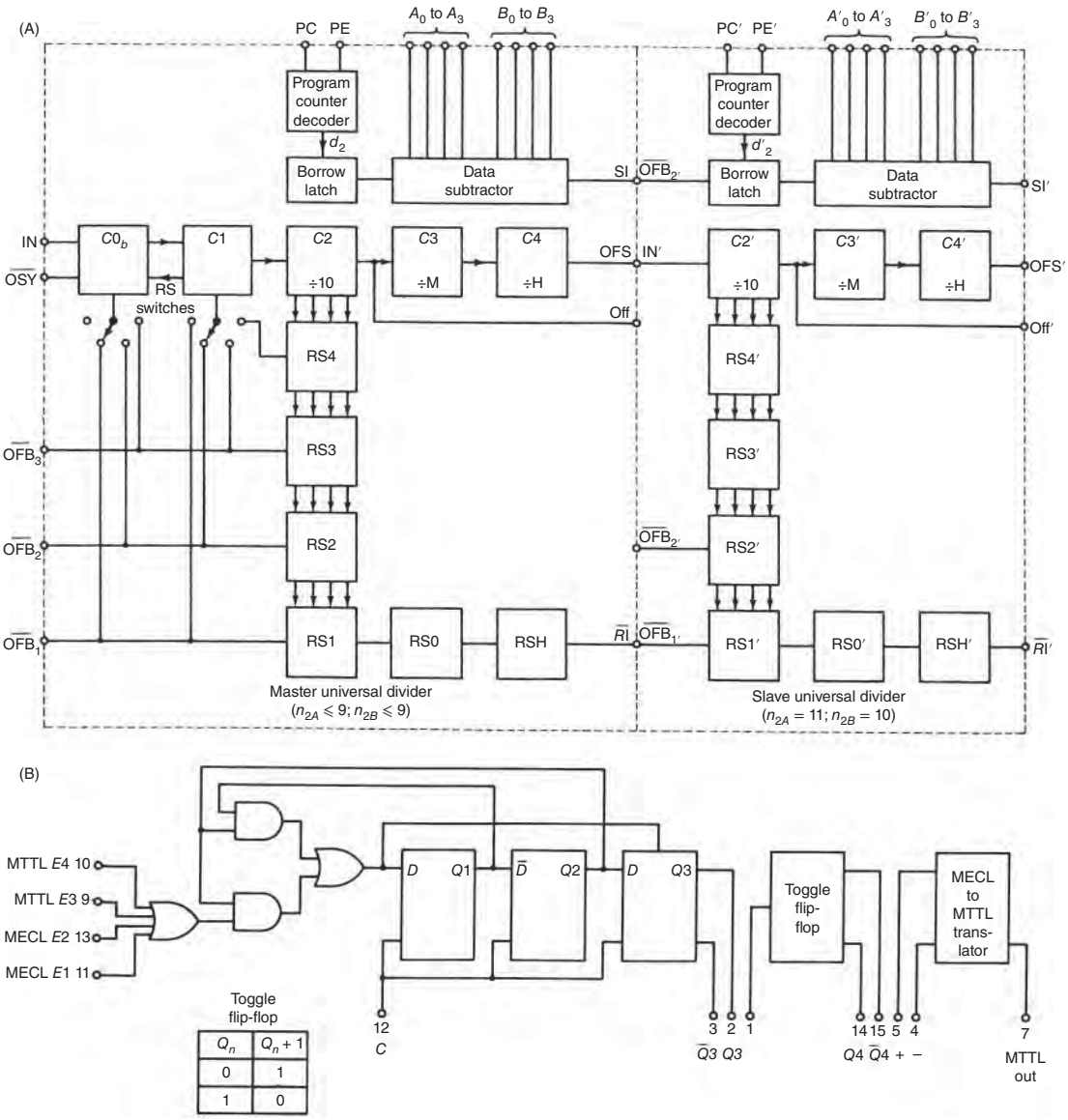


Figure 4-146 Block diagram of the Motorola MC1202 universal dual-modulus counter. (*Courtesy of Motorola Semiconductor Products, Inc.*)

The most popular swallow counters are the 95H90 (350 MHz) and 11C90 (520 MHz) made by Fairchild, and the Plessey SP8692 (200 MHz, 14 mA, 5/6), SP8691 (200 MHz, 14 mA, 8/9), SP8690 (200 MHz, 14 mA, 10/11), and SP8786 (1300 MHz, 85 mA, 20/22). The division ratio of a swallow counter is controlled by two inputs. The counter will divide by 10 when either input is in the high state and by 11 when both inputs are in the low state.

This 10/11 division ratio enables one to build fully programmable dividers to 500 MHz. The switch counting principle means that high frequency prescaling occurs without any reduction in comparison frequency. The disadvantage of this technique is that a fully programmable divider is required to control the 10/11 division ratio and that a minimum limit is set on the possible division ratio, although this is not a serious problem in practice. Figure 4-147 uses a division ratio of $P/(P+1)$, which is set to 10/11. The A counter counts the units, and the B counter counts the tens.

Consider the system shown in Figure 4-147. If the $P/(P+1)$ is a 10/11 divider, the A counter counts the units and the M counter counts the tens. The mode of operation depends on the type of programmable counter used, but the system might operate as follows. If the number loaded into A is greater than zero, then the $P/(P+1)$ divider is set to divide by $P+1$ at the start of the cycle. The output from the $P/(P+1)$ divider clocks both A and M. When A is full, it ceases counting and sets the $P/(P+1)$ divider into the P mode. Only M is then clocked, and when it is full, it resets both A and M and the cycle repeats.

The divider chain therefore divides by

$$(M-A)P + A(P+1) = MP + A \tag{4-268}$$

Therefore,

$$f_{\text{out}} = (MP + A)f_{\text{ref}} \tag{4-269}$$

If A is incremented by one, the output frequency changes by f_{ref}. In other words, the channel spacing is equal to f_{ref}. This is the channel spacing that would be obtained with a fully programmable divider operating at the same frequency as the $P/(P+1)$ divider.

For this system to work, the A counter must underflow before the M counter does; otherwise, $P/(P+1)$ will remain permanently in the $P+1$ mode. Thus, there is a minimum system division ratio, M_{min}, below which the $P/(P+1)$ system will not function. To find that minimum ratio, consider the following.

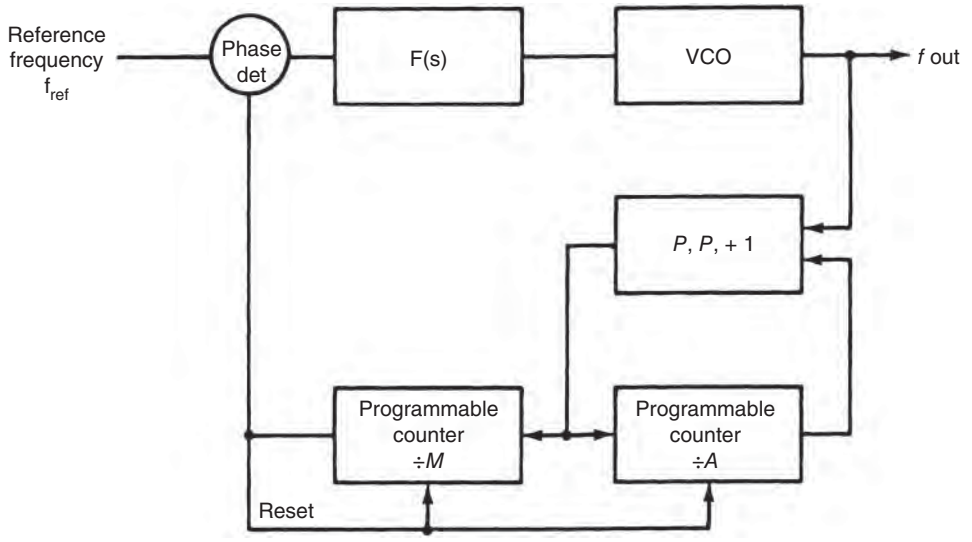


Figure 4-147 System using dual-modulus counter arrangement.

The A counter must be capable of counting all numbers up to and including $P-1$ if every division ratio is to be possible, or

$$A_{\max} = P - 1 \tag{4-270}$$

$$M_{\min} = P \text{ since } M > A \tag{4-271}$$

The divider chain divides by $MP + A$; therefore, the minimum system division ratio is

$$\begin{aligned} M_{\min} &= M_{\min}(P + A_{\min}) \\ &= P(P + 0) = p^2 \end{aligned} \tag{4-272}$$

Using a 10/11 ratio, the minimum practical division ratio of the system is 100.

In the system shown in Figure 4-147, the fully programmable counter, A, must be quite fast. With a 350-MHz clock to the 10/11 divider, only about 23 ns is available for counter A to control the 10/11 divider. For cost reasons it would be desirable to use a TTL fully programmable counter, but when the delays through the ECL-to-TTL translators have been taken into account, very little time remains for the fully programmable counter. The 10/11 function can be extended easily, however, to give a $+N(N+1)$ counter with a longer control time for a given input frequency, as shown in Figures 4-149 and 4-150. Using the 20/21 system shown in Figure 4-148, the time available to control 20/21 is typically 87 ns at 200 MHz and 44 ns at 350 MHz. The time available to control the 40/41 (Figure 4-149) is approximately 180 ns at 200 MHz and 95 ns at 350 MHz.

This frequency-division technique can, of course, be extended to give 80/81, which would allow the control to be implemented with CMOS, but which would increase the minimum division ratio to 6400 (80^2). This ratio is too large for many synthesizer applications, but it can be reduced to 3200 by making the counter an 80/81/82. Similarly, a 40/41 can be extended to 40/41/42, as shown in Figure 4-150 to reduce the minimum division ratio from 1600 to 800. The available time to control the 40/41/42 is a full 40 clock pulses (i.e., 200 ns with a 200-MHz input clock or 110 ns at 350 MHz). The principle of operation is as follows:

$$\text{Minimum division ratio}$$

$$800 = (20 \times 40) + (0 \times 41) + (0 \times 42)$$

$$801 = (19 \times 40) + (1 \times 41)$$

$$802 = (19 \times 40) + (2 \times 42)$$

More information can be found in [85].

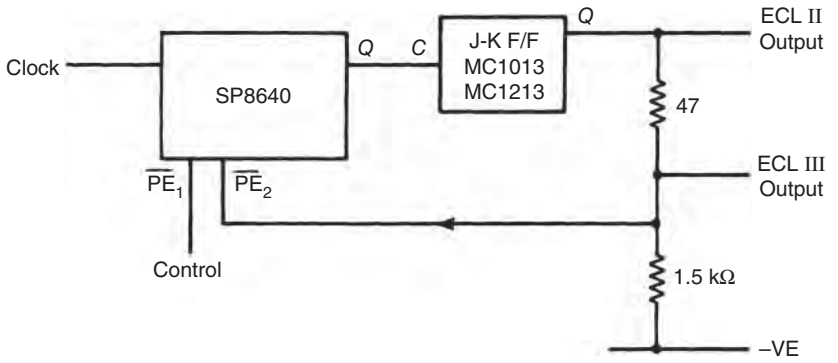


Figure 4-148 Level shifting information for connecting the various ECL2 and ECL3 stages.

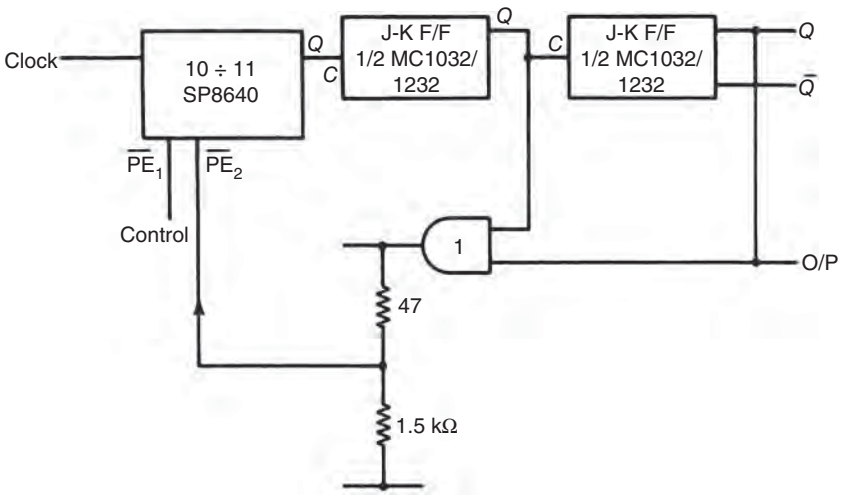


Figure 4-149 Level shifter diagram to drive from ECL2 and ECL3 levels.

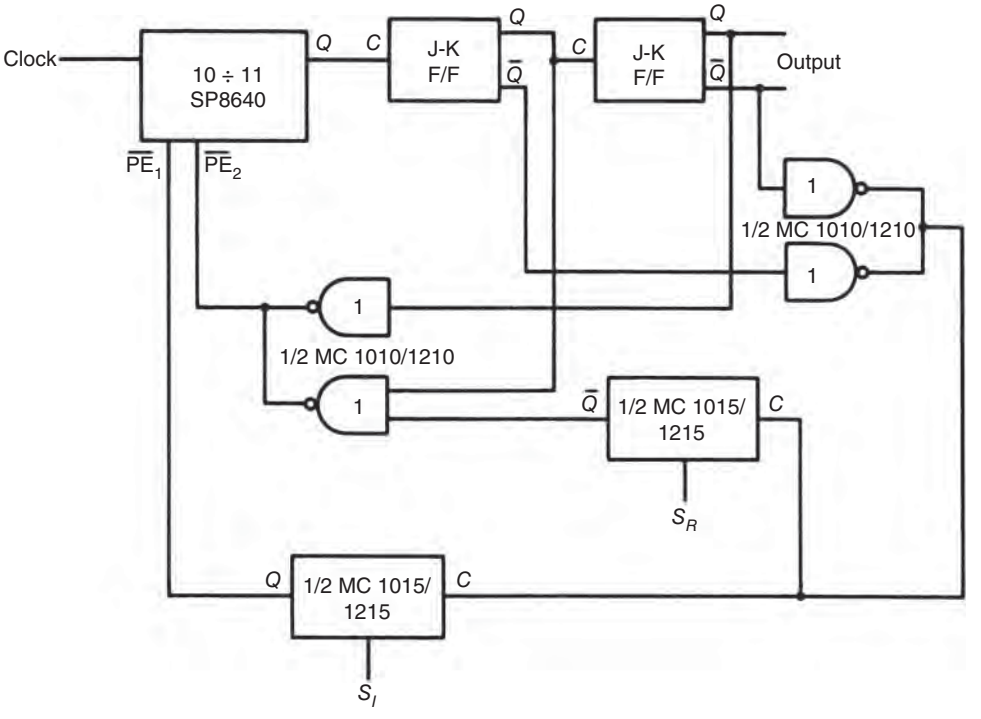


Figure 4-150 40/41/42 three-modulus counter.

4-9-5 Look-Ahead and Delay Compensation

The swallow counter can be used, as we have seen, as a synchronous counter, often referred to as a prescaler. The term "prescaler" for a dual-modulus or swallow counter is really not recommended because a prescaler refers to a divider inserted between the VCO and the programmable divider, which is not necessarily resettable at the same clock rate, and therefore, one loses resolution. Let us consider a typical example. Assume that we have a VCO operating from 100 to 200 MHz, and we use a divide-by-10 prescaler followed by a programmable divider that drives a phase comparator with a reference input of 1 kHz. If this phase-locked loop is closed, we will find that, for each 1-kHz step, the programmable divider is changed; in reality, we get a 10-kHz step at the output frequency of the VCO. This indicates that the prescaler is not in synchronous condition with the other counters. The dual-modulus technique, when applied properly, allows the frequency extension of standard dividers without losing resolution.

All the various integrated circuits have a propagation delay, especially the CMOS integrated circuits, as they are much slower than the ECL.

We are now concerned with analyzing a programmable divider using a 95H90 divide-by-10/11 counter.

Let us take look at Figure 4-151. The frequency range of 21.500–49.990 from a VCO will be divided down to a 10-kHz reference. Four counters and several flip-flops are required to provide the necessary timing. It seems convenient to divide this module into two portions and analyze them first.

- 10/11 divider with control counter.
- Programmable dividers with decoding.

The programmable dividers, as well as decoders, can be built in discrete CMOS technology. A programmable divider is the CD4018. They can be used as divide-by-N counters and will operate at a maximum clock frequency of 5 MHz. Therefore, we will use the 95H90 Fairchild divide-by-10/11 counter. [Note that the device is called a $P/(P+1)$ counter rather than a prescaler.] It was mentioned earlier that there are several different dividers available in ECL technology, and this particular circuit was later used in the design of the Plessey 8940 to reduce power consumption. However, this change does not affect the operating principle. The three programmable dividers permit a division ratio from 002 to 999. The dividers are being programmed via five lines using the Johnson code, where a 00001 equals 0 in decade count, 00011 is equivalent to 1, and so on. As the counter always returns to the zero position, the input must be arranged so that the 9 is equivalent to a 0 count in the counter, position 8 is equivalent to a 1 count, position 7 to a 2 count, and so on. In this case, the counter gets the command to divide by 10, which means that the following counter gets one-tenth of the input. At the same time, the outputs $\overline{Q}_1$ to $\overline{Q}_5$ of the divider can be decoded, and it can be checked whether the end pulse has reached the divider and one cycle is finished. This information will be used to reset the counter to its original condition. In the case of the three-digit counter,

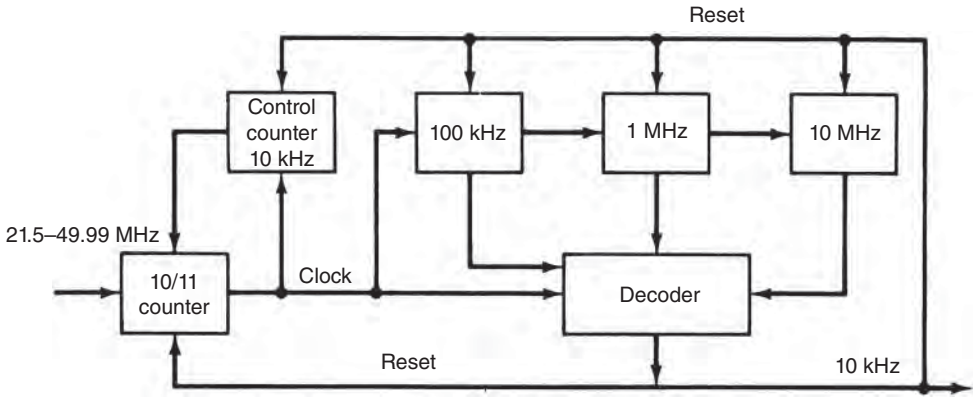
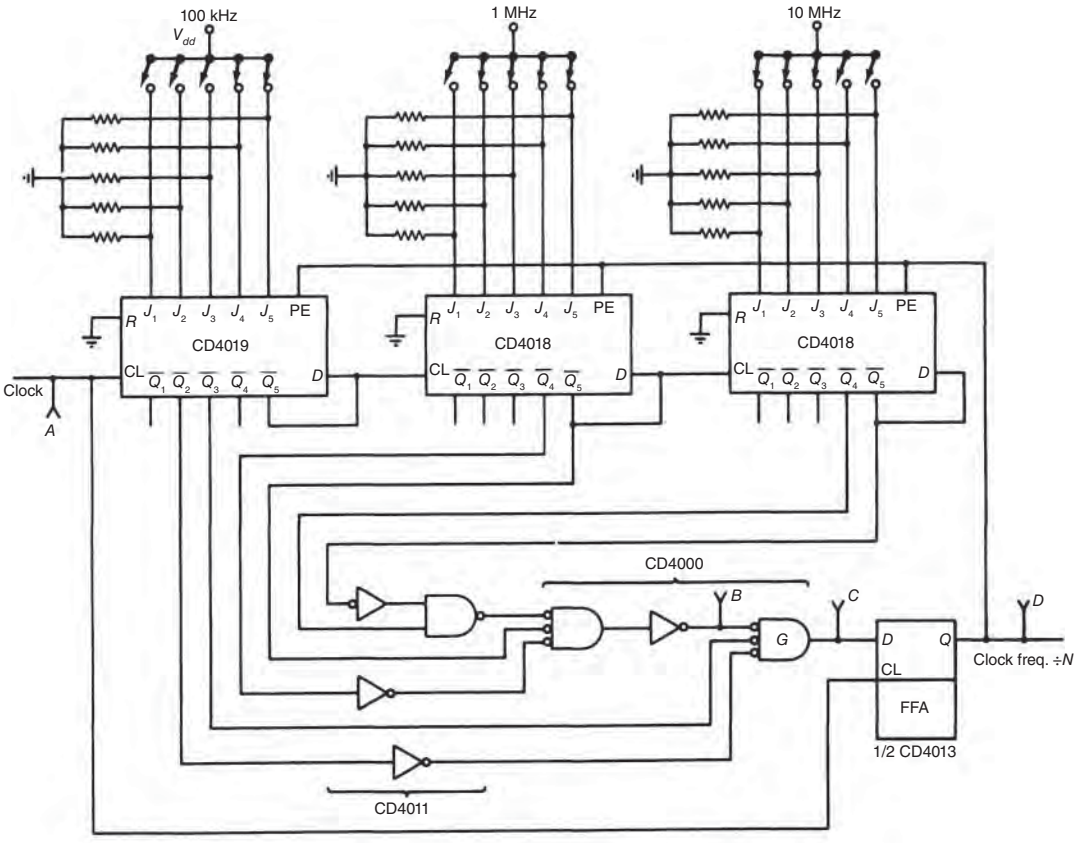


Figure 4-151 Simplified block diagram of the four-stage counter using swallow counter principle and programmable counters.



First decade

SW. POS. *N*	Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0

Second decade

SW. POS. *N*	Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0

Third decade

SW. POS. *N*	Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0

Note: "*N*" is selected by dialing in the desired preset count indicated by the switch settings: The "g" counts from the second and third decade (shown as 1|0) are geted with the "7" count (shown as 1|0) from the first decade to activate the "preset enable" once per counter cycle.

Figure 4-152 Schematic of the CMOS divider section and its truth table.

one cycle is finished after all three stages deliver the pulses simultaneously, which are decoded and form the output and reset pulse. Figure 4-152 shows the CMOS divider chain including the truth table. The programmable inputs J_1 through J_5 are tied to Vdd via 100 kΩ resistors. If the switch is closed, logic 1 applies. The complete divider is being reset via PE after one cycle is complete and the output flip-flop goes to logic 1. Since each of the dividers contains five flip-flops, $\overline{Q}_5$ outputs are available, which, connected with *D*, allow the determination of the division.

$\overline{Q}_5$-*D* results in divide by 10, $\overline{Q}_4$, $\overline{Q}_5$-*D* results in divide by 9, $\overline{Q}_4$-*D* results in divide by 8, and so on. It is important to understand that the five outputs $\overline{Q}_1$ to $\overline{Q}_5$ provide a pulse sequence that allows a function of the clock pulses to obtain the output pulse. This is shown in the previously indicated truth table. Let us assume that the third input pulse should be detected at the $\overline{Q}$ outputs; the 3-equivalent, 6, has to be programmed. Therefore, the divider requires three steps until $\overline{Q}_4$ is at 1 and $\overline{Q}_5$ is at 0. Now it becomes apparent that, regardless of what combination is chosen, the final result at the $\overline{Q}$ outputs are always the same. That is the reason why $\overline{Q}_4$ and $\overline{Q}_5$ of the 100-kHz and 10-kHz dividers are being used. The 1-MHz divider decodes at $\overline{Q}_2$ and $\overline{Q}_3$, which means that, two pulses prior to the cycle count, the information is extended. The reason for this, as we will see in more detail, is to compensate for the delays in the decoders, gates, and flip-flops.

Division by 584

Let us assume that $\overline{Q}_4$ and $\overline{Q}_5$ of the 1-MHz divider decode *t*. Also, the 100-kHz and 10-kHz dividers have reached their final count. Point *B* of the decoder is at zero, and the 1-MHz divider now supplies the pulses as shown in Figure 4-153. It becomes apparent that two pulses of the cycle are lost because of the delay in gate 3 and flip-flop A. If the 1-MHz divider is decoded in such a way that it provides an output two pulse counts earlier, the delay is compensated.

10/11 Counter (ECL)

We have learned that the CMOS divider can operate up to a maximum of 5 MHz. Higher frequencies can be handled by using the 10/11 counter. The combination of the 10/11 counter and the control circuit together with the additional counter is referred to as a "swallow" counter. This term is used because of the fact that one pulse count is "swallowed" from time to time using the divide-by-10 or divide-by-11 principle. Figure 4-154 shows the truth table determining divide by 10 or divide by 11 as a function of the input at E_1 and E_2 of the 10/11 counter shown in Figure 4-155. To control this facility, a control counter that determines how often one divides by 10 or 11 is required. This circuit works on the principle that, as required, either 10 or 11 input pulses produce one output pulse. At times, one pulse gets removed or swallowed.

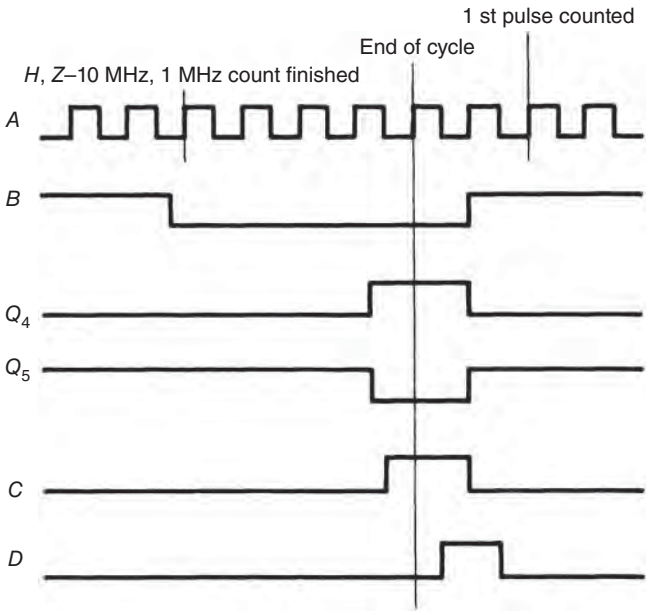


Figure 4-153 Timing diagram of the decoder.

E_1	E_2	÷
0	0	11
0	1	10
1	0	10
1	1	10

Figure 4-154 Truth table of the 10/11 divider.

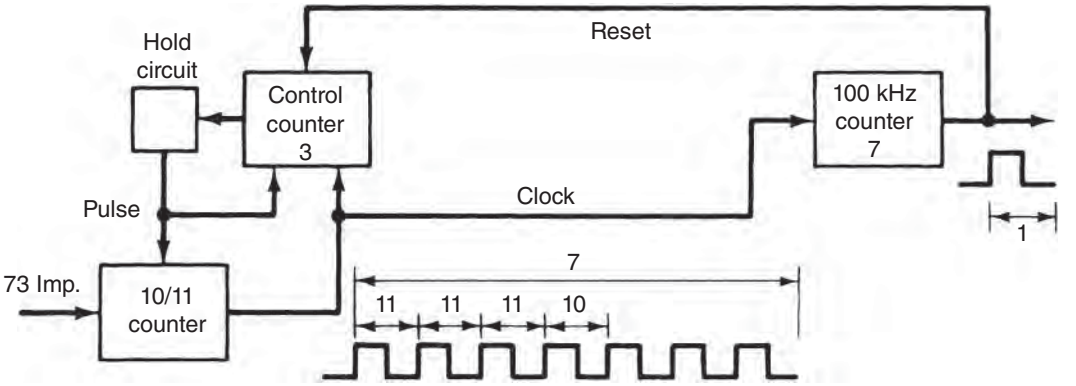


Figure 4-155 Timing of the 10/11 divider.

Example Implementation Let us assume that a two-digit counter is constructed using the 95H90 with a control counter following a CMOS divider. If a division ratio of 73 is required, the 10/11 counter will divide three times by 11; then the control counter is full and the 10/11 counter is set to divide by 10. The programmable divider must take four more sequences, during which it divides by 10. As a result, the output pulse occurs after 73 input pulses. Figure 4-155 shows a block diagram with the timing. The control counter is responsible for the 1-MHz digit, and the programmable counter is responsible for the 10-MHz digit.

Delays

A limitation of this system is that there is a clearly defined minimum division ratio at which the system will no longer function. More critical is the fact that there is a time delay in the 10/11 division path. The delay must not be more than $1/(10/f_{in})$, typically 6 ns, determined by the ECL/CMOS level shifters, the CMOS logic, and back through the CMOS/ECL level shifters. This means that 6 ns prior to the critical pulse, it has to be known whether division by 10 or 11 is required. Only $5/f_{in} - 6$ ns time is available between two pulses. This can be seen from the pulse diagram, Figure 4-156, showing the switching time of the 95H90. Thus, there are limits for the delay.

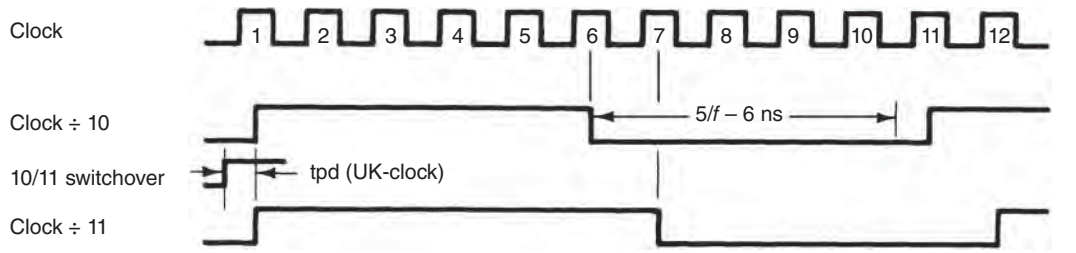


Figure 4-156 Switching and delay times of the 95H90 counter.

Figure 4-157 shows the complete schematic of the divider chain. Before we analyze this circuit in further detail, let us note that the 10/11 counter is shown in the last portion of the figure; the 2N2907 is used as a level shifter from ECL to CMOS and drives the counter chain.

The first CD4018 is the control counter. The swallow counter therefore consists of the 10/11 counter, the control counter, the flip-flop (CD4013), the ECL-to-CMOS level shifter transistor, and the CMOS-to-ECL level shifter being clamped by the two diodes. The gates shown in the circuit are used for decoding purposes, and this function will be discussed when we go into the details of the programmable counter that uses the three CD4018s on the right of the figure. Let us go back to our delays.

(1) There is a limit for the delay. The control counter has to determine the division ratio, divide 10 or 11. It has to be remembered that the prescaler has to be clamped to 10 and the logic that is doing this attains additional delay.
(2) There is a delay from the flip-flop CD4013 via PE and $\overline{Q}_4$ of the control counter to the logic to reset to divide by 11 at the end of the cycle.

According to the data sheet, the CD4018 has a propagation delay for PE–$\overline{Q}_4$ and clock–$\overline{Q}_4$ of 125 ns at 10 V.

To compensate for the delay from clock to $\overline{Q}_4$, it is sufficient to decode the output pulse one count before it actually occurs.

To compensate for the delay in the output flip-flop and PE–$\overline{Q}_4$, a different circuit is required. It is not possible to take the reset pulse for the divide by 10 from the $\overline{Q}$ output of FFN to the 95H90; instead, it has to go through the control counter. In the case where a straight division by 10 is possible, the 10/11 counter must be prevented from dividing by 11. This decision can be made only by the control counter, with the disadvantage that the additional circuit adds additional delay. In a test circuit, it was found that despite the attempted presetting of the control counter, the timing was still not correct. The width of the PE pulse is a function of the clock frequency, and the delays are constant. As a result of this, there are crossovers between the two areas, which prevent proper functioning of the circuit.

Since this is a technological problem, it has to be taken into consideration in the decoding circuit. To understand this better, let us analyze the divider cycle. Let us assume that the divider of the whole system is set at 3754, which means that the output pulse has to occur after 3751 pulses at the input. Regarding the 10/11 counter, the following happens:

$4x \div 11$	44	Control counter full
$296x \div 10$	2960	10-MHz counter full
$70x \div 10$	700	1-MHz counter full
$5x \div 10$	50	100-kHz counter full
	3754	

Figure 4-158 shows the complete cycle. The critical time intervals and positions a, b, c, d, e, f, g, h, and i are indicated.

(a) In this moment, the control counter has to have told the 10/11 counter to switch the division ratio.
(b) Two pulses before final count, decoding is activated.
(c) The *D* input of the flip-flop A receives information "Logic High."
(d) The next clock pulse (e) triggers flip-flop *A*.
(e) This information appears much later at the control counter.
(f) It is now too late to be fed into the 10/11; the same applies for the changing for h and i.

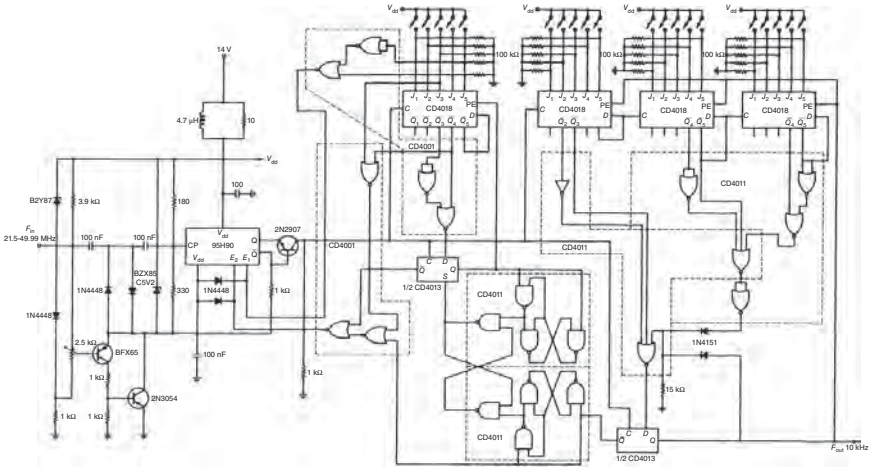


Figure 4-157 Schematic of the 21.5–49.99 MHz divider used for determining the design of delay compensation and look-ahead schematic.

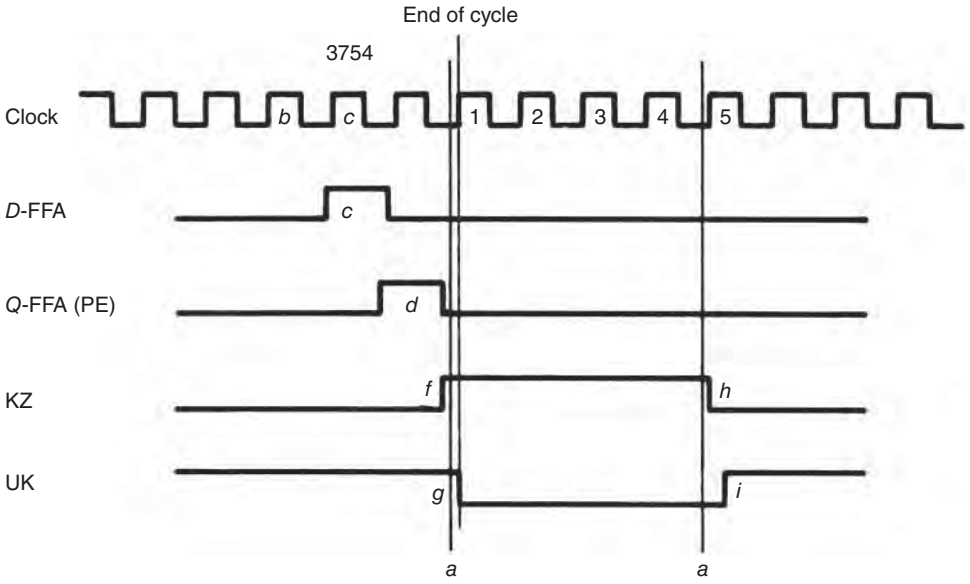


Figure 4-158 Timing diagram for an entire cycle, showing the effects of the various delays.

Analysis During the entire cycle, we divide N times by 11 and it does not matter when in time this happens. It is important only how often the division by 11 occurs. Let us assume that the 10/11 divider receives the "change to" information only after the second pulse, and the control counter follows. This only means that the entire pulse chain is shifted by one count. The final result remains the same. We then get

$$\begin{aligned} 1x \div 10 &\quad 10 \\ 4x \div 11 &\quad 44 \\ 295x \div 10 &\quad 2950 \\ 70x \div 10 &\quad 700 \\ 5x \div 10 &\quad 50 \\ &\quad \overline{3754} \end{aligned}$$

As the 10/11 counter is still set to divide by 10, it will divide by 10 first and then switch over. To do this, a second flip-flop B is required, as well as an NAND latch and two edge detectors FD1 and FD2, which provide only negative pulses at positive edges.

Function The rising signal at $\overline{Q}$ is fed to FD1; at the output of FD1 a very narrow pulse is generated that switches the NAND latch and FFB is set to zero via the S input. The $\overline{Q}$ output of FFB changes the divide ratio of the 10/11 counter using some gates in line. These gates are necessary to support the control counter. As the control counter is being decoded to 1 before its final count, it is not possible to determine the division ratio $1x \div 11$. In this case, the output is taken directly from the control counter, connected with $\overline{Q}$ of FFA and applied to the input E_1.

Figure 4-159 shows the minimum configuration, consisting of the swallow counter (10/11 counter, 95H90 control counter, FFB, latch, FD1, FD2) and the programmable divider chain with its decoder and FFA.

In case there is no requirement to divide by 11, we can take the output from the control counter and apply it directly to the second input of the 10/11 counter. This blocks any switching into the other mode. This can be seen

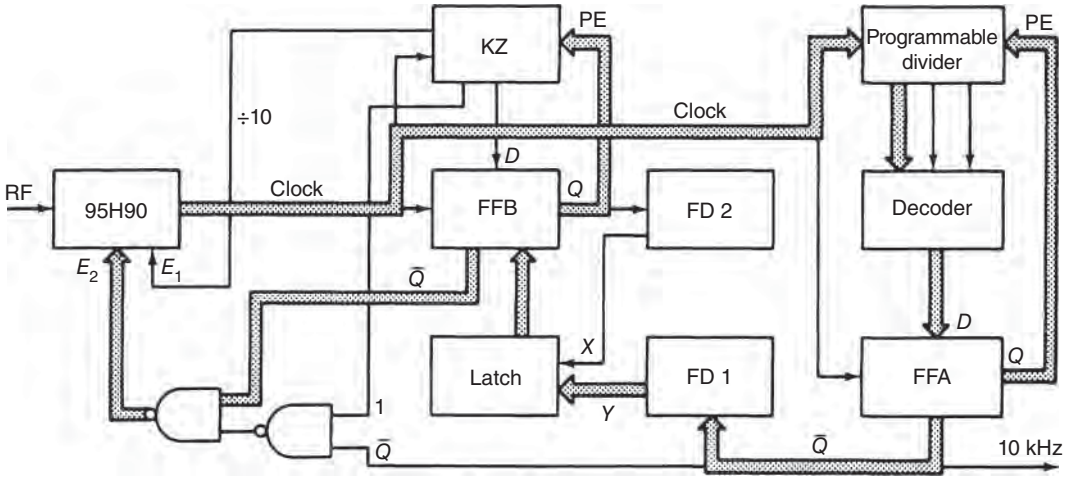


Figure 4-159 Presetting for division-by-11 beginning of the cycle.

from the truth table of the 10/11 counter that was listed earlier. For all other division ratios after the initial division by 11, the 10/11 counter has to be switched to divide by 10. One pulse before the control counter is full, it will supply a logic high to the *D* input of FFB. With the next clock pulse, this information appears at $\overline{Q}$ via the gates to the input E_2. At the same time, FD2 resets the latch and is holding FFB, and therefore the control counter, via the input *S*. Now this cycle is repeated. To further help understanding, the following figures will give more insight. Figure 4-160 shows how the divider chain is set to divide by 10 after the control counter is full; Figure 4-161 shows division $1x \div 11$; Figure 4-162 shows constant division by 10. This circuit was built as indicated by the previously shown complete schematic, and the result confirmed the theoretical discussions. The pulse diagram in Figure 4-163 explains this. The 10-kHz digit (swallow counter) is set $3x \div 11$. The clock pulses are numbered, and the delays are indicated (ns). The critical positions are marked a, b, c, d, and e (see Figure 4-163).

(a) Because of crosstalk on the printed circuit board, a pulse stretching of the output of FFA became apparent. Two diodes were used to force input *D* of FFA immediately after the output pulse $\overline{Q}$ appears at logic 0. This guarantees that FFA is reset to the next cycle.

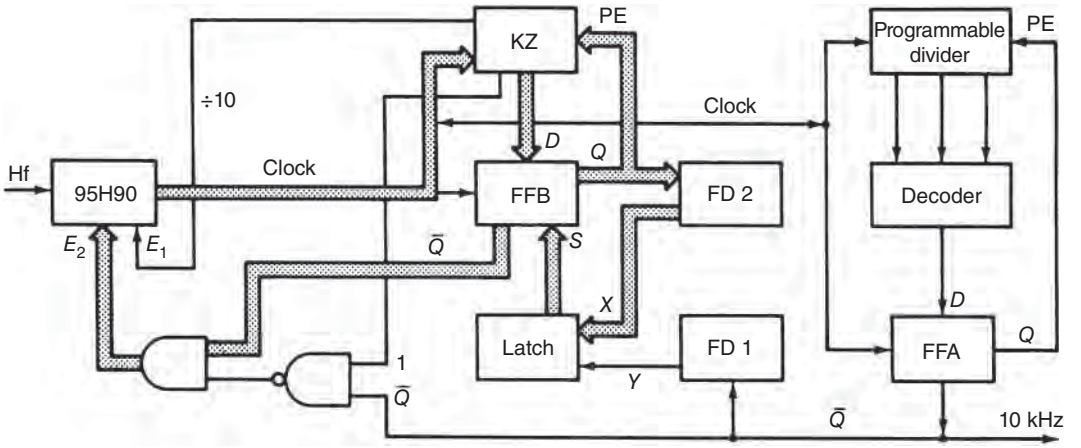


Figure 4-160 Programming of the divider chain to divide by 10 after the control counter is finished.

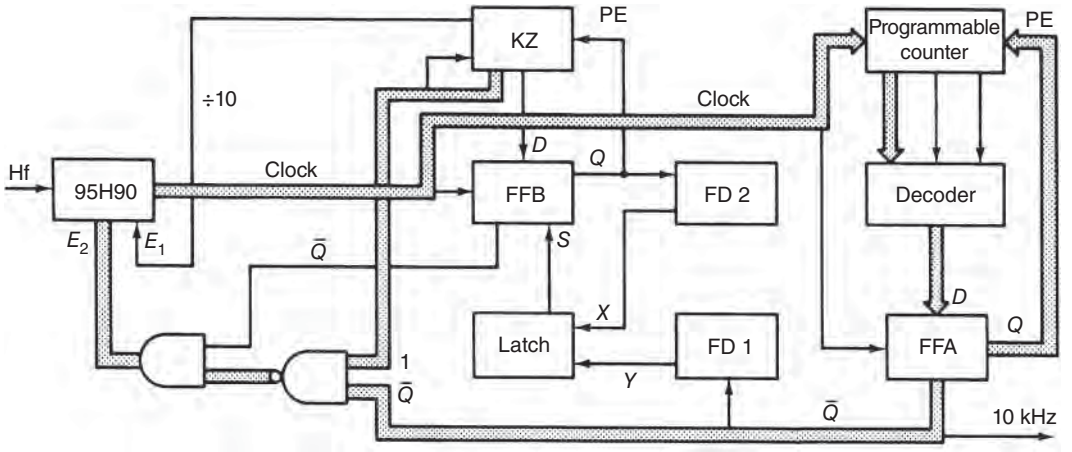


Figure 4-161 $1x \div 11$.

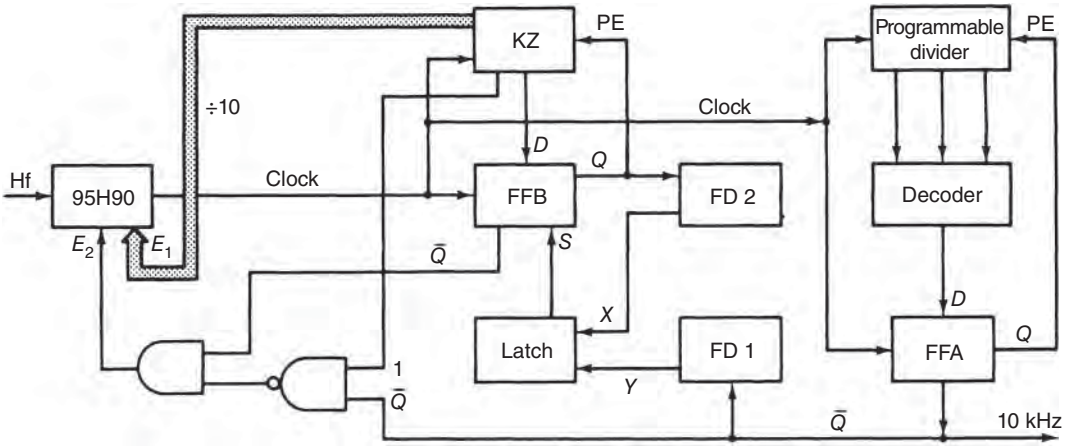


Figure 4-162 Constant division by 10.

(b) Start of the cycle; this can also be seen, as pulse counts start with 1. The clock pulse is shown from −2 to +5.

(c) Maximum time delay is rest.

(d) Maximum time limit for switching divide by 11 to divide by 10.

(e) Maximum time safety margin.

We can deduce from this that the second cycle pulse is being considered as the first pulse to the control counter, while the programmable divider chain reacts to the first clock count of the cycle. Depending on the timing, FFB–$\overline{Q}$ the swallow counter will divide 2 to $9x \div 11$. To divide by 11 only once, a different arrangement is used that sees to it that the changeover command for the divide by 10/11 does not occur at the same time as the other reset pulses occur. This is because the pulse is being fed from FFA–$\overline{Q}$ to E_2 independent of FFB. A several-nanosecond time delay is available, and the actual circuit operated up to 55 MHz without difficulties.

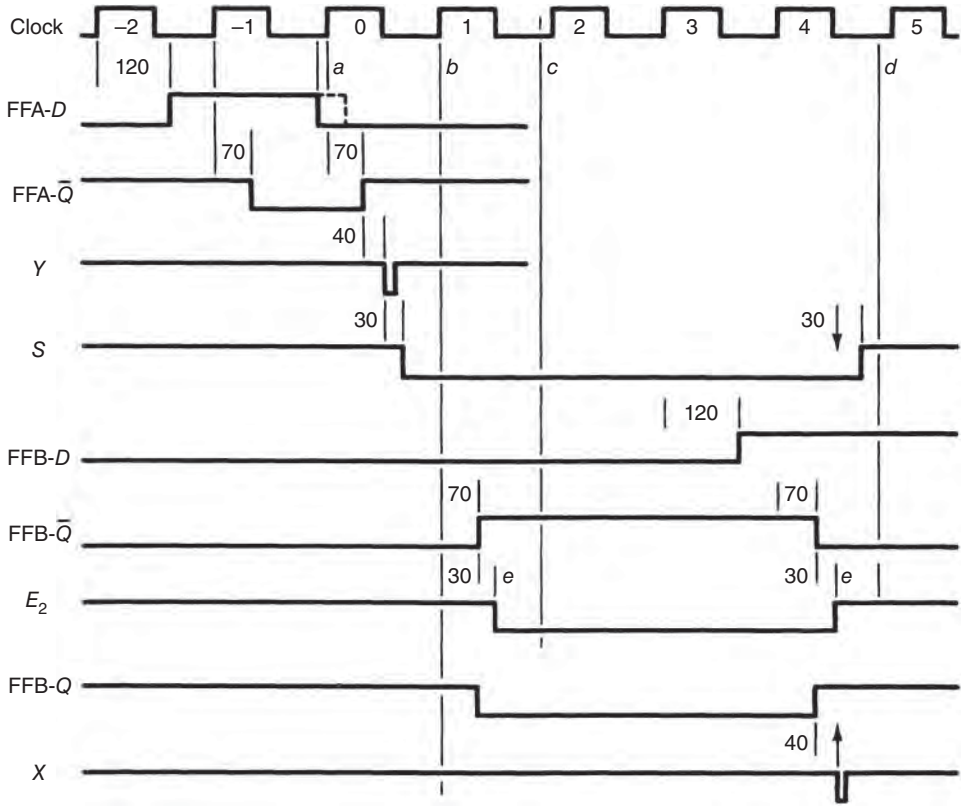


Figure 4-163 Pulse diagram for reset and switchover area for the $3x \div 11$ of the entire system.

Final Comments The circuit has some peculiarities:

(1) Since the entire circuit operates from 14 V and the ECL divider can only be operated from 5.2 V, additional circuitry to provide a voltage drop of 8.8 V, using transistors BFX65 and 2N3054, was used. In a practical battery-operated device, this two-transistor circuit would be replaced by something like the IF and/or RF stages of the receiver to conserve energy, instead of using a voltage regulator, which dissipates energy.

(2) The input of the 95H90 has to be biased with the two resistors. The voltage is set in such a way that 50 mV rms is sufficient to drive the divider at 50 MHz.

(3) There is a voltage difference between the ECL and CMOS dividers, as the ECL operates at 5.2 V and the CMOS at 14 V. The transistor 2N2907 performs the necessary level shift. In order to interface the CMOS to the ECL voltage, a configuration was chosen to avoid a transistor circuit for inputs E_1 and E_2. Two diodes clamp the high-level signals to the V_{ee} level of the 95H90.

(4) Because of the peculiarities of the divider, the 9-equivalent had to be programmed, and nonstandard encoder switches had to be used. This can be avoided by connecting the main contact of the switch to +Vdd.

Finally, the complete circuit was temperature cycled. At 80 °C, the current was 145 mA, and the maximum frequency was 50 MHz. At −20 °C, the current was 128 mA, and the cutoff frequency was 54.5 MHz.

Although this system today could be constructed simply by a few integrated circuits, or even one, the circuit discussed has the advantage that one is forced to go through this detailed analysis, and a better understanding is possible. Some of the other circuits we use later are much easier to deal with. In Chapter 6, a somewhat simpler circuit is analyzed using the same principles.

4-10 LOOP FILTERS

Earlier, we became acquainted with some loop filters, and therefore this may be a repeat of some of the things already treated. As a convenient reference, the four most important filter types are described in the following text.

4-10-1 Passive RC Filters

Figure 4-164 shows the simple RC filter with the transfer equation

$$F(s) = \frac{1/sC}{R + 1/sC} \tag{4-273}$$

or the frequency response

$$F(j\omega) = \frac{1}{j\omega\, CR + 1} \tag{4-274}$$

The magnitude of the frequency response is

$$|F(j\omega)| = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} \tag{4-275}$$

and the phase is

$$\phi(\omega) = -\arctan \omega\, CR \tag{4-276}$$

The lag filter, Figure 4-165, has the transfer function

$$F(s) \frac{sCR_2 + 1}{sC(R_1 + R_2) + 1} \tag{4-277}$$

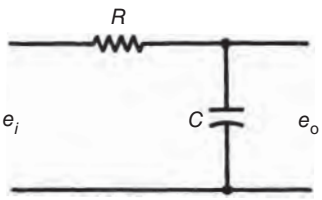


Figure 4-164 RC network.

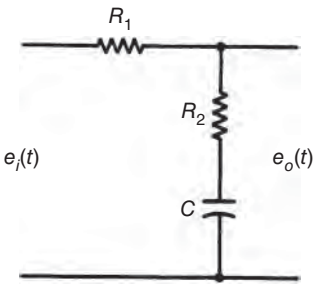


Figure 4-165 Lag filter.

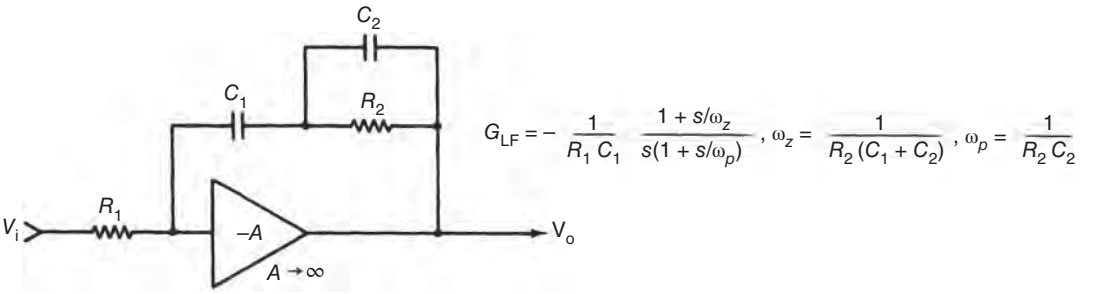


Figure 4-166 Type 2 third-order loop active filter.

The frequency response is

$$|F(j\omega)| = \sqrt{\frac{1 + \omega^2 R_2^2 C^2}{1 + \omega^2 C^2 (R_1 + R_2)^2}} \tag{4-278}$$

4-10-2 Active RC Filters

Any high-performance loop will use an active filter because of the second integrator. Figure 4-166 shows such a circuit. In this particular case, the phase/frequency comparator, B5, having two outputs, drives the inverting and noninverting inputs of an operational amplifier B6. While the same equations hold true as those used with the passive device, note that the same bias as found in the inverting input is provided in the noninverting input to provide a precisely symmetrical load. The additional RC network ahead of the loop filter is used for spike suppression. The 560 Ω/2200 pF RC combination can be calculated, and its effect can be determined by using the last of the computer programs. However, in the practical world, this filter is optimized experimentally.

A type 2 third-order loop, as well as higher-order loop versions, is created by adding additional *RC* time constants.

The real-life situation always requires some additional filtering, or the parasitic elements in a circuit act as such. Figure 4-166 shows the filter of the type 2 third-order loop that was discussed earlier.

Taking the three time constants as

$$T_1 = C_1 R_1 \tag{4-279}$$

$$T_2 = R_2 (C_1 + C_2) \tag{4-280}$$

$$T_3 = C_2 R_2 \tag{4-281}$$

the transfer characteristic is

$$F(s) = \frac{1}{sT_1}\frac{1 + sT_2}{1 + sT_3} \tag{4-282}$$

Sometimes higher orders occur because of some additional LPF requirement. Figure 4-166 can be redrawn in the form of Figure 4-167, which is electrically equivalent provided that V_0 is unloaded.

The correlations are

$$G_{LF1} = -\frac{1}{R_1 C_1}\frac{1 + s/\omega_z}{s(1 + s/\omega_p)} \tag{4-283}$$

$$\omega_z = \frac{1}{R_2 (C_1 + C_2)} \tag{4-284}$$

$$\omega_p = \frac{1}{R_2 C_2} \tag{4-285}$$

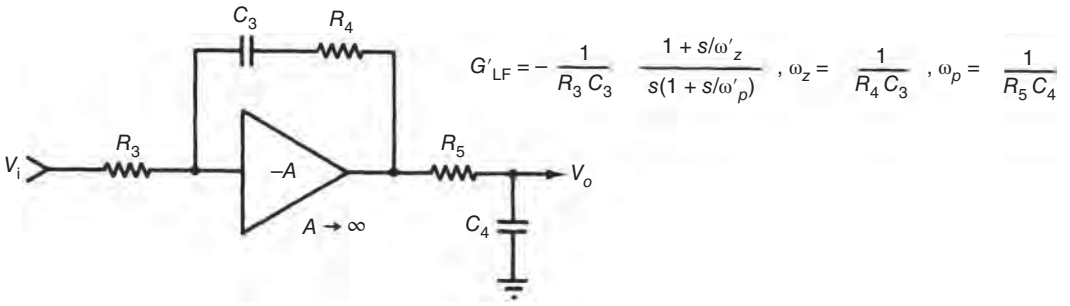


Figure 4-167 The additional RC output filtering converts this into a type 2 third-order loop filter.

$$G_{\mathrm{LF2}} = -\frac{1}{R_3 C_3}\frac{1 + s/\omega_z}{s(1 + s/\omega_p)} \tag{4-286}$$

$$\omega_z = \frac{1}{R_4 C_3} \tag{4-287}$$

$$\omega_p = \frac{1}{R_5 C_4} \tag{4-288}$$

Using these equations, one schematic can be transformed into the other.

In a type 2 fifth-order loop, an active LPF was added. The following sections give some insight into the mathematics of the active LPF, which then becomes part of the loop filter.

4-10-3 Active Second-Order Low-Pass Filters

Active filters, compared with their passive counterpart, have a more rectangular frequency response, allowing for better noise suppression without sacrifice of reference suppression.

In Chapter 1 we saw the transient response of the type 2 fifth-order loop, which was generated from a type 2 third-order loop with the addition of a second-order LPF. Although there are various configurations available with which to build a second-order LPF, the one shown in Figure 4-168 is probably the most useful if noninverting operation is desired. The following is a short derivation of this type of filter and some applications of its use. We would like to state here that with this filter, depending on whether a Butterworth or Chebyshev response or something in between is chosen, different phase shifts and amplitude responses are obtained. By trading off skirt slope versus phase shift, it can be adapted for the purpose. The advantage of an active LPF over a passive attenuator such as the T-notch filter is its LPF action; the T-notch filter filters out only the particular frequency to which it is tailored. It seems that generally the second-order LPF is a better choice provided that the operational amplifier used for this circuit does not introduce intolerable noise.

Let us use the abbreviation $j\omega = p$ and assume that the inverting and noninverting inputs have the same potential. We obtain the following equations:

$$V_o = V - i_1 R - i_2 R - i_1 R \tag{4-289}$$

$$V_o = V - i_1 R - i_2 R - i_2 \frac{1}{pC_1} \tag{4-290}$$

$$V_o = i_1 \frac{1}{pC_2} \tag{4-291}$$

or

$$i_1 = V_o p C_2 \tag{4-292}$$

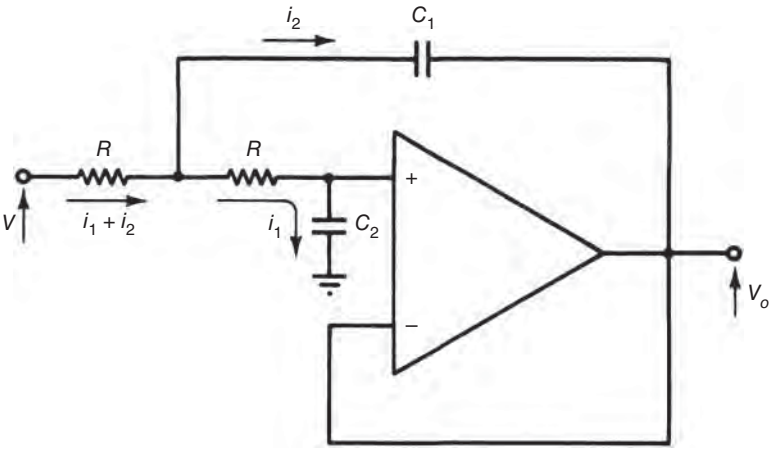


Figure 4-168 Active second-order low-pass filter.

Substituting Eq. (4-292) into Eq. (4-289), we obtain

$$V_o = V - 2RV_o pC_2 - i_2 R \tag{4-293}$$

and from Eq. (4-293),

$$i_2 = \frac{V - V_o - 2RV_o pC_2}{R} \tag{4-294}$$

With Eq. (4-292), and Eq. (4-294) in Eq. (4-290), we obtain

$$V_o = V - RV_o pC_2 - V + V_o + 2RV_o pC_2 - \frac{V - V_o - 2RV_o pC_2}{Rp\,C_1} \tag{4-295}$$

$$R^2 V_o p^2 C_1 C_2 - V + V_o + 2RV_o pC_2 = 0 \tag{4-296}$$

$$V_o(R^2 p^2 C_1 C_2 + 2RpC_2 + 1) = V \tag{4-297}$$

The transfer function is

$$\frac{V_o}{V} = \frac{1}{R^2 p^2 C_1 C_2 + 2RpC_2 + 1} \tag{4-298}$$

from

$$R^2 C_1 C_2 = \frac{1}{\omega_n^2} \tag{4-299}$$

We define the frequency as

$$\omega_n = \frac{1}{R\sqrt{C_1 C_2}} \tag{4-300}$$

Normalizing the values p, C_1, and C_2 yields

$$p_o = \frac{p}{\omega_c} \tag{4-301}$$

where ω_c is the cutoff frequency, and

$$C_{1N} = RC_1\omega_c \tag{4-302}$$

$$C_{2N} = RC_2\omega_c \tag{4-303}$$

We finally obtain

$$\frac{V_o}{V} = \frac{1}{p_o^2 C_{1N} C_{2N} + 2p_o C_{2N} + 1} \tag{4-304}$$

To solve this equation, we find the binomial expression for the denominator,

$$\frac{1}{p_o^2 C_{1N} C_{2N} + 2p_o C_N + 1} = \frac{1}{(p - P_1)(p - P_2)} \tag{4-305}$$

where P_1 and P_2 are conjugate roots of the form $(a \pm jb)$ and

$$\frac{1}{(p - P_1)(p - P_2)} = \frac{1}{(p + a \pm jb)^2} = \frac{1}{p^2 + 2ap + a^2 + a^2} \tag{4-306}$$

or

$$p_o^2 C_{1N} C_{2N} + 2p_o C_{2N} + 1 = p_o^2 + 2ap_o + a^2 + b^2 \tag{4-307}$$

with

$$p_o^2 C_{1N} C_{2N} = p_o^2 \tag{4-308}$$

$$2p_o C_{2N} = 2ap_o \tag{4-309}$$

$$1 = a^2 + b^2 \tag{4-310}$$

We finally obtain the coefficients C:

$$(a^2 + b^2) C_{2N} 2p_o = 2ap_o \tag{4-311}$$

$$C_{2N} = \frac{a}{a^2 + b^2} \tag{4-312}$$

$$C_{1N} = \frac{1}{a} \tag{4-313}$$

The conjugate roots of the Chebyshev approximation are

$$P_v = -\sin \frac{2v - 1}{2n} \pi \sinh \phi + j \cos \frac{2v - 1}{2n} \pi \cosh \phi \tag{4-314}$$

where

$$\sinh \phi = \frac{1}{2} \left\{ \left[\left(1 + \frac{1}{\varepsilon^2} \right)^{1/2} + \frac{1}{\varepsilon} \right]^{1/n} - \left[\left(1 + \frac{1}{\varepsilon^2} \right)^{1/2} + \frac{1}{\varepsilon} \right]^{-1/n} \right\} \tag{4-315}$$

$$\cosh \phi = \frac{1}{2} \left\{ \left[\left(1 + \frac{1}{\varepsilon^2} \right)^{1/2} + \frac{1}{\varepsilon} \right]^{1/n} + \left[\left(1 + \frac{1}{\varepsilon^2} \right)^{1/2} + \frac{1}{\varepsilon} \right]^{-1/n} \right\} \tag{4-316}$$

with ε^2 the ripple tolerance.

Rather than looking up normalized values from published tables (Chebyshev filters have good stopband attenuation with small passband phase distortion), a ripple factor can be chosen and then the loop should be analyzed for phase margin. If the ripple is too high, it can be changed to obtain the desired response. This is done very easily by defining a damping factor,

$$d^2 = \frac{1}{a^2 + b^2} = \frac{C_2}{C_1} \tag{4-317}$$

The ripple is inversely proportional to the damping factor. With $d = 1/\sqrt{2}$, the ripple is zero (i.e., Butterworth response). Smaller d values render increased ripple and increased stopband attenuation. What remains to be determined is ω_n, of which a good starting value is five times the required loop cutoff frequency. Modifying

$$d = \sqrt{\frac{C_2}{C_1}} \tag{4-318}$$

and ω_n in the overall open-loop transfer function while Bode plotting will render the required phase and gain margins for stable loop performance. A phase margin of >30° to <70° for $|A(p) \doteq 1|$ and a gain margin of −10 dB for a phase value of 180° should be sought.

The overall open-loop transfer function is followed by including the damping factor d and the natural pole frequency ω_n:

$$A^* = \frac{\omega_n^2}{-\omega^2 + 2dp\omega_n + \omega_n^2} \tag{4-319}$$

and therefore, the open-loop gain of a type 2 fifth-order loop as an example would become

$$A(p) = \frac{\omega_n^2 K_o K_\theta}{NT_1\omega^2} \frac{-pT_2 - 1}{p[2d\omega_n + T_3(\omega_n^2 - \omega)] + (\omega_n^2 - \omega^2 - 2dT_3\omega_n\omega^2)} \tag{4-320}$$

4-10-4 Passive LC Filters

While the active loop RC filter is a convenient way of improving reference suppression, as the realization of LC filters at times may be difficult, the use of normalized tables and an analysis program permits optimizing loops with LC filters. The LC filter in the loop has the distinct advantage that the passive devices do not introduce noise, and filter design is well established. Figure 4-169 shows an LPF with its proper termination at the input and output.

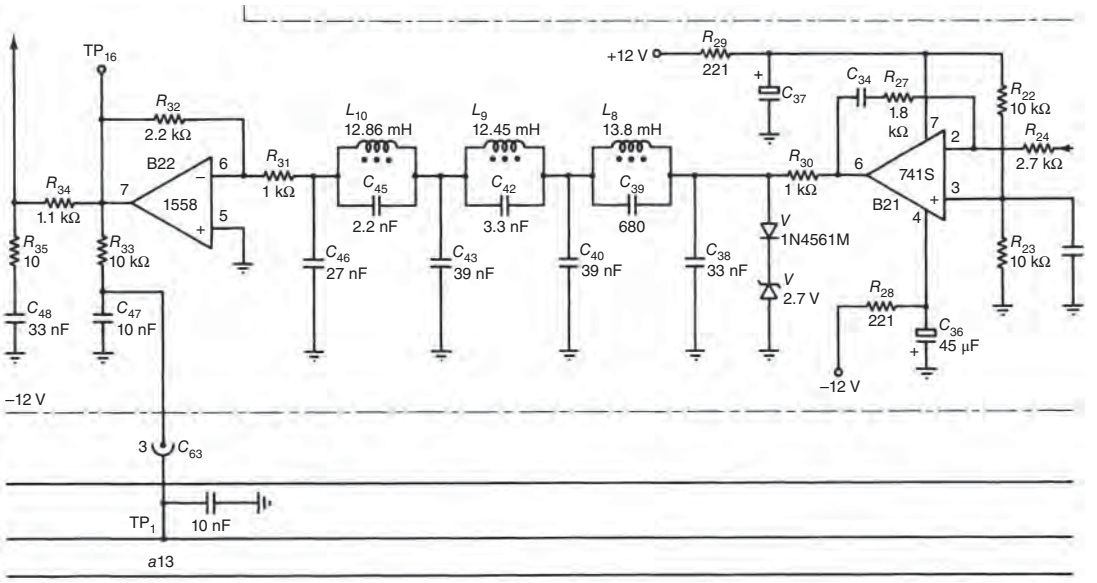


Figure 4-169 Passive *LC* low-pass filter.

Table 4-9 Elliptical low-pass filter CC300750.

θ	30.0
C_1	0.7085
C_2	0.0389
L_2	1.3566
C_3	1.6029
C_4	0.1604
L_4	1.4917
C_5	1.6792
C_6	0.1016
L_6	1.5876
C_7	1.4569
Ω_S	2.0000
$A_{\min}$	105.37
σ_0	0.2036327
σ_1	0.0364992
σ_3	0.1103824
σ_5	0.1756643
Ω_1	0.9936072
Ω_2	4.3544
Ω_3	0.8183516
Ω_4	2.0445
Ω_5	0.4701232
Ω_6	2.4903

The 741 operational amplifier driving the filter theoretically would have zero impedance, but since this is not permissible, the proper filter source resistor R_{30} has to be added. Similarly, R_{31} serves as output termination since pin 6 of B22 is essentially at ac ground potential.

The particular filter chosen here is of the order of 7. Table 4-9 shows the values that can be taken from Anatol Zverev's *Handbook of Filter Synthesis*, page 287 [86]. Similar elliptical filters are found in Rudolf Saal's *Handbook of Filter Design* (AEG Telefunken, West Germany). A description of how to design filters is given in the book and is not repeated here.

4-10-5 Spur-Suppression Techniques

While several methods have been proposed in the literature (see patents in Chapter 3, Section 4.2, "Some Special Past Patents for Fractional Division *N* Synthesizers"), the method of reducing the noise by using a sigma-delta modulator has shown to be most promising. The concept is to get rid of the low-frequency phase error by rapidly switching the division ratio to eliminate the gradual phase error at the discriminatory input. By changing the division ratio rapidly between different values, the phase errors occur in both polarities, positive as well as negative, and at an accelerated rate that explains the phenomenon of high frequency noise push-up. This noise, which is converted to a voltage by the phase/frequency discriminator and loop filter, is filtered out by the LPF. The main problem associated with this noise shaping technique is that the noise power rises rapidly with frequency. Figure 4-170 shows noise contributions with such a sigma-delta modulator in place.

On the other hand, we can now, for the first time, build a single-loop synthesizer with switching times as fast as 6 µs and very little phase-noise deterioration inside the loop bandwidth. Since this system maintains the good phase noise of the ceramic-resonator-based oscillator, the resulting performance is significantly better than the phase noise expected from high-end signal generators. However, this method does not allow us to increase the loop bandwidth beyond the 100 kHz limit, where the noise contribution of the sigma-delta modulator takes over.

Table 4-10 shows some of the modern spur-suppression methods. These three-stage sigma-delta methods with larger accumulators have the most potential [87].

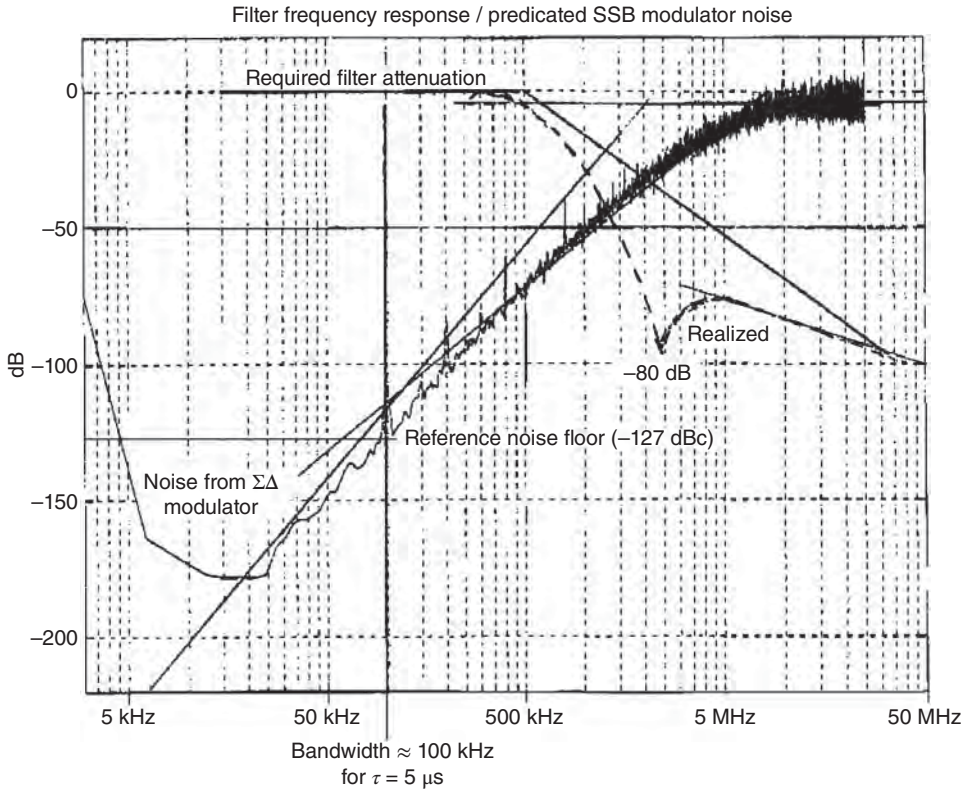


Figure 4-170 The filter frequency response/phase noise analysis graph shows the required attenuation for the reference frequency of 50 MHz and the noise generated by the sigma-delta converter (three steps) as a function of the offset frequency. It becomes apparent that the sigma-delta converter noise dominates above 80 kHz unless attenuated.

Table 4-10 Spur-suppression methods.

Technique	Feature	Problem
DAC phase estimation	Cancel spur by DAC	Analog mismatch
Pulse generation	Insert pulses	Interpolation jitter
Phase interpolation	Inherent fractional divider	Interpolation jitter
Random jittering	Randomize divider	Frequency jitter
Sigma-delta modulation	Modulate division ratio	Quantization noise

The power spectral response of the phase noise for the three-stage sigma-delta modulator is calculated from

$$L(f) = \frac{(2\pi)^2}{12 \cdot f_{\text{ref}}} \cdot \left[2 \sin\left(\frac{\pi f}{f_{\text{ref}}}\right)\right]^{2(n-1)} \text{rad}^2/\text{Hz} \tag{4-321}$$

where n is the number of the stage of the cascaded sigma-delta modulator [87]. Eq. (4-321) shows that the phase noise resulting from the fractional controller is attenuated to negligible levels close to the center frequency, and further from the center frequency, the phase noise is increased rapidly and must be filtered out prior to the tuning input of the VCO to prevent unacceptable degradation of spectral purity. A loop filter must be used to filter the noise in the PLL loop. Figure 4-170 showed the plot of the phase noise versus the offset frequency from the center frequency. A fractional-N synthesizer with a three-stage sigma-delta modulator as shown in Figure 4-171 has been built. The synthesizer consists of a phase/frequency detector, an active LPF, a VCO, a dual-modulus prescaler, a three-stage sigma-delta modulator, and a buffer. Figure 4-172 shows the inner workings of the chip in greater detail.

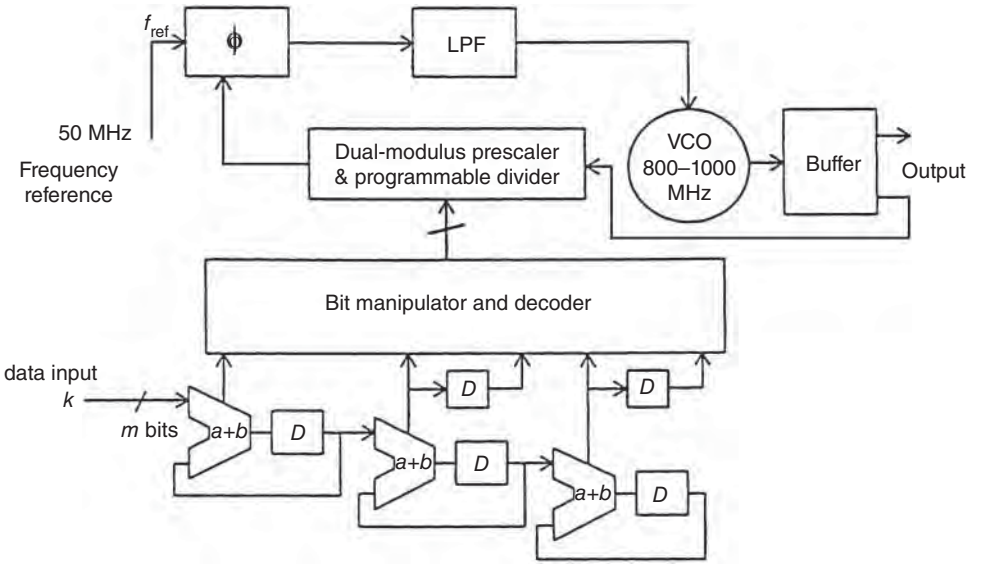


Figure 4-171 Three-stage converter block diagram.

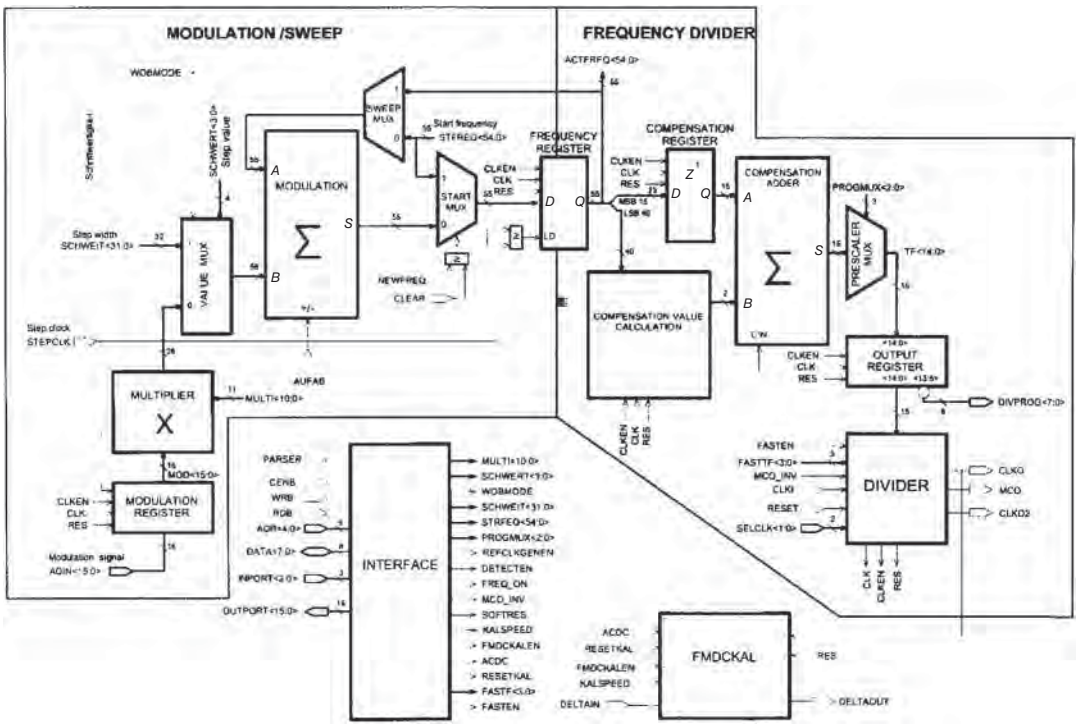


Figure 4-172 Implementation of the synthesizer.

After designing, building, and predicting the phase noise performance of this synthesizer, it becomes clear that the measuring the phase noise of such a system becomes tricky. Standard measurement techniques that use a reference synthesizer would not provide enough resolution because there are no synthesized signal generators on the market sufficiently good enough to measure such low values of phase noise. Therefore, we had to build a comb generator that would take the output of the oscillator and multiply this up 10–20 times.

4-11 MICROWAVE OSCILLATOR DESIGN

The difference between oscillators and microwave oscillators has to do with the fact that microwave oscillators do not rely on lumped elements but rather on distributed ones. Also, certain types of oscillator circuits just cannot be implemented. A good example is that while we can design and build a wideband transformer for the purpose of phase inversion, there is no equivalent to this for microwave applications. This is also true for specialty oscillators such as eight oscillators, where the actual resonant portion is a three-dimensional (3-D) structure. Other types of millimeter-wave oscillators use SAW devices, ceramic resonators, and dielectric resonators (DRs). In certain applications, such as wireless data transmission, the low-cost design requires printed circuit production and a similar approach is true for monolithic microwave integrated circuit (MMIC) oscillators up to millimeter-wave application. Here the resonator is part of the layout and generally the phase noise is determined both by the low Q of the resonator and the low Q of the tuning diodes.

In designing microwave oscillators based on the linear approach (has only educational merit), we continue to look for the negative impedance generated by the transistor, which will overcome the losses and therefore provide oscillation. The two major differences between RF oscillators and microwave oscillators are the following:

(1) For discrete active devices, we will use S-parameters.
(2) For higher frequencies, we will move away from the lumped elements to distributed elements.

We will use different types of resonators, however; their Q will be less than those of crystal oscillators.
The conditions for oscillation can be expressed as

$$k < 1 \tag{4-322}$$

$$\Gamma_G S'_{11} = 1 \tag{4-323}$$

$$\Gamma_L S'_{22} = 1 \tag{4-324}$$

The stability factor should be less than unity for any possibility of oscillation. If this condition is not satisfied, either the common terminal should be changed or positive feedback should be added. Next, the passive terminations Γ_G and Γ_L must be added to resonate the input and output ports at the frequency of oscillation. This is satisfied by either Eq. (4-322) or (4-324). It will be shown that if Eq. (4-232) is satisfied, Eq. (4-324) must be satisfied, and vice versa. In other words, if the oscillator is oscillating at one port, it must be simultaneously oscillating at the other port. Normally, a major fraction of the power is delivered only to one port, since only one load is connected. Since $|\Gamma_G|$ and Γ_L are less than unity, Eqs. (4-323) and (4-324 imply that $|S'_{11}| > 1$ and $|S'_{22}| > 1$.

The conditions for oscillation can be seen from Figure 4-173, where an input generator has been connected to a two-port. Using the following representation,

$$a_1 = b_G + \Gamma_L \Gamma_G a_1 \tag{4-325}$$

and defining

$$\Gamma_L = S'_{11} \tag{4-326}$$

$$S'_{11} = \frac{b_1}{a_1} \tag{4-327}$$

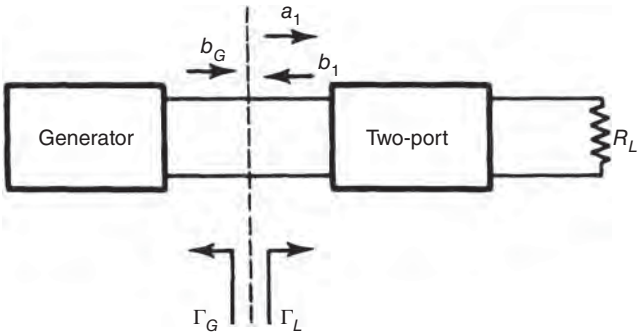


Figure 4-173 Two-port connected to a generator.

we find

$$b_G = a_1(1 - \Gamma_{L1}\Gamma_G)$$
$$= \frac{b_1}{S'_{11}}(1 - S'_{11}\Gamma_G) \tag{4-328}$$
$$\frac{b_1}{b_G} = \frac{S'_{11}}{1 - S'_{11}\Gamma_G} \tag{4-329}$$

Thus, the wave reflected from the two-port is dependent on Γ_G and Γ_L. If Eq. (4-232) is satisfied, b_G must be zero, which implies that the two-port is oscillating. Since Γ_G is normally less than or equal to unity, this requires that $|S'_{11}|$ be greater than or equal to unity.

The oscillator designer must simply guarantee a stability factor less than unity and resonate the input port by satisfying Eq. (4-323), which implies that Eq. (4-324) has also been satisfied. Another way of expressing the resonance condition of Eq. (4-323) is the following:

$$R_{\text{in}} + R_G = 0 \tag{4-330}$$
$$X_{\text{in}} + X_G = 0 \tag{4-331}$$

This follows from substituting

$$S'_{11} = \frac{R_{\text{in}} + jX_{\text{in}} - Z_0}{R_{\text{in}} + jX_{\text{in}} + Z_0} \tag{4-332}$$

$$\Gamma_G = \frac{R_G + jX_G - Z_0}{R_G + jX_G + Z_0}$$
$$= \frac{-R_{\text{in}} - Z_0 - jX_{\text{in}}}{-R_{\text{in}} + Z_0 - jX_{\text{in}}} \tag{4-333}$$

into Eq. (4-232), giving

$$\Gamma_G S'_{11} = \frac{-R_{\text{in}} - Z_0 - jX_{\text{in}}}{-R_{\text{in}} + Z_0 - jX_{\text{in}}} \times \frac{R_{\text{in}} + jX_{\text{in}} - Z_0}{R_{\text{in}} + Z_0 + jX_{\text{in}}} = 1$$

which proves the equivalence of Eq. (4-232) to Eqs. (4-330) and (4-331).

Before proceeding with the oscillator design procedures, some typical oscillator specifications are given in Table 4-11 for the major types of oscillators. The high-Q or cavity-tuned oscillators usually have better spectral

Table 4-11 Typical oscillator specifications.

Parameter	High-Q or cavity-tuned (e.g., YIG)	Low-Q or varactor-tuned VCO
Frequency	2–4 GHz	2–4 GHz
Power	+ 10 dBm	+ 10 dBm
Power variation versus f	±2 dB	±2 dB
Temperature stability versus f	±10 ppm/°C	±500 ppm/°C
Power versus temperature (−30 to 60 °C)	±2 dB	±2 dB
Modulation sensitivity	10–20 MHz/mA	50–200 MHz/V
FM noise	−110 dBc/Hz at 100 kHz	−100 dBc/Hz at 100 kHz
AM noise	−140 dBc/Hz at 100 kHz	−140 dBc/Hz at 100 kHz
FM noise floor	−150 dBc/Hz at 100 MHz	−150 dBc/Hz at 100 MHz
All harmonics	−20 dBc	−20 dBc
Short-term post	±2 MHz	±2 MHz
Tuning drift	1 μs	1–100 μs
Long-term post	±2 MHz	±2 MHz
Tuning drift	5–30 s	5–30 s
Pulling of f for all phases of 12-dB return loss	±1 MHz	±20 MHz
Pushing of f with change of bias voltage	5 MHz/V	5 MHz/V

purity than do the low-Q VCOs, which have faster tuning speeds. The FM noise is usually measured at about 100 kHz from the carrier in units of dBc, which means decibels below the carrier level, in a specified bandwidth of 1 Hz. If the measurement bandwidth is 1 kHz, the specification changes by 10^3.

In selecting a transistor to meet the specifications, the amplifier transistors with the same frequency and power performance are usually suitable. Lower close-in noise can be achieved from silicon bipolar transistors compared with GaAs MESFETs because of the $1/f$ noise difference.

4-11-1 The Compressed Smith Chart

The normal Smith chart is a plot of the reflection coefficient for $|\Gamma| \leq 1$. The compressed Smith chart includes $|\Gamma| > 1$, and the chart is given in Figure 4-174 for $|\Gamma| \leq 3.16$ (10 dB of return gain). This chart is useful for plotting the variation of S'_{11} and S'_{22} oscillator design. The impedance and admittance properties of the Smith chart are retained for the compressed chart. For example, a Γ_{in} of 1.2/150° gives the following values of Z and Y normalized to $Z_0 = 50\,\Omega$:

$$Z_{in}/Z_0 = -0.10 + j0.25$$
$$Z^*_{in}/Z_0 = -0.10 - j0.25$$
$$Y_{in}/Y_0 = -1.0 - j3.0$$
$$Y^*_{in}/Y_0 = -1.0 + j3.0$$

These values are plotted in Figure 4-174 for illustration.

A frequency resonance condition simply requires the circuit imaginary term be zero. If the impedance resonance is on the left-hand real axis, this is a series resonance; that is, at frequencies above resonance the impedance is inductive and below resonance the impedance is capacitive. If the impedance resonance is on the right-hand real axis, the resonance is a parallel resonance; that is, at frequencies above resonance the impedance is capacitive and below resonance the impedance is inductive.

An oscillator resonance condition implies that both the circuit imaginary term and the circuit real term are zero, as given by Eqs. (4-330) and (4-331). Impedances and admittances can be transformed on the compressed Smith chart by the methods discussed; however, when $|\Gamma|$ is greater than unity, the goal of impedance transformation is usually to achieve either a series or a parallel resonance condition. Another method for visualizing negative resistance is to plot $1/S_{11}$ and multiply the result by −1. This allows the designer readily to use available Smith

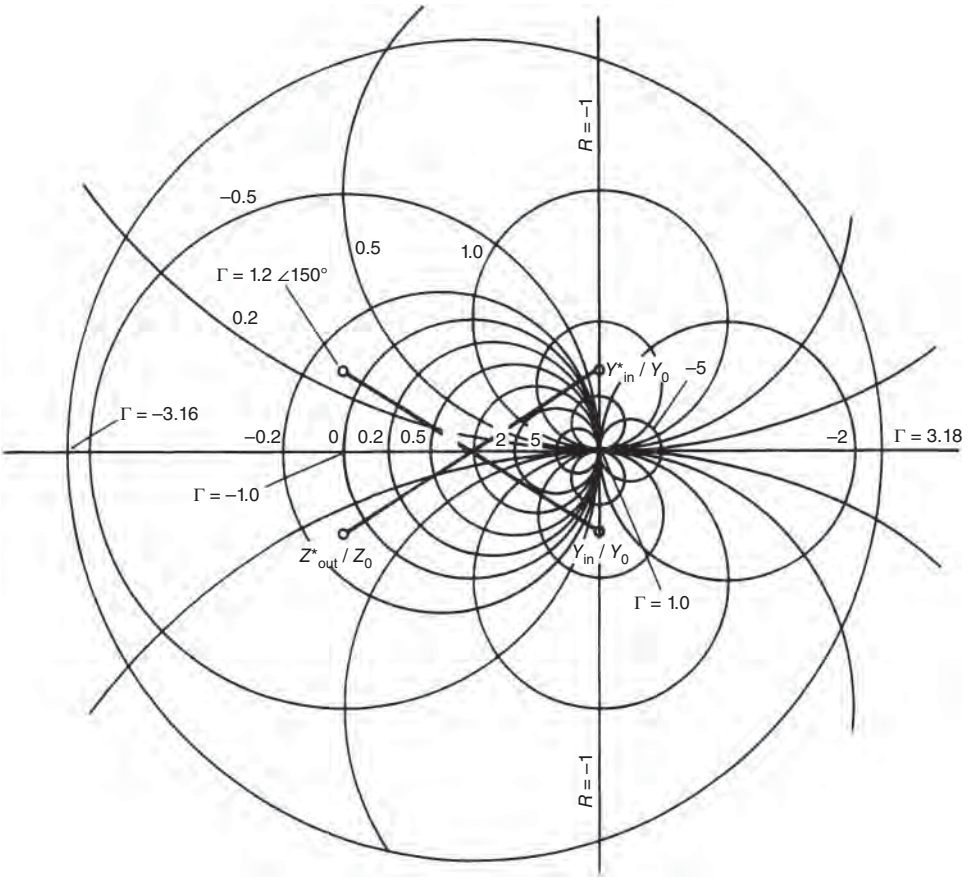


Figure 4-174 Compressed Smith chart.

charts, with $|\Gamma| \geq 1$, to analyze circuits with $|\Gamma| \geq 1$. The proof of this concept can be shown by expressing the reflection coefficient of a one-port by

$$S_{11} = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{4-334}$$

$$\frac{1}{S_{11}} = \frac{Z_s + Z_0}{Z_s - Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{4-335}$$

where $Z_1 = -Z_s$, which gives a negative resistance on Smith chart coordinates. For example, using the case in Figure 4-174, we have

$$S_{11} = 1.2\angle 150°$$

$$\frac{1}{S_{11}} = 0.833\angle -150°$$

$$\frac{Z_1}{Z_0} = 0.10 - j0.25$$

$$\frac{Z_s}{Z_0} = -0.10 + j0.25$$

The impedance of the one-port is plotted at Z_1 but understood to be Z_s.

4-11-2 Series or Parallel Resonance

Oscillators can be classified into two types—series-resonant or parallel-resonant— as shown in Figure 4-175a, b. The equivalent circuit of the active device is chosen from the frequency response of the output port, that is, the frequency response of Γ_L. For the series-resonant condition, the negative resistance of the active device must exceed the load resistance Γ_L at start-up of oscillation by about 20%. As the oscillation builds up to a steady-state value, the resonance condition will be reached as a result of limiting effects, which cause a reduction of Γ_G under large-signal drive.

For start-up of oscillation,

$$|R_G| > 1.2R_L \tag{4-336}$$

For resonance,

$$R_G + R_L = 0 \tag{4-337}$$

$$X_G + X_L = 0 \tag{4-338}$$

For the parallel-resonant condition, the negative conductance of the active device must exceed the load conductance G_L at start-up of oscillation by about 20%. The parallel-resonant oscillator is simply the dual of the series-resonant case. For start-up of oscillation,

$$|G_G| > 1.2G_L \tag{4-339}$$

For resonance,

$$G_G + G_L = 0 \tag{4-340}$$

$$B_G + B_L = 0 \tag{4-341}$$

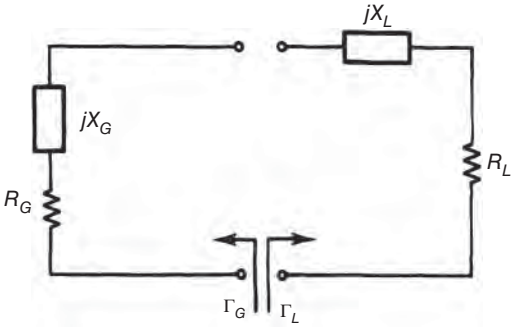


Figure 4-175a Oscillator equivalent circuits: series-resonant.

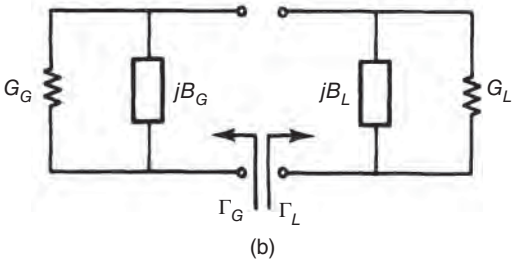


Figure 4-175b Oscillator equivalent circuit: parallel-resonant.

To design the oscillator for series resonance, the reflection coefficient of the active transistor is moved to an angle of 180° (i.e., the left-hand real axis of the compressed Smith chart). Keeping in mind Eq. (4-322) for the input resonating port, we see that a nearly lossless reactance will resonate the transistor. For the example in Figure 4-175a, b, we have

$$\Gamma = 1.2\angle 150° = S'_{11}$$
$$\Gamma_G = 0.83\angle -150° \simeq 1.0\angle -150°$$

The large-signal drive of the transistor will reduce to about $1.0\angle 150°$. For parallel-resonant oscillator design, the reflection coefficient of the active transistor is moved to an angle of 0° (i.e., the right-hand real axis of the compressed Smith chart). Alternatively, the reflection coefficient associated with impedance can be inverted to an admittance point, and the admittance can be moved to an angle of 180° (i.e., the left-hand real axis of the compressed Smith chart).

4-11-3 Two-Port Oscillator Design

A common method for designing oscillators is to resonate the input port with a passive high-Q circuit at the desired frequency of resonance. It will be shown that if this is achieved with a load connected on the output port, the transistor is oscillating at both ports and is thus delivering power to the load port. The oscillator may be considered a two-port structure, where M_3 is the lossless resonating port and M_4 provides lossless matching such that all of the external RF power is delivered to the load. The resonating network has been described. Nominally, only parasitic resistance is present at the resonating port, since a high-Q resonance is desirable for minimizing oscillator noise. It is possible to have loads at both the input and the output ports if such an application occurs, since the oscillator is oscillating at both ports simultaneously.

Note: Using the hopefully high-Q tuned circuit also as a filter gives better far-out phase noise than the more common method of taking the energy from the collector if the circuit is based on the Colpitts design.

The simultaneous oscillation condition is proved as follows. Assume that the oscillation condition is satisfied at port 1:

$$1/S'_{11} = \Gamma_G \tag{4-342}$$

Thus,

$$S'_{11} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - D\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4-343}$$

$$\frac{1}{S'_{11}} = \frac{1 - S_{22}\Gamma_L}{S_{11} - D\Gamma_L} = \Gamma_G \tag{4-344}$$

By expanding Eq. (4-344), we find

$$\Gamma_G S_{11} - D\Gamma_L\Gamma_G = 1 - S_{22}\Gamma_L$$
$$\Gamma_L(S_{22} - D\Gamma_G) = 1 - S_{11}\Gamma_G$$
$$\Gamma_L = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{4-345}$$

Thus,

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_\Gamma} = \frac{S_{22} - D\Gamma_G}{1 - S_{11}\Gamma_G} \tag{4-346}$$

$$\frac{1}{S'_{22}} = \frac{1 - S_{11}\Gamma_G}{S_{22} - D\Gamma_G} \tag{4-347}$$

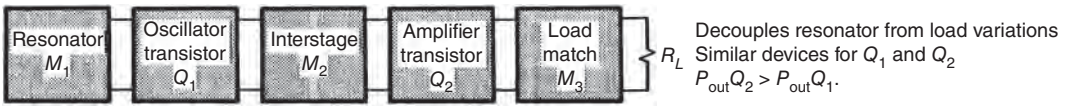


Figure 4-176 Buffered oscillator design.

Comparing Eqs. (4-345) and (4-347), we find

$$1/S'_{22} = \Gamma_L \tag{4-348}$$

which means that the oscillation condition is also satisfied at port 2; this completes the proof. Thus, if either port is oscillating, the other port must be oscillating as well. A load may appear at either or both ports, but normally the load is in Γ_L, the output termination. This result can be generalized to an n-port oscillator by showing that the oscillator is simultaneously oscillating at each port:

$$\Gamma_1 S'_{11} = \Gamma_2 S'_{22} = \Gamma_3 S'_{33} = \cdots = \Gamma_n S'_{nn} \tag{4-349}$$

Before concluding this section on two-port oscillator design, the buffered oscillator shown in Figure 4-176 must be considered. This design approach is used to provide the following:

(1) A reduction in loading-pulling, which is the change in oscillator frequency when the load reflection coefficient changes.
(2) A load impedance that is more suitable to wideband applications, Eq. (4-322).
(3) A higher output power from a working design, although the higher output power can also be achieved by using a larger oscillator transistor.

Buffered oscillator designs are quite common in wideband YIG applications, where changes in the load impedance must not change the generator frequency.

Two-port oscillator design may be summarized as follows:

(1) Select a transistor with sufficient gain and output power capability for the frequency of operation. This may be based on oscillator data sheets, amplifier performance, or S-parameter calculation.
(2) Select a topology that gives $k < 1$ at the operating frequency. Add feedback if $k < 1$ has not been achieved.
(3) Select an output load matching circuit that gives $|S'_{11}| > 1$ over the desired frequency range. In the simplest case this could be a 50 Ω load.
(4) Resonate the input port with a lossless termination so that $\Gamma_G S'_{11} = 1$. The value of S'_{22} greater than unity with the input properly resonated.

In all cases, the transistor delivers power to a load and the input of the transistor. Practical considerations of readability and dc biasing will determine the best design.

For both bipolar and FET oscillators, a common topology is common-base or common-gate, since a common-lead inductance can be used to raise S_{22} to a large value, usually greater than unity even with a 50 Ω generator resistor. However, it is not necessary for the transistor S_{22} to be greater than unity, since the 50 Ω generator is not present in the oscillator design. The requirement for oscillation is $k < 1$; then resonating the input with a lossless termination will provide that $|S'_{11}| > 1$.

A simple example will clarify the design procedure. A common-base bipolar transistor (HP2001) was selected to design a fixed-tuned oscillator at 2 GHz. The common-base S parameters and stability factor are given in Table 4-12. Using the load circuit in Figure 4-177, we see that the reflection coefficients are

$$\Gamma_L = 0.62\angle 30°$$
$$S'_{11} = 1.18\angle 173°$$

Table 4-12 HP2001 bipolar chip common base ($V_{CE} = 15$ V, $I_c = 25$ mA).

$L_B = 0$	$L_B = 0.5$ nH
$S_{11} = 0.94\angle 174°$	$1.04\angle 173°$
$S_{21} = 1.90\angle -28°$	$2.00\angle -30°$
$S_{12} = 0.013\angle 98°$	$0.043\angle 153°$
$S_{22} = 1.01\angle -17°$	$1.05\angle -18°$
$k = -0.09$	-0.83

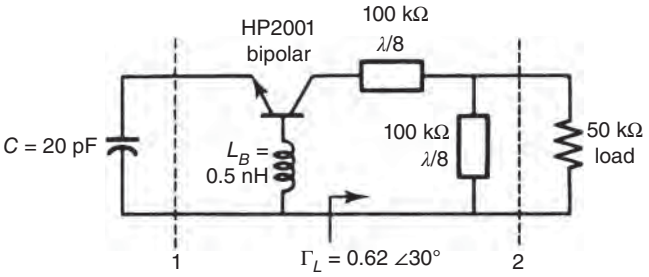


Figure 4-177 Oscillator example at 2 GHz.

Thus, a resonating capacitance of $G = 20$ pF resonates the input port. In a YIG-tuned oscillator, this reactive element could be provided by the high-Q YIG element. For a dielectric resonator oscillator (DRO), the puck would be placed to give $\Gamma_G \approx 1.0\angle -173°$.

Another two-port design procedure is to resonate the Γ_G port and calculate S'_{22}, until $|S'_{22}| > 1$, then design the load port to satisfy. This design procedure is summarized in Figure 4-178.

One word of caution: At these high frequencies a good modeling is necessary, meaning that where possible the lumped elements have to be replaced by distributed elements. An example is given in Figure 4-179. Predicted performance characteristics are shown in Figures 4-180a–4-180c.

An example using this procedure at 4 GHz is given in Figure 4-181 using an AT 41400 silicon bipolar chip in the common-base configuration with a convenient value of base and emitter inductance of 0.5 nH. The feedback parameter is the base inductance, which can be varied if needed.

The two-port common-base S-parameters were used to give

$$k = -0.805$$

$$S'_{11} = 1.212\angle 137.7°$$

Since a lossless capacitor at 4 GHz of 2.06 pF gives $\Gamma_G = 1 - 0\angle -137.7°$, this input termination is used to calculate S'_{22}, giving $S'_{22} = 0.637\angle 44.5°$. This circuit will not oscillate into any passive load. Varying the emitter capacitor about 20° on the Smith chart to 1.28 pF gives $S'_{22} = 1.16\angle -5.5°$, which will oscillate into a load of $\Gamma_L = 0.861\angle 5.5°$. The completed lumped element design is given in Figure 4-182.

Predicted oscillator performance is charted in Figure 4-183a–4-183c.

We now switch from the lumped design to a microstrip design that incorporates a DR. This oscillator circuit is given in Figure 4-184, where the DR will serve the function of the emitter capacitor. This element is usually coupled to the 50 Ω microstripline to present about 1000 Ω of loading ($\beta = 20$) at f_0, the lowest resonant frequency of the dielectric puck, at the correct position on the line. The load circuit will be simplified to 50 Ω ($\Gamma_L = 0$), so

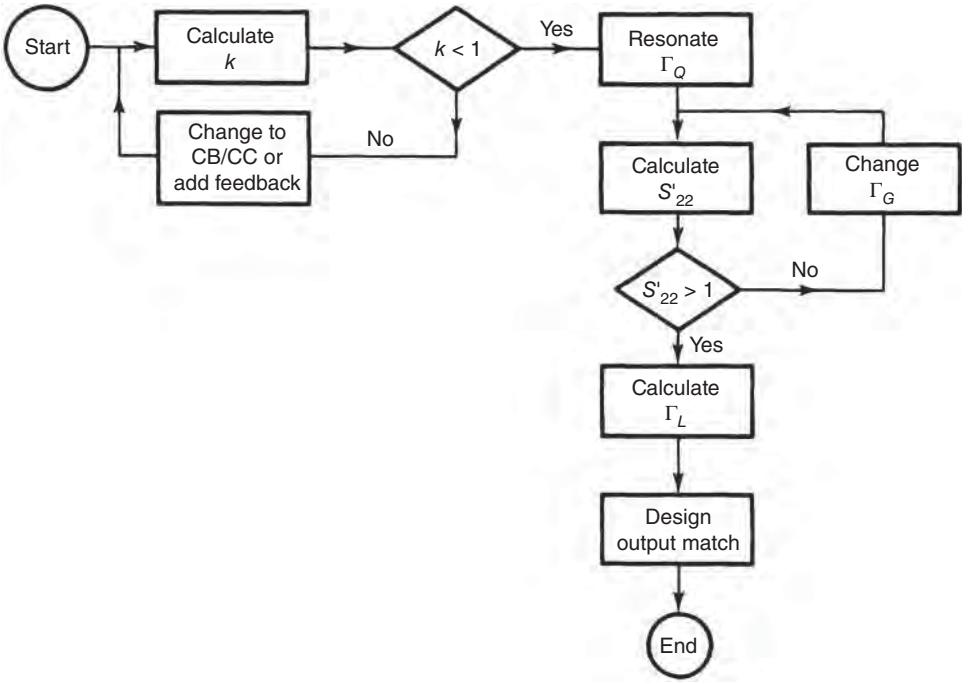


Figure 4-178 Oscillator design flowchart.

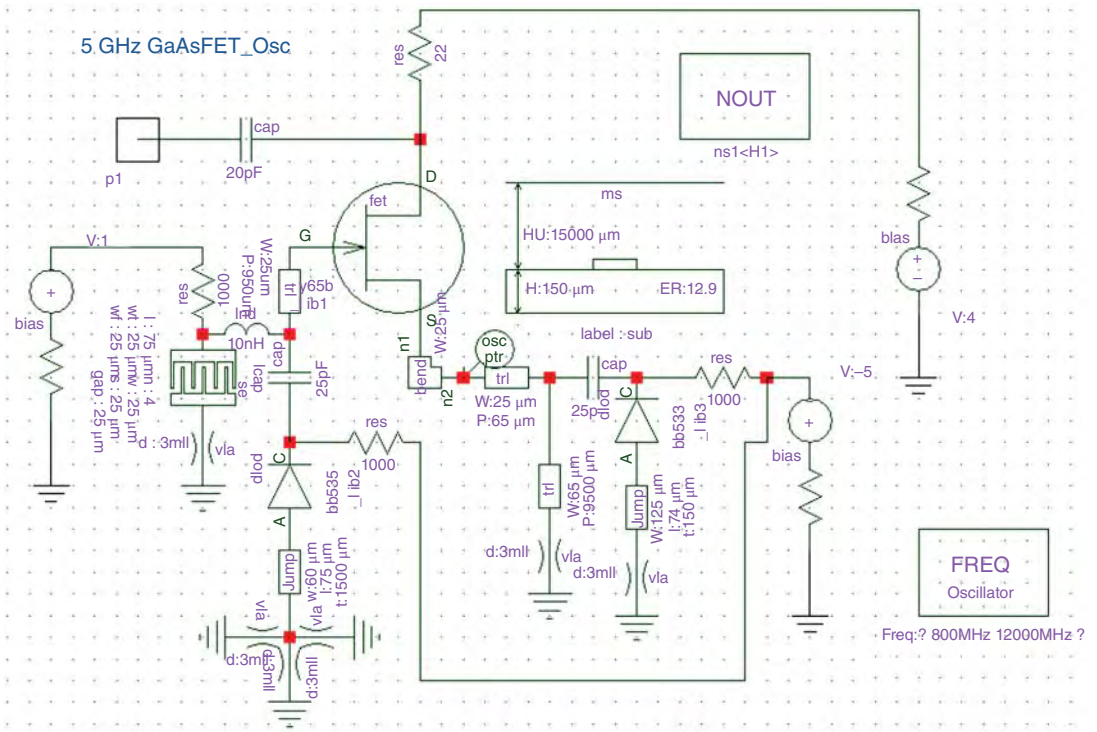


Figure 4-179 5 GHz GaAs FET oscillator.

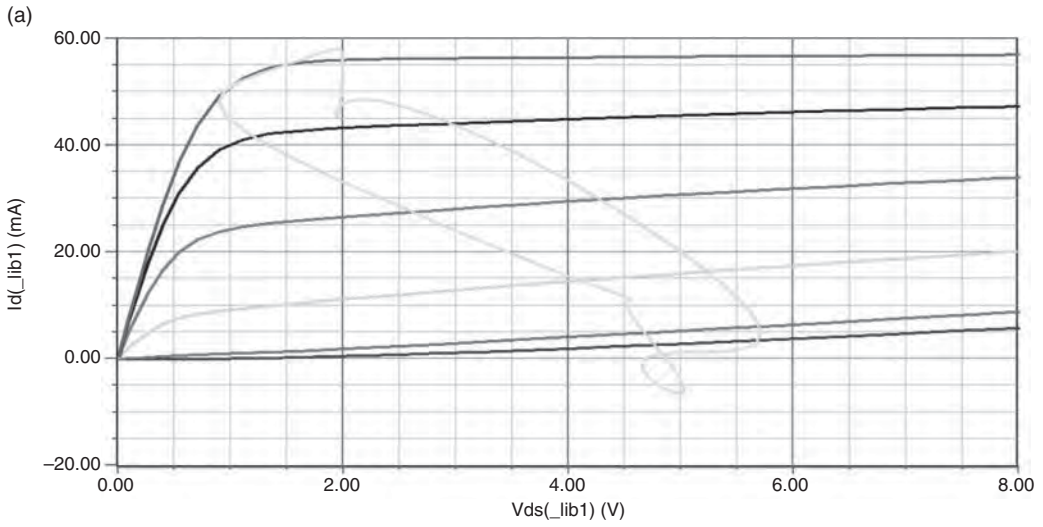


Figure 4-180a 5 GHz oscillator operating characteristics.

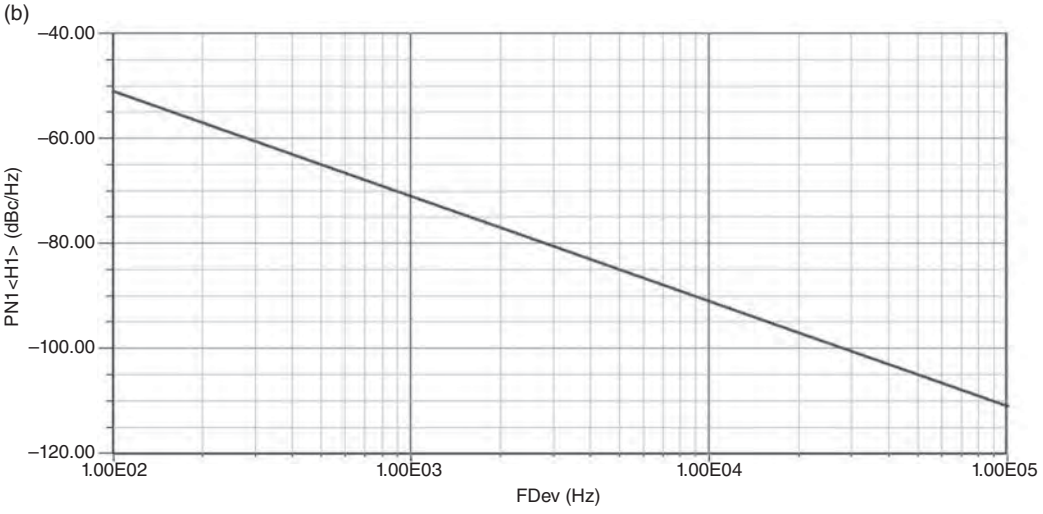


Figure 4-180b Phase noise characteristics.

the oscillator must have an output reflection coefficient of greater than 100, thus presenting a negative resistance between −49 and −50 Ω. The computer file for analyzing this design is given in Table 4-13, where the variables are the puck resistance, the −50 Ω microstripline length, and the base feedback inductance. The final design is given in Figure 4-185, where the 10 μH coils are present for the dc bias connections that need to be added to the design. It is important to check the stability of this circuit with the DR removed. The input −50 Ω termination will usually

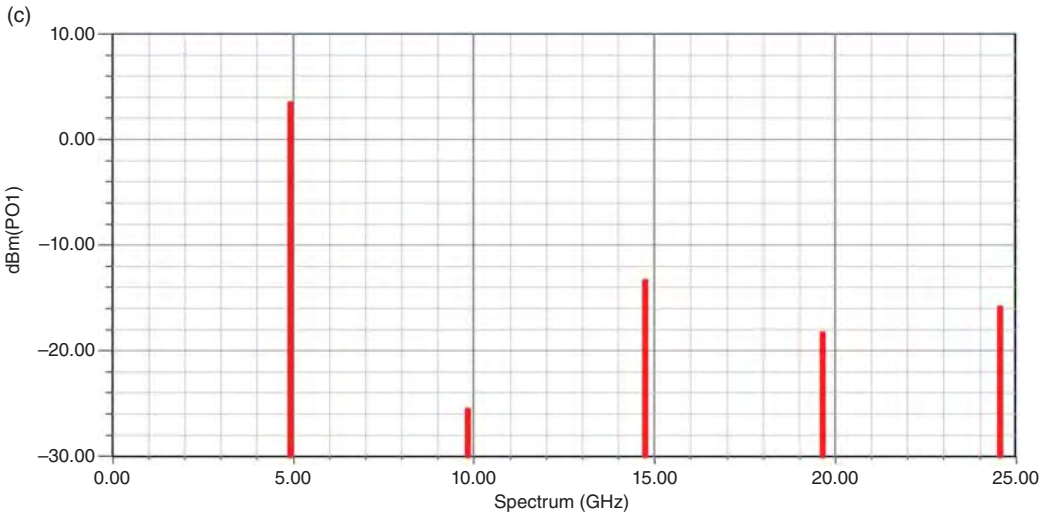


Figure 4-180c Power output characteristics.

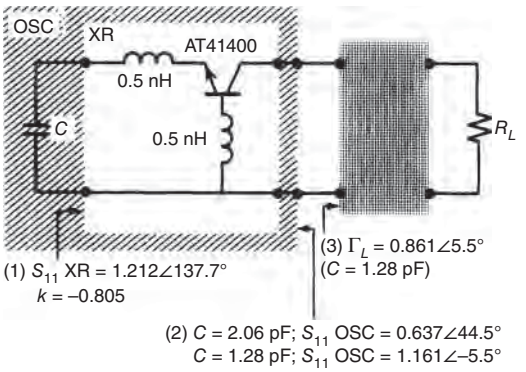


Figure 4-181 A 4 GHz lumped resonator oscillator using the AT41400.

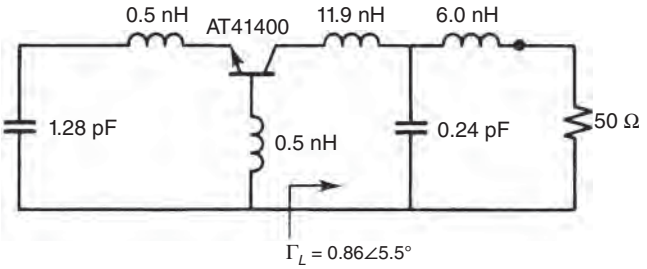


Figure 4-182 Completed lumped resonator oscillator (LRO).

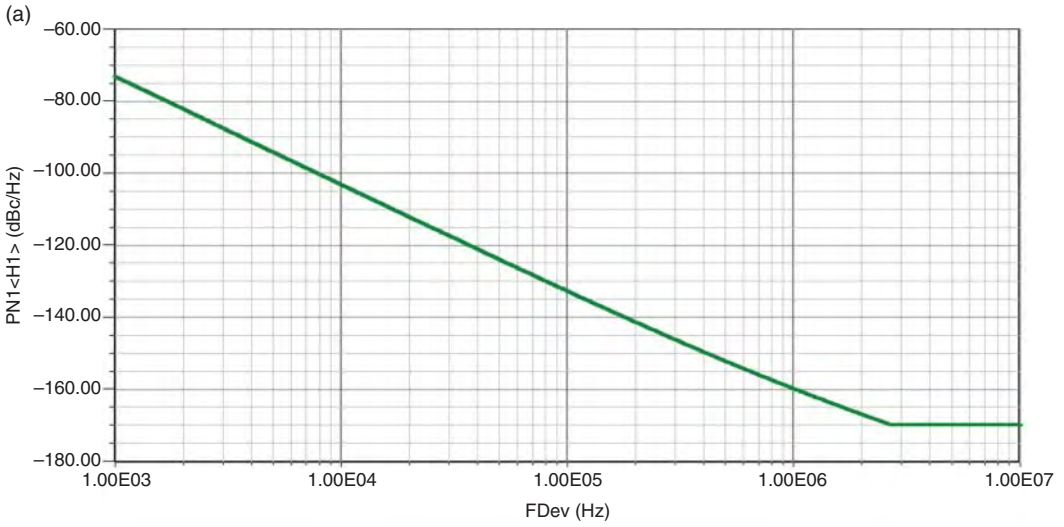


Figure 4-183a Phase noise performance.

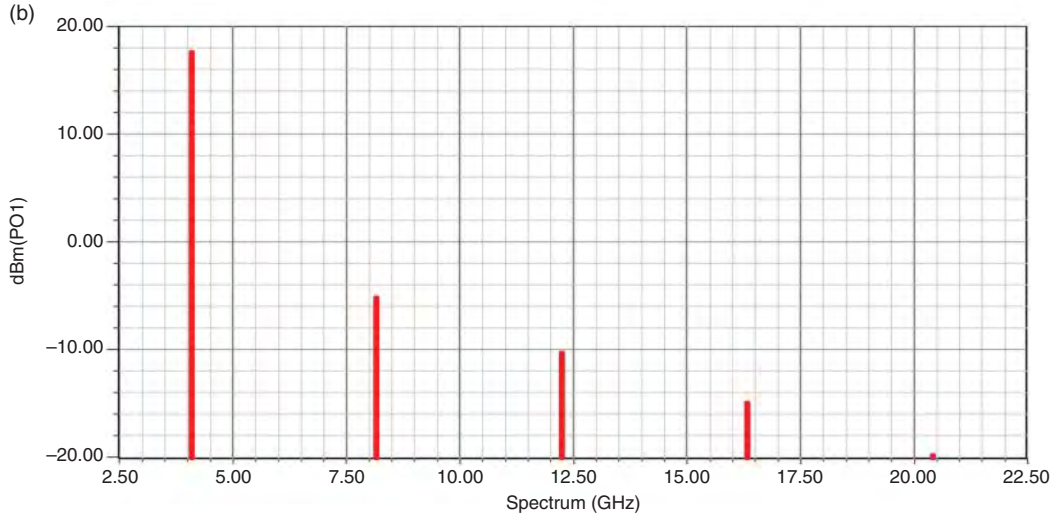


Figure 4-183b Power output.

guarantee unconditional stability at all frequencies. The phase noise of this oscillator is very low at −117 dBc/Hz at 10-kHz frequency offset.

For simple oscillators with no isolating stage, one can expect a certain amount of pulling. Figure 4-186 shows the tuning parameters as the load varies from 50 Ω. The load $C_L = R + jX$ influences the required input capacitance C_E and the base inductor L_B. The numbers in the graph are the resonant portion of the load impedance and the ratio

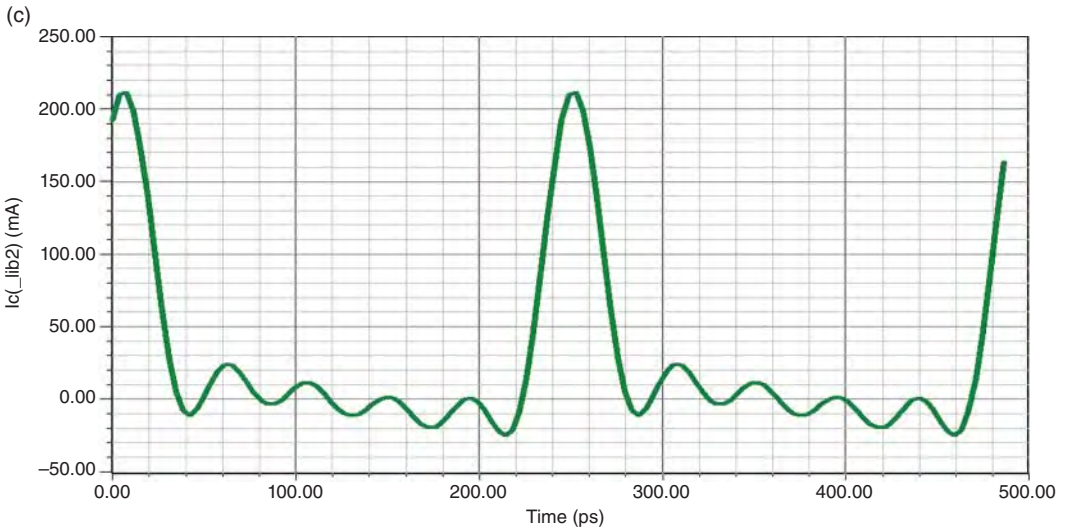


Figure 4-183c I_c versus time.

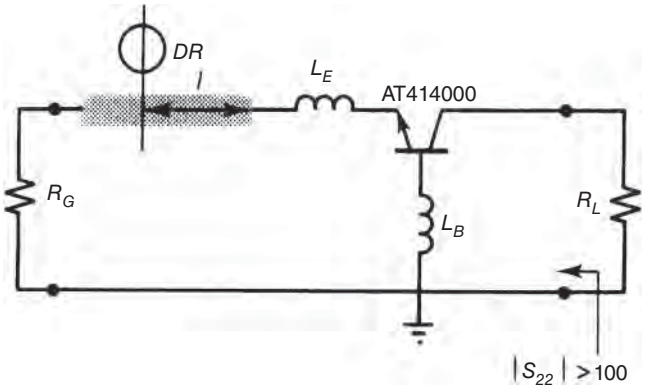


Figure 4-184 Transmission line oscillator with dielectric resonator.

X/*R* determines the *Q* line. It is obvious that such a circuit is quite interactive. As to the model for the DR, the valid relationship is shown in Figure 4-187.

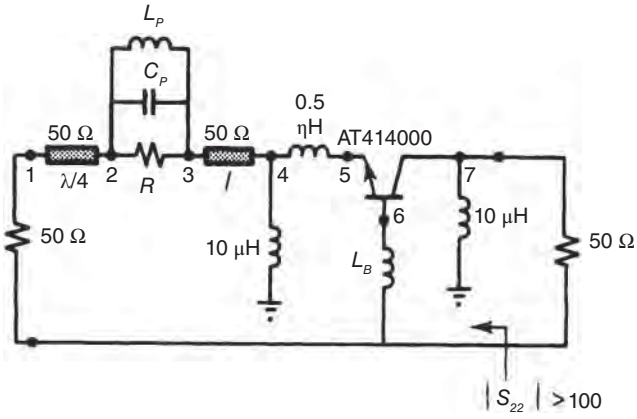
In Section 4-12 on microwave resonators, we will look at a more physical model.

Finally, Table 4-14 describes the same DRO in the familiar Spice format. This particular Compact Software Inc. Spice model uses transmission elements Tl and T2 and the resonant frequency of the oscillator is determined by both the DR and its position relative to the transmission line. In the equivalent circuit of the transistor, no values for a base-spreading resistor have been assumed. This modeling is done for demonstration purposes and does not relate to an actual transistor. A more practical circuit will follow.

Table 4-13 Super-compact file for DRO design in Figure 4-185.

```
*
-
* AT41400 AT 7.5V, 30 mA IN DRO
* OSCILLATOR By Vendelin et a I. Microwave Journal June 1986pp. 151-152
BLK
TRL 1 2 Z=50 P=250MIL K=6.6
RES 2 3 R=?955.06?
TRL 3 4 Z=50 P=?224.16MIL? K=6.6
IND 4 0 L=1E4NH
IND 4 5 L=.5NH
TWO 6 7 5 Q1
IND 6 0 L = ?.33843NH?
IND 7 0 L=1E4NH
0SC:2P0R 1 7
END
*
FREQ
4GHZ
END
OUT
PRI OSC S
END
OPT
OSC
MS22 = 100 GT
END

Q1 : S
4 . 8057-176.14 2.5990 74.77.0316 56.54 .4306 -22.94
END
```



Variables: R (coupling of puck) = 955 Ω
l (placement of puck) = 224.2 mils
(ε_L = 10, h = 25 mils)
L_B (base inductance) = 0.34 nH

Figure 4-185 Equivalent circuit for dielectric resonator oscillator (DRO).

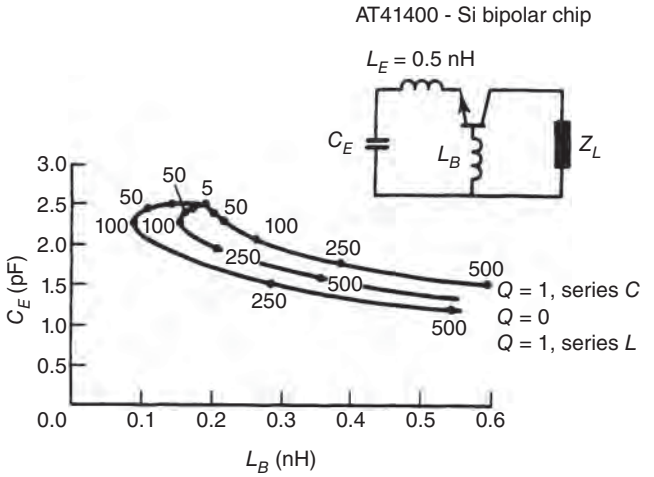
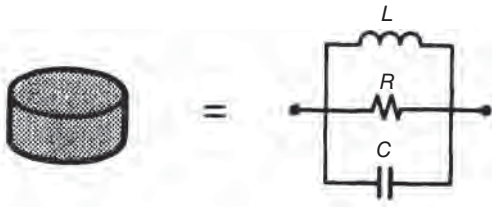


Figure 4-186 Tuning parameters for a 4-GHz oscillator versus load impedance as the load varies from 50 Ω.



$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \qquad \beta = \frac{R}{2Z_o} \qquad Q = \frac{R}{\omega L}$$

$$\frac{1}{Q_L} + \frac{1}{Q_U} = \frac{1}{Q_{ext}}$$

Where $Q_u = R/\omega L$ (unloaded Q)

$$Q_{ext} = \frac{\omega L}{R_G} \text{ (series resonator)}$$

or

$$Q_{ext} = \frac{R_G}{\omega L} \text{ (parallel resonator)}$$

Figure 4-187 Simple equivalent circuit for the dielectric resonator.

4-12 MICROWAVE RESONATORS

For microwave applications, designers are rapidly moving away from lumped to distributed elements. In Section 4-11, we looked at the case of a transmission line-based oscillator, which by itself has a low Q and was shown only for descriptive and design purposes. In similar fashion, we looked at the simplified description of a DR-based oscillator.

Table 4-14 Spice format.

```
Compact Software - SUPER-SPICE 1.1 08/09/95 13:38:56
File: C:\SPICE\CIR\DR0.cir
Dielectric Resonator Oscillator with a BJT
Q1 1 2 3 Q2NXXXX
C1 2 4 100pf
L1 4 0 0.3384nh
L2 1 100 1uh
L3 3 6 0.5nh
lb1 6 0 1uh
T1 6 0 7 0 Z0=50 TD=5.4378e-11
cdro 7 8 .0397p
Idro 7 8 40nh
rdro 7 8 955
T2 8 0 9 0 Z0=50 TD=4.876e-11
R1 9 0 50
C4 1 10 100pf
P1 10 0 PNR=1 ZL=50
*Biasing
R3 100 2 3.6k
R4 2 0 1.2k
V1 100 0 7.5V
• model Q2NXXXX NPN(Is=1-65e-18 Vaf=20 Bf=50 Nf=1.03
+ Ise=5f lkf=.1 Xtb=1.818 Br=5 cjc=.75p
+ Fc=.5 Cje=.75p Mje=.6 Vje=1.01 xcjc=.5
+ Tf=14p Itf=.3 Vtf=6 Xtf=4 Ptf=35)
• IC V(2)=.001
• TRAN 2N 500N
• AC LIN 500 3GHZ 5GMZ
• opt i 115 = 0
• PROBE
• END
```

From a practical design point of view, most relevant applications are SAW resonators, DRs, and YIG oscillators. These are the three types of resonators we will cover in this section.

4-12-1 SAW Oscillators

The SAW oscillator has an equivalent circuit similar to a crystal but should be enhanced by adding the appropriate capacitance to ground. Figure 4-188 shows this. SAW oscillators are frequently used in synthesizers and provide a low phase noise, highly stable source, as can be seen in Figure 4-188. The SAW oscillator comes as either a one-port or two-port device.

The SAW resonator has fairly high insertion loss, as can be seen from Figure 4-189. The actual circuit of a high-performance SAW oscillator, as shown in Figure 4-190, consists of a bipolar transistor with a dc stabilizing circuit, SAW oscillator, and a feedback loop, which allows the phase to be adjusted. The SAW oscillator provides very good phase noise. The measured phase noise of such an oscillator is shown in Figure 4-191. The actual measured phase noise agrees quite well with this prediction [88].

4-12-2 Dielectric Resonators

In designing DR-based oscillators, several methods of frequency stabilization are available that have been proposed by various authors. Figure 4-192 shows some recommended methods of frequency stabilization for DROs. The DR consists of some high dielectric material coupled to a transmission line or microstrip structure.

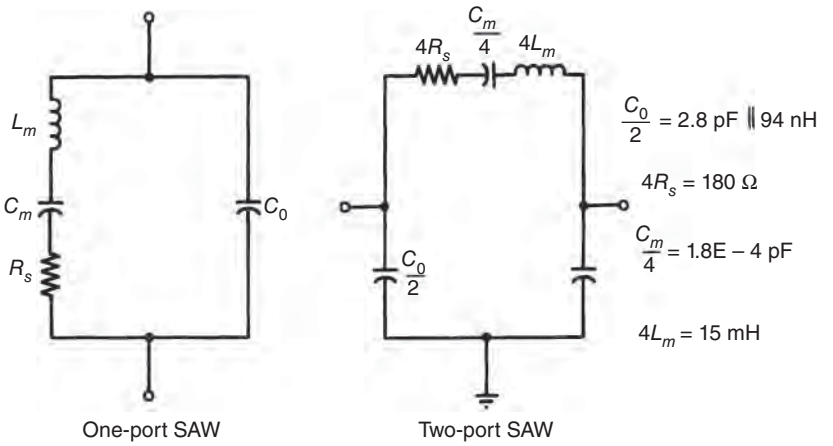


Figure 4-188 Appropriate capacitance to ground for the SAW resonator.

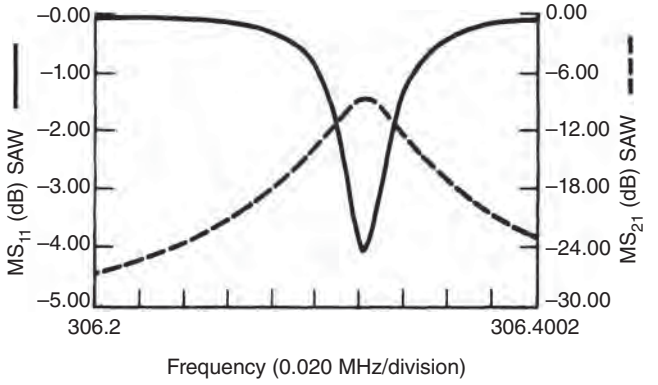


Figure 4-189 Frequency response of an SAW oscillator.

Figure 4-192 shows the field distribution and interaction between the microstrip and the DR. The two resulting applications, BandStop and BandPass filters, are displayed. Modeling this type of resonator is done by describing the resonator in the form of its physical dimensions.

Table 4-15 shows the physical dimensions of the DR in Super-Compact/Microwave Harmonica format.

A practical example of a 6-GHz DR-based oscillator is shown in Figure 4-193a–4-193c, and its predicted phase noise is shown in Figure 4-194.

For calibration purposes, it may be useful to plot the phase noise of different oscillators, including YIG oscillators, as shown in Figure 4-195, but normalized to a center frequency of 6 GHz. Another way of plotting this is to show the phase noise of silicon bipolar transistors versus FETs at 10 kHz offset from the carrier, as shown in Figure 4-196a and 4-196b. This plot does not incorporate for heterojunction bipolar transistors because they are not yet readily or commercially available.

As an example implementation, a 6.6 GHz DRO is shown in schematic form in Figure 4-197. Predicted performance is charted in Figure 4-198a and 4-198b.

For more detailed information on DROs, please refer to Appendix E.

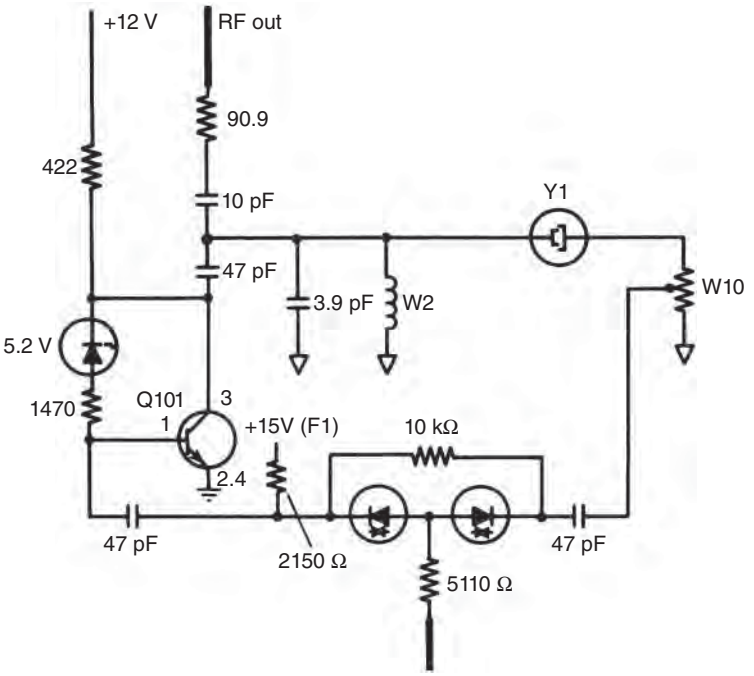


Figure 4-190 Schematic of an SAW oscillator.

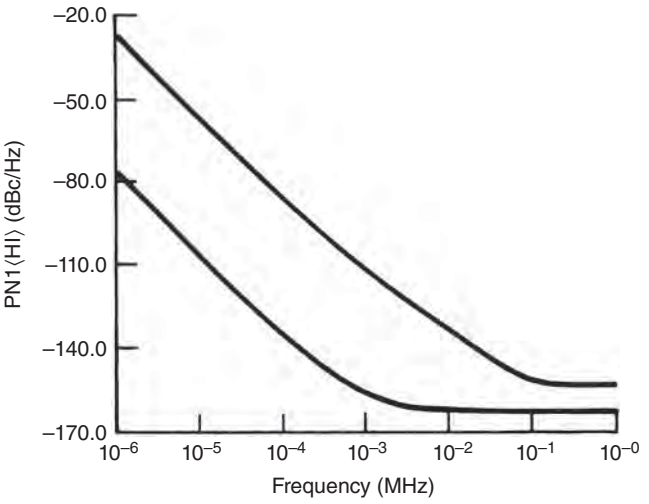


Figure 4-191 Phase noise as determined by the initial start-up values and after optimization.

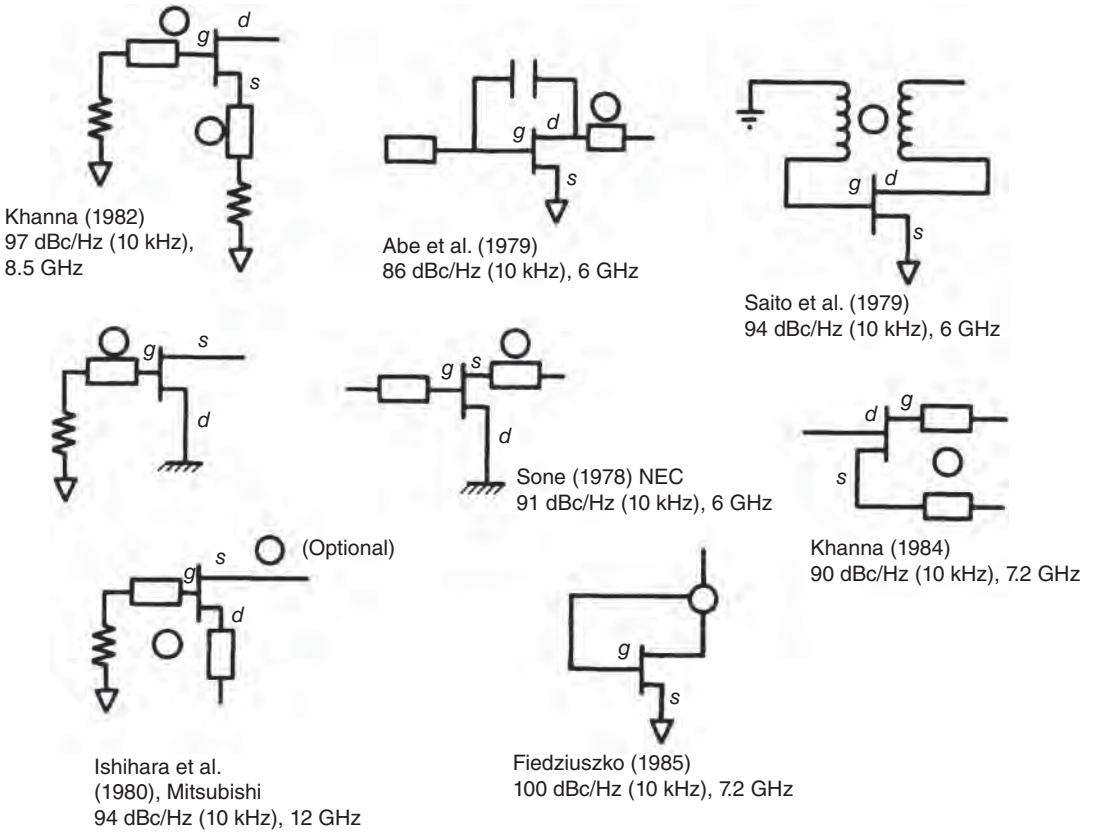


Figure 4-192 Recommended methods of frequency stabilization for DROs.

Table 4-15 Physical dimensions of DR.

```
BLK
DRM 1 2     D = 6.12e-3 HD-2.45e-3 ER = 38 HT = 1.5e-3 S = .5e-3; + W = 1.1e-3 L = 4e-3 SRD = 1e-4
              BPF SUB;
              trf 2 0 0 3 N = 1
              pug: 2P0R 1 3
END
DATA
              SUB: MS er = 2.4 h = 0.380e-3 met1 = cu 3.175e-6 and = 0.0001
END
```

4-12-3 YIG Oscillators

For wideband electrically tunable oscillators, we use either a YIG or a varactor resonator. The YIG resonator is a high-Q, ferrite sphere of yittrium ion garnet, Y_2Fe_2 $(FeO_4)_3$, that can be tuned over a wide band by varying the biasing dc magnetic field. Its high performance and convenient size for applications in microwave integrated circuits make it an excellent choice in a large number of applications, such as filters, multipliers, discriminators, limiters, and oscillators. A YIG resonator makes use of the ferrimagnetic resonance, which, depending on the

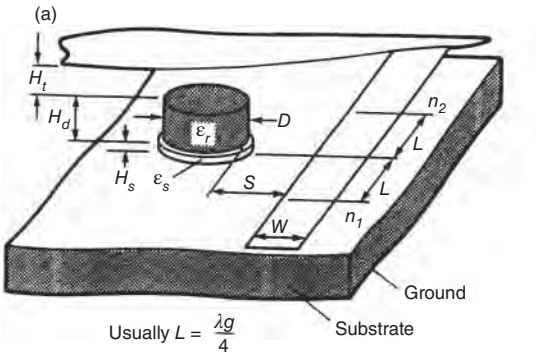


Figure 4-193a DRO on microstrip as BandStop filter.

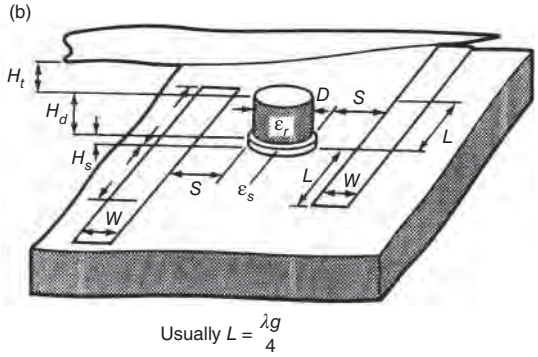


Figure 4-193b DRO on microstrip as BandPass filter.

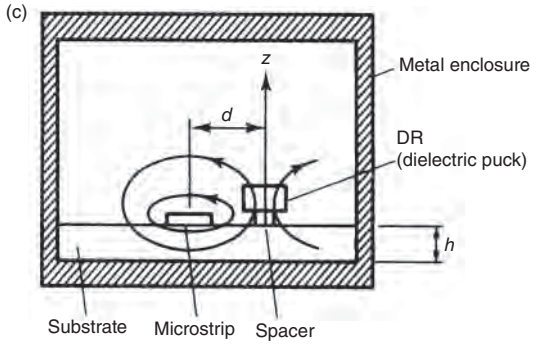


Figure 4-193c Field distribution and interaction between the microstrip and the DRO.

material composition, size, and applied field, can be achieved from 500 MHz to 50 GHz. An unloaded Q greater than 1000 is usually achieved with typical YIG material.

Figure 4-199 shows the mechanical drawing of a YIG oscillator assembly. The drawing is somewhat simplified, and the actual construction is actually more difficult to do. Its actual circuit diagram is shown in Figure 4-200.

An example implementation of 10 GHz YIG oscillator is shown in Figure 4-201. Predicted performance is charted in Figures 4-202a and 4-202b.

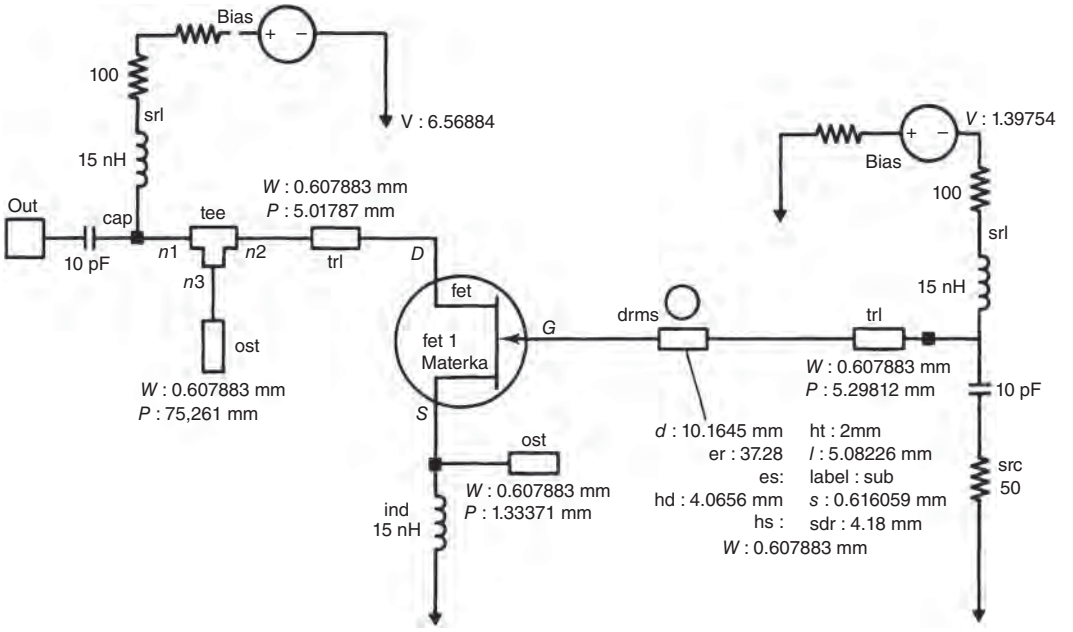


Figure 4-194 Schematic of 6-GHz DRO.

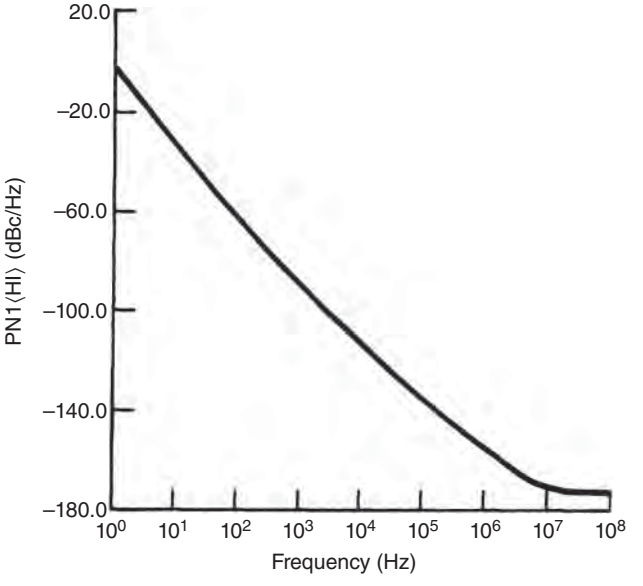


Figure 4-195 Predicted phase noise of the 6-GHz DRO pictured in Figure 4-193a–4-193c.

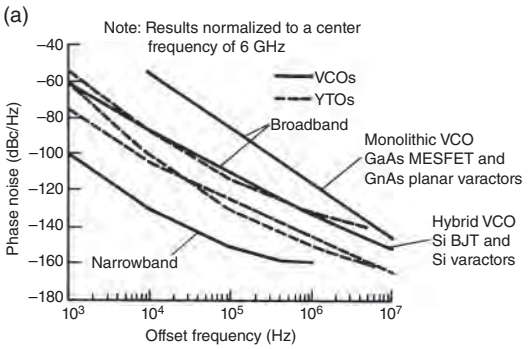


Figure 4-196a Phase noise comparison of different YIG and varactor tuned oscillators.

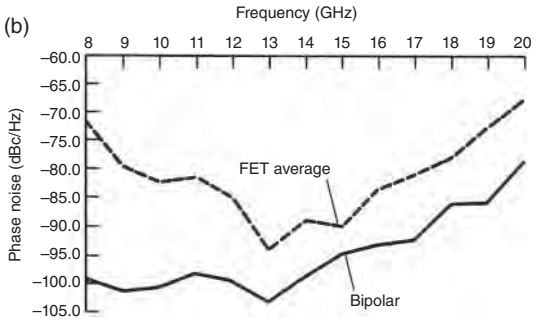


Figure 4-196b Phase noise at 10 kHz off the carrier of silicon bipolar transistors versus FETs.

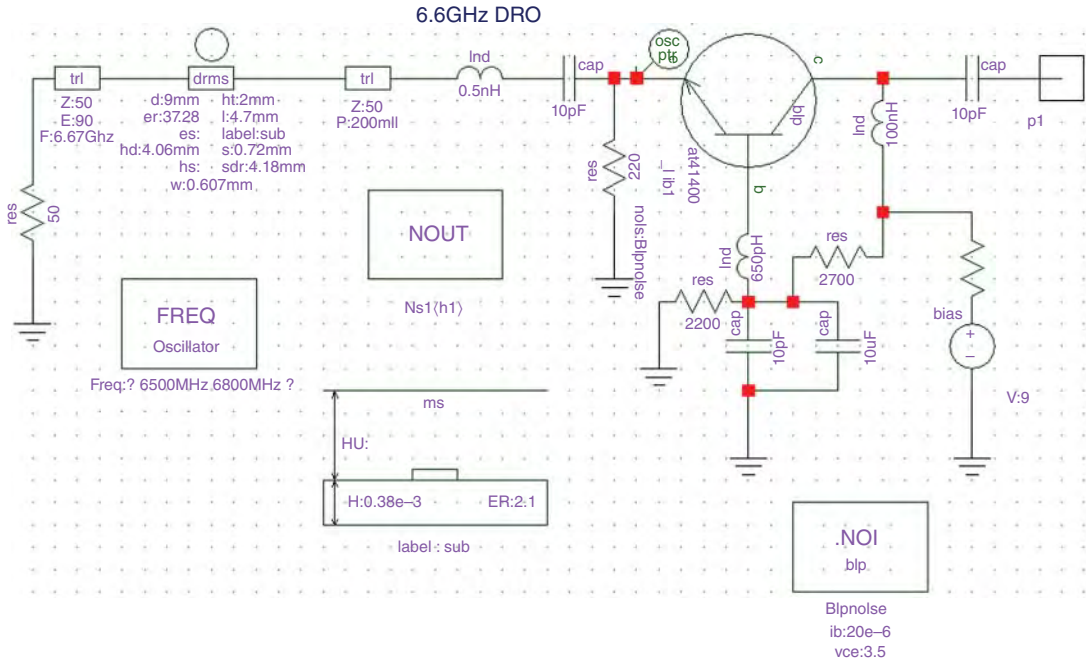


Figure 4-197 Example implementation of a 6.6 GHz DRO.

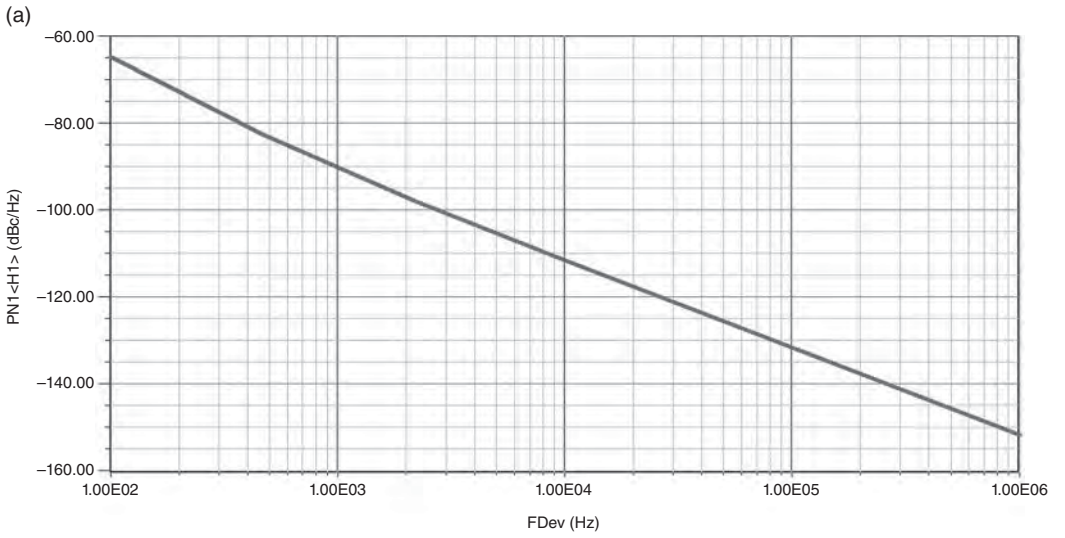


Figure 4-198a Predicted phase noise performance.

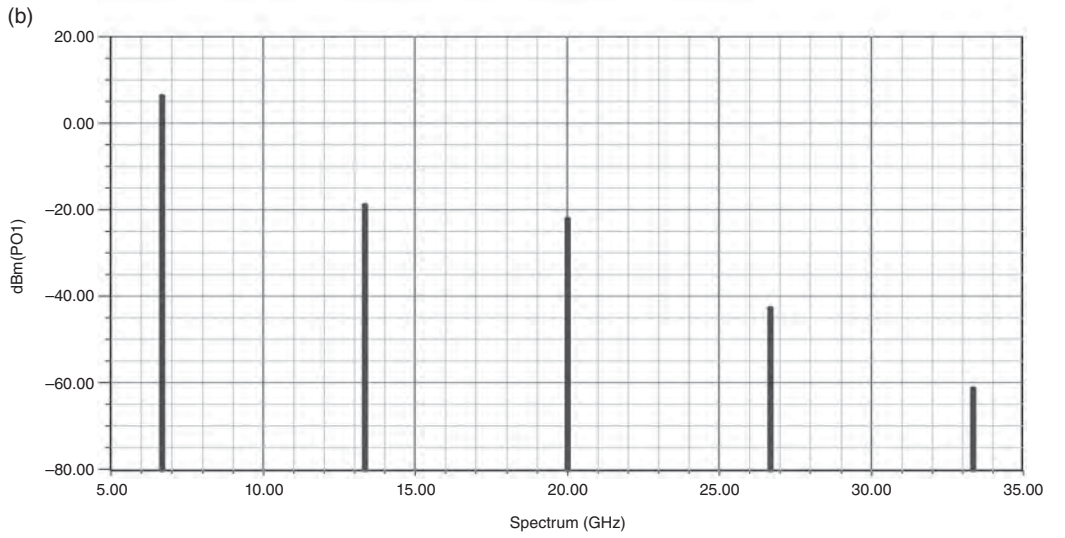


Figure 4-198b Predicted power output performance.

4-12-4 Varactor Resonators

The dual of the current-tuned YIG resonator is the voltage-tuned varactor, which is a variable reactance achieved from a low-loss, reverse-biased semiconductor PN junction. These diodes are designed to have very low loss and therefore high Q. The silicon varactors have the fastest settling time in fast-tuning applications, but the gallium arsenide varactors have higher Q values. The cutoff frequency of the varactor is defined as the frequency where $Q_v = 1$. For a simple series RC equivalent circuit, we have

$$Q_v = \frac{1}{\omega R C_v} \tag{4-350}$$

$$f_{c0} = \frac{1}{2\pi R C_v} \tag{4-351}$$

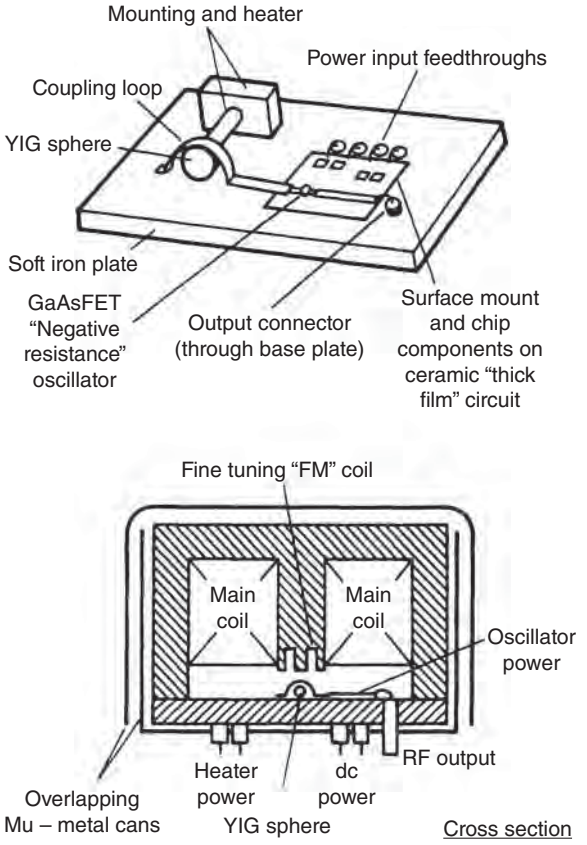


Figure 4-199 The yttrium–iron–garnet (YIG) sphere serves as the resonator in the sweep oscillators used in many spectrum analyzers.

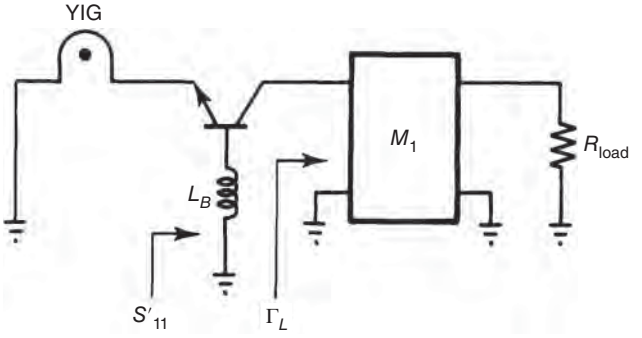


Figure 4-200 Actual circuit diagram for YIG-tuned oscillator depicted in Figure 4-199.

The tuning range of the varactor will be determined by the capacitance ratio C_{max}/C_{min}, which can be 12 or higher for hyper-abrupt varactors. Since R is a function of bias, the maximum cutoff frequency occurs at a bias near breakdown, where both R and C_v have minimum values. Tuning diodes or GaAs varactors for microwave and millimeter-wave applications are frequently obtained by using a GaAs FET and connecting source and drain together. Figure 4-203 shows the dynamic capacitance and dynamic resistors as a function of tuning voltage. In using a transistor instead of a diode, the parameters become more complicated. Figure 4-204 shows the capacitance,

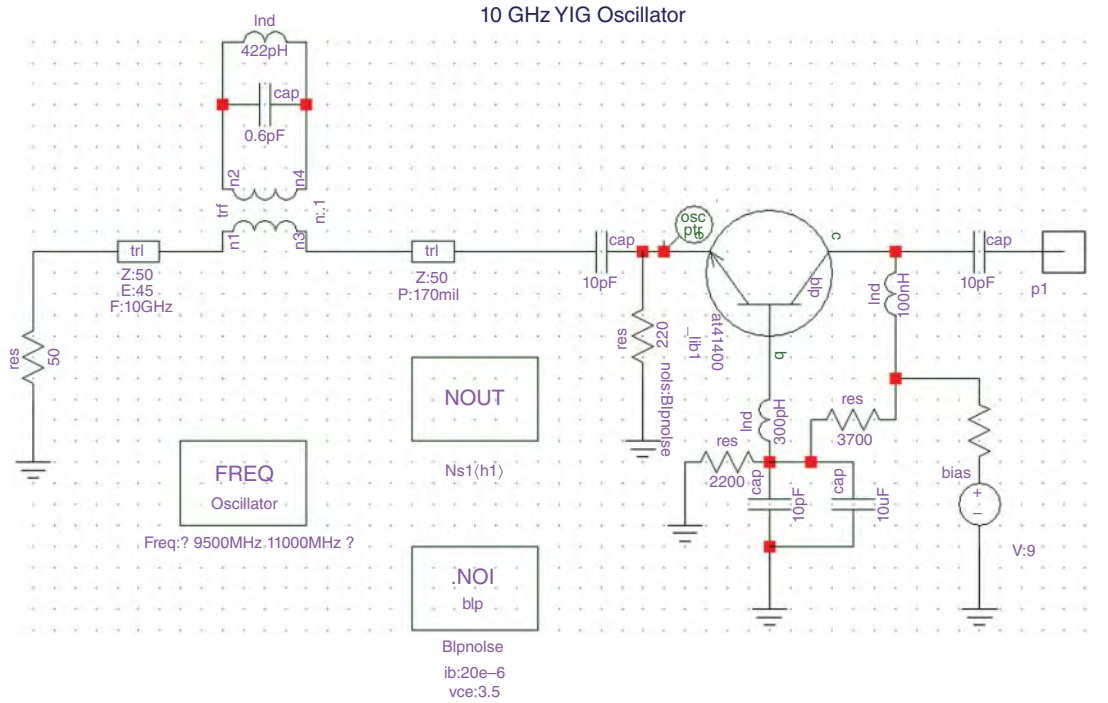


Figure 4-201 Example implementation of a 10 GHz YIG oscillator.

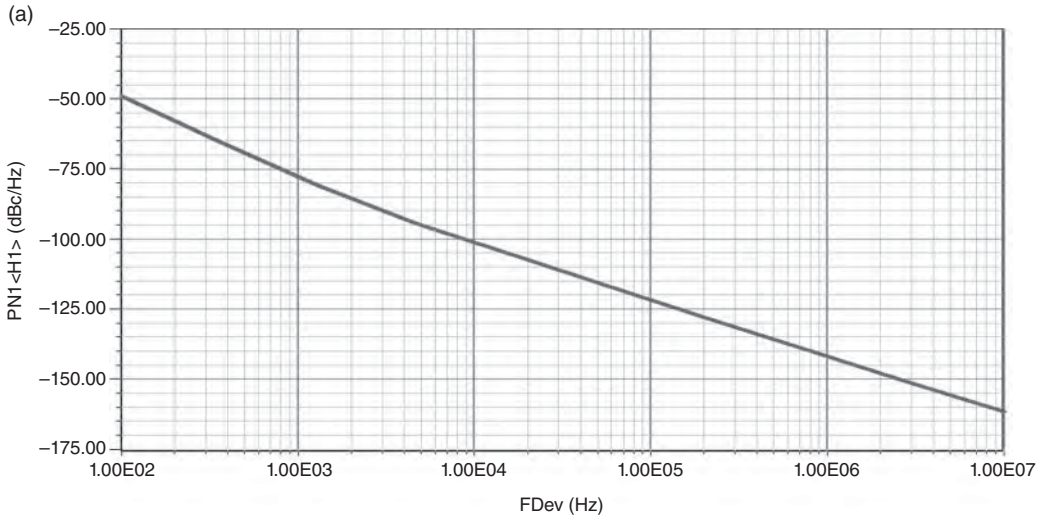


Figure 4-202a Predicted phase noise performance.

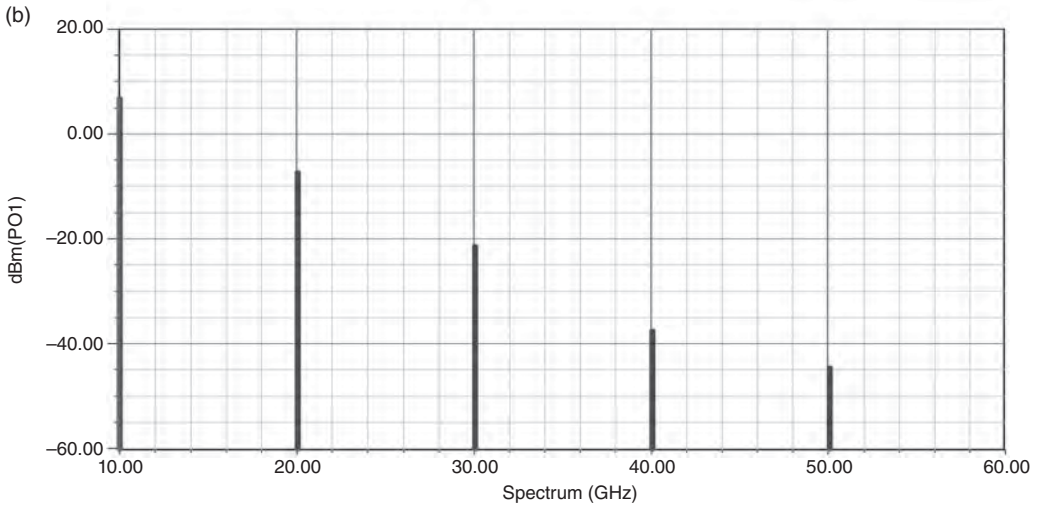


Figure 4-202b Predicted power output performance.

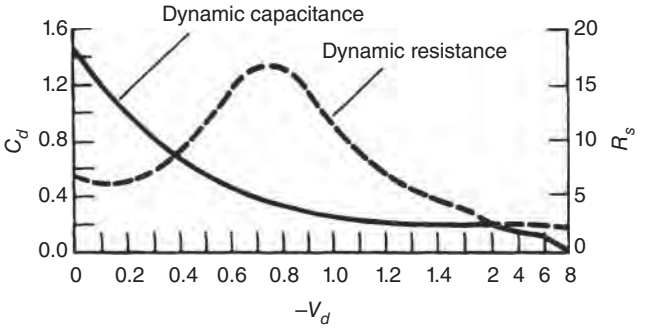


Figure 4-203 Dynamic capacitance and dynamic resistors as a function of tuning voltage for GaAs varactor.

equivalent resistor, and Q, as well as the magnitude of S_{11}, as a function of reverse voltage. This is due to the breakdown effects of the GaAs FET.

Previously, we had discussed in great detail the tuning diode applications. The major differences between these applications and microwave applications have to do with the resulting low Q and different technology. This is the reason why discussions of both applications were separated.

Figure 4-205 shows an example 5.5–6.6 GHz oscillator using the BFP405 device. Predicted phase noise is given in Figure 4-206.

4-12-5 Ceramic Resonators

An important application for a new class of resonators called *ceramic resonators* (CRs) has emerged for wireless applications. The CRs are similar to shielded coaxial cable, where the center controller is connected at the end to the outside of the cable. These resonators are generally operating in quarter-wavelength mode and their characteristic impedance is approximately 10 Ω. Because their coaxial assemblies are made for a high-ε low-loss material with good silver plating throughout, the electromagnetic field is internally contained and therefore provides very little radiation. These resonators are therefore ideally suited for high-Q, high-density oscillators. The typical application

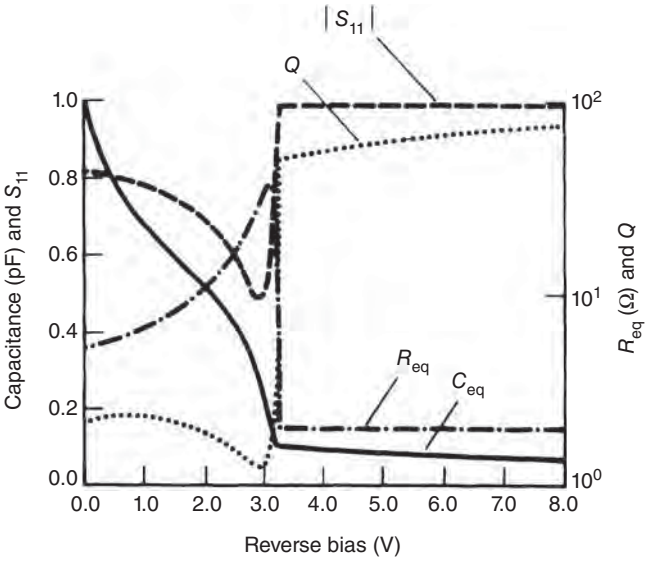


Figure 4-204 Varactor parameters: capacitance, equivalent resistor, and Q, as well as the magnitude of S_{11}, as a function of reverse voltage.

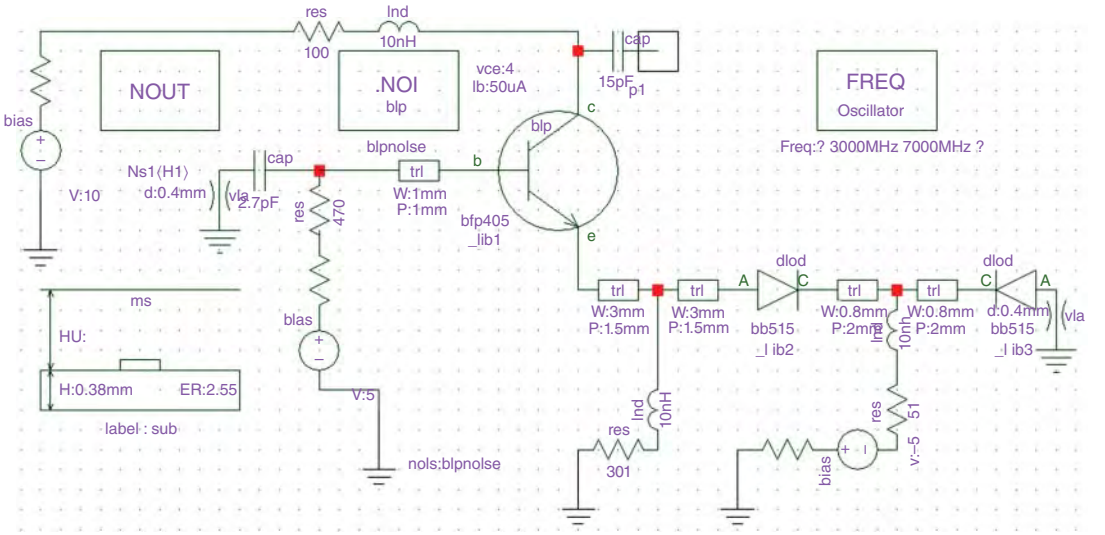


Figure 4-205 Example implementation of a 5.5–6.6 GHz oscillator.

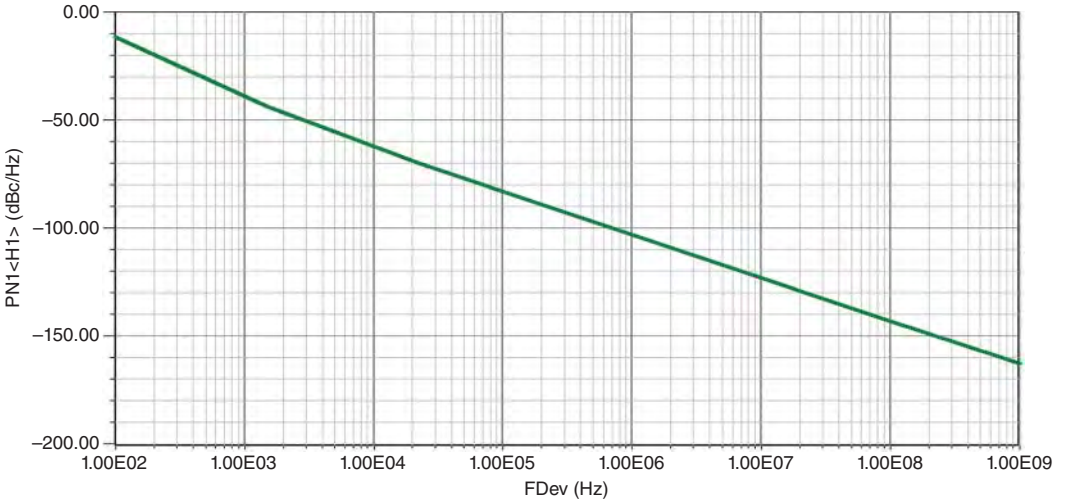


Figure 4-206 Predicted phase noise performance.

for this resonator is VCOs ranging from not much more than 200 MHz up to about 3 or 4 GHz. At these high frequencies, the mechanical dimensions of the resonator become too tiny to offer any advantage. One of the principal requirements is that the physical length is considerably larger than the diameter. If the frequency increases, this can no longer be maintained.

Calculation of Equivalent Circuit

The equivalent parallel-resonant circuit has a resistance at resonant frequency of

$$R_p = \frac{2(Z_0)^2}{R^* l}$$

where Z_0 = characteristic impedance of the resonator

l = mechanical length of the resonator

R^* = equivalent resistor due to metalization and other losses

As an example, one can calculate

$$C^* = \frac{2\pi\varepsilon_0\varepsilon_r}{\log_e(D/d)} = 55.61 \times 10^{-12}\frac{\varepsilon_r}{\log_e(D/d)} \tag{4-352}$$

and

$$L^* = \frac{\mu_r\mu_0}{2\pi} = \log_e\left(\frac{D}{d}\right) = 2 \times 10^{-7}\log_e\left(\frac{D}{d}\right) \tag{4-353}$$

$$Z_0 = 60\ \Omega\frac{1}{\sqrt{\varepsilon_r}}\log_e\left(\frac{D}{d}\right) \tag{4-354}$$

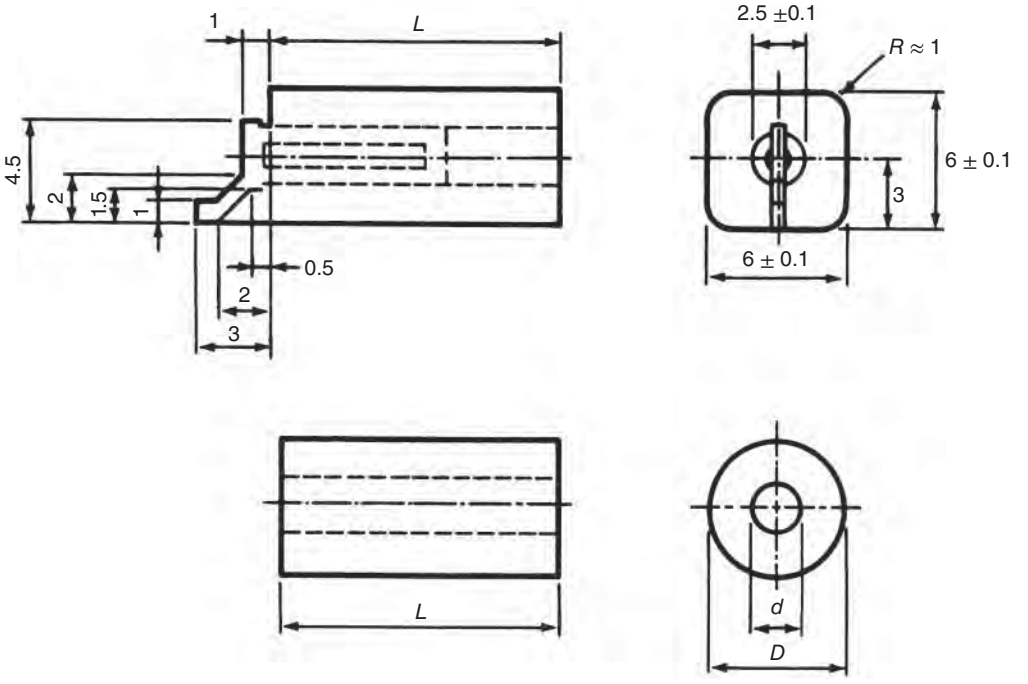


Figure 4-207 Standard round/square packaging.

A practical example for $\varepsilon_r = 88$ and 450 MHz is

$$C_p = \frac{C^* l}{2} = 49.7 \text{ pF} \tag{4-355}$$

$$L_p = 8L^* l = 2.52 \text{ nH} \tag{4-356}$$

$$R_p = 2.5 \text{ k}\Omega \tag{4-357}$$

Manufacturers supply these resonators on a prefabricated basis. Figure 4-207 shows the standard round/square packaging available and the typical dimensions for a ceramic resonator.

The available material has a dielectric constant of 88 and is recommended for use in the 400–1500 MHz range. The next higher frequency range (800 MHz to 2.5 GHz) uses an ε of 38, while the top range (1–4.5 GHz) uses an ε of 21. Given the fact that ceramic resonators are prefabricated and have standard outside dimensions, the following quick calculation applies:

Relative dielectric constant of resonator material	$\varepsilon_r = 21$	$\varepsilon_r = 38$	$\varepsilon_r = 88$
Resonator length in millimeters	$l = \frac{16.6}{f}$	$l = \frac{12.6}{f}$	$l = \frac{8.2}{f}$
Temperature coefficient (ppm/°C)	10	6.5	8.5
Available temperature coefficients	−3 to +12	−3 to +12	−3 to +12
Typical resonator Q	800	500	400

Figure 4-208 shows the schematic of such an oscillator. Figure 4-209a–4-209c gives the simulated performance of the circuit.

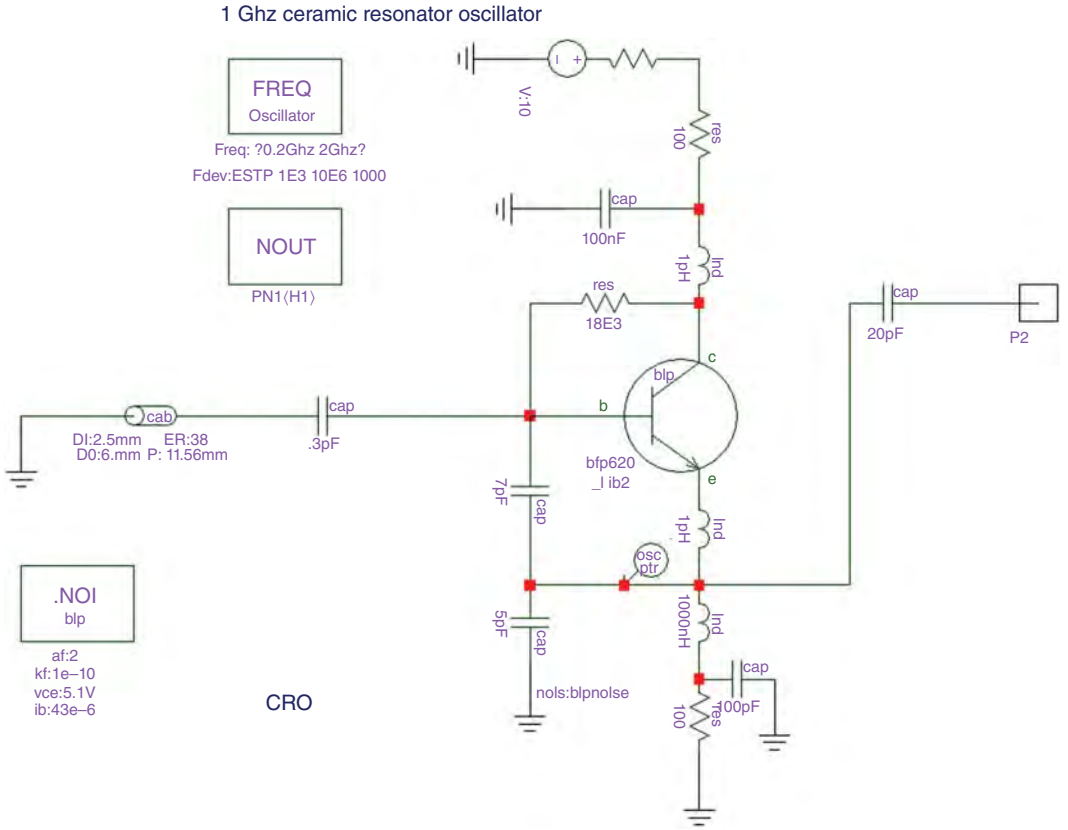


Figure 4-208 Schematic of the ceramic resonator-based oscillator.

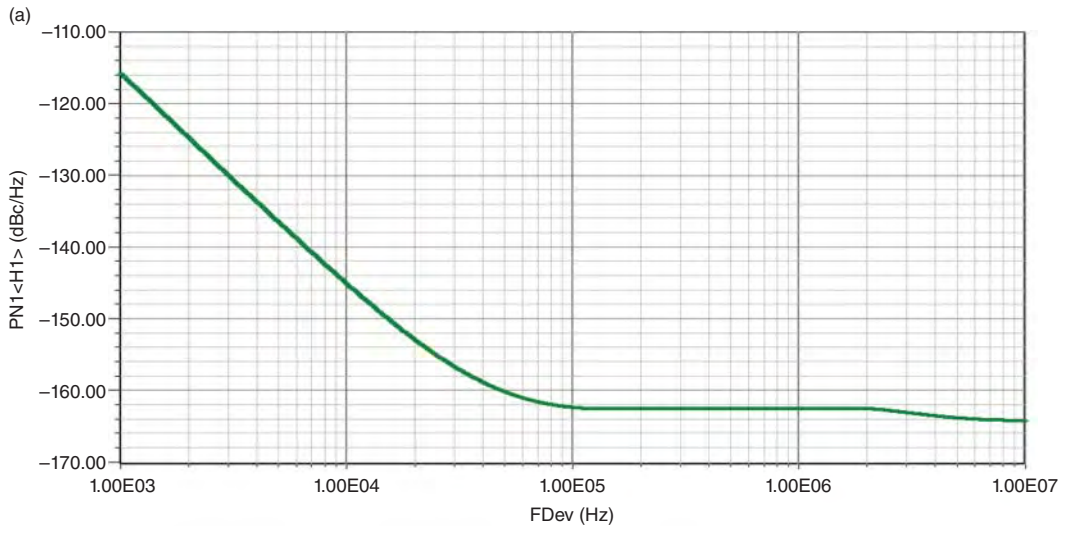


Figure 4-209a Simulated phase noise of an NPN bipolar 1-GHz ceramic resonator-based oscillator.

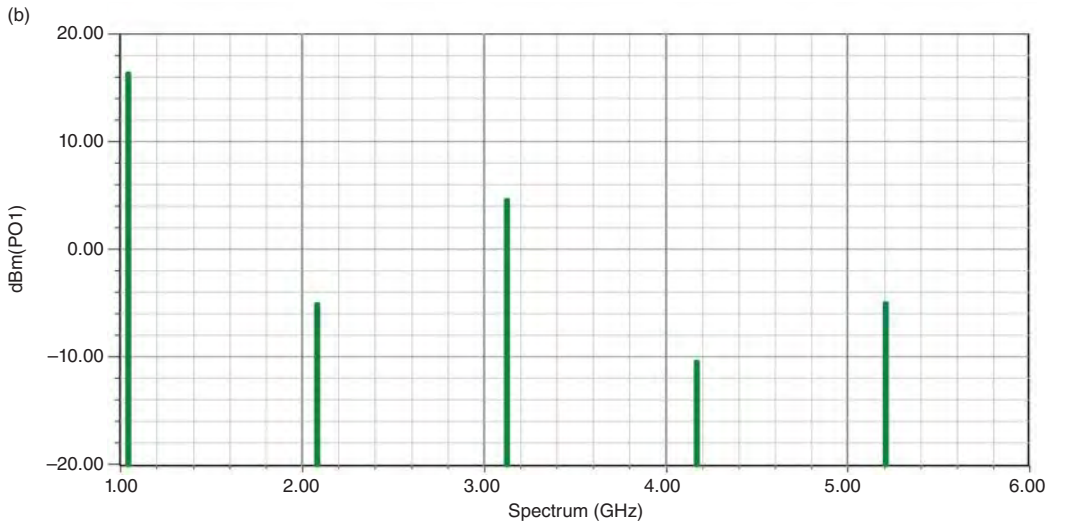


Figure 4-209b Predicted power output.

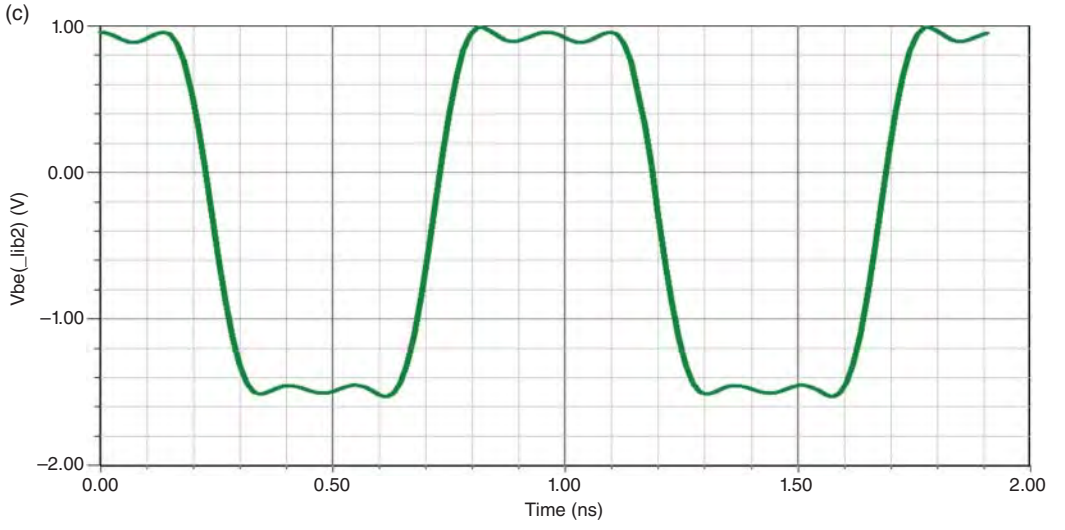


Figure 4-209c V_{be} characterists of the oscillator.

By using ceramic-resonator-based oscillators in conjunction with miniature synthesizer chips, it is possible to build extremely small phase-locked loop systems for cellular telephone operation. Figure 4-210 shows one of the smallest available PLL-based synthesizers manufactured by Synergy Microwave Corporation. Because of the high-Q resonator, these types of oscillators exhibit extremely low phase noise. Values of better than 150 dB/Hz, 1 MHz off the carrier, are achievable. The ceramic resonator reduces the sensitivity toward microphonic effects and proximity effects caused by other components.

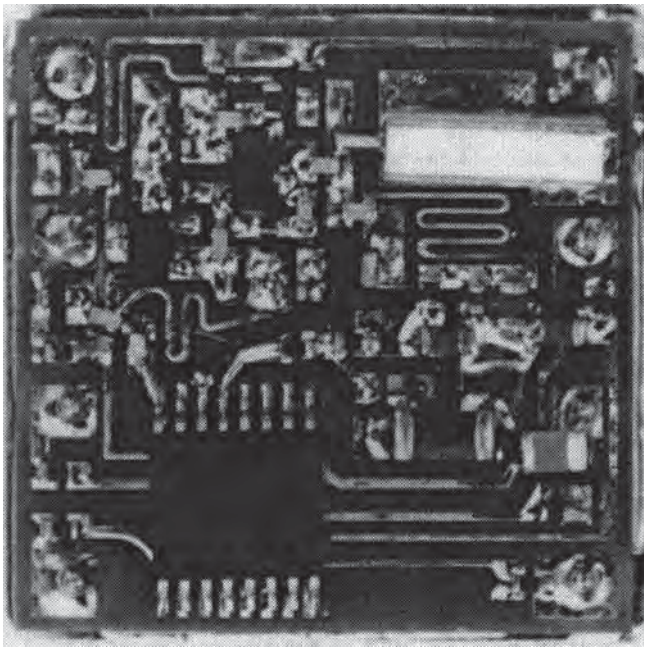


Figure 4-210 Miniature PLL-based synthesizer manufactured by Synergy Microwave Corporation.

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5

DIGITAL PLL SYNTHESIZERS

5-1 MULTILOOP SYNTHESIZERS USING DIFFERENT TECHNIQUES

By now, we have accumulated a large amount of knowledge about single-loop synthesizers. In Chapter 1 a loop with a mixer was described, which probably represents the most simple dual-loop synthesizer.

Adding an auxiliary frequency is the first step toward building a two-loop synthesizer, with this auxiliary frequency generated by another loop rather than by multiplying the reference frequency to mix down the voltage-controlled oscillator (VCO) frequency to a lower frequency range for convenience of being able to use lower dividers. The frequency resolution is then equal to the reference frequency unless special techniques are used.

We have heard already about the fractional division N synthesizer, and we have seen the sequential phase shifter that enabled us to get additional resolution. In addition, the pure digital frequency synthesizer was explained where the waveform is generated with the aid of a lookup table. Multiloop synthesizers use a combination of these techniques.

Modern frequency synthesizers no longer use designs where each decade uses phase-locked loops that operate at the same frequency with the output divided by 10. These *mix-and-divide systems*, or *triple mix systems* with cancellation of drift, are seldom used, as they require an enormous amount of filtering, shielding, and power consumption. However, to be able to decide which building blocks to use, some of them have to be discussed here, and we will start with direct frequency synthesis showing various degrees of resolution.

5-1-1 Direct Frequency Synthesis

Direct frequency synthesis refers to the generation of new frequencies from one or more reference frequencies using a combination of multipliers, dividers, bandpass filters, and mixers. A simple example of direct synthesis is shown in Figure 5-1. The new frequency $\frac{2}{3}f_0$ is realized from f_0 by using a divide-by-3 circuit, a mixer, and a bandpass filter. In this example $\frac{2}{3}f_0$ has been synthesized by operating directly on f_0.

Figure 5-2 illustrates the form of direct synthesis module most frequently used in commercial frequency synthesizers of the direct form. The method is referred to as the "double-mix-divide" approach. An input frequency f_{in} is combined with a frequency f_1, and the upper frequency $f_1 + f_{\text{in}}$ is selected by the bandpass filter. This frequency is then mixed with a switch-selectable frequency $f_2 + f^*$. (In the following, f^* refers to any one of 10 switch-selectable frequencies.) The output of the second mixer consists of the two frequencies $f_{\text{in}} + f_1 + f_2 + f^*$ and $f_{\text{in}} + f_1 - f_2 - f^*$; only the higher-frequency term appears at the output of the bandpass filter. If the frequencies f_{in}, f_1, and f_2 are

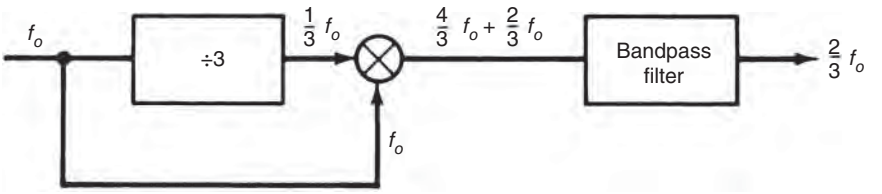

Figure 5-1 Direct frequency generation using the mix-and-divide principle. It requires excessive filtering.

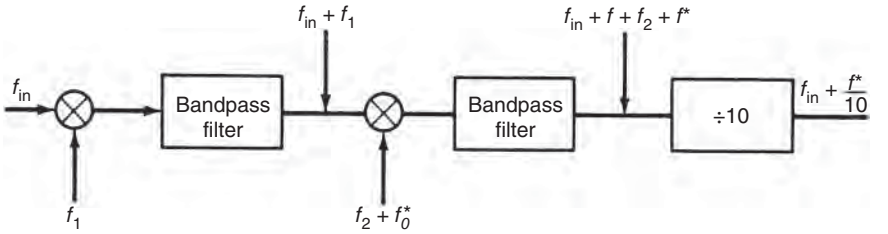

Figure 5-2 Direct frequency synthesizer using a mix-and-divide technique to obtain identical modules for high resolution.

selected so that

$$f_{in} + f_1 + f_2 = 10 f_{in} \tag{5-1}$$

then the frequency at the output of the divide by 10 will be

$$f_{out} = f_{in} + \frac{f^*}{10} \tag{5-2}$$

The double-mix-divide module has increased the input frequency by the switch-selectable frequency increment $f^*/10$. These double-mix-divide modules can be cascaded to form a frequency synthesizer with any degree of resolution. The double-mix-divide modular approach has the additional advantage that the frequencies f_1, f_2, and f_{in} can be the same in each module, so that all modules can contain identical components.

A direct frequency synthesizer with three digits of resolution is shown in Figure 5-3. Each decade switch selects one of 10 frequencies $f_2 + f^*$. In this example the output of the third module is taken before the decade divider. For example, it is possible to generate the frequencies between 10 and 19.99 MHz (in 10-kHz increments), using the three-module synthesizer, by selecting

$$f_{in} = 1 \text{ MHz}$$
$$f_1 = 4 \text{ MHz}$$
$$f_2 = 5 \text{ MHz}$$

Since

$$f_{in} + f_1 + f_2 = 10 f_{in}$$

the output frequency will be

$$f_0 = 10 f_{in} = f_3^* + \frac{f_2^*}{10} + \frac{f_1^*}{100} \tag{5-3}$$

Since f^* occurs in 1-MHz increments, $f_1^*/100$ will provide the desired 10-kHz frequency increments.

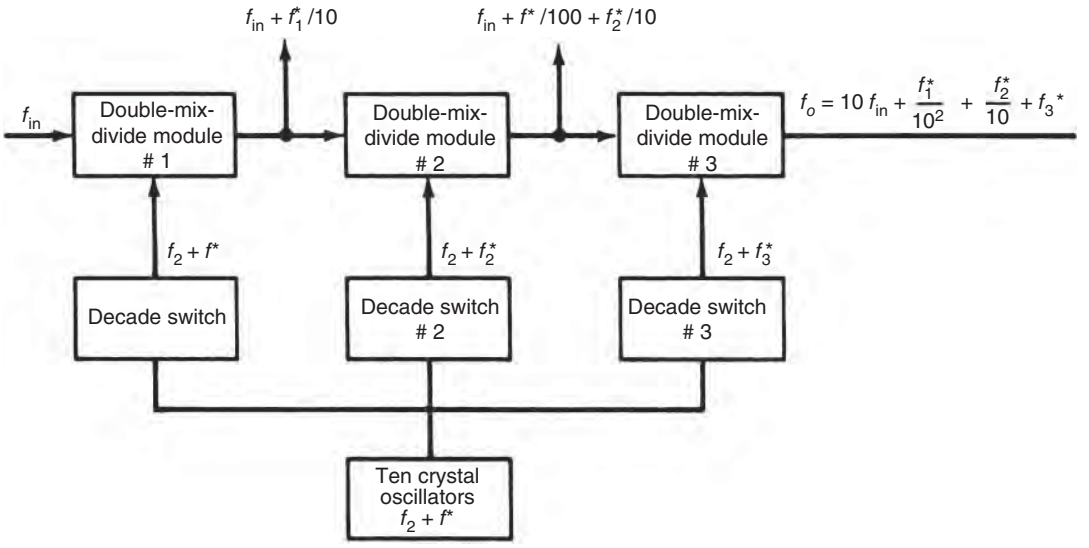

Figure 5-3 Phase incoherent frequency synthesizer with three-digit resolution.

Theoretically, either f_1 or f_2 could be eliminated provided that

$$f_{in} + f_1 \text{ (or } f_2) = 10 f_{in} \tag{5-4}$$

but the additional frequency is used in practice to provide additional frequency separation at the mixer output. This frequency separation eases the bandpass filter requirements. For example, if f_2 is eliminated, $f_1 + f_{in}$ must equal $10f_{in}$ or 10 MHz. If an f_1^* of 1 MHz is selected, the output of the first mixer will consist of the two frequencies 9 and 11 MHz. The lower of these closely spaced frequencies must be removed by the filter. The filter required would be extremely complex. If, instead, a 5-MHz signal f_2 is also used so that $f_{in} + f_1 + f_2 = 10$ MHz, the two frequencies at the first mixer output will (for an f_1^* of 1 MHz) be 1 and 11 MHz. In this case the two frequencies will be much easier to separate with a bandpass filter. The auxiliary frequencies f_1 and f_2 can only be selected in each design after considering all possible frequency products at the mixer output.

Direct synthesis can produce fast frequency switching, almost arbitrarily fine frequency resolution, low phase noise, and the highest-frequency operation of any of the methods. Direct frequency synthesis requires considerably more hardware (oscillators, mixers, and bandpass filters) than the two other synthesis techniques to be described. The hardware requirements result in direct synthesizers being larger and more expensive. Another disadvantage of the direct synthesis technique is that unwanted frequencies (spurious) can appear at the output. The wider the frequency range, the more likely that spurious components will appear in the output. These disadvantages are offset by the versatility, speed, and flexibility of direct synthesis.

5-1-2 Multiple Loops

Multiple-loop synthesizers, as found in signal generators and in communication equipment, are probably best understood when examining their block diagrams. Let us take a look at Figure 5-4, which provides us with the information about the frequency generation of a shortwave receiver; several multiloop synthesizers are being used here. This block diagram shows the various methods that are currently being used.

The shortwave receiver operating from 10 kHz to 29.99999 MHz has a first IF of 81.4 MHz. The oscillator injection therefore requires operating from 81.465 to 111.45499 MHz, as seen in the block diagram.

The oscillator marked "G" in the block diagram uses an auxiliary frequency of 69.255–69.35499 MHz to down-convert the output loop to an IF from 11.2 to 41.4 MHz. Note that a bandpass filter is used to avoid any

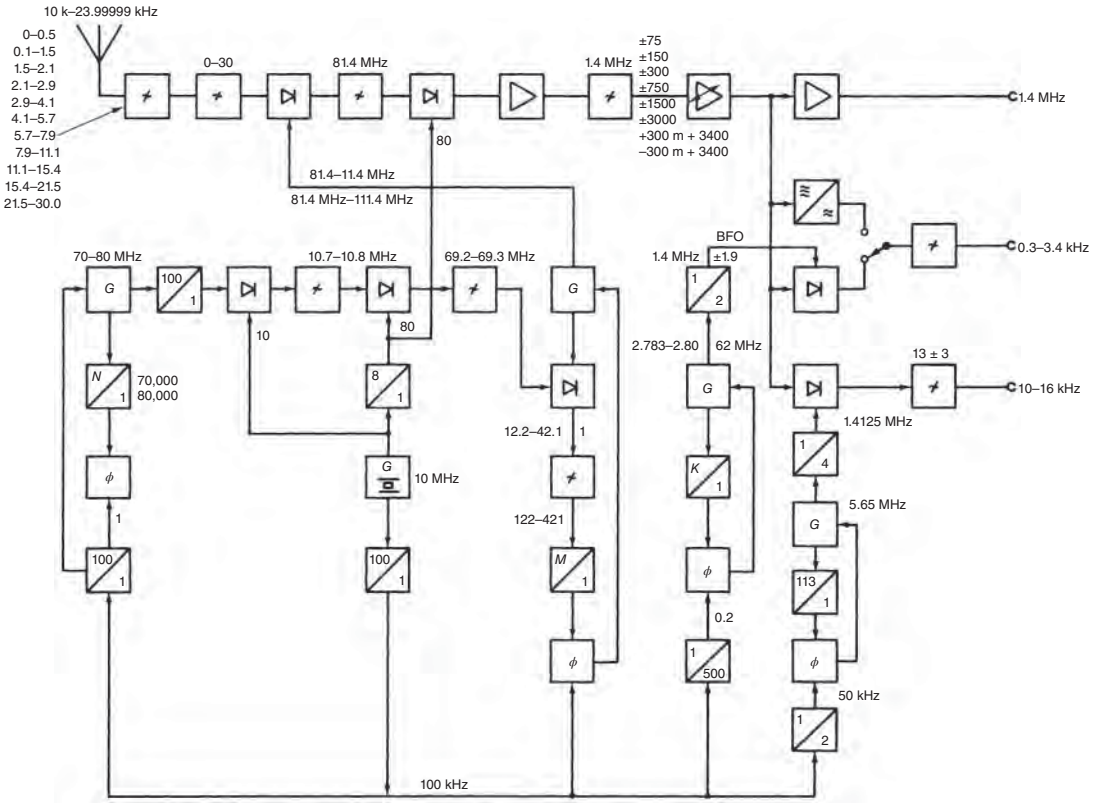

Figure 5-4 Block diagram of the frequency synthesizer of the Rohde & Schwarz EK070 shortwave receiver.

feedthrough of the higher frequencies in the mixer. A programmable divider divides this frequency band down to the reference frequency of 100 kHz, switching the output loop in 100-kHz increments.

The master standard is multiplied up to 80 MHz by using a phase-locked loop (PLL) at 80 MHz to generate the auxiliary frequency, which, together with the fine-resolution synthesizer portion on the left, is used to generate the 69.255–69.35499 MHz window.

The fine resolution is achieved by operating a single-loop synthesizer from 64.501 to 74.5 MHz in 1-kHz steps and then dividing it by 100. The division by 100 gives a step size of 10 Hz, while good switching speed is offered by operating at 1 kHz reference. The output of about 700 kHz is mixed with the 10-MHz frequency standard to a 10.645–10.745-MHz IF. A crystal filter can be used to take out all unwanted frequencies, and this 10.7-MHz signal, together with the 80 MHz generated from the 10-MHz standard, then results in the auxiliary frequency to be mixed into the output loop.

This system has several advantages. The output loop is extremely fast, and the division ratio inside the loop is fairly small. The mixer inside the loop reduces the division ratio from approximately 1104 to about 421 at the most, and therefore the noise generated because of the multiplication is kept small relative to a single-loop approach. However, the divider ratio is now 4:1; without the mixing, the ratio would have been 11:8. Therefore, the loop has to cope with higher gain variations, and the loop filter has to incorporate a mechanism that changed the loop gain corresponding somewhat with the gain variation.

We have learned that the VCO, when switching diodes are used to add capacitance, has a lower loop gain at the lower frequency, where more capacitance is added than at the higher frequency. This provides a simple method to adjust the gain variation inside the loop. With a 100-kHz reference, a loop bandwidth of 2 or 3 kHz will provide enough suppression of reference, and a settling time in the vicinity of several milliseconds is achievable.

The fine-resolution loop that provides the 10-Hz increments now limits the switching time. Most likely, the loop filter will be in the vicinity of 10 Hz or 1% of reference, which will provide 40 dB of reference suppression. The division by 100 at the output increases the reference suppression by another 100, so that the reference at the output is suppressed by at least 80 dB. The use of special inductor-capacitor (LC) filters can easily increase this to 100 dB.

The noise sideband of the 70–80 MHz oscillator depends mainly on the VCO. Even a very simple LC oscillator should provide 120 dB/Hz 20 kHz off the carrier, and the additional 40-dB improvement based on the division by 100 will theoretically increase the noise to 160 dB. This is not very likely, and the noise floor is now determined by the noise floor of the dividers, the mixers, and post-amplifiers and will be in the vicinity of 150 dB.

The output loop operating with about 2 kHz of bandwidth will, outside the loop bandwidth, reproduce the noise performance of the oscillator. We have learned a great deal about low-noise oscillators in this book, and it would be considered standard practice to divide the output loop into at least three oscillators of 10-MHz range so that relative bandwidth $\Delta f/f$ is about 10% or less.

The radio frequency (RF) has to pass an 81.4-MHz crystal filter ±6 kHz wide and then is mixed down to the second IF of 1.4 MHz. The second LO is derived from the same 80 MHz that is used inside the synthesizer loop. This avoids another PLL because of the clever combination of frequencies.

The IF of 1.4 MHz offers the choice of different band filters, as can be seen from the block diagram, and in continuous wave (CW) and single-sideband modes, a beat frequency oscillator (BFO) is required. In addition, this receiver offers, as a novel approach, a recorder output where the IF frequency is mixed to a frequency band from 10 to 16 kHz. As a result of this, additional synthesizers are required. For reasons of short-term stability and noise, the BFO synthesizer is operated at twice the frequency and the output is divided by 2 to obtain the final frequency. A similar approach is used to generate the 468 kHz required to obtain the 10–16 kHz of output.

Let us assume that the frequency resolution of this synthesizer has to be increased by a factor of 10. What would be the easiest approach? The easiest approach would be to take advantage of the HEF4750 and HEF4751 synthesizer integrated circuits (ICs) made by Philips.

The fractional offset portion of this single-loop synthesizer would allow a 100-Hz step size with the 1-kHz reference, and therefore the same switching speed would be maintained. The division by 100 is sufficient to suppress any possible reference problems if the loop filter is changed. This simple change would allow the required resolution.

A much higher resolution would be gained by substituting the 64.5–74.5 MHz single-loop synthesizer with a high-resolution fractional division synthesizer, which then could give almost any arbitrary resolution. In doing so, it would be possible to increase the reference frequency to the 100 kHz used in the output loop, and as a result, the entire switching speed of the synthesizer would be a few milliseconds while at 1 kHz reference, and the 10-Hz loop filter would currently dictate a switching time of about 100 ms. This approach, because of the high division ratio at the output, guarantees the necessary cleanliness. The multiloop synthesizers require a certain amount of hand-holding as far as the construction is concerned. It is highly desirable to provide adequate shielding. Figure 5-5 shows the mechanical construction of an output loop similar to the one described. The metal can on the left contains the VCO. All voltages are fed to the VCO via feed-through capacitors. On the top right side of the printed circuit (PC) board, one can see the crystal filter marked 20.095 MHz. In this case, the 40–70 MHz oscillator is being mixed down to a 50–20 MHz IF, and the crystal filter shown on the PC board assembly is used to clean up the output from the fine-resolution synthesizer. Although this picture was taken from a lab model rather than a production unit, it indicates that it has to be built extremely carefully to give any meaningful results. Note the solid copper surface of the PC board, with all the wire connections underneath the PC board in printed form. Shielding is the next important thing for good reference suppression, and very frequently the design goal will not be met if the shielding is not optimized.

It is advisable to separate RF and logic circuits as much as possible. Figure 5-5 shows the separation between microwave and lower frequency operation. The PC board (Figure 5-6) is a combination of printed circuit board and carefully selected enclosures. In the top right corner several microstrip coupled lines can be seen which acts as a bypass filter. Figure 5-7 shows another part of the SMA100B. All circuits rely heavily on via connections. This provides a good RF ground on the back and top side of the PC board.

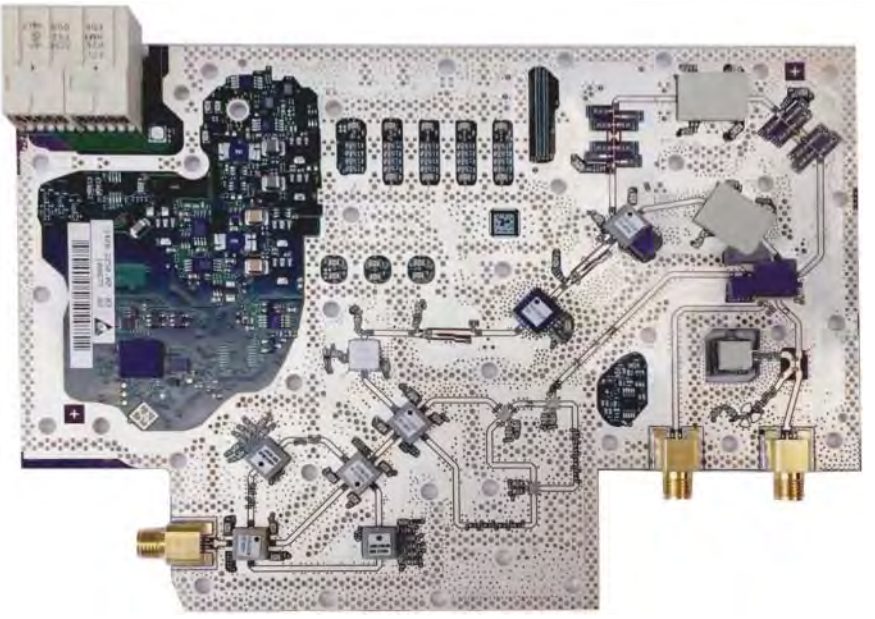

Figure 5-5 Photograph of a building block of the R&S SMA100B: it contains both RF and microwave circuitry.

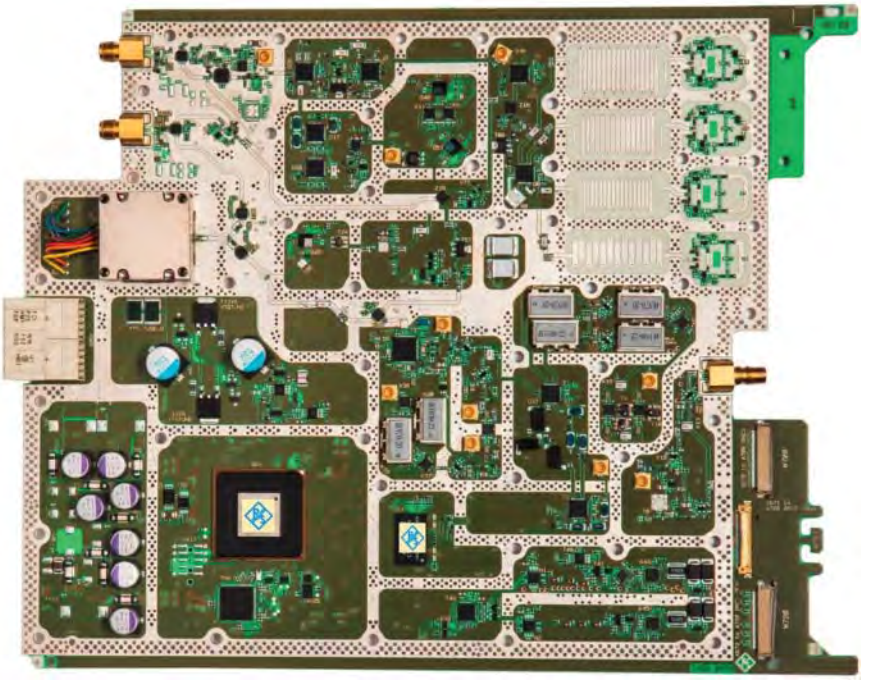

Figure 5-6 Photograph of a part of the SMA100B. Top right corner shows the four microstrip based bandpass filters. The shielding chambers can be easily identified.

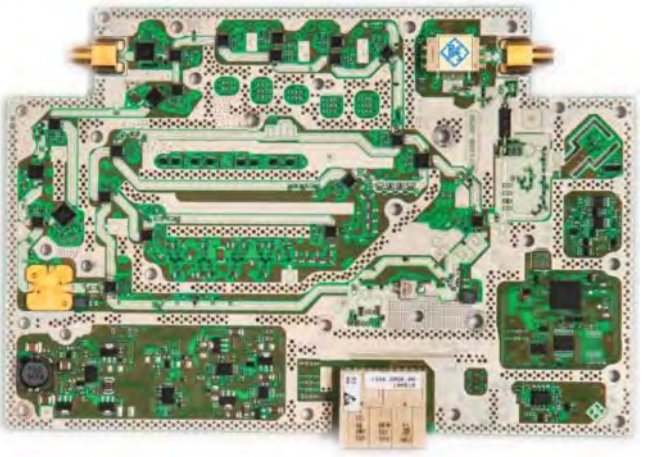

Figure 5-7 Photograph of another assembly module of the SMA100B. The shielded chambers are easily detected.

5-2 SYSTEM ANALYSIS

During our various discussions, it has become apparent that the single-loop synthesizer really is somewhat limited in its application. Unless the fractional division N principle or other methods are used, it is really not possible to build a clean frequency synthesizer at a high frequency output, say, 100–150 MHz, in small increments such as 100 Hz or even 1 kHz with good switching time, reference suppression, and other important parameters. This is probably most easily understood when we analyze various systems. Let us start with a single-loop synthesizer operating from 260.7 to 460.7 MHz, as may be used for a receiver (see Figure 5-8). These are the requirements:

Frequency range	260.7–460.7 MHz
Frequency increments	1 kHz
Frequency stability	1×10^{-8} per day
Spurious outputs	−70 dB
Switching time	20 ms
Phase noise	120 dB/Hz, 20 kHz off the carrier

These are the six most important requirements that have to be analyzed and kept track of in a system. The single-loop synthesizer is not really a system but a single phase-locked loop with a number of inherent limitations.

The frequency range is determined by the VCO. The phase noise of the loop outside the loop bandwidth is determined by the influence of the tuning diodes and the question of whether or not the oscillator is coarse-tuned and whether or not several oscillators are used to cover the range. Table 5-1 shows the noise typically found in a free-running oscillator in this area of operation.

Figure 5-9 shows a graph that compares the noise sideband of several different oscillators. It becomes apparent from this that similar designs have quite different noise performance if the design is not carefully analyzed and the purpose of the synthesizer is not fully understood from the beginning. Both the 41–71 MHz VCO and the Rohde & Schwarz SMDU signal generator use free-running oscillators. The 41–71 MHz VCO is divided into three subranges, and the SMDU uses mechanical tuning, while the maximum electronic tuning is about 1 MHz. This explains the difference in the noise performance, and, in addition, the higher slope of the SMDU indicates also the higher Q of the circuit. The Schomandl ND100M is a frequency synthesizer constructed from many loops, and there is improvement in noise due to division inside the loops, as we will see later in the chapter.

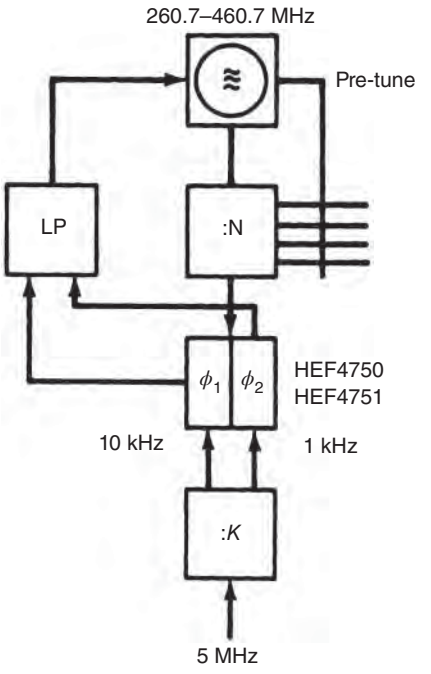

Figure 5-8 Single-loop synthesizer operating from 260.7 to 460.7 MHz in 1-kHz steps.

Table 5-1 Typical noise in an example free-running oscillator

Phase noise, $\pounds(f)$ (dB/Hz)	Offset from the carrier
−55	10 Hz
−75	100 Hz
−95	1000 Hz
−120	10 kHz
−140	100 kHz
−160	1 MHz

Two crystal oscillators are shown: the 5-MHz one-stage crystal oscillator shows fairly high noise below 10 Hz compared with the 5-MHz two-stage crystal oscillator. The phase noise discussions in Chapters 1 and 4 have explained the reason for the different performance.

Let us assume for a moment that our one-loop synthesizer, as shown in Figure 5-8, uses a 5-MHz two-stage crystal oscillator and a tuned-cavity oscillator ranging from 260.7 to 460.7 MHz.

Because of the high Q of the cavity, the VCO noise of this oscillator will be substantially better than that of the 41–71 MHz VCO shown in Figure 5-9.

In order to multiply the 1-kHz reference up to an average frequency of 300 MHz, a division ratio of 300,000 or a multiplication of 300,000 is required. Assuming that a −160-dB/Hz reference signal is present at the output of the reference divider chain at 1 kHz, we can calculate the noise at 300 MHz from this multiplication. The multiplication of 300,000 is equivalent to 109.54 dB, and if we subtract this from 160 dB, the noise floor, the resulting signal-to-noise ratio is 50.46 dB/Hz, 1 kHz off the carrier.

However, if a 1-kHz reference is used, the loop filter has to be narrower than 1 kHz in order to get, say, 70-dB reference suppression.

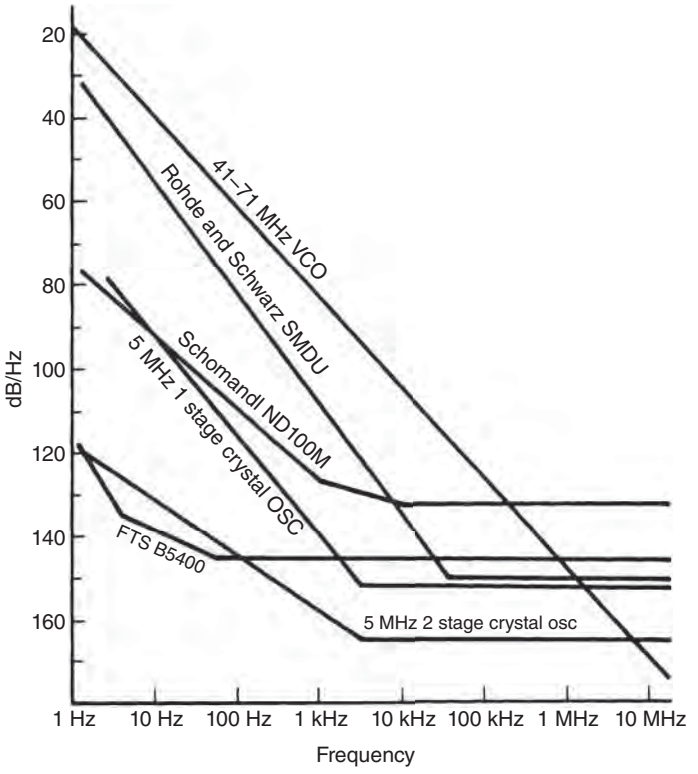

Figure 5-9 Measured noise sideband performance of a 41–71 MHz VCO, Rohde & Schwarz SMDU signal generator, Schomandl ND100M frequency synthesizer, frequency and time services (FTS) BS5400 modulator, and single- and double-stage 5-MHz crystal oscillators.

It can be assumed that a carefully built tri-state phase/frequency comparator will have 40-dB reference suppression by itself, while at least an additional 30 dB of reference suppression has to be provided by the loop filter.

This roughly leads to a natural loop frequency of the PLL in the vicinity of 50 Hz. The reference noise removed more than 50 Hz from the carrier is then reproduced in the output, and we have to reduce our calculation and take 50 Hz rather than 1 kHz off the 5-MHz reference. For 50 Hz our frequency standard shows a noise sideband of −140 dB/Hz, and we have to do the same calculation and deduct 109.54 dB from 140 dB, resulting in a signal-to-noise ratio of 30.46 dB. This signal-to-noise ratio is now less than the VCO would have had by itself, which means that we are actually making the VCO noisier than it would be by itself.

In order to have less influence from the loop, it would theoretically be better to use a wider-loop bandwidth to take advantage of the lower noise of the VCO, since the multiplication inside the loop is so tremendous. However, the reference suppression will then suffer.

Taking a 50-Hz loop bandwidth into consideration, lockup time will be in the vicinity of 60–100 ms, and we are not going to meet our target as far as switching time is concerned. We learned in Chapter 1 that the type 2 third-order loop provides faster lock and higher reference suppression than the type 2 second-order loop. Much-higher-order loops, such as fifth order or higher, have an advantage only if the reference frequency is much higher than the loop bandwidth, as the additional phase shift that is being introduced if both frequencies get too close will make the loop unstable; then the simple type 3 second-order loop is better.

Another way to overcome this problem is to use a sample/hold comparator, where the phase shift seems to be smaller.

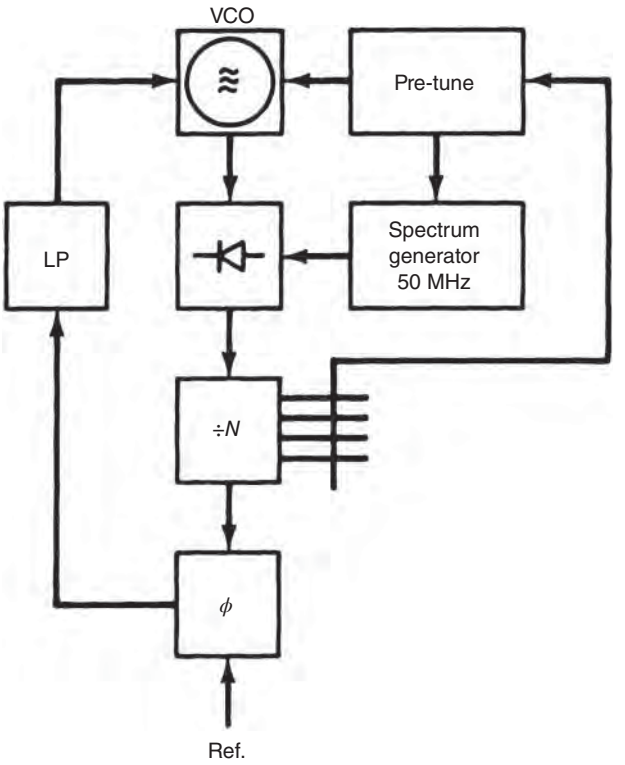

Figure 5-10 A 260.7–460.7 MHz dual-loop approach with a comb generated to obtain a low IF for the dividers.

The fractional division N principle with the zero averaging detector allows an extension of resolution. This method was explained previously and will not be treated again here.

The noise sideband performance outside the loop bandwidth is determined by the VCO, and the switching time by the loop filter. In order to increase the switching speed and improve the noise performance of the oscillator, let us use a design as shown in Figure 5-10. Here we split the range 260.7–460.7 MHz into a number of 50-MHz subbands by selecting the appropriate harmonic of a 50-MHz comb spectrum generated by the 5-MHz frequency standard with the help of a times-10 multiplier and a comb generator (using snap-off or metal–semiconductor field-effect transistor [MESFET] varactors).

Let us take the same 300-MHz center frequency and use a 350-MHz comb line to beat the 300 MHz down to an IF of 50 MHz. By doing this, we have decreased the division ratio inside the loop by 10 or 20 dB, and by using 10 discrete oscillators covering the range 260.7–460.7 MHz, we have decreased the noise sideband performance of the VCO by 20 dB. In doing so we have achieved both goals, increasing the close-in noise performance as well as the noise outside the loop bandwidth at the expense of additional circuits.

The additional circuits incorporate the following:

- A large number of VCOs (can be simulated by the coarse switching range in increments of 50 MHz).
- Designing a 5–50 MHz multiplier and a comb generator to mix frequency ranges down to a lower IF.
- Developing circuitry selecting the appropriate harmonic of the comb and steering the VCO to prevent lockup against the wrong comb harmonic.

This is a somewhat drastic but effective method.

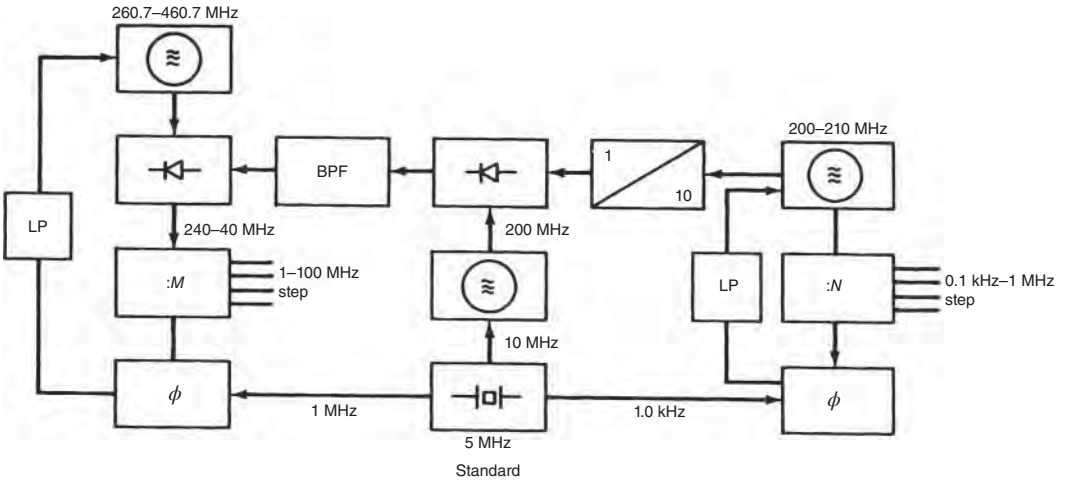

Figure 5-11 Dual-loop frequency synthesizer operating from 260.7 to 460.7 MHz with 100-Hz resolution.

Figure 5-11 shows another way of achieving this. The dual-loop synthesizer now takes advantage of a high-gain loop using a reference frequency of 1 MHz; omitting the influence of the mixing for a moment, the multiplication in the coarse loop is now only 300 or the reduction in noise relative to the 5-MHz reference is about 50 dB.

As the noise floor-out is about 160 dB/Hz for the particular crystal oscillator, the noise floor is increased to −110 dB/Hz and we now can choose our loop filter to cross over with the VCO noise at this point. From the table we used to determine the noise performance of our ultra-high frequency (UHF) VCO, the 100-dB noise of the VCO can be measured at 5 kHz off the carrier.

It will therefore be reasonable to use a filter of 5-kHz bandwidth, as the VCO above this cutoff has less noise than the noise generated by the multiplication inside the loop.

Our reference frequency of 1 MHz would be suppressed by more than 60 dB from a filter having 1-kHz loop bandwidth, not taking the reference suppression of a tri-state and/or sample/hold comparator into consideration.

It is barely possible to build a 1-MHz sample/hold discriminator with low leakage, and the best possible choice will be a combination of some discrete flip-flops optimized in layout forming a flip-flop phase/frequency comparator. A reference suppression of 30–40 dB can be expected here, which adds to a total of 100 dB. The lockup time in this case will be in the vicinity of 1 ms, depending on the type of loop filter.

In Section 1-10 we learned that it is possible to use a dual-time-constant filter, where the frequency acquisition is speeded up by a factor of 20, and therefore the settling time is determined by phase lock rather than by frequency lock. The auxiliary synthesizer mixed into the loop is now responsible for the final resolution.

In our example, we have used an auxiliary synthesizer that has a 10-kHz reference rather than 1 kHz, and its output is also divided by 100. As a result of this, the switching speed of the auxiliary loop is now 10 times higher than the switching speed of our initial one-loop design, taking the same reference suppression into consideration, and the output noise from the VCO, even using the initial crude design where one VCO had to cover the entire frequency range, now permits 20-dB-better phase noise. Figure 5-12 shows the resulting phase noise (A + B) for the two frequency synthesizers as shown in Figures 5-8 and 5-11.

If finer frequency resolution is required and the digibase system, for which Hewlett-Packard and Racal seem to have patents, has to be avoided or if a microwave frequency synthesizer has to be designed, the number of loops has to be increased.

The introduction of the mixer, however, causes two problems:

(1) The required filter is designed with a variable divider. The mixer does not have constant delay and the change in delay can introduce loop stability problems. This filter must be optimized for flat delay inside the passband characteristic.

(2) The mixer has a large number of spurious products, as we learned in Chapter 4.

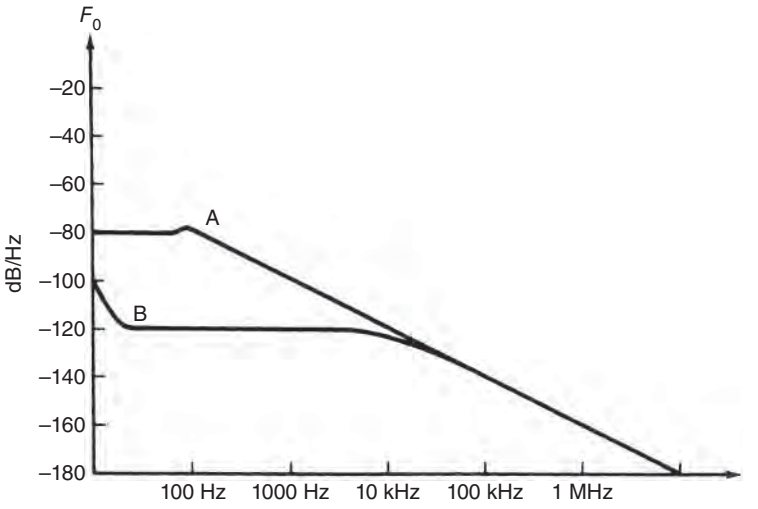

Figure 5-12 Noise sideband performance of synthesizer in Figures 5-8 and 5-11.

Besides the question of proper drive and termination, proper bandpass filters at the output of the mixer are important, and a proper choice of frequencies is similarly important. The phase/frequency detector by itself is a highly nonlinear device capable of mixing actions, which may cause problems when such output is fed into the programmable divider. The programmable divider has only a limited suppression of its input frequency, and therefore the phase comparator will receive not only the output frequency but also, with some limited suppression, unwanted mixer products. It is therefore vital to incorporate a low-pass filter at the output of the divider chain, unless a slow divider chain such as a complementary metal–oxide–semiconductor (CMOS) is used. We have found that combinations of swallow counters in emitter-coupled logic (ECL) with CMOS dividers do not suffer from this difficulty, whereas ECL/transistor-transistor logic (TTL) divider chains definitely require the additional low-pass filter. Similar difficulties have occurred in the past where the input signal from the fine-resolution loop, after being divided down by 10, was mixed into the main loop. It is absolutely necessary to incorporate a filter between the divide-by-10 stage and the mixer and to drive the mixer with a sine wave rather than a square wave.

The next important question is which of the two inputs of the mixer, the LO and RF portion, is being driven by the VCO output. This will determine the spurious response. In our particular case, where we suspect some spurious output to be generated because of the mixer action, it is advisable to use the fine-resolution loop as the LO and have the UHF VCO be at the RF input level.

Because of the losses inside the mixer, a post-amplifier will be required that can be included in the bandpass filter driving the programmable counter for the output loop.

Another way to reduce output noise, avoid spurious response at the output, and use a triple-loop synthesizer to achieve high resolution is shown in Figure 5-13. The output loop uses three VCOs covering the range from 75 to 105 MHz in 10-MHz increments. Each range has about 10% variations, where $\Delta f/f$ equals 10 MHz/85 MHz as the first range.

A second set of VCOs of identical design is locked in a single-loop synthesizer in increments of 100 kHz, and therefore, the programmable divider requires a division ratio between 750 and 1050. The fine resolution is achieved.

Let us take a look at the noise. The highest frequency, 105.1 MHz, dictates a multiplication of 1051 or reduces the noise relative to the reference at 100 kHz by 60.43 dB.

Let us assume that the VCO noise at 1 kHz is about −100 dB/Hz and about −130 dB/Hz at 10 kHz. If the 100-kHz reference noise is −160 dB/Hz (determined by the reference divider noise rather than the standard), the reference noise multiplied up would reduce the signal-to-noise ratio to about −100 dB/Hz, equivalent to the 1-kHz noise of the VCO. It is therefore advisable to set the loop bandwidth of the synthesizer at 1 kHz. Inside the loop bandwidth, the noise will now stay approximately −100 dB/Hz at 1 kHz, deteriorating to −60 dB/Hz at about 1 Hz

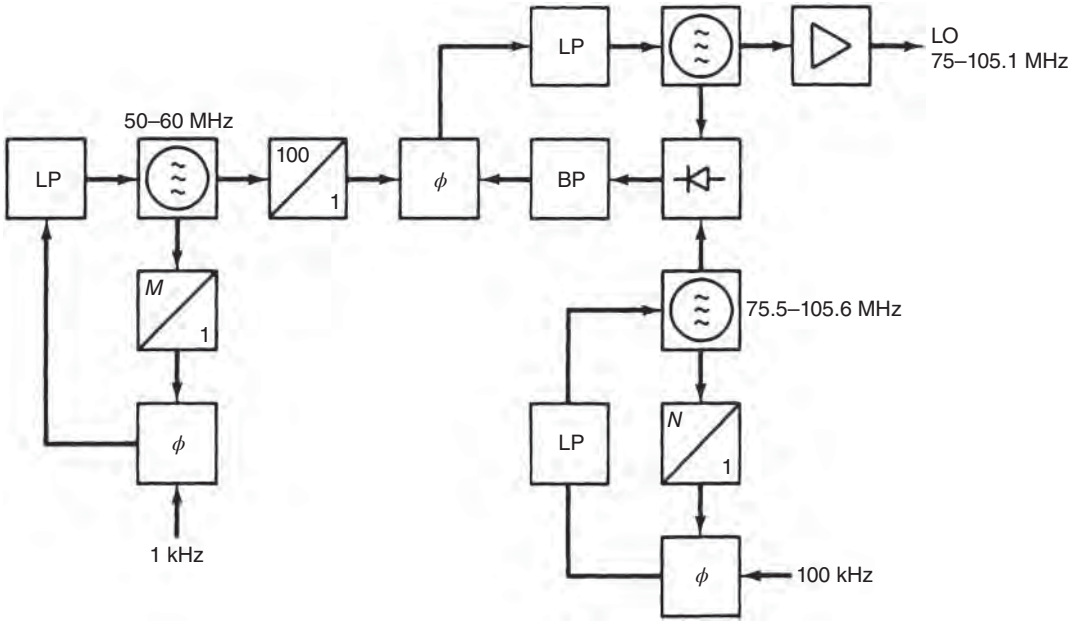

Figure 5-13 Triple-loop synthesizer covering 75–105 MHz.

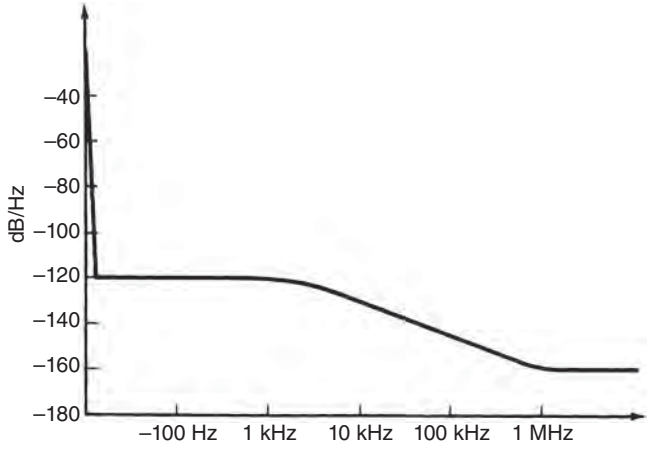

Figure 5-14 Noise sideband performance of the step loop of synthesizer in Figure 5-13.

off the carrier. Outside the loop bandwidth, the VCO determines the noise, and Figure 5-14 shows the resulting noise of this section of the synthesizer. We will call this the *coarse-tuning loop* or *step loop*, as we step through the entire frequency range in increments of 100 kHz. If those oscillator sections were totally identical and mixed against each other, the resulting difference frequency would be zero.

We can, however, use a third loop, a single-loop synthesizer as the fine-resolution loop, and therefore compare the output of the mixing of the two loops with the fine-resolution loop.

The fine-resolution loop uses a 50–60 MHz VCO inside a 1-kHz reference loop.

If this loop is divided by 100 at the output, the resulting output frequency is 500–600 kHz in increments of 10-Hz steps.

The triple-loop synthesizer has several unique features:

(1) There is no divider at the output loop, and therefore the noise present at the phase comparator is not multiplied at the output.

(2) The output noise is equal to the geometric average of the noises between the fine-resolution loop and the step loop.

(3) The noise of the output loop is determined outside the loop bandwidth by the performance of the VCO and inside the loop bandwidth by the 500–600 kHz reference, which is improved by 40 dB because of the division and the step loop, which has a low-noise performance because of the low division ratio, where N remains less than 1100.

The 100-kHz loop can be designed in such a way that the loop filter, together with the phase/frequency discriminator, achieves more than 90-dB suppression with enough safety margin for stability, and the switching time is in the vicinity of 1 ms.

(4) The settling time of the fine-resolution loop can be made much faster due to the fact that the output frequency is divided by 100, and therefore, the reference suppression is increased by an additional 40 dB.

Let us assume that the required reference suppression of the 1-kHz reference is 100 dB. We know that the division by 100 at the output reduces the reference by 40 dB, so we have to achieve an additional 60 dB between the loop filter and the phase/frequency comparator.

A tri-state phase/frequency comparator enables us to obtain at least 40 dB of reference suppression, so that the output filter only has to supply an additional 20 dB. As a result of this, the loop filter can be set to a loop bandwidth of approximately 100 Hz. In practice, however, one would drop the requirement of the reference suppression of 100 dB, setting it at 90 dB, and then a loop bandwidth of 300 Hz is sufficient. In doing this, a settling time in the vicinity of 6 ms is achievable, providing a total system's settling time in this vicinity, as the output loop and the step loop are much faster.

(5) There is, however, a potential hazard. As both VCOs operate very close at such a high frequency, care has to be taken that one VCO always remains higher than the other to avoid an image problem. Such an image problem would definitely allow false lock, and therefore make the loop unstable, and would give the wrong output frequency. To avoid this, the output loop is receiving coarse-steering information from the step loop, and the step loop by itself is coarse set by a 100-kHz, 1-MHz, and 10-MHz activated D/A converter.

An additional auxiliary circuit is provided, which assures that the one frequency always remains higher than the other, and a set of operational amplifiers, together with a frequency detector, takes care of this problem.

At first, this type of circuit may appear difficult, but this principle allows the design of an extremely low-noise synthesizer together with a substantial reduction in spurious signal inside the loop, as two large frequencies are mixed against each other down to a low IF, which in our case is 500–600 kHz. Other combinations may have some advantages from certain design points but definitely have more spurious outputs and have worse noise performance. Table 5-2 shows the performance of this multi-loop synthesizer.

5-3 LOW-NOISE MICROWAVE SYNTHESIZERS

Low-noise microwave synthesizers, although they operate above 1 GHz, consist of a number of different building blocks. These blocks are either analog or digital in nature. The digital interfaces such as microprocessors will not be addressed here but are necessary to perform some of the number crunching involved in controlling the

Table 5-2 Performance of 75–105 MHz multiloop synthesizer, 10-Hz step size

Stability	Depends on standard
Phase noise	−90 dB/Hz 1 kHz off the carrier −135 dB/Hz 20 kHz off the carrier −140 dB/Hz 100 kHz off the carrier −85 dB/Hz 60 Hz off the carrier
Switching speed	6 ms
Spurious output	−90 dB

internal synthesizer auxiliary stages. Synthesizer building blocks are comprised of oscillators, dividers, and various loops, such as translation loops. We will first look at a number of block diagrams and then proceed from the more traditional approach toward the very latest technology. Despite progress made in the various disciplines, fundamental performance as far as phase noise is concerned is still determined by the loop and its components (such as transistors and tuned circuits). The achievable figure of merit, or Q, depends solely on mechanical size and materials used. We do not believe that we will see the development of any additional high-Q resonators, that is, crystals, dielectric resonators, surface acoustic wave (SAW) resonators, ceramic resonators, yttrium iron garnet (YIG) oscillators, and LC oscillators.

For microwave applications, the YIG oscillator (while temperamental in nature) combines the best tunability, linearity, and widest frequency range. The electronic equipment used to provide coarse and fine steering, however, is complex and costly. Modern computer-aided design (CAD) tools will permit us to look at the loop response for phase noise, gain (stability), and lock-in time.

We will examine critical stages of various oscillator types, as available, and look at CAD applications versus actual measurements and different technological application for clean signals.

Moving toward the millimeter-wave range, 40 GHz and higher, we will show an monolithic microwave integrated circuit (MMIC) oscillator used for "smart" ammunition purposes. It turns out that even these applications require low-noise high-performance synthesizers. Finally, we will present a quick look at the transient response of oscillators for the purpose of examining the actual time it takes the oscillator to settle, which is a limiting factor generally not considered by designers.

5-3-1 Building Blocks

Microwave synthesizers are essentially an extension of the RF synthesizers, which are found in test and communication equipment. The traditional approach for building synthesizers with fairly simple structures pretty much ends at 1 GHz. There are many reasons for this. The number one reason, of course, is that the resulting division ratio becomes very high. As a result of such high division ratios, the output phase noise can change quite drastically. By tightening the loop bandwidth, one can use the output VCO to be the dominant noise source outside the loop bandwidth; however, this has its limits. One of the early high-performance microwave synthesizers designed by California Microwave is shown in Figure 5-15 [1]. It shows all the typical building blocks one must consider when looking into microwave synthesizer design. A voltage-controlled crystal oscillator, which is locked to a stable reference, is first multiplied by 2 and then by 10. This provides an output frequency between 1280 and 1380 MHz, and the phase detector is typically a harmonic sampler consisting of two diodes as a microstrip discriminator. The output VCO can be locked with a fairly wide bandwidth (up to several hundred kHz) and will have sufficient suppression for the subharmonic frequencies generated in the loop (80–90 dB).

Actually, one can replace this subsystem with a comb generator, but then it becomes quite tricky to filter out the appropriate spectral line and sufficiently suppress the adjacent unwanted line. If the output frequency has only a

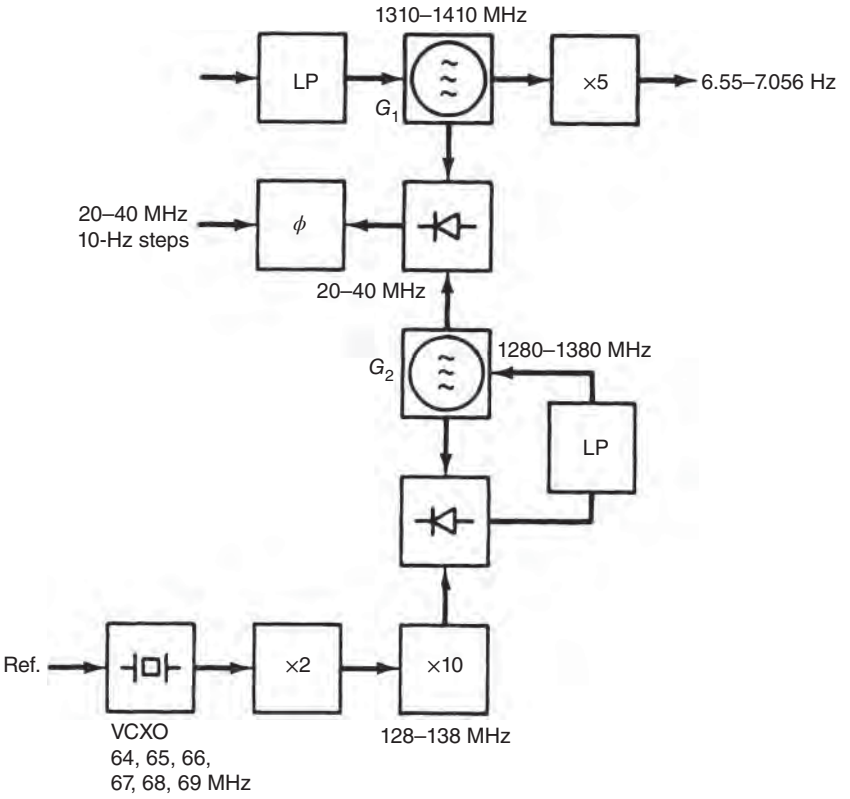

Figure 5-15 Block diagram of a microwave frequency synthesizer using an internal IF of 20–40 MHz. G_1 and G_2 are cavity oscillators. If a wider frequency range is required, YIG oscillators may be used to replace those oscillators and the ×5 multiplier in the output may not be necessary.

fairly narrow bandwidth requirement, the actual output loop can be mixed down to a low IF, in this case 20–40 MHz, and then the fine resolution can be obtained here. A ×5 multiplier at the output then brings the signal up to the desired value. The actual tuning range is about 8% and if both G_1 and G_2 are cavity-tuned oscillators with very high Q, the resulting phase noise is quite good. Figure 5-16 shows the noise sideband performance of the model CV3595 microwave down-converter measured at 7 GHz and Figure 5-17 shows the actual block diagram of the total system.

This early type of microwave synthesizer, while achieving quite good phase noise, has a large number of building blocks and is both bulky and expensive. On the other hand, if the output is divided down (for comparison purposes) into a very high frequency (VHF) like 150 MHz, the phase noise can be reduced by 33.4 dB. In two-way communications a spacing of 30 kHz off the carrier is always a critical number and the resulting phase noise would be roughly 148 dB. Compared with modern signal generators, this is not an extremely high performance, but even today's state of the art in this frequency range is approximately 150 dB and the 2-dB variance is not significant. The major drawback of this design, of course, lies in the fact that it only shows a very narrow frequency, which for general applications is not very useful.

This method can be extended as shown in Figure 5-18 [2]. The phase noise analysis, however, shows that the resulting phase noise is in a similar category, which is obvious since the division ratios are fairly high. The resulting phase noise depends strongly on the quality of the oscillators labeled VTO1 and VT02, and because of the fixed divide-by-10 ratio, the phase noise is worsened by 20 dB (multiplied inside the loop). The fact that the oscillator VT02 is divided by a fairly large number also means that one should keep the loop bandwidth fairly

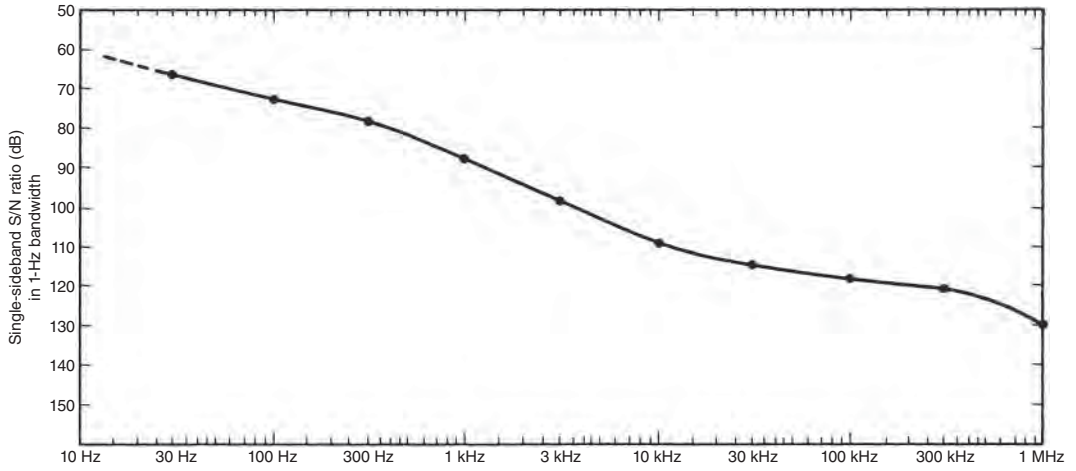

Figure 5-16 Noise sideband performance of model CV3594 microwave down-converter measured at 7000 MHz.

narrow, otherwise the phase noise is multiplied up into the VCO. The drawbacks of a narrow loop bandwidth are that the switching speed is slow and the VCO is subject to microphonic effects.

When building a 20–30 MHz oscillator, there are no particular high-Q resonators available and such an LC oscillator will have a general operating $Q_L \leq 200$. This is small compared with the Q of ceramic resonator oscillators (CROs) or dielectric resonator oscillators (DROs), which would be used in a different frequency scheme. The same applies to VTO1 as well, since its output is multiplied inside the loop. The sample in Ref. [2] uses approximately 1 GHz for the VTO1. This is an ideal frequency for using a CRO.

A different approach, which results in overall better performance, is shown in Figure 5-19. Figure 5-19 shows the block diagram of the YIG oscillator-based first local oscillator (LO) of a spectrum analyzer with very low phase noise. While the basic approach of the synthesizer is similar to the previous two examples, there are some exceptions to the rule. First, in order to have a very low phase noise oscillator, a 200-MHz CRO is used as input for the multiplier.

At a frequency of 200 MHz, an operating Q_L of 600 is obtainable for such an oscillator and because of the pulling range of <5%, there is very little noise contribution from the tuning diode. By mixing the oscillator down to an IF of 3.84–11.54 MHz, using a 200-MHz VXCO-based reference frequency, the actual division ratio is 1. Therefore, the added phase noise caused by a divider chain is avoided. The phase noise of the 200-MHz oscillator itself is determined by the operating Q_L and by the output power of the transistor oscillator. At these frequencies, one has the option to use either field effect transistors (FETs) or low phase noise bipolar transistors (BIPTs). Device and oscillator topology will be addressed later. Fine resolution for this oscillator is achieved by a fractional division N dual-loop system, whereby both the divide by N and divide by M use both integer and fractional values. This particular principle has two distinct advantages. One is that despite the fairly low division ratio one obtains fine resolution, and the second is that the actual spurs that occur are at least 500 kHz away. Since their location is predetermined, notch filters can remove those discrete spurs while maintaining the widest possible loop bandwidth. This method does not require all the complicated housekeeping mathematics required by the full fractional division N. The 50–95 MHz oscillator can be made quite clean and the divide-by-N stage, which feeds the phase detector, has an extremely low phase noise floor, in the vicinity of −170 dBc/Hz operating with several hundred kHz loop bandwidth. The divide-by-M loop, which controls the 50–95 MHz oscillator, is also very clean and its phase noise depends on the actual oscillator.

In many cases, it is desirable not only to have fixed frequencies but also to have the ability to have very fast sweeps. The 5–20 MHz signal required for the phase detector can be generated either from a very fast fractional divide-by-N synthesizer or from a double-loop fine-resolution synthesizer, as shown in the block diagram. The

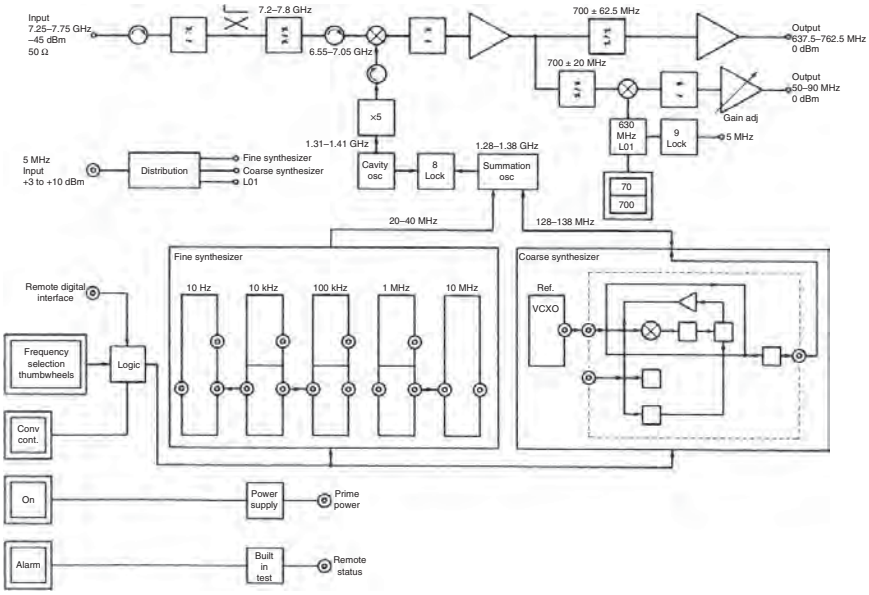

Figure 5-17 Block diagram of model CV3594 microwave down-converter.

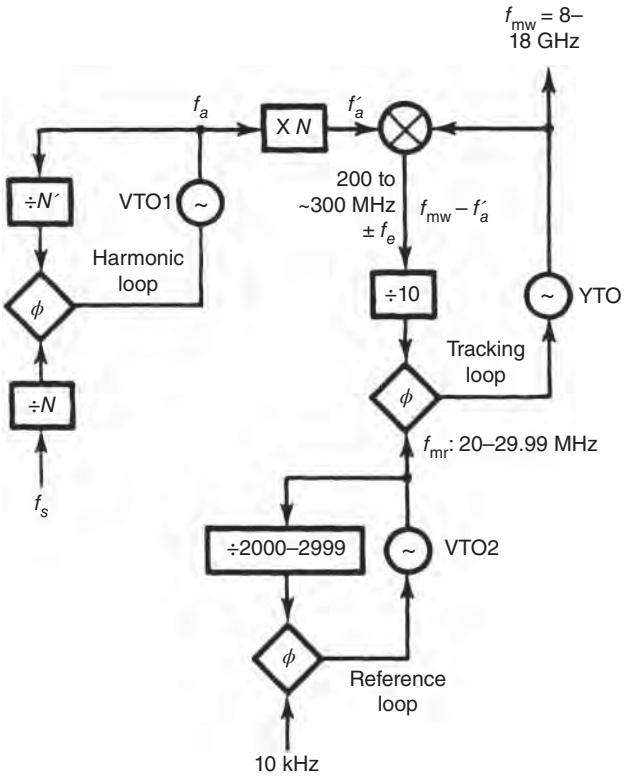

Figure 5-18 Wideband microwave frequency synthesizer, 8–10 GHz.

decision to use either the fractional divide-by-*N* synthesizer or a direct digital synthesizer (DDS) will be discussed shortly.

5-3-2 Output Loop Response

For the purpose of analyzing the output loop, we are going to look into the VCO (YIG) oscillator and other contributors to get a better understanding of what the overall response is. Figure 5-20 shows the phase noise of a free-running high-*Q* YIG oscillator at 7 GHz. The particular YIG is based on the Siemens 15-GHz f_t silicon transistor and uses a combination of coarse and fine steering. The topic of YIG stabilization will be addressed later. This phase noise performance is based on stabilization with very narrow bandwidth, and free-running measurement even with a delay line discriminator would be difficult. The approach selected here allows a switch in the loop bandwidth, which results in a speed-versus-phase-noise comparison.

Figures 5-21 and 5-22 show the single-sideband phase noise as a function of the loop bandwidth. The loop bandwidth certainly influences the locking of the phase lock loop. The higher-order loop, as applicable here, uses complex filters and the stability border diagram as shown in Figure 5-23 indicates such a design. The open-loop gain curve indicates a sharper roll-off above 500 kHz and the response components will be suppressed by 12 more than 90 dB. It is very important to select the proper time constants in the loop filter. Figure 5-24 shows an optimized response and Figure 5-25 shows the ringing that occurs if the postfilters do not provide the desirable 45° of phase margin. Figure 5-26 shows the phase noise achieved by a fine-resolution system.

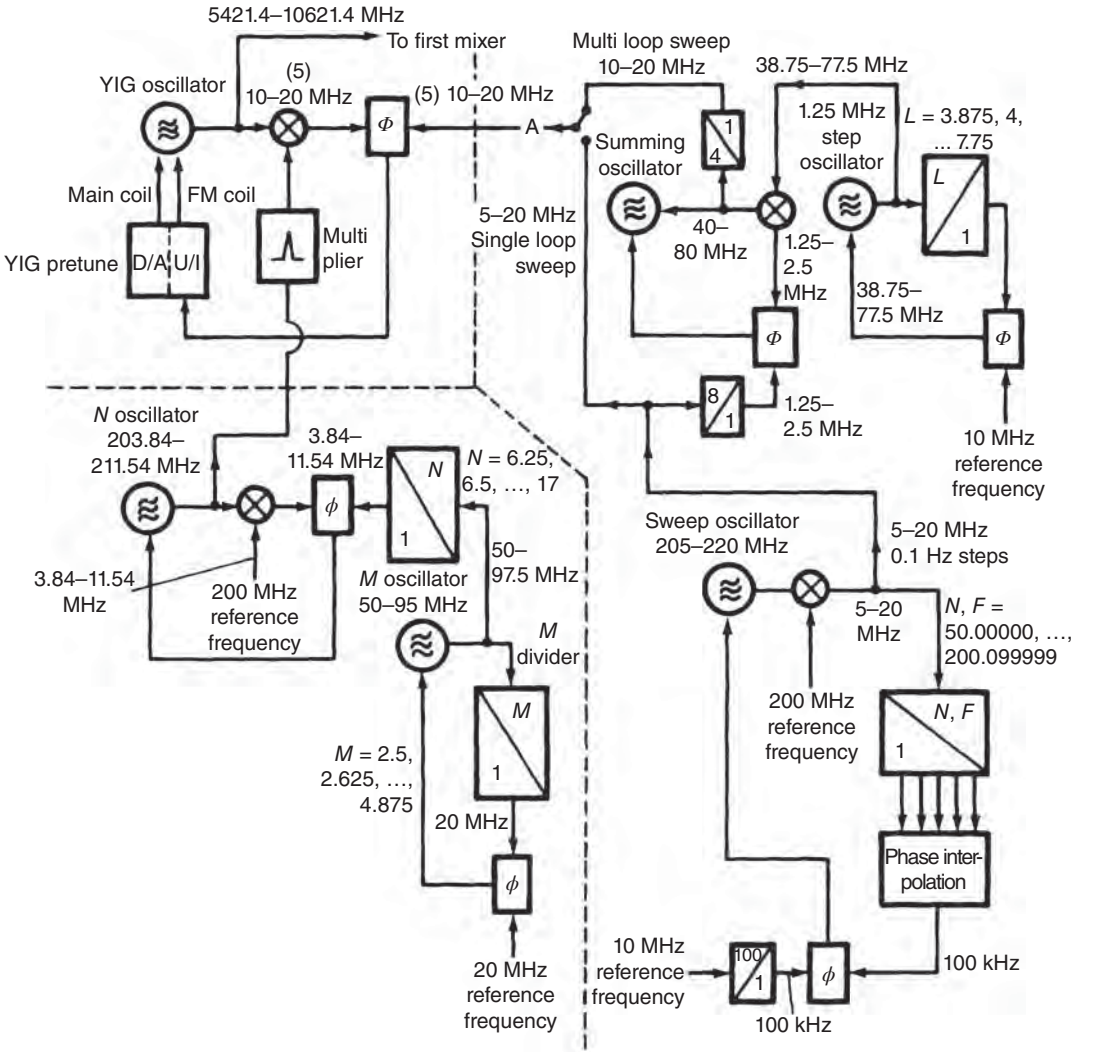

Figure 5-19 Interaction of the frequency-determining modules of the first local oscillator of a microwave spectrum analyzer.

5-3-3 Low Phase Noise References: Frequency Standards

The synthesizer's architecture requires a number of auxiliary frequencies that are all traceable to a master standard. However, requirements for long-term stability and low phase noise are diametrically opposed. Long-term stability means low aging, and, therefore, the operating mode for the crystal oscillator is different from that used in a high signal-to-noise ratio operation. A similar case is found in a rubidium atomic frequency standard (second standard) or in a primary cesium standard. These features are combined, but their cost may exceed the budget for the appropriate time/frequency standard. Therefore, an acceptable approach is to dedicate crystal oscillators at 10 or 100 MHz, which will serve sufficiently as low phase noise auxiliary sources.

Figure 5-27 shows the reference source generation for fixed frequencies as used in a complex synthesizer. Another item one needs to consider is the pulling effect or interaction between the different outputs. For

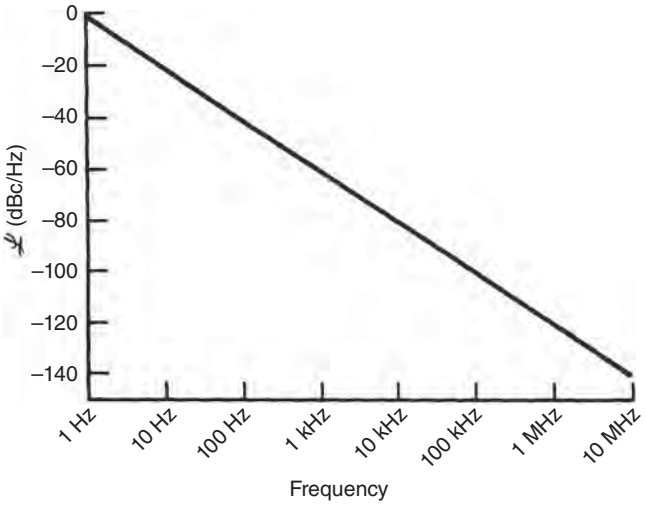

Figure 5-20 Predicted worst-case single-sideband phase noise of a YIG oscillator operating at 7 GHz.

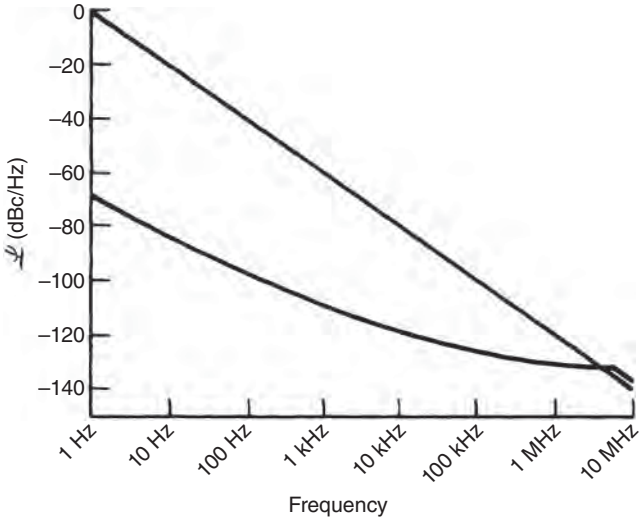

Figure 5-21 Predicted worst-case open- and closed-loop phase noise of a YIG oscillator with loop filter frequency of 4 MHz.

high-performance synthesizers, one needs not only frequency but also phase stability, and therefore, the change of load must not change any output phase relationship.

A typical case is where the frequency divider is driven by a reference frequency as a time-dependent loading, and therefore, the phase will jump as a function of the toggle occurring at the input of the integrated circuit. To prevent these effects, one has to design very special isolation stages.

In a similar fashion, one has difficulties with the YIG oscillator relative to the comb generator. The tuning sensitivity of the main coil is extremely high and complex circuitry is required to properly position the YIG oscillator prior to when the frequency/phase lock will occur.

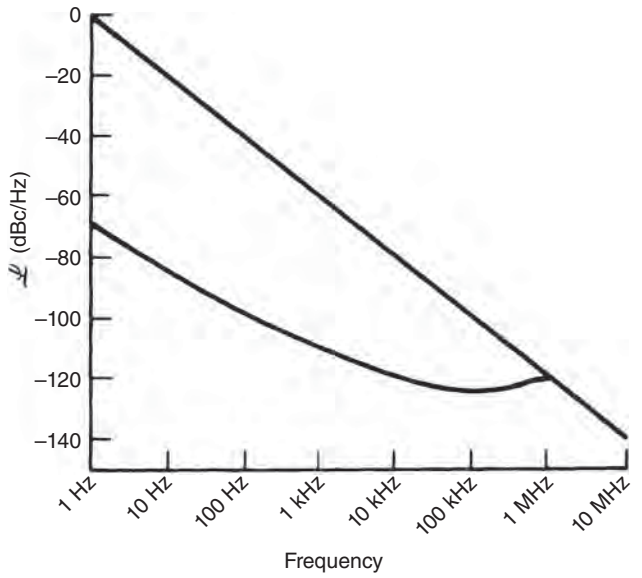

Figure 5-22 Predicted worst-case open- and closed-loop phase noise of a YIG oscillator with 1-MHz loop bandwidth.

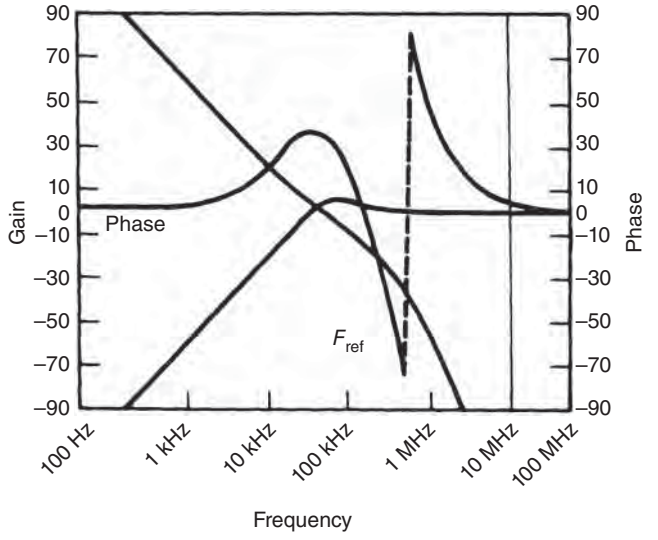

Figure 5-23 Bode plot of the fifth-order PLL system for a microwave synthesizer. The theoretical reference suppression is better than 90 dB.

Figure 5-28 shows the block diagram of this pretuning circuit for the YIG oscillator. By analyzing the circuit, it becomes apparent that the level of effort to do this properly is quite high. There are also provisions for the modulating the system, and therefore, there are also inputs for frequency modulation (FM). Figure 5-29 shows the YIG's synchronization in greater detail.

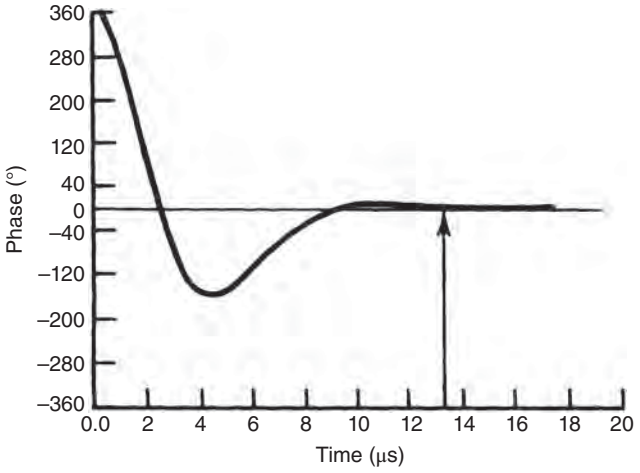

Figure 5-24 Look-in function of the fifth-order PLL. Note that the phase lock time is approximately 13.3 μs.

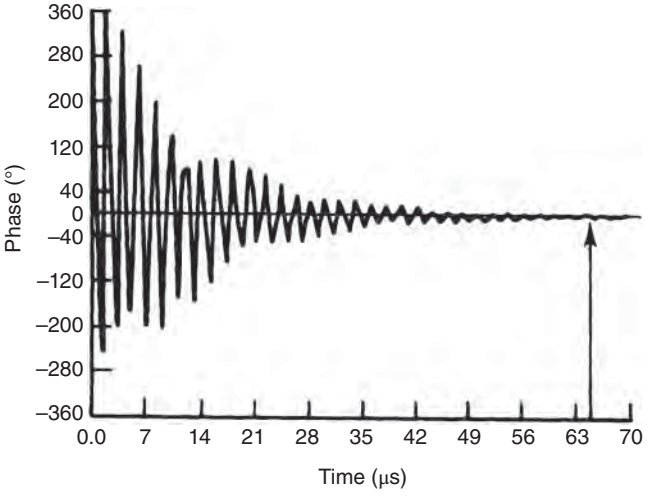

Figure 5-25 Lock-in function of the fifth-order PLL. Note that the phase margin has been reduced to 33° from the ideal 45°. This results in a much longer settling time of 62 μs.

5-3-4 Critical Stage

Oscillators

While YIG oscillators are specialty items and must be purchased from select manufacturers, such as Hewlett-Packard, Avantek, and Watkins–Johnson, the general tendency is to custom-build VCOs for each application. At the lower frequencies, below 200 MHz, there are two types of VCOs. One is actually a voltage-controlled crystal oscillator and the other is a high-performance LC oscillator.

Figure 5-30 shows the low phase noise of a 10-MHz voltage-controlled crystal oscillator, where its phase noise is about 8–10 dB better than the HP10811A frequency standard; however, its long-term stability obviously is not as good.

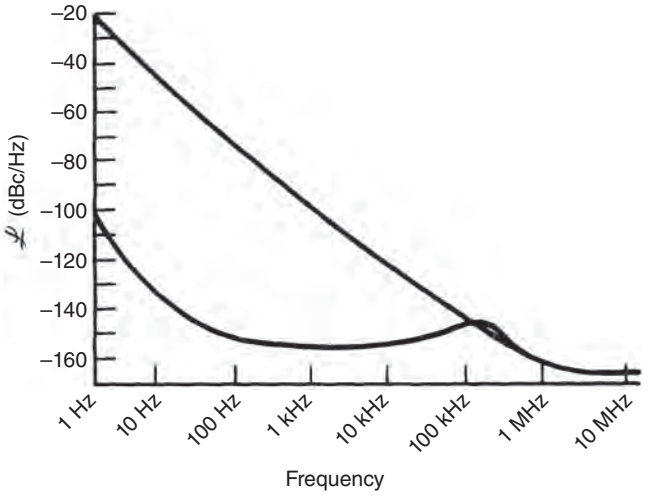

Figure 5-26 Predicted worst-case phase noise as achieved by the fine-resolution system (open-and closed-loop).

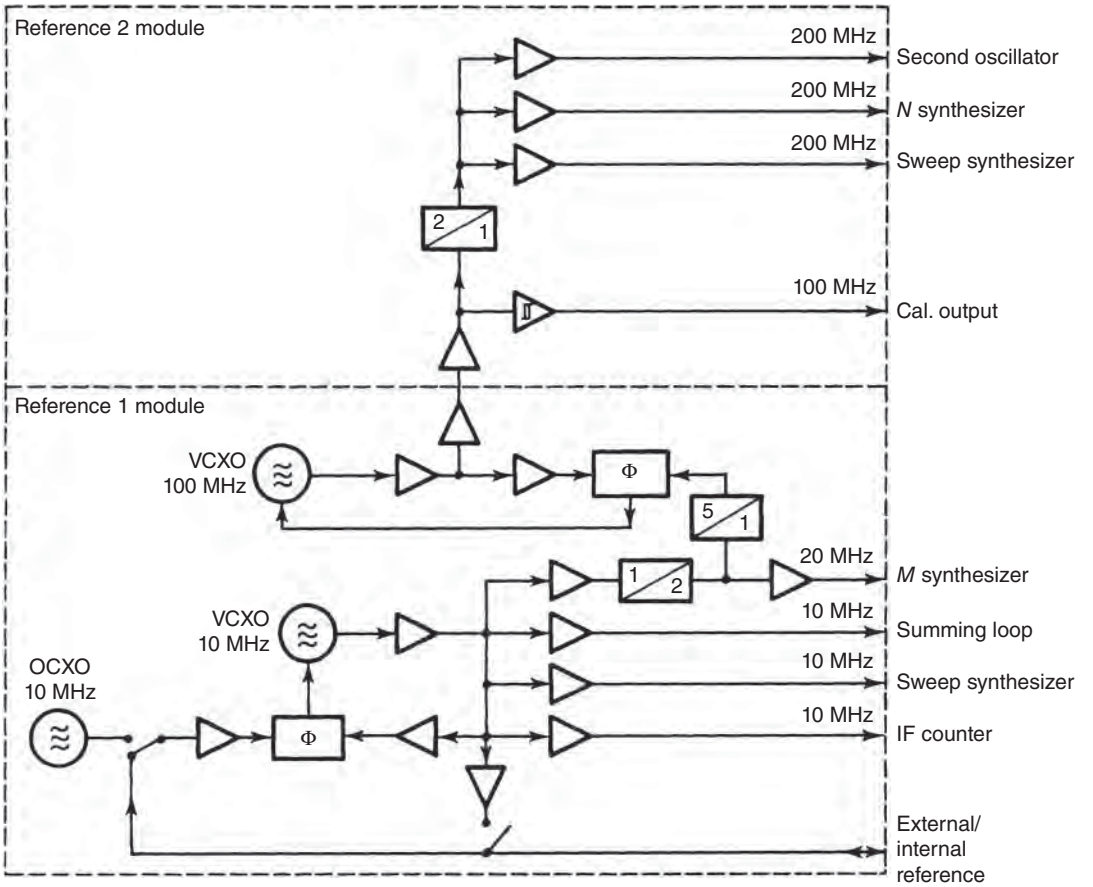

Figure 5-27 Generation of phase/frequency coherent reference frequencies.

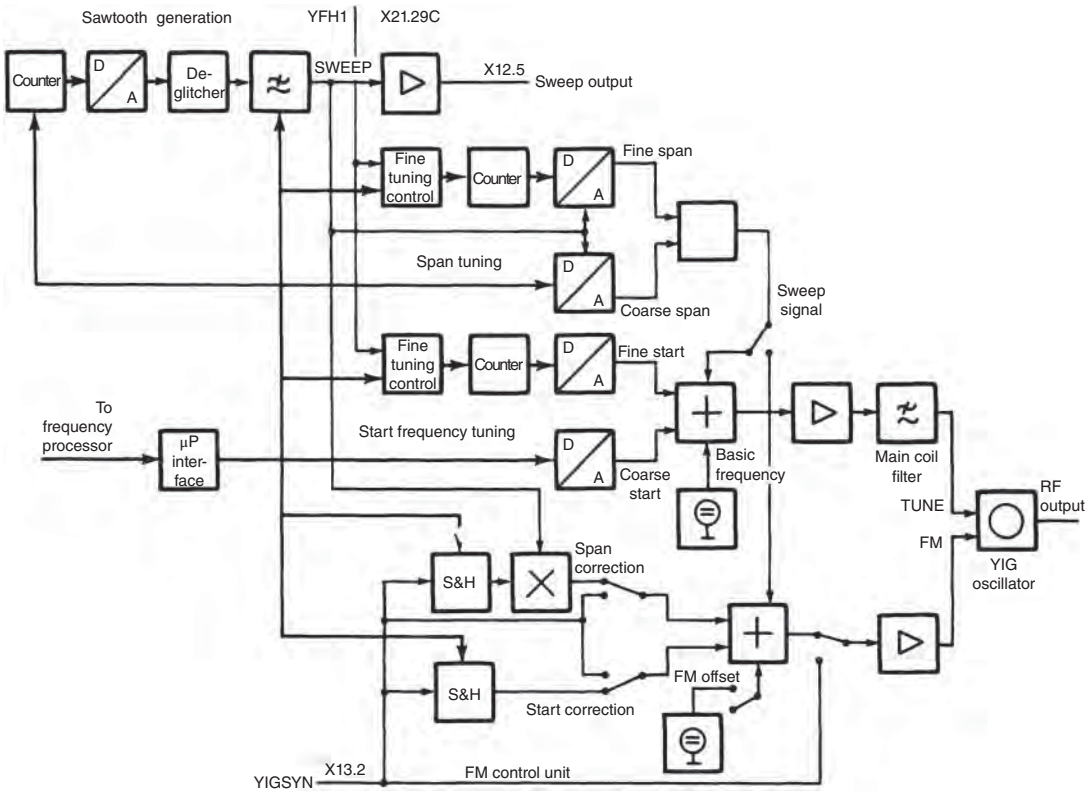

Figure 5-28 Coarse/fine steering of the YIG oscillator including sweeping capability.

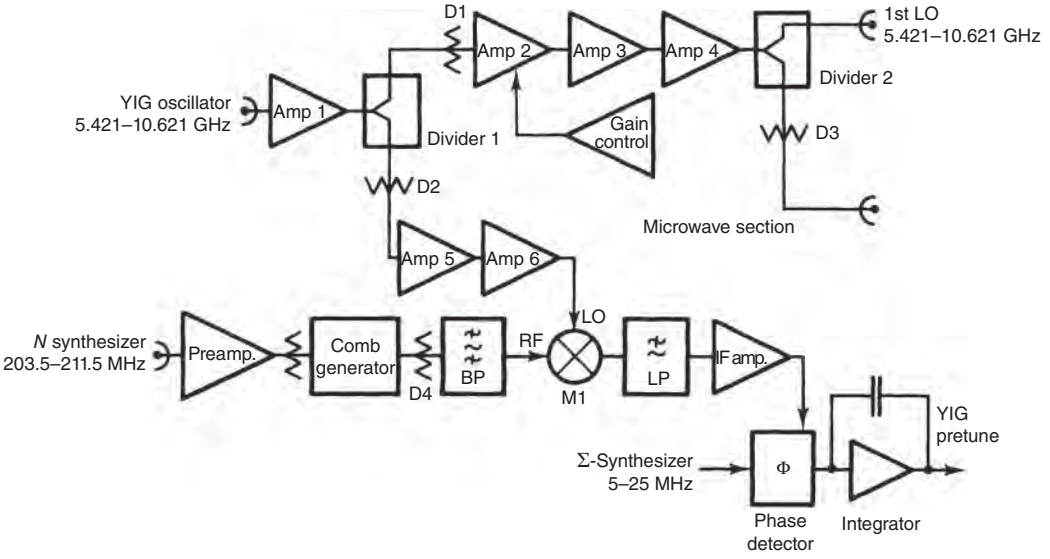

Figure 5-29 Block diagram of the YIG synchronization.

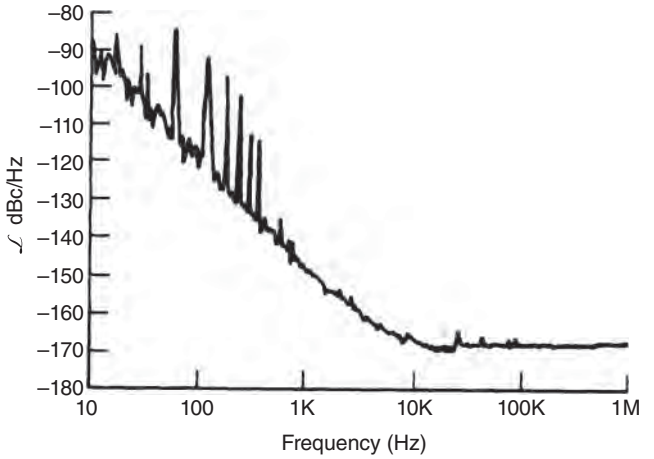

Figure 5-30 VCXO short-term frequency stability for 200 μW crystal dissipation.

Figure 5-31 shows the actual circuit diagram. The oscillator's configuration is similar to what is referred to as a Butler oscillator in common literature. This means the frequency-selective device is located between two emitters and the tuned circuit is in the collector of one of the transistors.

The PNP transistors type 2N5160 are 2-W plus devices with an f_t above 1 GHz. By having a two-stage crystal oscillator, the feedback loop can be made high enough so dissipation in the crystal remains reasonable.

Figure 5-32 shows the circuit of the 100-MHz voltage-controlled crystal oscillator. Modern CAD tools like harmonic balance simulators allow accurate phase noise predictions for any type of oscillator and can also handle optimization.

Figure 5-33 depicts a screen capture of the simulator used for predicting the phase noise. The simulator shows the circuit file including the nonlinear parameters for the bipolar transistor and, after performing the harmonic balance simulation, shows the harmonic contents of the oscillator signal in the frequency domain and in the time domain (distorted waveform rather than sinusoidal curve). Finally, it also shows the single-sideband (SSB) phase noise. Our experience with these types of circuits has been that accuracy is within 1 or 2 dB compared with the measured data. By allowing the component's values to vary and by varying the dc bias point, one can optimize the circuit for the best phase noise.

Figure 5-34 shows that the close-in phase noise of the free-running oscillator was improved by 32 dB. By introducing negative resistance feedback, we change the feedback loop gain and therefore the loading of the tuned circuit. The "cleanup" of the close-in phase noise is done at the expense of the far-out noise. This oscillator example shows that for frequencies greater than 20 MHz away, the noise source is now marked to 160 dBc/Hz compared with 168 dBc/Hz. However, this is still far better than needed for practical application.

Other Key Components

Other key components for low phase noise are the use of SAW devices and DROs. These oscillators cannot be pulled too much but can be phase-locked fairly narrow against a frequency standard. This is useful in obtaining auxiliary frequencies that are very clean. Figure 5-35 shows the measured phase noise spectrum for one laboratory prototype 675-MHz SAW delay line VCO.

Figure 5-36 shows the measured phase noise spectrum for one *L*-band (982 MHz) dielectric resonator oscillator. The measured data for Figures 5-35 and 5-36 were provided by Don Parker, National Institute of Standards and Technology (NIST), formerly of Raytheon Corp.

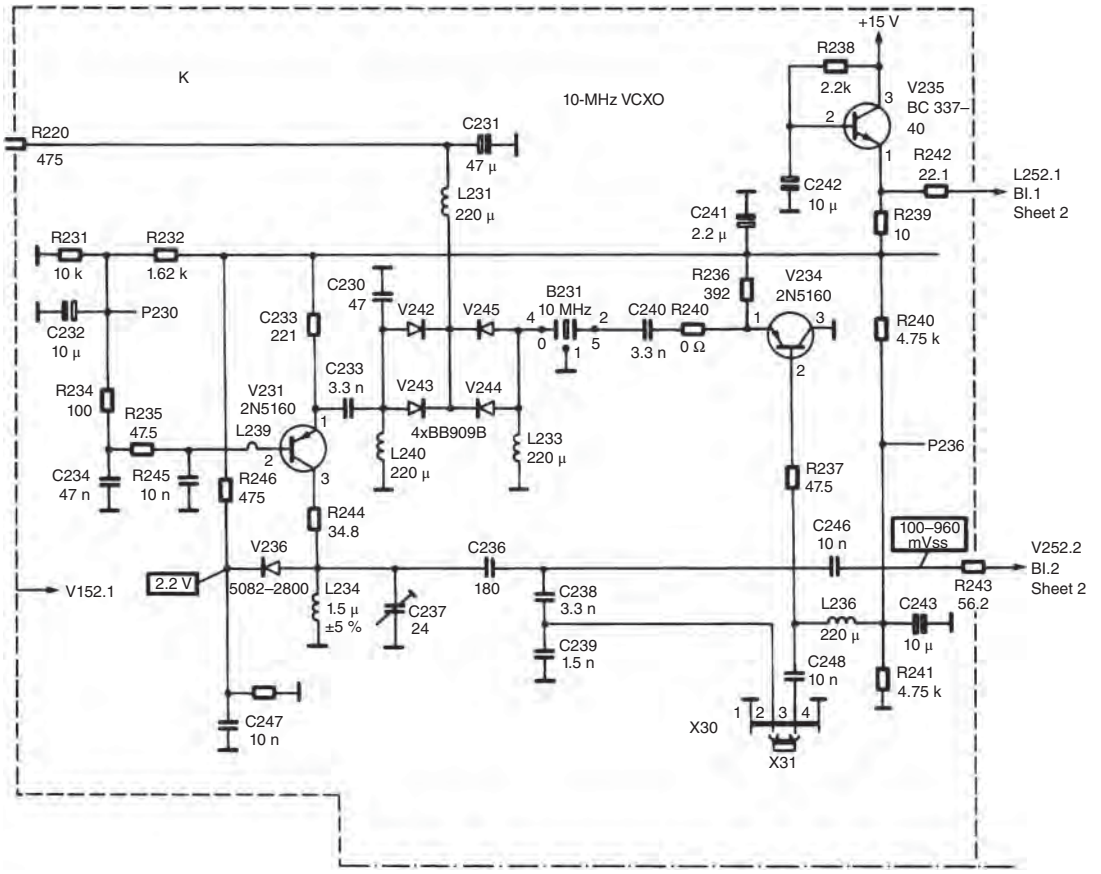

Figure 5-31 Low phase noise crystal oscillator for 10-MHz generation will be locked against the master standard.

Now we turn to VCOs. Figure 5-37 shows a cavity-based low phase noise oscillator with a decoupling stage. Its performance is similar to the HP8640 signal generator or the Rohde & Schwarz SMDU. The phase noise at 400 MHz, 25 kHz off the carrier, is generally 145–148 dBc/Hz. A hybrid for the very-high-Q resonator oscillator and LC oscillator is the CRO. This type of oscillator uses a ceramic resonator that is electric quarter-wavelength and uses dielectric material for an ε_r of 38–88.

The advantage of this type of oscillator is that it combines small mechanical size with high Q and low cost. Figure 5-38 shows the schematic of such a CRO. In modeling this circuit, the CRO should be modeled with a cable for high dielectric constant.

Figure 5-39 shows the measured phase noise of the oscillator shown in Figure 5-38.

Figure 5-40 shows the predicted phase noise of the 1-GHz ceramic resonator VCO without the tuning diode, and Figure 5-41 shows the predicted phase noise of the 1-GHz ceramic resonator VCO with the tuning diode attached. Note the good agreement between the measured and predicted phase noise.

For lower frequency application and wider tuning range, a different approach is necessary. The previous example has shown that the tuning diode adds a lot to the phase noise and, therefore, the pulling range should be kept minimal. Figure 5-40 shows a narrowband VCO that has been optimized for low phase noise operation at 200 MHz.

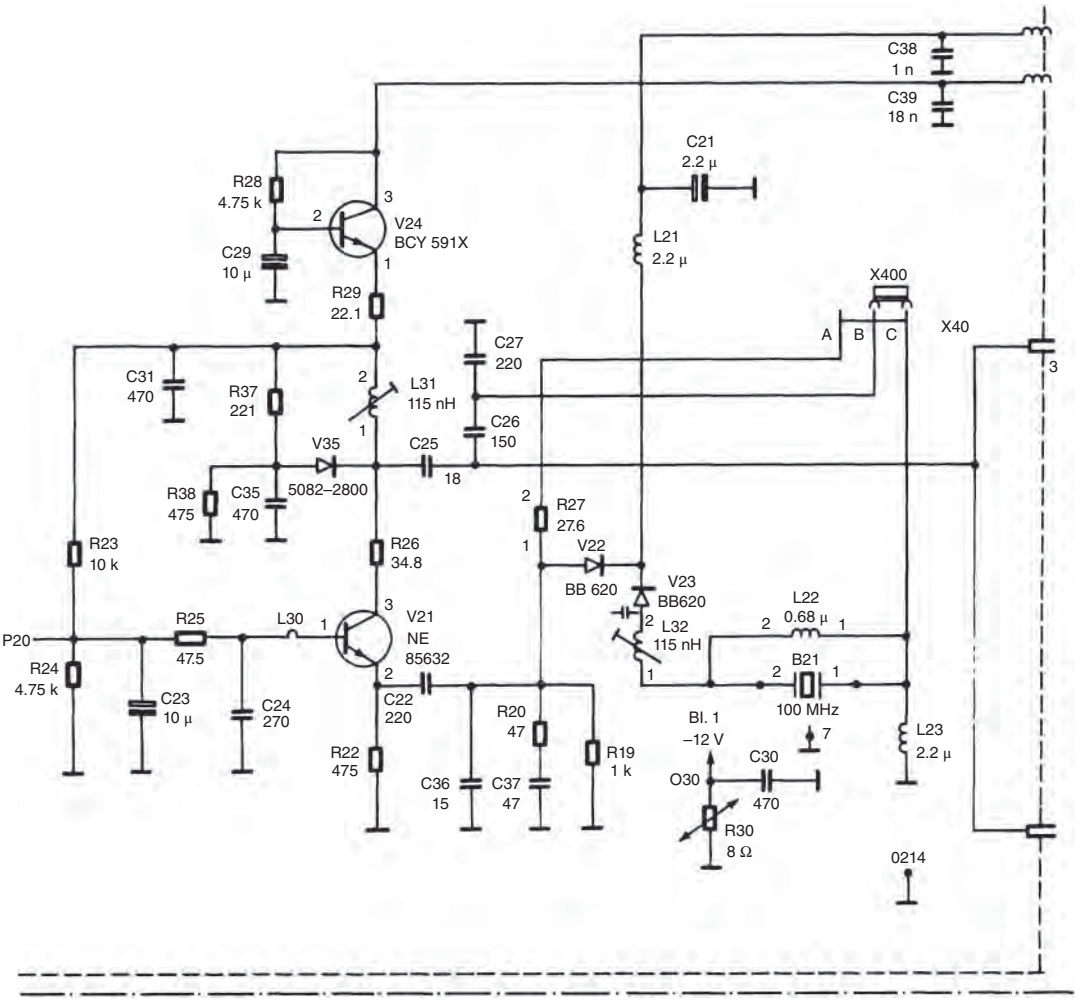

Figure 5-32 A 100-MHz VCXO with extremely low phase noise.

In order to maintain very low phase noise, the decoupling is done by taking energy off the tuned circuit with magnetic coupling and making the output part of the resonator circuit. This improves the phase noise and the harmonic content.

Figure 5-42 depicts the schematic of a 205–225 MHz very low phase noise oscillator system. It uses FETs for low flicker noise contribution and multiple-diode arrangement to reduce the diode noise.

Figure 5-43 shows the bipolar equivalent of this circuit operating in the vicinity of 200 MHz. In instances where a much wider tuning range like 1:2 is required, a single circuit with multiple parallel diodes of high voltage gain must be used, as shown in Figure 5-44. The diode clamping circuit marked V9 is responsible for preventing the RF voltage from exceeding certain values and from allowing the gate source area of the U310 to become conductive.

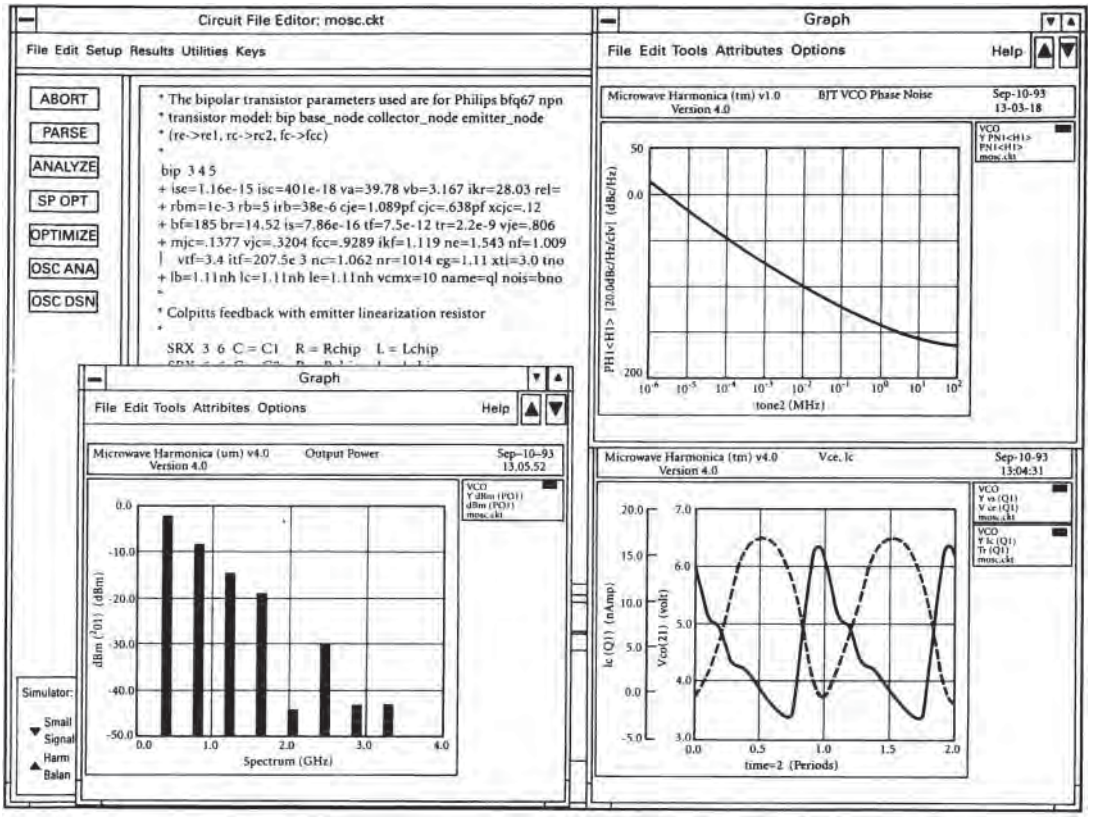

Figure 5-33 Screen capture of the simulator used for predicting the phase noise.

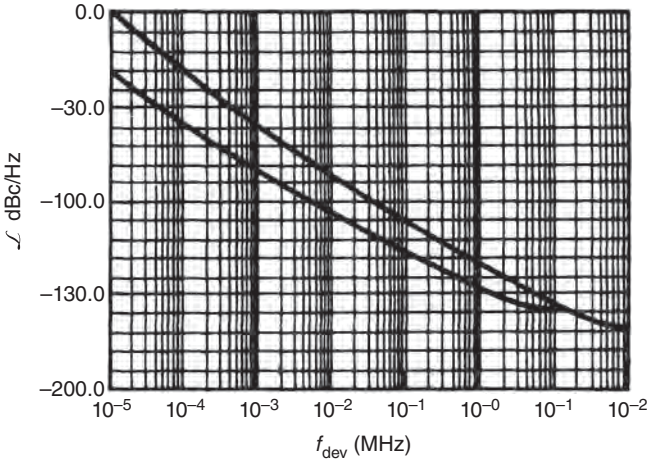

Figure 5-34 Phase noise before and after automatic optimization, which improved close-in phase noise by 32 dB.

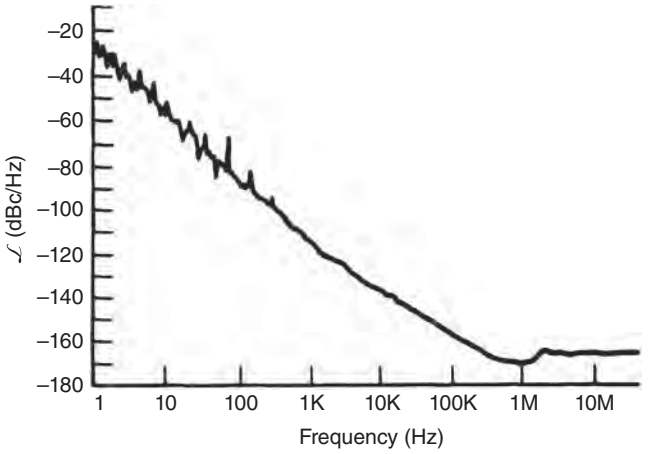

Figure 5-35 Measured phase noise spectrum for 675-MHz SAW delay line VCO.

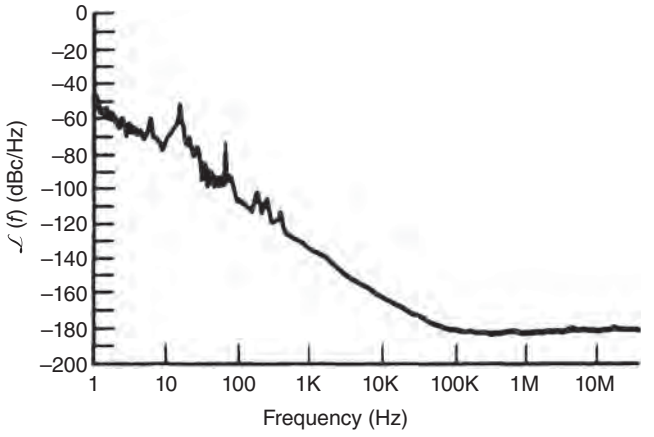

Figure 5-36 Measured phase noise spectrum for one *L*-band (982-MHz) dielectric resonator oscillator.

Isolation Stage

As previously mentioned, the success of low phase noise operation depends highly on preventing any load changes resulting in phase jumps. Figure 5-45 shows a combination of a power splitter and low feedback buffer stage. The neutralization of this circuit makes it possible to minimize loading effects on different channels.

Harmonic Generators

Figure 5-46 shows a harmonic generation circuit. The BFW16 transistor drives the snap-off diode and the output filter in tune selects the appropriate output frequency. Such a filter can be made tunable and can track the appropriate desired harmonic. The multiplier circuit is extremely critical because any noise from additional unwanted nonlinear effects will deteriorate the performance.

The harmonic multiplier diodes have flicker noise, and there must be a good compromise between the flicker noise contribution and efficiency.

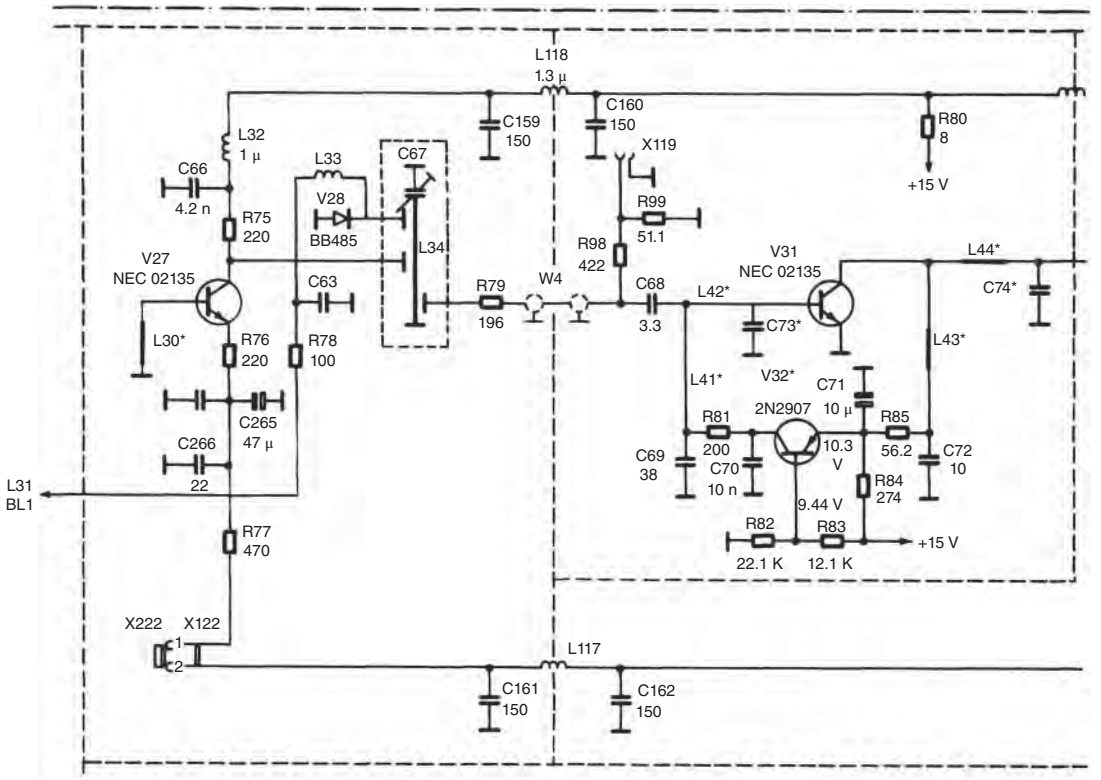

Figure 5-37 Schematic of low phase noise cavity stabilized VCO.

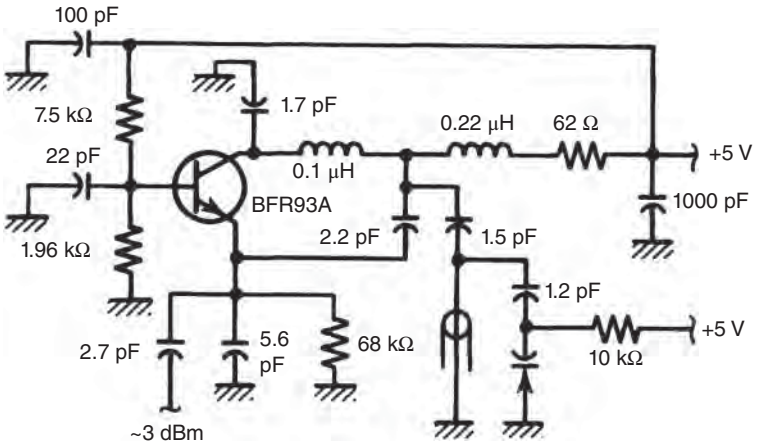

Figure 5-38 Typical test circuit for use in a ceramic resonator. These resonators are available in the 500-MHz to 2-GHz range. For higher frequencies, dielectric resonators are recommended.

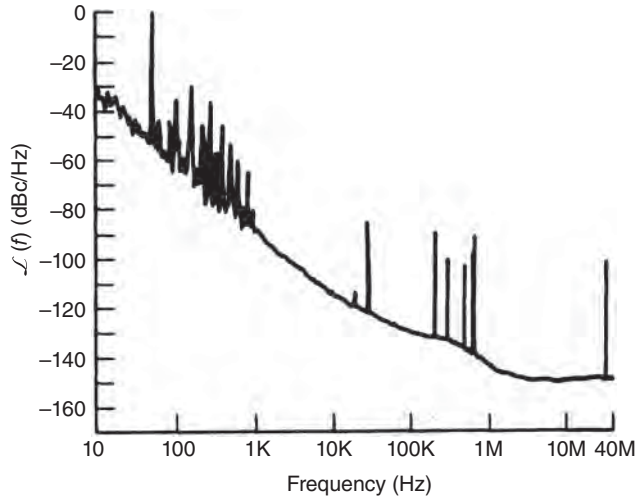

Figure 5-39 Measured phase noise of the oscillator shown in Figure 5-38.

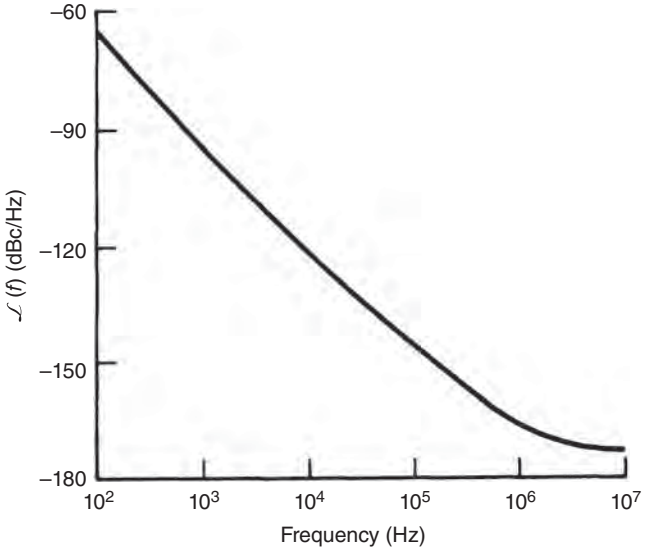

Figure 5-40 Predicted phase noise of the 1-GHz ceramic resonator VCO without the tuning diode.

Millimeter-Wave Oscillators

At frequencies above 20 GHz, the bipolar technology runs out of steam. One is faced with two options: (1) using a frequency doubler, which requires additional volume and power, or (2) using GaAs FETs. Depending on the application, either of the two options may be chosen; however, at this point, we would like to highlight the performance of millimeter-wave oscillators built with GaAs FETs. Figure 5-47 shows a Texas Instrument VCO.

This arrangement uses two tuning diodes to increase the tuning range. This basic approach can be extended to frequencies as high as 100 GHz. The initial implementation of the oscillator was pushed up in frequency and its

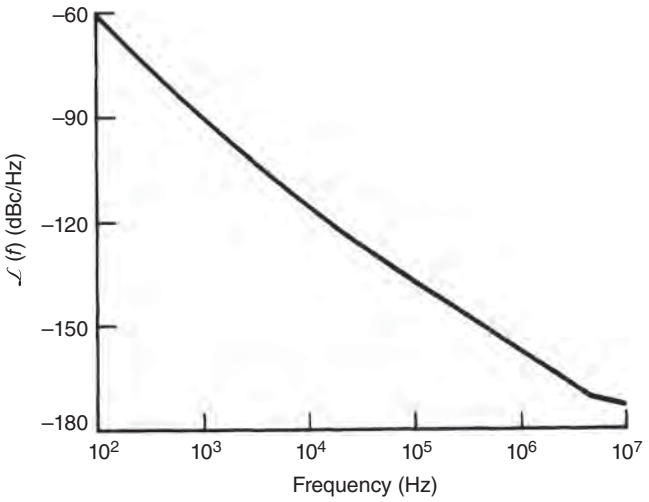

Figure 5-41 Predicted phase noise of the 1-GHz ceramic resonator VCO with the tuning diode attached. Note the good agreement between the measured and predicted phase noise.

layout is shown in Figure 5-48. It is obvious that in this case the tuning diodes also exert a major influence on the phase noise, and a number of studies have been done to improve the performance of those diodes.

Figure 5-48 shows the first GaAs based VCO, using bent (curved) transmission line that was successfully analyzed for phase noise validation. This effort was part of the Raytheon/TI joint venture performed by Compact Software.

In most cases these diodes are built by using an FET and connecting the gate and drain together. A nonlinear junction is then used as a tuning diode.

Figure 5-49 shows a 39-GHz oscillator design that uses a symmetrical ring type of arrangement as a test vehicle. This oscillator was developed under MIMIC activities by General Electric (now Martin Marietta/Sanders). Please note that two of the transmission lines have extensions for possible laser trimmings. Again, the highest reported approach for this is about 100 GHz on the fundamental sources. Consistent with previous statements, one can use modern CAD tools to predict the output power and the phase noise of such a circuit (Figures 5-50 and 5-51).

5-3-5 Time Domain Analysis

One of the requirements for the synthesizers is a very fast switching time and we would like to highlight that there is a trade-off between the high-Q oscillator and switching time or start-up condition for the oscillator. Figure 5-52 shows a DRO, which is being utilized for the purpose of examining the switching time but otherwise shows no particular performance advantages. The operating Q of the DRO is kept as high as possible in order to obtain low phase noise and the active elements determine the phase noise of the transistor and resonator.

For time domain analysis, one needs to use a Spice program as harmonic balance programs used for phase noise analysis only consider steady-state conditions.

Consistent with the linear approach, one should first determine the presence of negative resistance or the equivalent of $S_{11} > 1$ to guarantee start-up of the oscillator, which is shown in Figure 5-53. Unless this is established, one cannot determine the output power shown in Figure 5-54.

Finally, following an examination of the start-up condition of the oscillator shown in Figure 5-55, it becomes apparent that it requires approximately 180 ns for the oscillator to start and it is fair to assume that the oscillator has started after 500 ns.

In order to establish the feedback pass, the DRO uses inductor feedback. If one simulates the current in the inductor, a pattern consistent with the output voltage develops. Fifty nanoseconds after the switch-on time, an

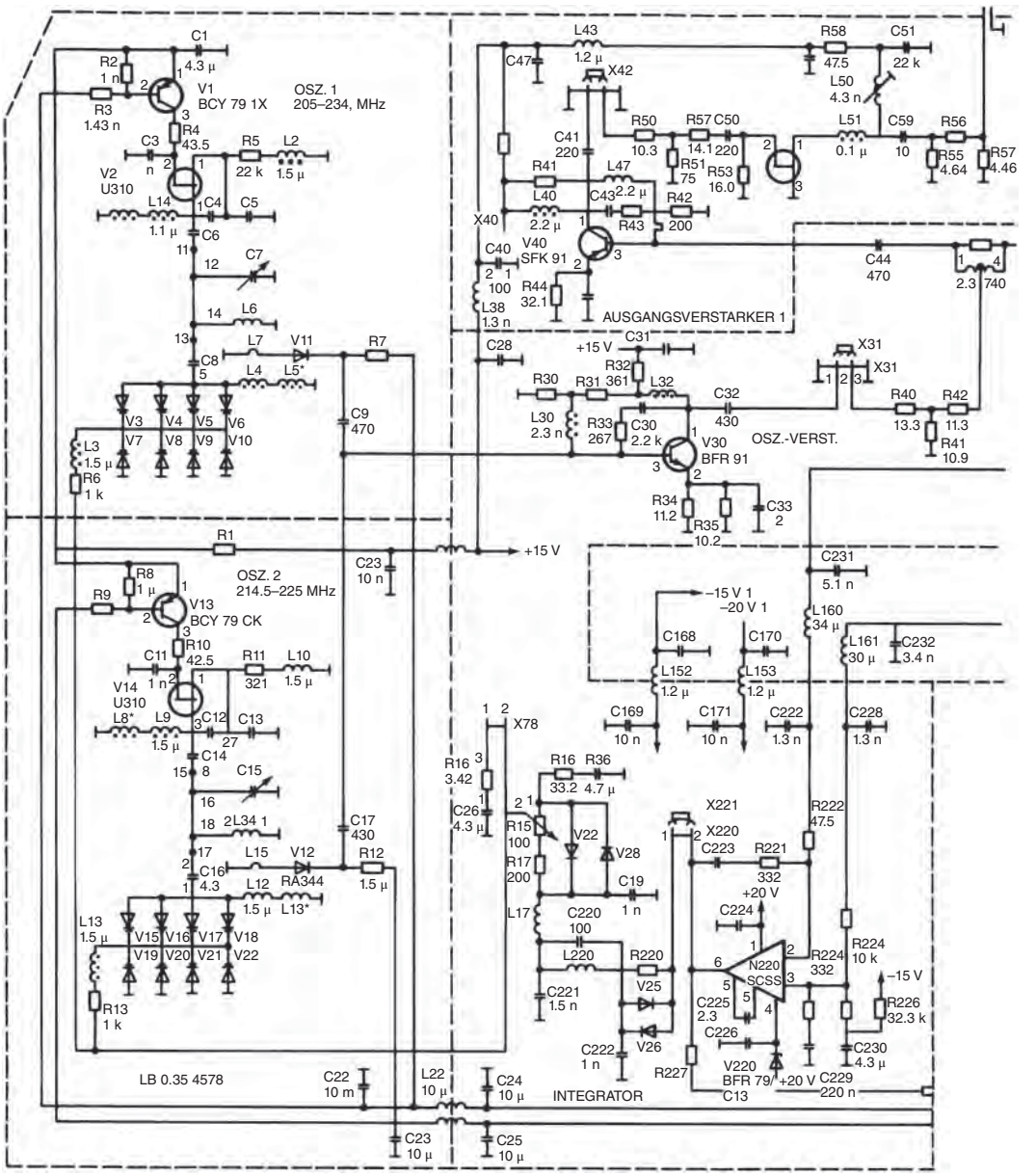

Figure 5-42 Schematic of 205–225 MHz very low phase noise oscillator system. It uses FETs for low flicker noise contribution and multiple-diode arrangement to reduce the diode noise.

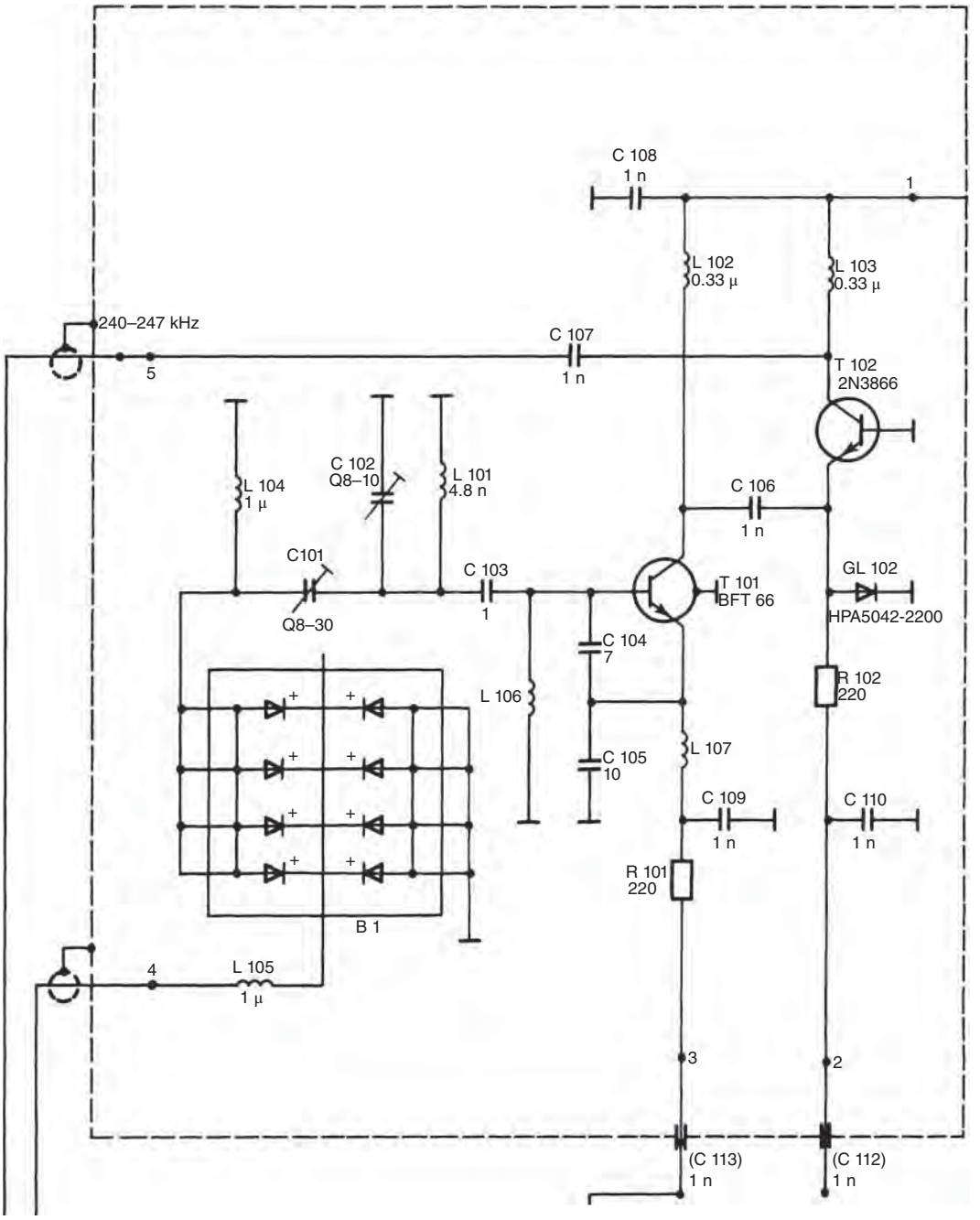

Figure 5-43 Bipolar implementation of the low phase noise 205–225 MHz oscillator. Note that the tuning range is much smaller and set from 240 to 247 MHz.

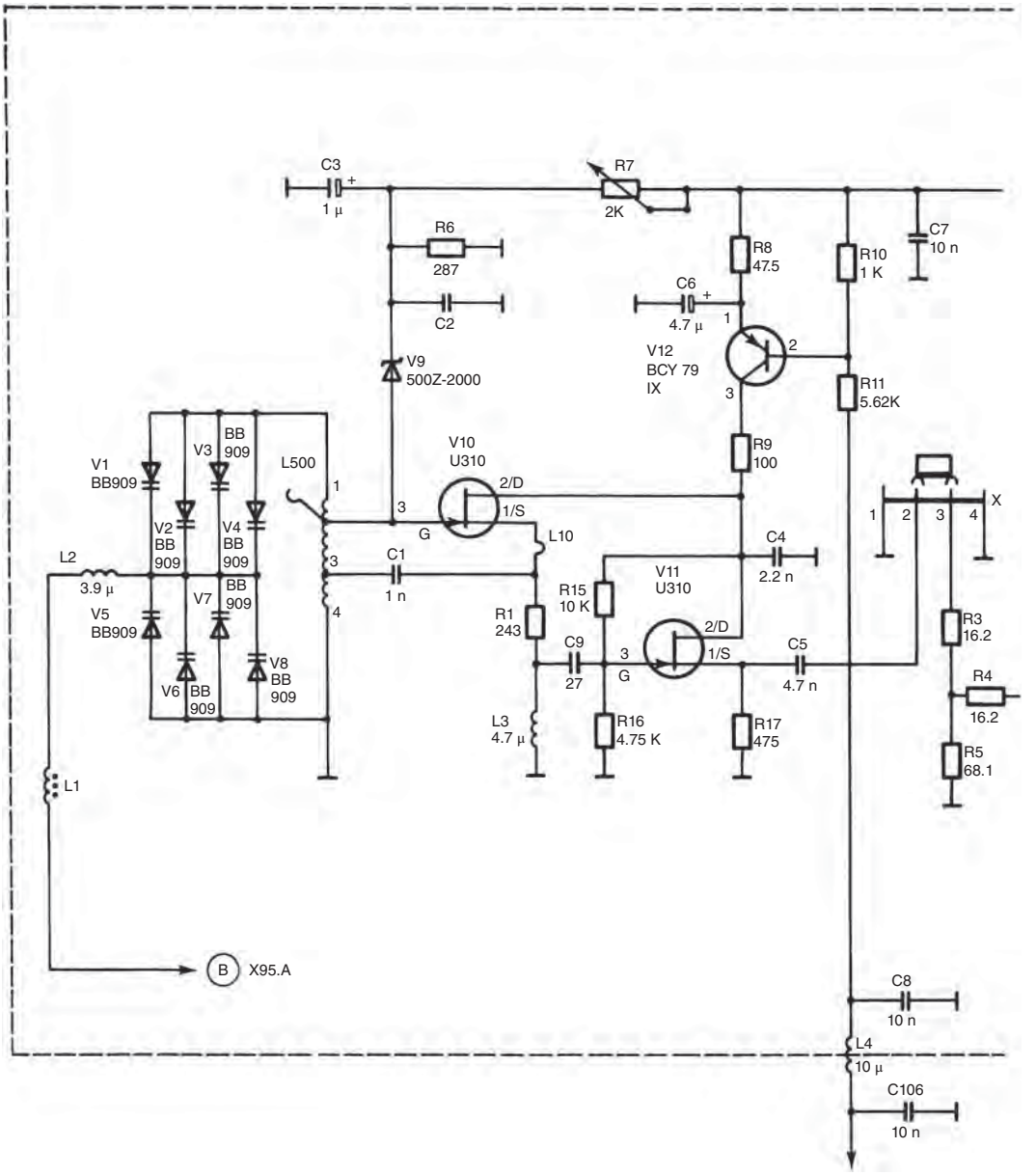

Figure 5-44 Very wideband low phase noise oscillator for frequency range 40–80 MHz. The design takes advantage of the multiple-diode arrangement and clamping diode V9 for good signal purity.

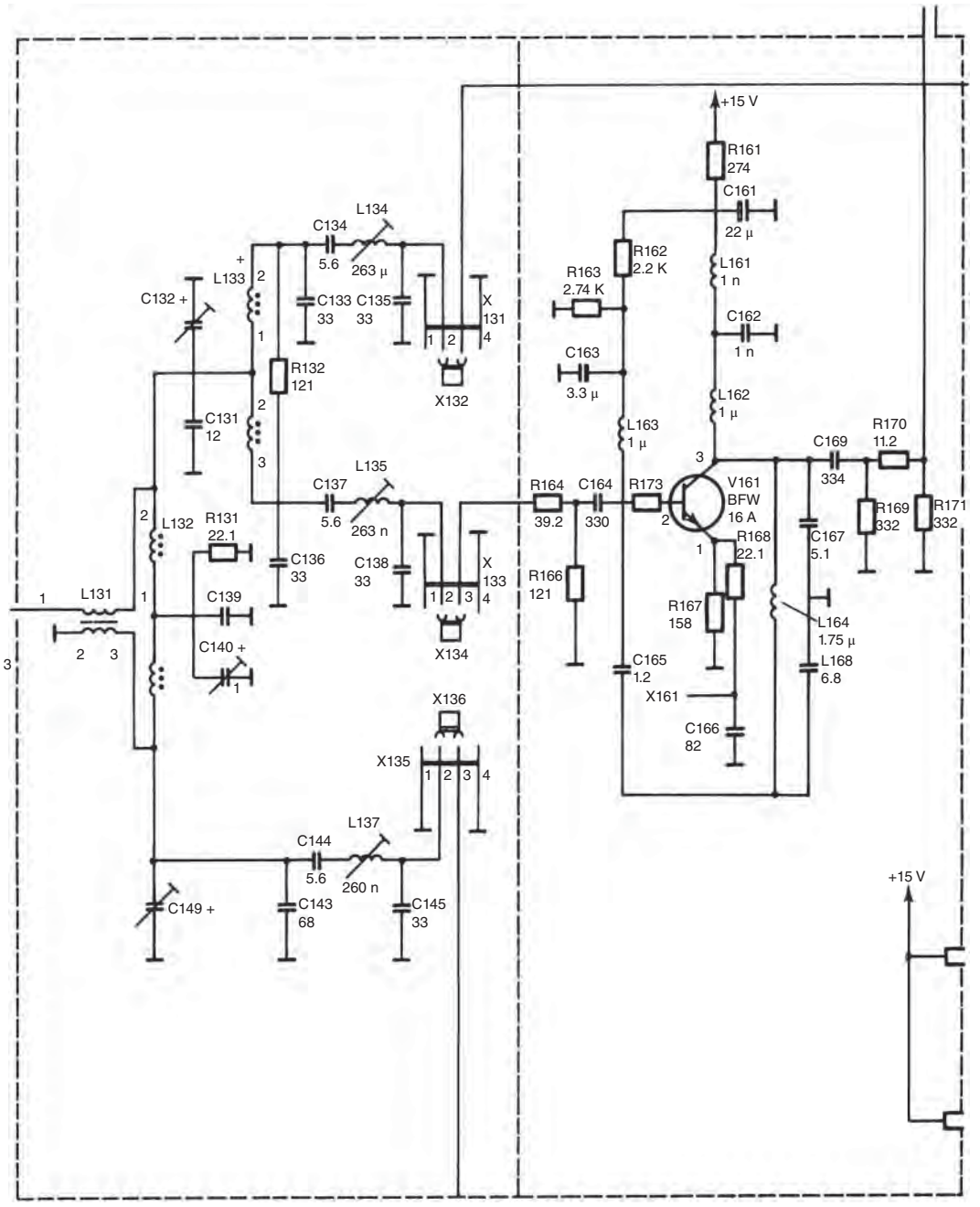

Figure 5-45 Distribution amplifier system that combines the input power splitter and a feedback amplifier with neutralization.

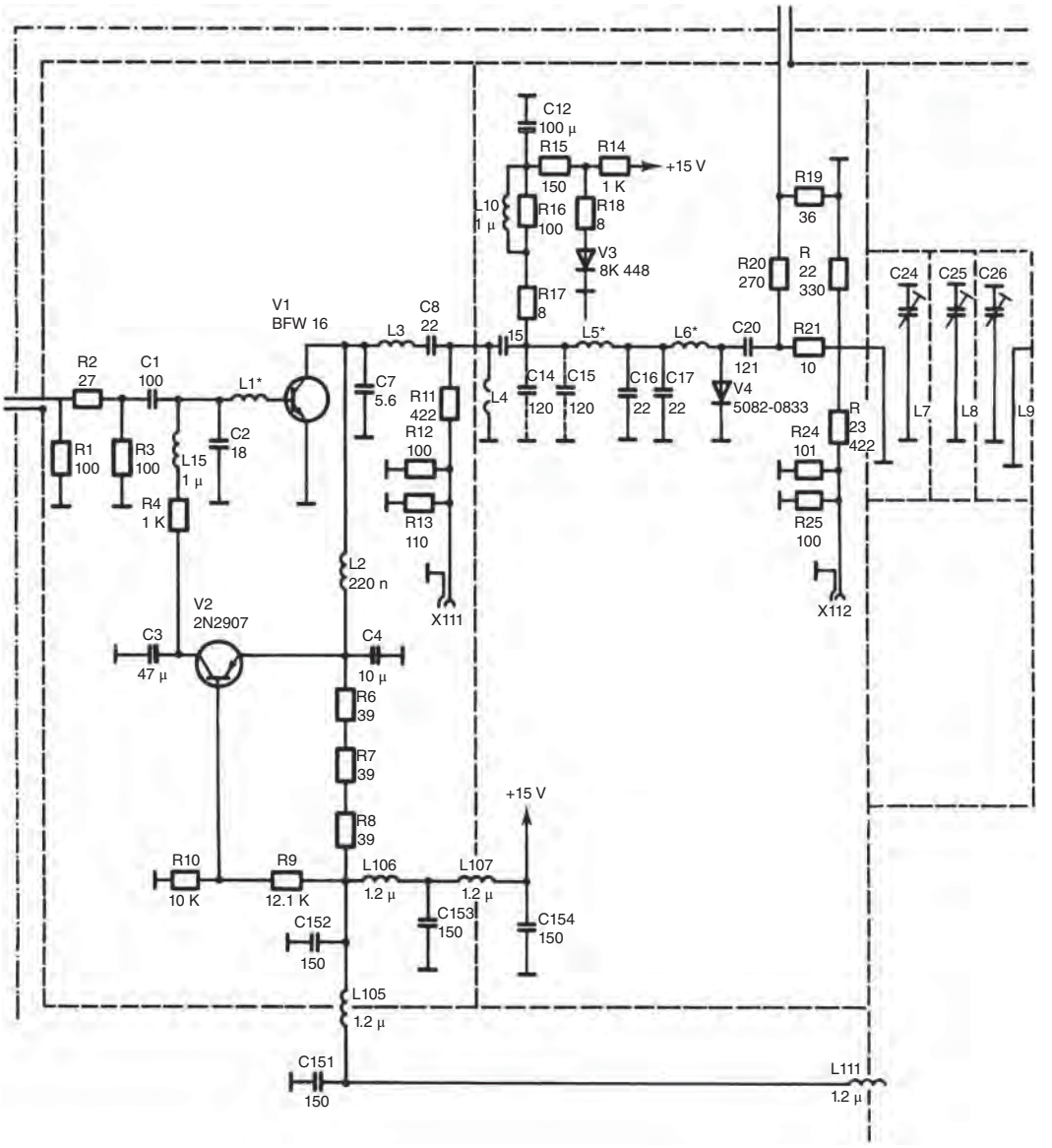

Figure 5-46 Comb generator and post-selection filter for reference oscillator. Note that the biasing of the step recovery diode or snap-off diode is very important for good phase noise performance.

initial current surge occurs that gets the oscillator started. Figure 5-56 depicts the initial current surge occurring 52 ns after switch-on time.

5-3-6 Summary

We have shown both the multiloop approaches and the contribution from dependent building blocks as they affect the overall performance of millimeter-wave synthesizers. Table 5-3 gives a list of the key elements.

Figure 5-57 shows the SSB of a 10-GHz oscillator made by Rohde & Schwarz.

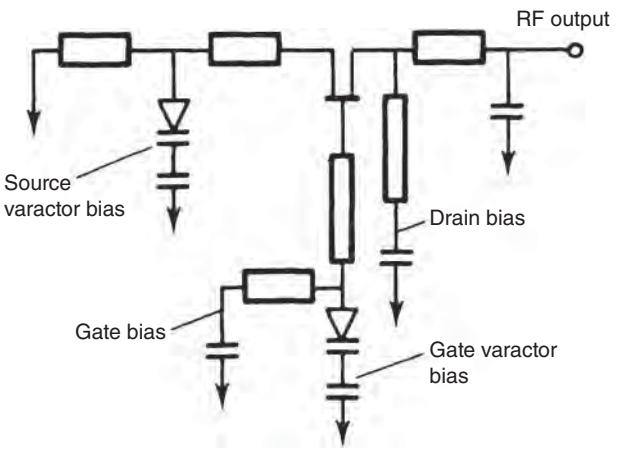

Figure 5-47 Texas Instrument 8132 VCO topology.

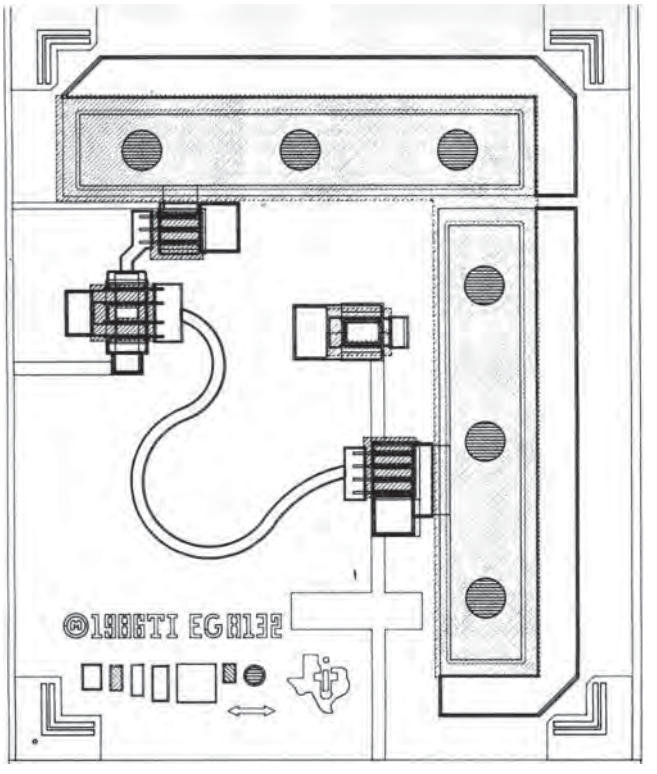

Figure 5-48 Layout of the oscillator shown in Figure 5-47 (Texas Instruments 8132 VCO).

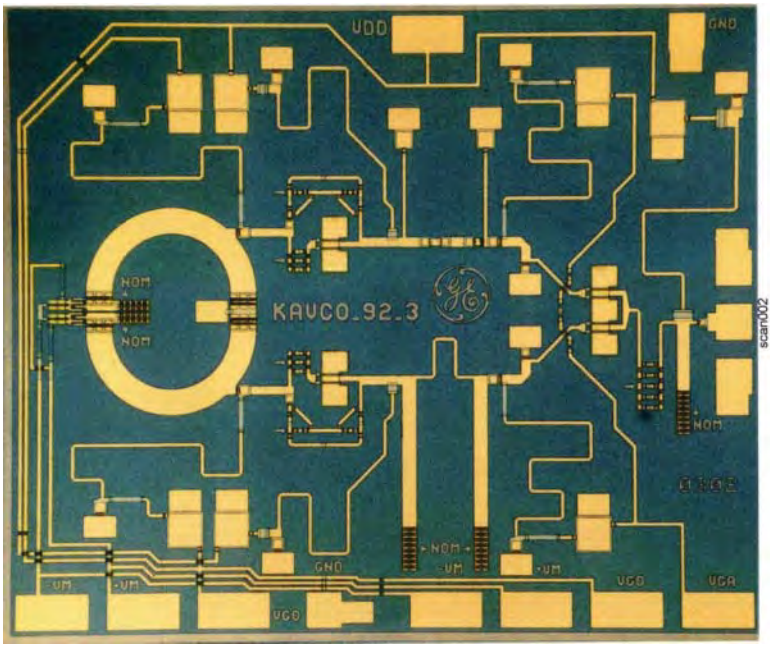

Figure 5-49 A 39 GHz oscillator design that uses a symmetrical ring type of arrangement.

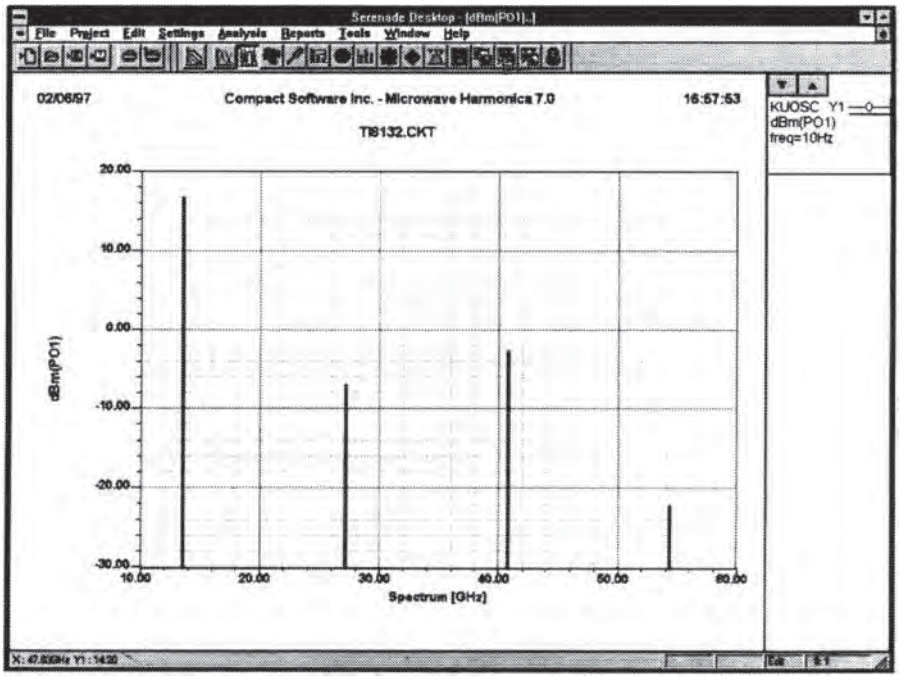

Figure 5-50 Harmonic output power.

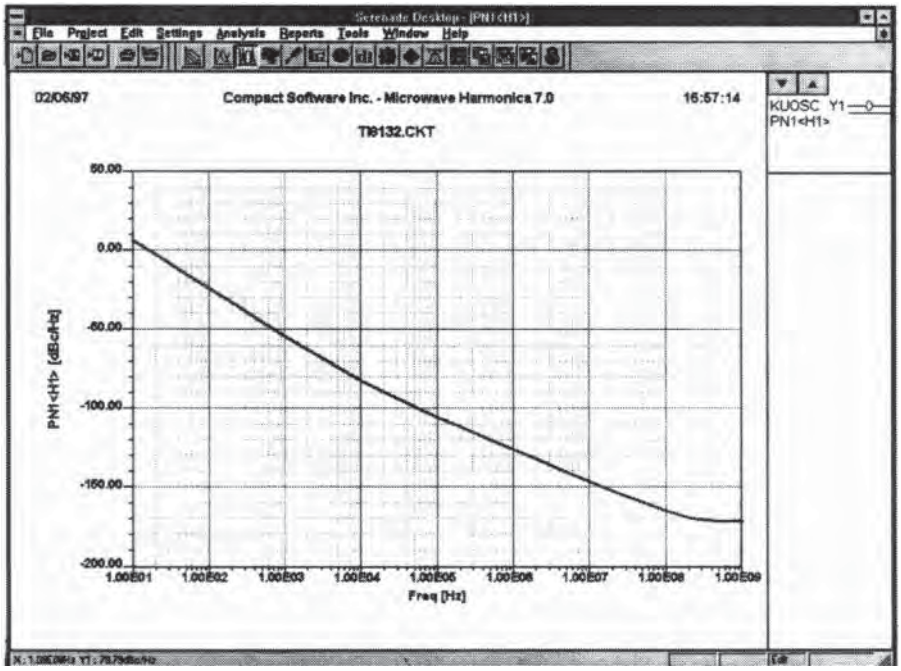

Figure 5-51 Phase noise simulation of Figure 5-49.

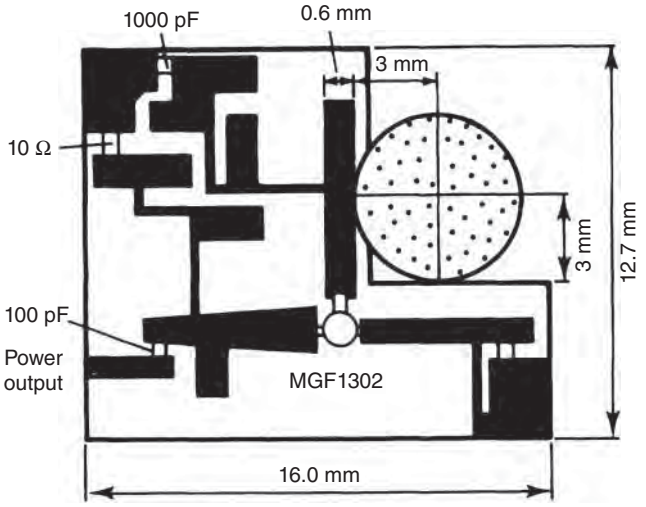

Figure 5-52 A 10-GHz DRO.

Finally, Figure 5-58 shows the measured phase noise of a 47.104-GHz frequency source as advertised by Fujitsu Limited.

These types of microwave circuits are being used in both signal generators, such as the Rohde & Schwarz SMP22, now replaced with the SMA100B as shown in Figure 5-59, and in the Rohde & Schwarz Spectrum Analyzer Series FSEA-30, replaced by R&S FSW as shown in Figure 5-60.

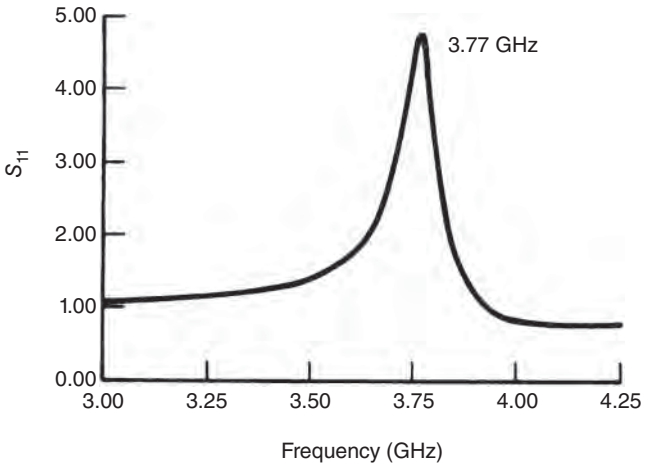

Figure 5-53 Calculation of S_{11}, as a function of frequency. Note that the resonant frequency occurs at roughly 3.77 GHz.

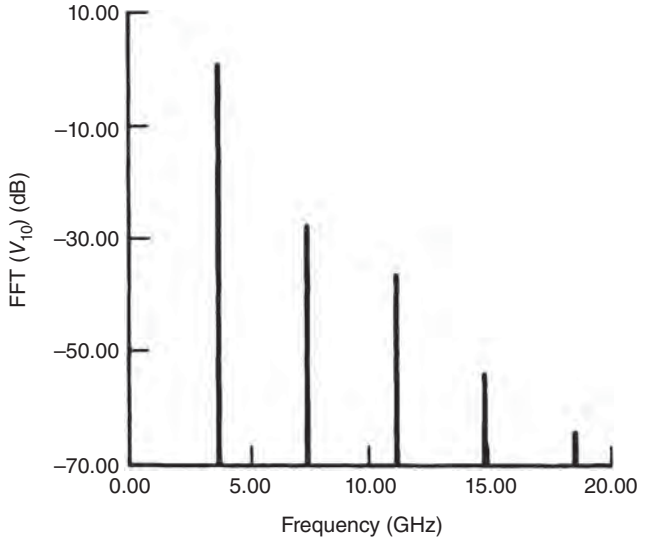

Figure 5-54 Output power of DRO with a BJT. BJT, bipolar junction transistor.

Some typical applications are detailed in Figure 5-60.
The actually measured phase noise is shown in Figure 5-61.

5-3-7 Two Commercial Synthesizer Examples

The previously detailed microwave synthesizer example was based on the Rohde & Schwarz FSB spectrum analysis synthesizer, which operates from 100 Hz to 5 GHz at the input (Figure 5-62).

For test signal generators, the requirements are slightly different. All signal generators require modulation capabilities. An interesting approach implemented in the HP8642B signal generator is that its synthesizer is a combination of a number of reference signals generated by SAW oscillators and based on the mixing scheme shown in Figure 5-63, using various oscillator frequency images ranging between 607.5 and 967.5 MHz. These

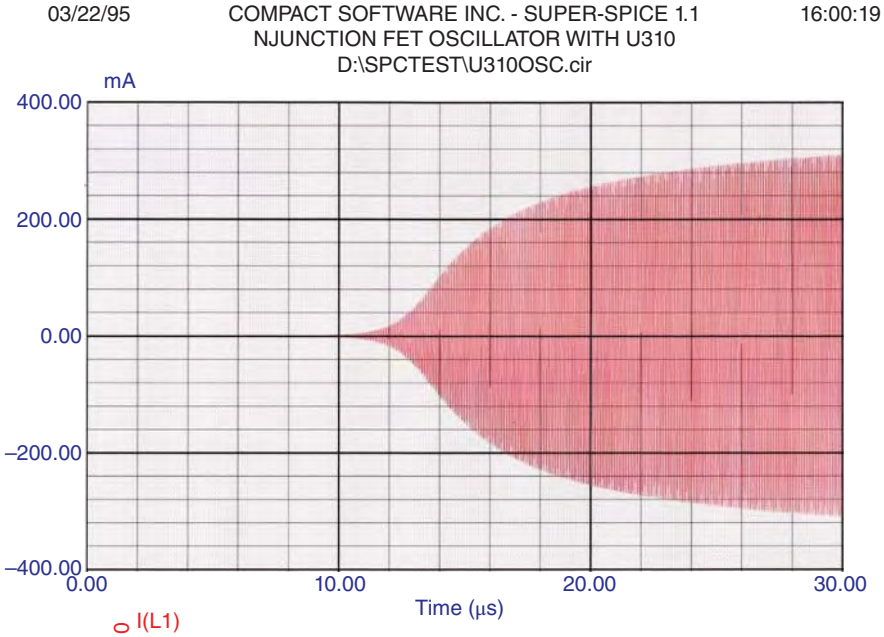

Figure 5-55 Start-up condition of the DRO with a U310 junction gate field-effect transistor (JFET)

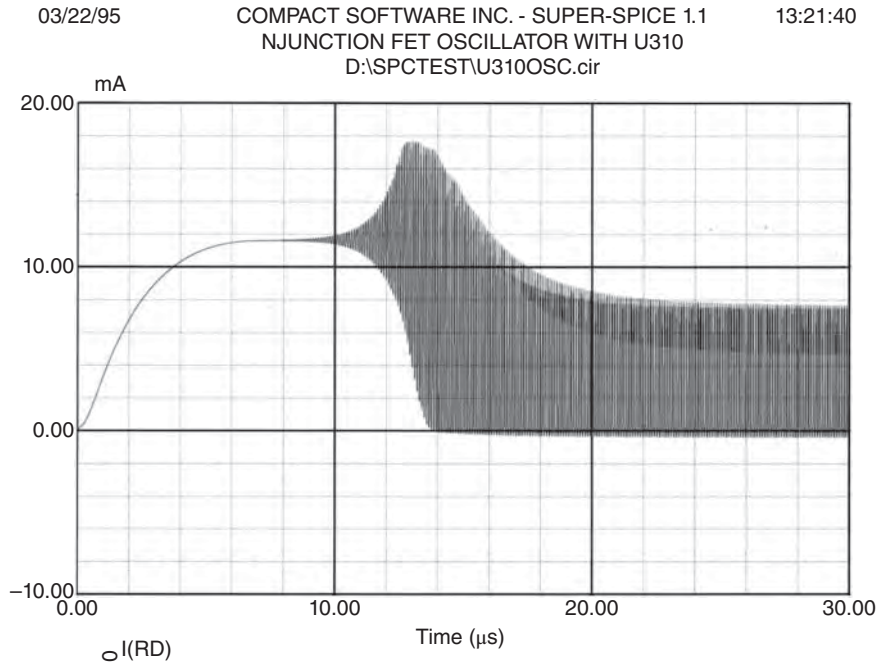

Figure 5-56 Initial current surge occurring 52 ns after switch-on-time.

Table 5-3 Key elements for millimeter-wave synthesizers

Techniques
- Basic PLL principles for digital and analog loops including use of delay line stabilizers and variable reference frequency
- Fractional division *N* with high-resolution counters and accumulators (using gate arrays)
- Direct digital synthesizers having arbitrary resolution and picosecond access time
- Selection of low noise summing loops with high bandwidth and fast response
- Availability of computer program for evaluating SSB noise for different VCOs (SONATA available through Compact Software, Inc., PLL DESIGNKIT also available through Compact Software, Inc.)
- Selection of low-noise transistors: bipolar transistors (*N*-junction FETs) and bipolar heterojunction transistors (GaAs FETs)

Sources
- Crystal oscillator—designed for low aging
- Use of buffer oscillator at 10 and 100 MHz for auxiliary frequencies (voltage-controlled crystal oscillators [VCXOs] and DROs)
- Choice of lowest possible phase noise design for all VCOs (modern low-gain YIG oscillators)
- Buffer amplifiers selected for highest isolation and low amplitude modulation (AM)-to-phase modulation (PM) conversion
- Adaptive loop bandwidth for fast locking and low noise operation
- Selection of low noise dividers with low spike operation
- All op amps in loops must be of low noise design
- Choice of harmonic sampling over division due to 1/*f* noise
- Use of analog phase/frequency detectors

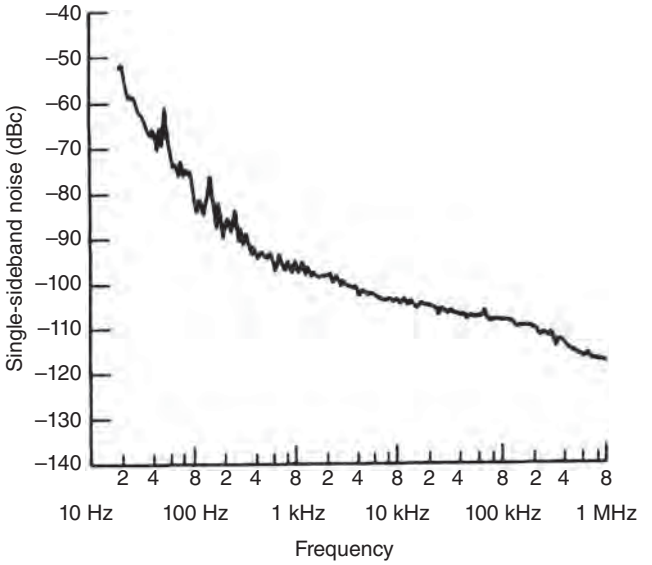

Figure 5-57 SSB noise of 10-GHz oscillator.

frequencies are a combination of mixing the SAW frequencies with a very clean 135 MHz signal, which contains the FM components. The SAW oscillators are stabilized against a 45 MHz reference. Please note that 135 MHz is the third harmonic of 45 MHz.

A fractional *N* division synthesizer with a window of 45–90 MHz is then used as a fine-resolution synthesizer to generate the output frequency from dividers and higher frequencies from a frequency doubler. While the block diagram looks fairly simple, a great deal of care must be taken to generate clean signals and the spurious-free

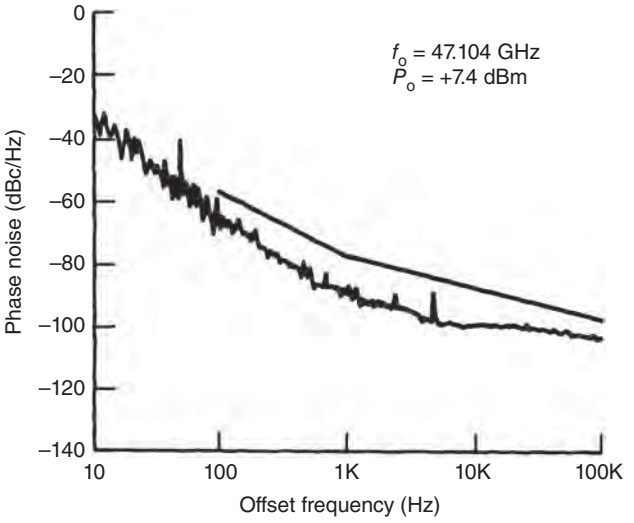

Figure 5-58 Measured phase noise of 47.104 GHz frequency source.

Figure 5-59 Rohde & Schwarz signal generator type SMA100B.

requirements for its reference oscillator are very high. The arrangement shown allows the use of a very wide loop bandwidth, as can be shown in Figure 5-64. The noise pedestal between 80 kHz and 6 MHz indicates that the loop bandwidth is somewhere below 100 kHz and the phase noise of 20 kHz of better than 140 dB is quite good. This is possible because there is no multiplication within the loop and the close-in phase noise between 10 Hz and 10 kHz is typically that of a high-Q oscillator rather than that of a synthesizer. However, for a low-cost instrument this is quite acceptable.

Much higher performance at much higher costs is achieved from the multiloop approach found in the Rohde & Schwarz SMHU85 signal generator, which covers 100 kHz–4.320 GHz. The following provides an overview of its multiloop architecture. Figure 5-65 shows the RF oscillator assembly, which is housed in module A11. It consists of three oscillators covering the range from 1000 to 2160 MHz in three ranges. To achieve the output frequency of 4.320 GHz, an additional frequency doubler is used. The output phase-locked loop takes advantage of the separate

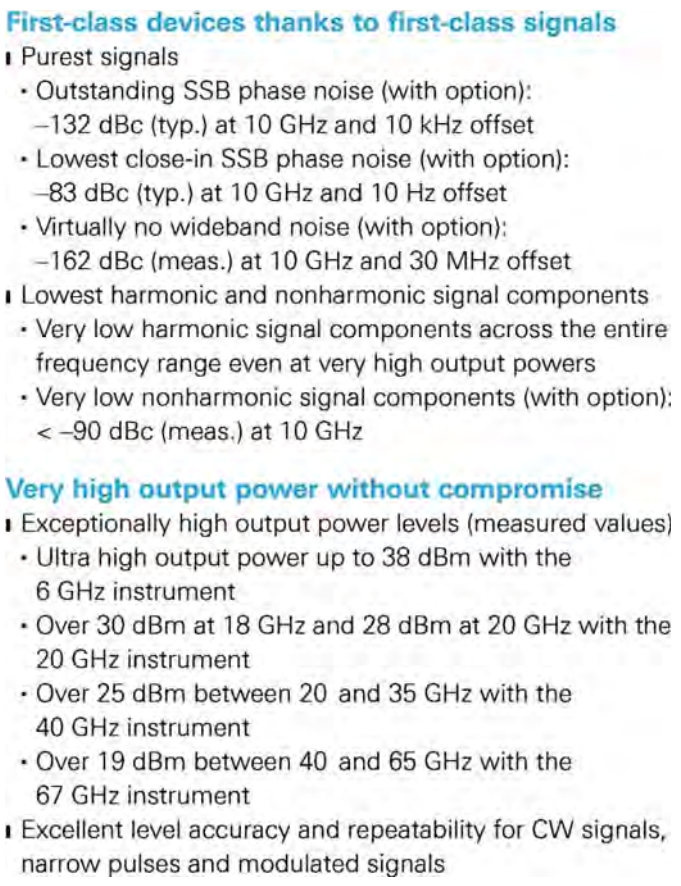

Figure 5-60 Basic features of the Rohde & Schwarz signal generator SMP100B.

oscillators, which receive pre tuning and are locked against the appropriate harmonic of the 40–41.575 MHz reference loop. The module underneath labeled A1 shows a block diagram, which explains the generation of the various reference frequencies. Three crystal oscillators, operating at 10, 40, and 130 MHz, are used to produce extremely clean, low phase noise signals, which are used in the auxiliary loops. The 10-MHz crystal oscillator is the internal reference, which can also be replaced by an external frequency standard. However, both the 103 MHz and the 40 MHz crystal oscillator are phase locked against the master standard. The modulation required for modern signal generators is fed into the input of module A8 (called step synthesis FM), which handles both frequency and phase modulation. The AM modulation is applied to the output module. The step synthesizer, which generates output between 23.125 and 29.375 MHz, uses the 40 MHz from the reference generator and also provides an FM output that goes back into the reference portion. The reference frequency output labeled X94 generates a 300-MHz modulated output, which is fed into the summing loop synthesizer, as seen in Figure 5-66. The fine-resolution signal of down to 1-Hz step size is obtained in module A7 (FRN synthesizer) of Figure 5-67, which internally operates from 38 to 58 MHz and also gets a 40-MHz reference from the reference portion. It is divided down into the frequency range from 3 to 3.625 MHz. This frequency output is then fed into the summing loop portion A10 (Figure 5-66) and each successive stage has approximately a 10× higher input frequency but achieves this by a mixing scheme rather than a multiplying scheme. The microprocessor system is extremely busy, finding all the right combinations; the phase noise of the RFO reference between 40 and 41.575 MHz within the loop bandwidth determines the output phase noise of the system. Figure 5-68 shows the measured phase noise of the SMHU synthesizer.

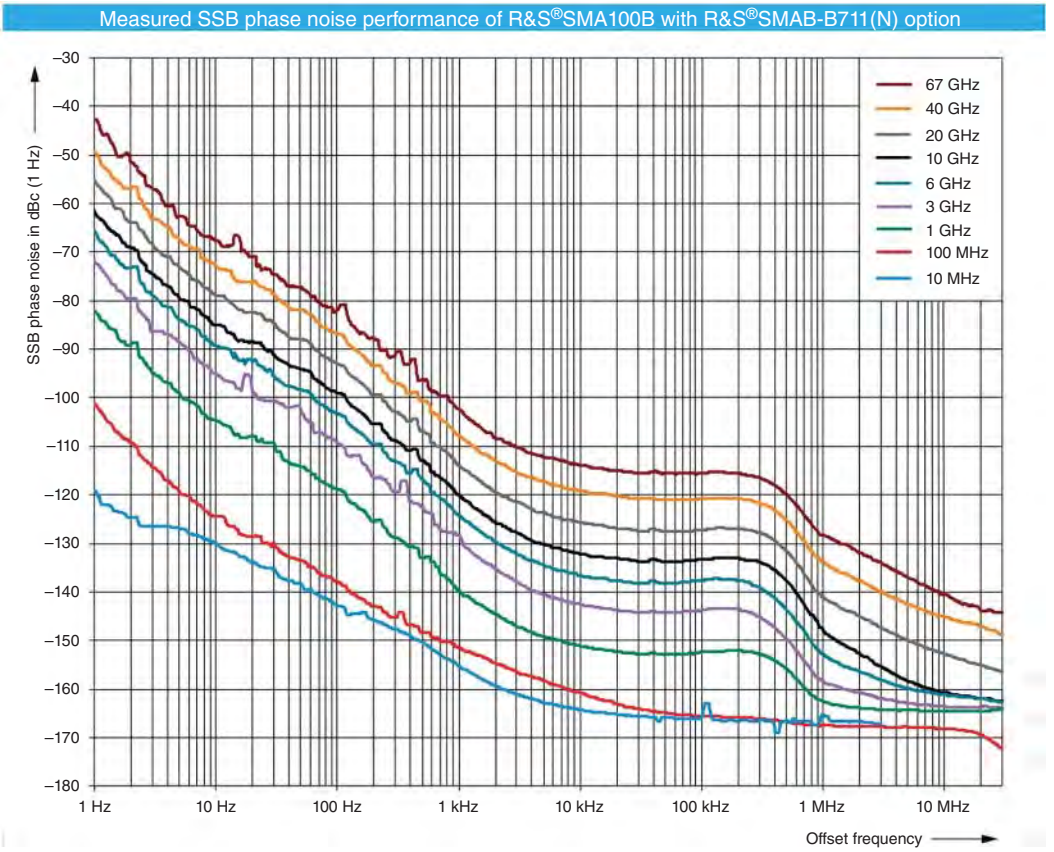

Figure 5-61 Measured SSB phase noise performance of R&S SMA100B with SMAB-B711 (N) option.

Figure 5-62 Rohde & Schwarz spectrum analyzer Series FSW.

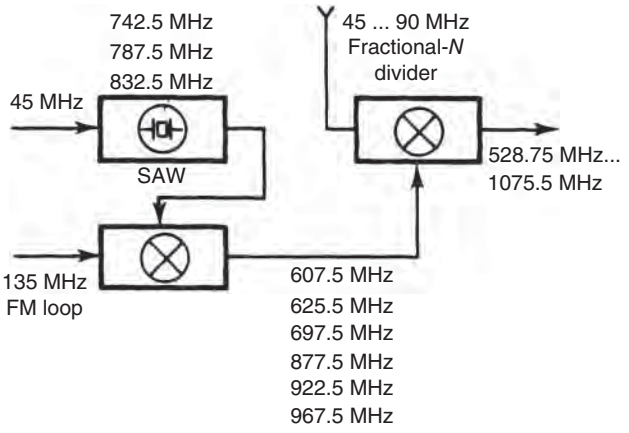

Figure 5-63 Mixing schemes using various oscillator frequency images ranging between 607.5 and 967.5 MHz for the HP8642 generator.

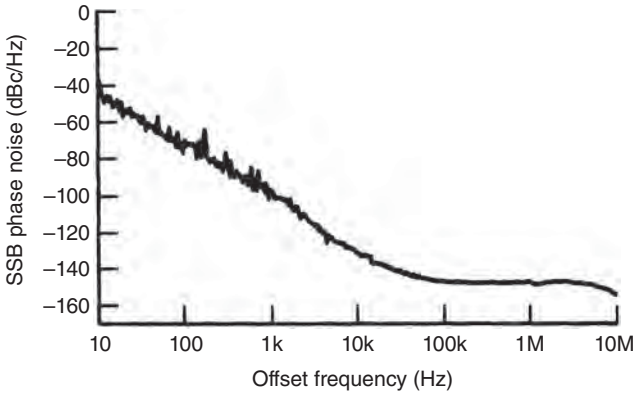

Figure 5-64 Noise pedestal between 80 kHz and 6 MHz indicates the loop bandwidth is somewhere below 100 kHz and the phase noise of 20 kHz of better than 140 dB is quite good.

As we are always interested in higher frequencies, Figure 5-69 shows the SSB phase noise of the 10-GHz synthesizer SMP made by Rohde & Schwarz.

Finally, Figure 5-70 shows the measured phase noise of a 47.104 GHz frequency source as advertised by Fujitsu Limited.

5-4 MICROPROCESSOR APPLICATIONS IN SYNTHESIZERS

Technology is changing at a fast pace, and it may be dangerous to go into great detail about microprocessor applications using specific devices, as constant improvements require the manufacturers to come out with new types of microprocessors. However, there are certain fundamentals that are independent of the particular manufacturer or device.

(1) Modern frequency synthesizers have a certain intelligence. This is accomplished by incorporating a number of routines in the system. The most frequently used is a scanning routine where a start frequency, a stop

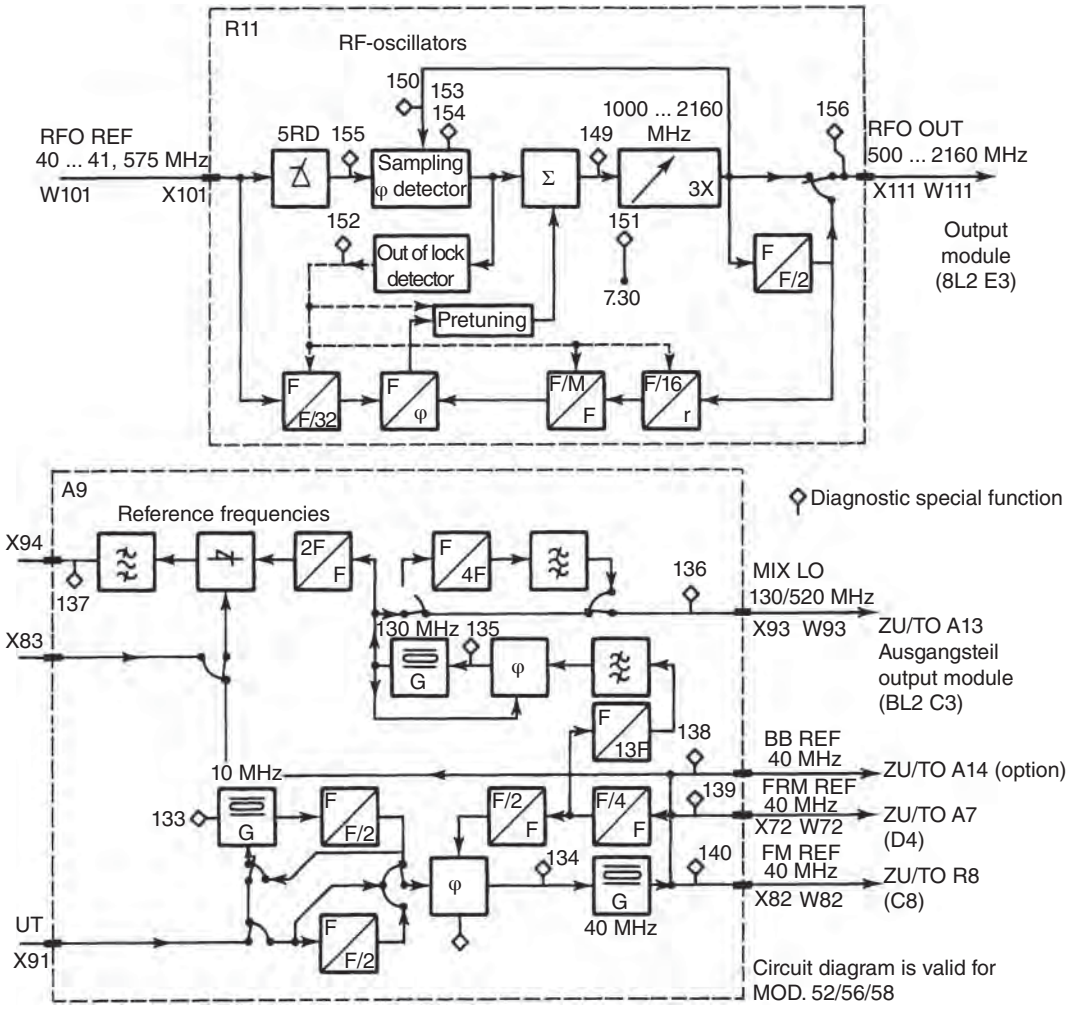

Figure 5-65 RF oscillator assembly, housed in module A11.

frequency, and a frequency increment or step size can be defined. In addition, modern signal generators can be programmed in output power (dBm), output voltage (μV, mV, V), or dB above 1 μV. Different users of signal generators will use different specifications in their system, and to avoid conversion tables and possible errors in translating one figure into the other, the built-in intelligence of the signal generator via the microprocessor is capable of converting one value into another, or receiving commands in different format.

(2) Frequency synthesizers found in signal generators are typically multiloop synthesizers. In Section 1-10 we have seen that, depending on a change of loop gain and change of frequency range, certain compensations have to be done within the loop, causing the loop to go out of lock for a certain time. If the out-of-lock sensor used in all superior circuits gives an error command to the microprocessor responsible for the housekeeping, the microprocessor will then either wait until lock is achieved, or, if this is not done within a reasonable time determined by the program, it will alert the user that the frequency synthesizer is out of lock. This so-called built-in self-check, sometimes referred to as BITE (for Built-in Test Equipment), refers to the housekeeping capability of a microprocessor whereby, under software control, certain routines are made

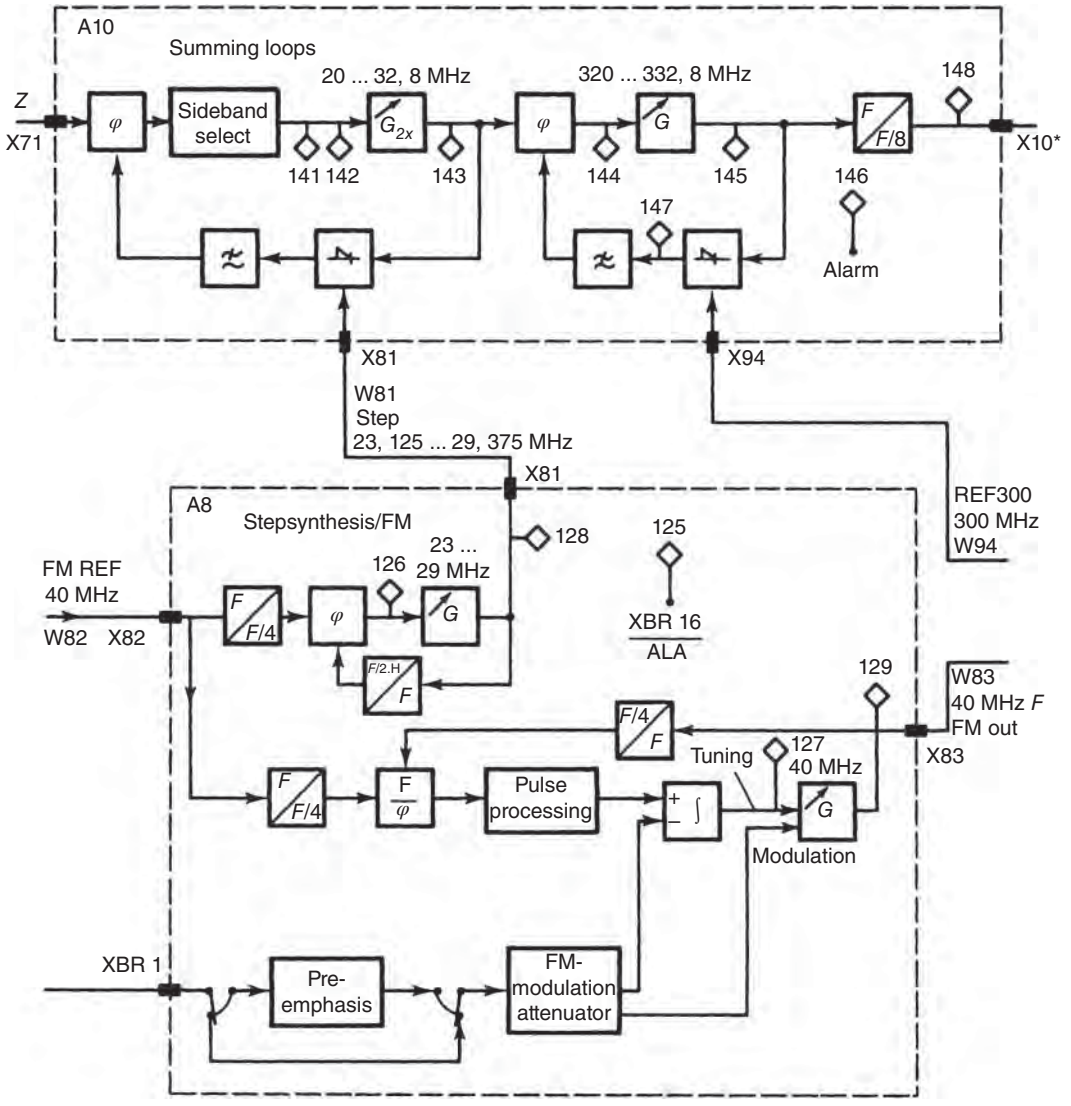

Figure 5-66 Reference frequency output labeled X94 generates a 300-MHz modulated output, which is fed into the summing loop synthesizer.

available to verify the system operation. This can occur immediately after switching on the instrument or by pressing a check button that activates the relevant circuitry.

(3) A number of loops may be used with what is called *offset*, which means that the actual command value given to the loop does not correspond to the value shown on the display. Therefore, the microprocessor has to perform certain arithmetic, offsetting certain frequencies. Again, this can be called housekeeping and is an essential part of the system. In addition to this, some loops are being mixed, and by determining which sideband is to be chosen from this mixing process, different output frequencies can be made available using the same oscillators. The microprocessor can keep track of the system's requirements, such as which

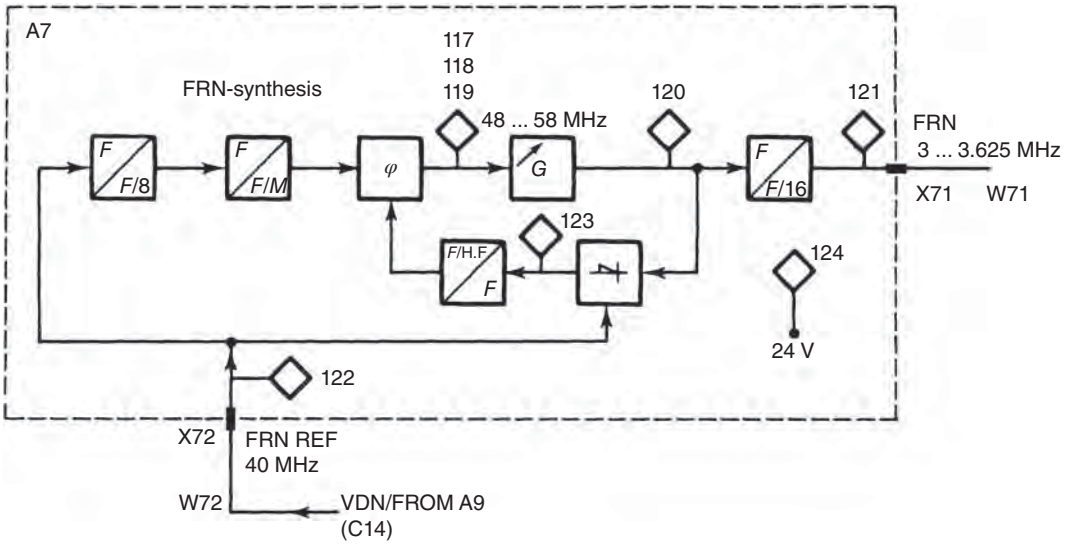

Figure 5-67 FRN synthesizer labeled module A7 operates from 38 to 58 MHz and also gets a 40-MHz reference from the reference point.

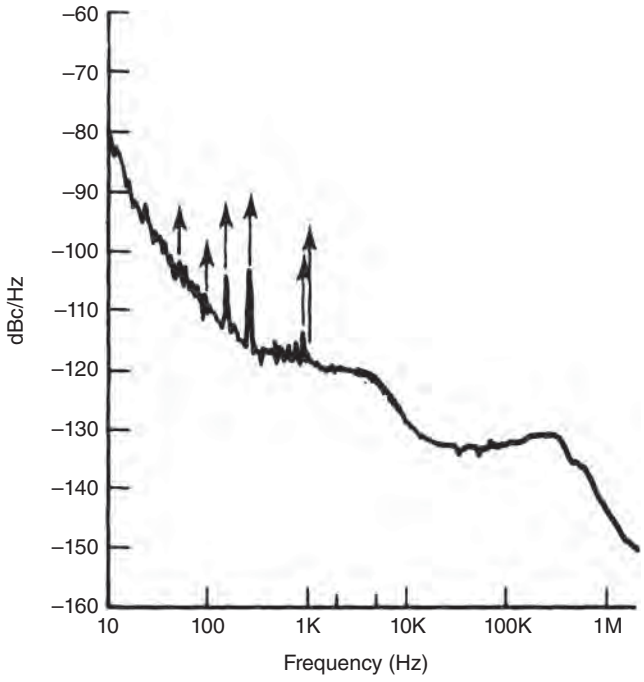

Figure 5-68 Measured phase noise of the SMHU synthesizer at 800 MHz.

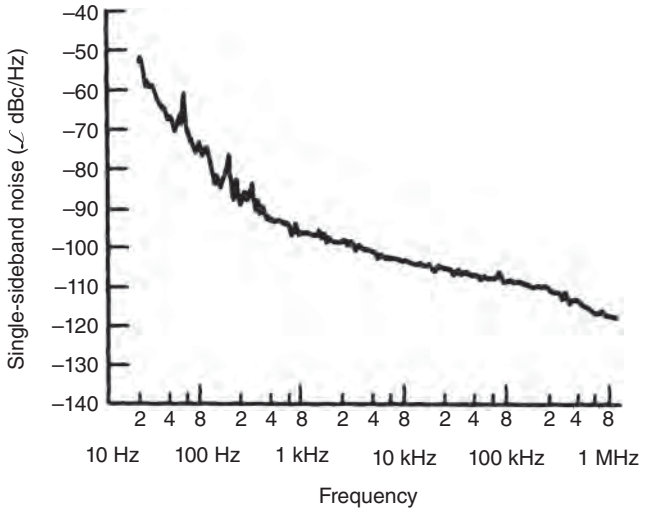

Figure 5-69 SSB phase noise of the SMP synthesizer at 10 GHz.

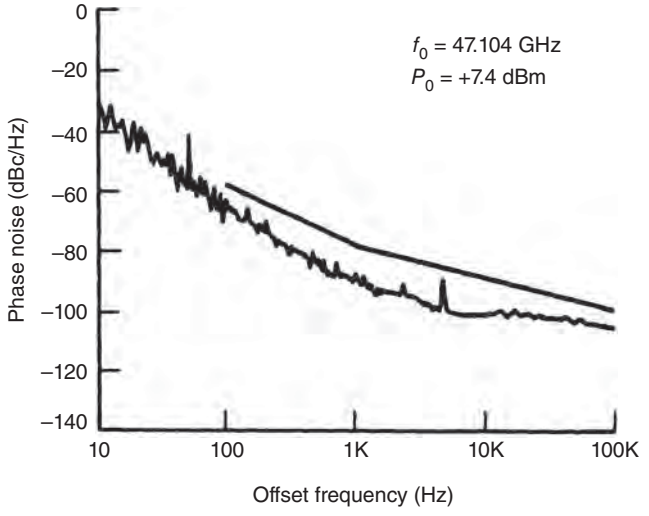

Figure 5-70 Measured phase noise of 47.104 GHz frequency source.

oscillator range has to be operated, which actual programming has to be done with the various loops, what output filters have to be activated, what modulation capabilities have to be considered, and so on.

(4) Advanced technology allows construction of synthesizers with large-scale integrated circuits. Because of the high complexity, several commands are required by the frequency divider. Supplied in parallel, the number of lines would be excessive. It is therefore a simplification to address the frequency dividers in serial format rather than parallel, and the microprocessor again has to keep track of the proper format.

What does this lead to? The various details we have just listed are most likely to be found in a modern frequency synthesizer and are all necessary at the same time. A microprocessor is essentially a serial device. This means that it performs one task after the other following a certain set of instructions. The programmed microprocessor sends

certain commands to the read-only memory (ROMs) and IO ports, which have latch circuits in them. Therefore, certain information can be initiated and held in latches. Updating is done by changing the contents of the latches and counters. It is apparent that once housekeeping, arithmetic, verifications, and switching exceed a certain amount, the microprocessor will be extremely busy.

Microprocessors and microcontrollers are available through well-established companies, such as Intel and Motorola to name the most dominant ones. Customarily, one uses microprocessors for instrumentation control. The main reason for this is the incorporation of high-powered devices in the hardware, where one obtains a PC as part of the instrumentation. For some applications, fairly simple calculations have to be performed; however, the very moment graphics become involved, the execution speed requirements change drastically. While this topic is not a subject of this book, it should be pointed out that a computer-like display requiring fast graphic and high throughput has become the industry standard for complicated test equipment. Over the years, 16-bit processors have been replaced by 32-bit, and in many cases, the actual calculation is done internally in 64-bits. Also, as higher integration occurs, the math coprocessors have become part of the "chip" and in fact are frequently referred to as floating-point calculation devices.

Consistent with experience in computers, where one uses a keyboard processor, graphics processor, memory manager, and central processing unit (CPU), modern communications test equipment with many synthesizers will also divide activities. The typical interface between the user and the instrument, such as a signal generator, is either keyboard entry from the front panel or parallel addressing via a parallel bus such as the IEEE 488. Chip manufacturers continue to develop dedicated chips to ease programming for these parallel and serial interfaces. Today's synthesizers are based on the Windows operating system, currently up to Windows 10. This combines a very nice user interface as well as sufficient computational power using multiple processors. Specifically, as we will look into hybrid synthesizers, the mathematical housekeeping will be very important.

5-5 TRANSCEIVER APPLICATIONS

Modern short-wave transceivers use the most advanced digital implementation both in the RF/IF section as well as in the synthesizer. These generally allow simplification of the frequency selection. In the case of this example, we will look at a short-wave transceiver (Model XK2100 by Rohde & Schwarz) that operates from 10 kHz to 1.5 MHz in receive and 1.5–30 MHz in transmit. The first IF is 40.025 MHz and the second IF is 25 kHz using a digital signal processing (DSP) implementation. Therefore, the transceiver is a dual conversion system that requires a first oscillator, commonly referred to as a local oscillator (LO), which generates frequencies between 40.025 and 70.025 MHz in small steps such as 1 Hz. Also, an additional auxiliary frequency of 40 MHz is required to translate the first IF down to the 25-kHz second IF. Figure 5-71 shows the block diagram of the RF input down to the second IF and backward for transmit.

The synthesizer as shown in Figure 5-72 consists of various loops. The internal reference of 10 MHz or an external reference of 1, 5, or 10 MHz is used to generate the first auxiliary frequency of 40 MHz. A VCO operating at 40 MHz is locked against the 1-MHz reference. Outputs from its programmable divider are used to obtain auxiliary frequencies such as 2 MHz, 5 MHz, and 100 kHz. The main RF synthesizer consists of two loops and a fine-resolution synthesizer. The output signal of VCO III, operating from 40.025 to 70.025 MHz, is mixed with the output signal of VCO II, resulting in an internal synthesizer IF of 39.8–69.8 MHz. The interface controller marked "SERBUS-interface" provides frequency information to the SERVDEV unit, which is clocked by the 5-MHz reference and obtains the frequency information sent from the front panel. As part of the DDS, the sinus lookup table generates a fine-resolution signal for 10-kHz steps down to 1-Hz steps and provides this to Phase Detector III. At the same time, a D/A converter scheme is used for coarse presteering of both VCO II and VCO III. This two-loop synthesizer with an embedded DDS minimizes the division ratio. The loop around VCO II is stepped in 100-kHz increments.

An example of a frequency calculation is presented next. The receive or transmit frequency set to 12.34567 MHz requires a local oscillator frequency of 52.37067 MHz. The division factor for PLL II (VCO II) must be $123 + 398 = 521$. VCO II therefore operates at 51.2 MHz. The DDS generates a frequency of $45.67 + 225$ kHz or 270.67 kHz. This occurs at the output frequency of VCO II of $52.1 + 0.277067$ MHz or the required 52.37067 MHz. In Chapter 6, we will look at a more advanced concept of a hybrid synthesizer.

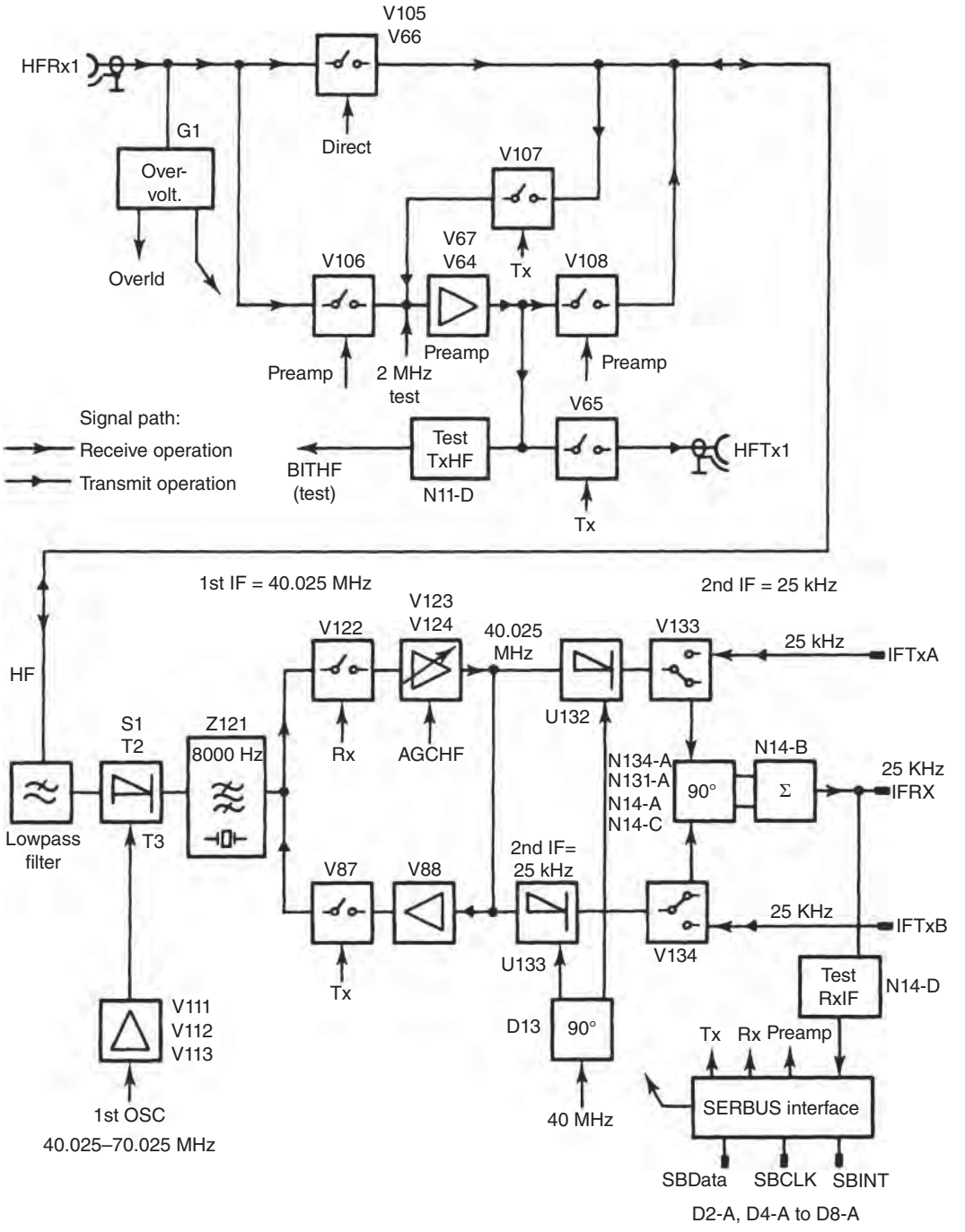

Figure 5-71 R&S transceiver HF unit block diagram.

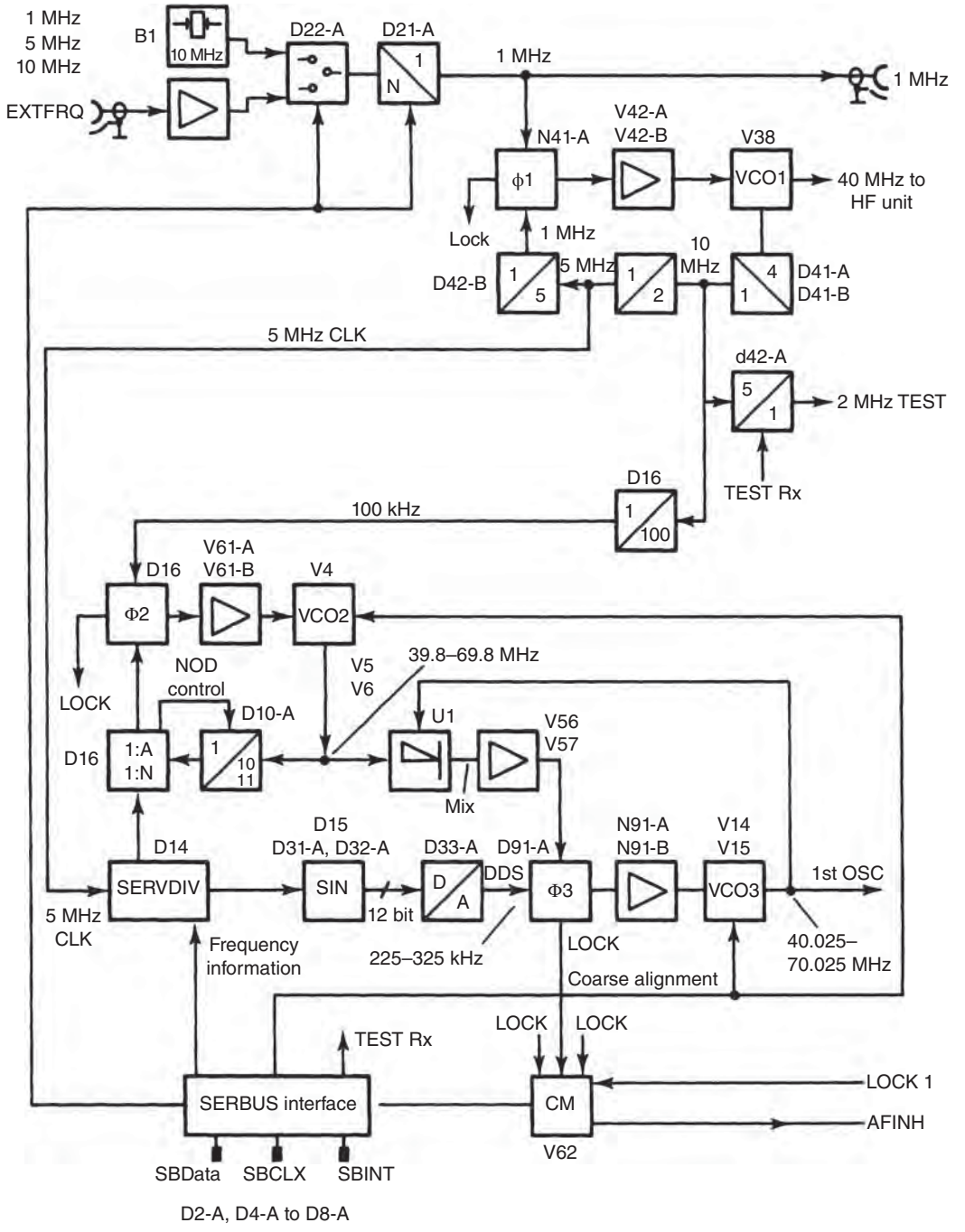

Figure 5-72 Synthesizer, block diagram.

Some of the tricky questions that must be addressed are the issue of switching speed, the combination of spurious products and shielding, and power consumption. In the hybrid synthesizer's case, seen in Chapter 6, we will see that instead of using the possible 0.007 Hz resolution, we will verify it to 1 Hz steps. The resolution is much finer than the customary 1 Hz and the microprocessor must now reduce the resolution and ensure the proper steps are selected. In this case, the DDS operating from 225 to 325 kHz is simply added to the auxiliary frequencies and therefore no offset calculation or compensation for multiplications has to be made. The penalty, however, is an overall more complex scheme. As new integrated circuits appear, some of these trade-offs will have to be reconsidered. We need to be reminded that in a mixing scheme, such as this, many noise sources are adding up and each mixer produces spurious signals. The choice of whether or not to use a DDS or fractional division *N* synthesizer is mostly determined by cost, power consumption, and shielding. In applications involving high-performance FM, there is some merit to modulating the division ratio, and this may result in a fractional division synthesis preference. Also, in many instances, established in-house technologies, short development times, and the ability to bring the product quickly to market determine its selection.

5-6 ABOUT BITS, SYMBOLS, AND WAVEFORMS

Digital modulation of an RF carrier is the allocation of physically existing RF waveforms to the single elements of an alphabet of logical symbols where the number of allowed waveforms is equal to the number of logical elements of the alphabet (Figure 5-73). The most common alphabet is the binary one with the two logical symbols "0" and "1," but we will also deal with quaternary, octernary, and hexadecimal alphabets or more generally with *M*-ary alphabets comprising many more elements when discussing the signal generation with signal generators and dedicated software packages. The waveforms representing these symbols differ from each other by their parameters amplitude $a(t)$, their frequency $f(t)$, and their phase $\varphi(t)$.

A modulator, therefore, is nothing more than a device by which this allocation is performed (Figure 5-74). From a coder it receives the logical symbols and emits at its output the corresponding waveforms $s_i(t)$. The waveform generation may be done by using a set of distinct generators (i.e., two oscillators to generate two signals with different frequencies in the case of binary frequency shift keying), by classical amplitude or frequency modulators or by more sophisticated equipment such as *I*/*Q*-modulators for *M*-ary modulations.

On their way across the RF channel from the transmitter to the receiver, these waveforms are distorted by noise and other disturbing properties of the RF channel.

The task of the receiver is to interpret the received waveforms $r_i(t)$ and to reallocate the proper logical symbols to them. For this purpose, it is not necessary to reconstruct the original waveforms from the distorted ones (Figure 5-75a). The important thing is to find out which symbol has most probably been sent when a certain signal $r_i(t)$ has been received a process that is known as maximum likelihood estimation (Figure 5-75b).

For meaningful receiver tests therefore, waveforms have to be generated that mimic real, distorted signals to prove the ability of a receiver to tolerate waveform distortions to a certain extent.

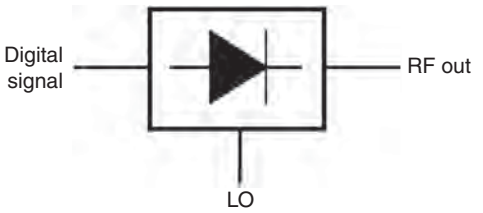

Figure 5-73 At base, digital modulation involves frequency-shifting a baseband digital signal to RF. In practice, the process is more complicated than this because of bandwidth constraints on the resulting RF signal [1].

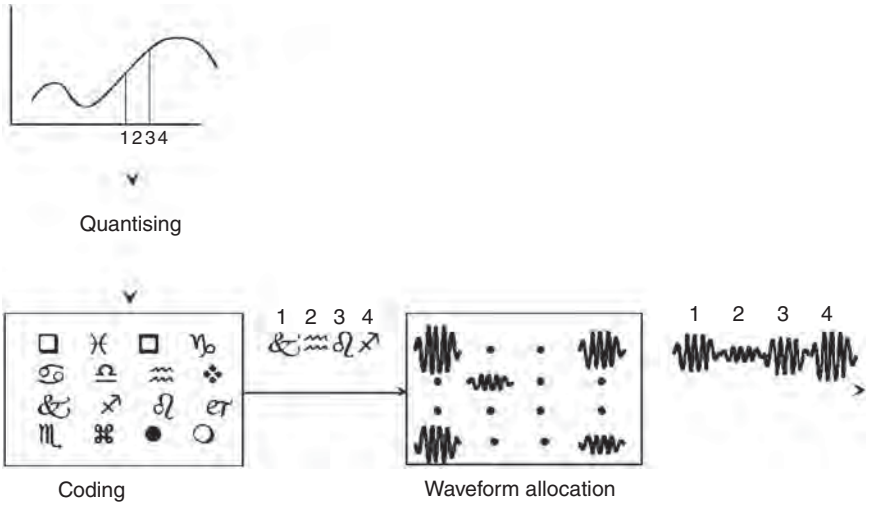

Figure 5-74 Digital modulator [1].

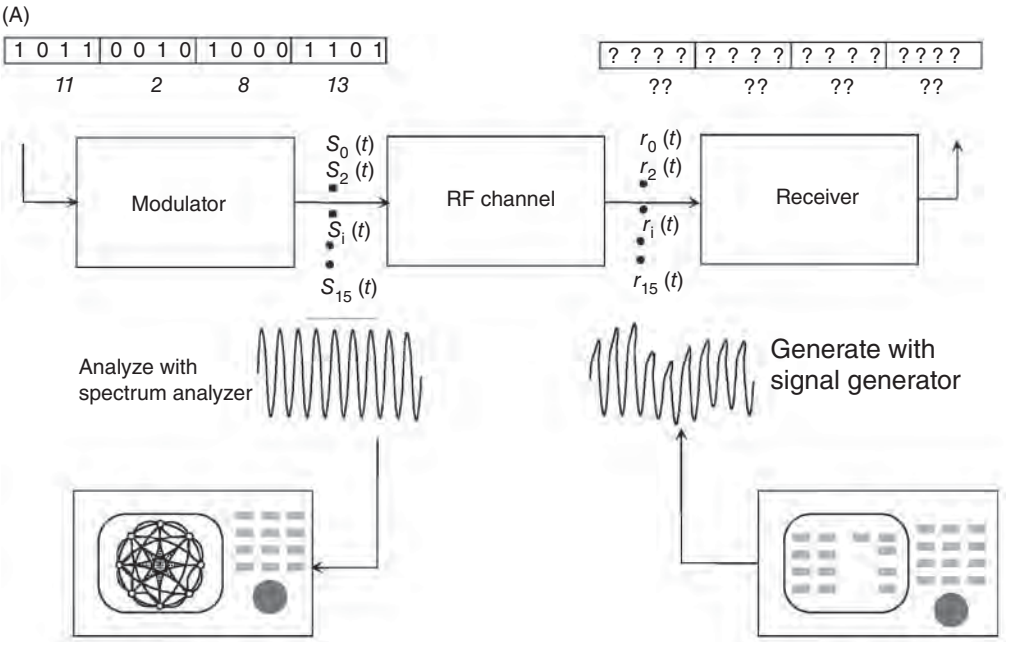

Figure 5-75a The information channel [1].

5-6-1 Representation of a Modulated RF Carrier

The waveform of a modulated RF-carrier can be expressed as

$$s(t) = a(t)\cos[2\pi f_c(t)t + \phi(t)] \tag{5-5}$$

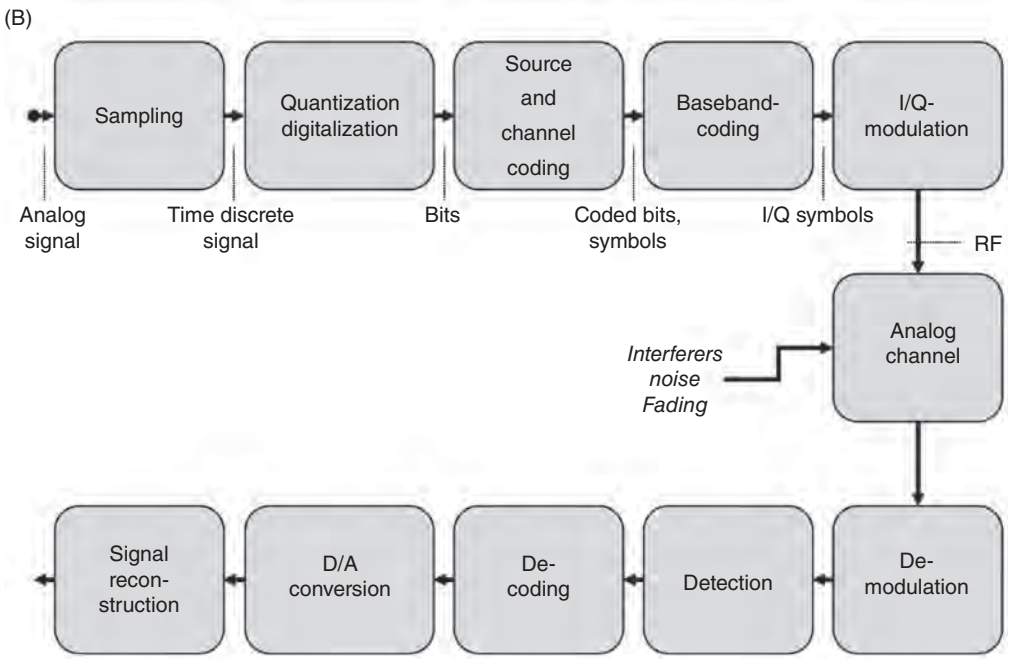

Figure 5-75b Block diagram for a system generating interference, noise, and fading.

and is defined by its amplitude $a(t)$, its carrier frequency $f_c(t)$, and its phase ϕ. All the three parameters are time variant and may be altered to generate different waveforms to represent logical symbols. If the occupied bandwidth of this modulated carrier is narrow, compared with the carrier frequency f_c, we call this signal the RF-bandpass signal (Figure 5-76).

As any frequency variation causes a phase variation and vice versa a phase variation always causes a frequency variation, we can replace any frequency modulation by a corresponding phase modulation. Therefore, we simplify the above equation to

$$s(t) = a(t)\cos[2\pi f_c t + \phi(t)] \tag{5-6}$$

that is, we consider the carrier frequency as a constant and concentrate all frequency and phase variations into the parameter $\phi(t)$.

For our purposes another representation is more suitable, we'll have to look up some trigonometric identities and our formula processor finds that

$$\begin{aligned} a(t)\cos[2\pi f_c t + \phi(1)] &= \cos[\phi(t)]a(t)\cos(2\pi f_c t) \\ &\quad - \sin[\phi(t)]a(t)\sin(2\pi f_c t) \end{aligned} \tag{5-7}$$

which we call the *I/Q* representation of the RF-signal. *I/Q* means that we have an *I* (in phase) signal, namely, $\cos[\phi(t)]a(t)\cos(2\pi f_c t)$, and a *Q* (quadrature) signal, namely $-\sin[\phi(t)]a(t)\sin(2\pi f_c t)$. These equations help us a lot in understanding an *I/Q* modulator. Because of the phase difference of 90° between the two carrier components, these are said to be orthogonal to each other.

All the information about the (modulated) carrier with the carrier frequency f_c is contained in the terms

$$c_I(t) = a(t)\cos[\phi(t)] \tag{5-8}$$

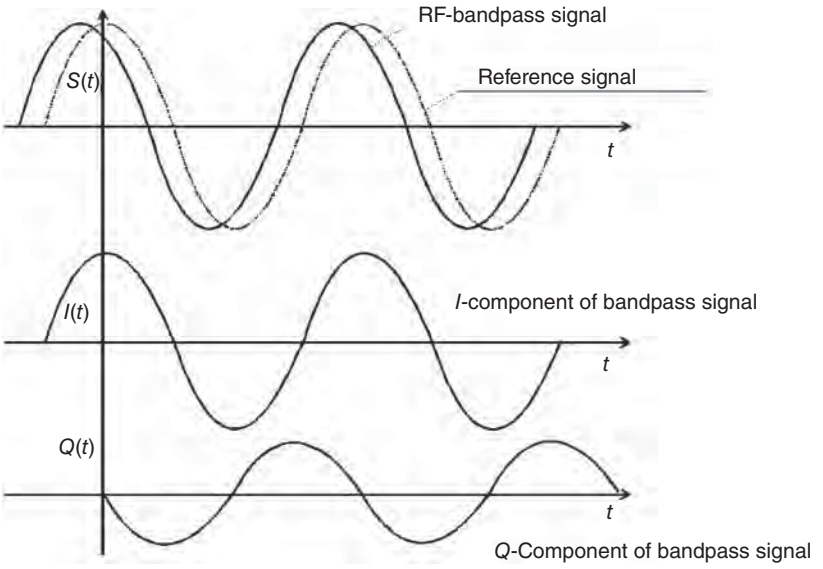

Figure 5-76 The bandpass signal and the *I*/*Q* representation of a carrier [1].

$$c_Q(t) = a(t)\sin[\phi(t)] \tag{5-9}$$

and, lazy as we are, we therefore disregard the terms $\cos(2\pi f_c t)$ and $-\sin(2\pi f_c t)$ for further considerations and denote the above signals $c_I(t)$ and $c_Q(t)$ as the components of the complex baseband waveform or baseband signal.

This leads us immediately to the *vector representation* of the signal, where we consider the two components $c_I(t)$ and $c_Q(t)$ of the complex baseband signal as the time-variant components of a time variant vector with the vector length $a(t)$ and the angle to the *I*-axis $\phi(t)$. We also get

$$a(t) = \sqrt{c_I^2(t) + c_Q^2(t)} \tag{5-10}$$

$$\phi(t) = \arctan\left(\frac{c_Q}{c_I}\right) \tag{5-11}$$

The vector can be depicted in the *I*/*Q* area (Figure 5-77).

5-6-2 Generation of the Modulated Carrier

Once we have realized that the modulated carrier can be represented as the sum of it's *I* and *Q* components, which are the product of the two baseband components with two orthogonal RF-carriers of the same frequency, it is easy to understand the hardware of the modulator (Figure 5-78). An unmodulated RF carrier is split up into two equal oscillations $\cos(2\pi ft)$; one of the two is then shifted by 0.5π, and therefore is described by $-\sin(2\pi ft)$. The component $\cos(2\pi ft)$ is multiplied with the *I* component of the baseband signal $c_I(t)$, the other one, $-\sin(2\pi ft)$, is multiplied with the *Q* component $c_Q(t)$ of the baseband signal. Each multiplication may be performed using a double-balanced mixer. Afterwards the two RF-components are added in a simple power combiner. As it is difficult to shift the carrier by 90° over a broad frequency range, the modulated carrier is generated at an intermediate frequency and then upconverted to the wanted output frequency in a second mixer stage.

The baseband signals are generated by mapping every digital symbol into a pair of digital pulses, which are fed to digital baseband filters. The output signal of these filters is D/A converted and smoothened by analog low-pass filters.

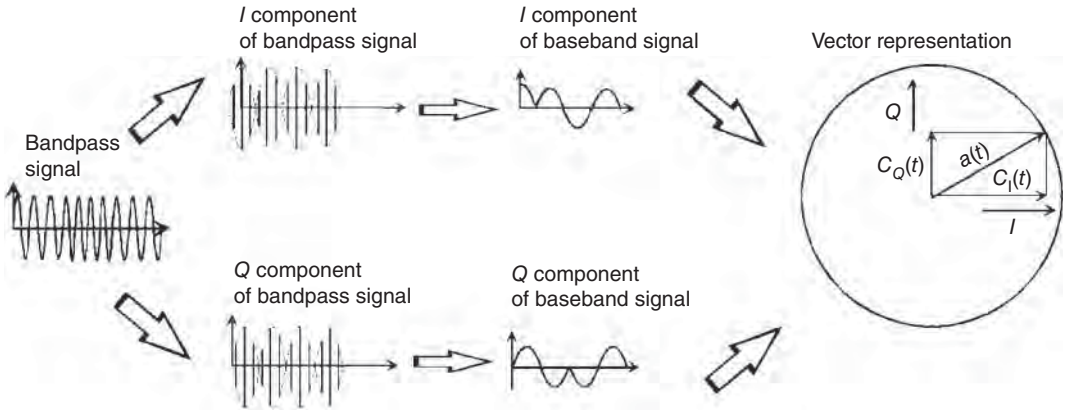

Figure 5-77 Different forms of signal representation [1].

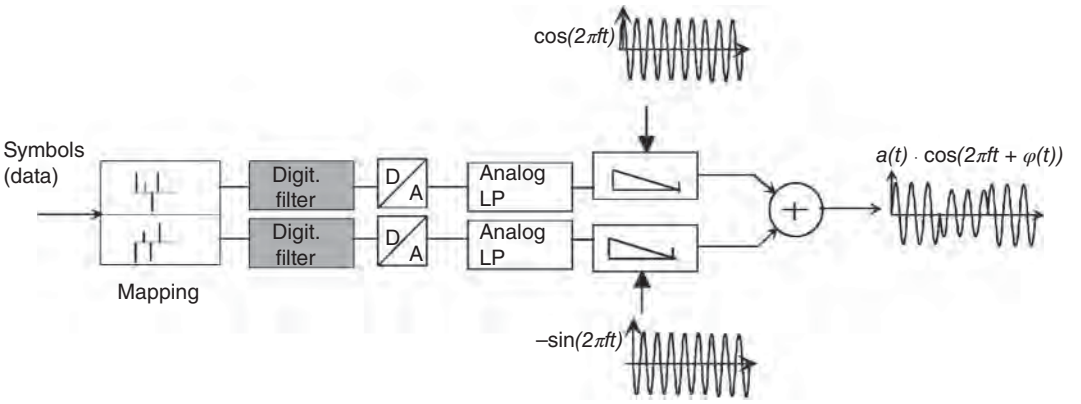

Figure 5-78 Principle of a digital *I*/*Q* modulator [1].

Figure 5-79 shows another example where, for a given modulation (minimum-shift keying [MSK] or Gaussian minimum shift keying [GMSK]), the instantaneous phase and then the corresponding co-sinusoid and sinusoid, that modulates the two carrier components, is calculated from the data signal.

Digital designs of the modulator also exist, in which the IF-carrier generation, the time-variant phase shift, the multiplication with the baseband signals, and the sum of the components are calculated in a digital signal processor, the output of which is D/A-converted and upconverted to the output frequency in the classical way. A further possibility is the generation of the modulated carrier with DDS, as it is used in the Rohde & Schwarz SME signal generator.

Mapping the Data into the Baseband Waveforms

The next question is, "How do we generate the baseband waveforms $c_I(t)$ and $c_Q(t)$?" There is no general answer to this question, as the generation of the baseband waveforms depends on the type of modulation. The following short descriptions will suffice for the moment.

Linear modulations (all kinds of amplitude and phase-shift keying, and *M*-ary quadrature amplitude modulation [QAM]).

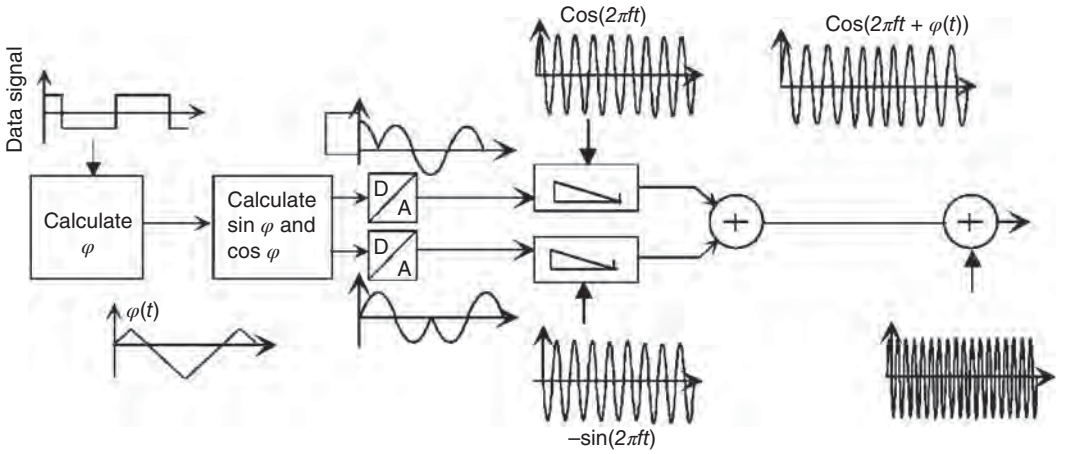

Figure 5-79 *I*/*Q* modulation (MSK and GMSK) [1].

- For binary amplitude and phase shift keying (amplitude-shift keying [ASK] and BPSK), the data signal itself represented as a unipolar (ASK) or bipolar (BPSK) non-return-to-zero (NRZ) signal is the baseband waveform $c_I(t)$; the component $c_Q(t)$ does not exist.
- For *M*-ary phase shift keying and *M*-ary quadrature amplitude modulation, *N* bits are combined to form new symbols that are elements of an alphabet with $M = 2N$ elements. In the simplest case, every symbol is allocated an *I* and a *Q* amplitude during the symbol duration, which is *N* times the bit duration. The modulating signals $c_I(t)$ and $c_Q(t)$ are then staircase functions, and the modulated carrier has a time-varying envelope with the instantaneous amplitude $a(t)$ (Figure 5-80). Because the steps of the envelope cause unwanted side lobes of the RF spectrum, the baseband signals are filtered to smooth the shape of the RF envelope and reduce the occupied bandwidth of the modulated RF signal.
- Nonlinear modulations (frequency-shift keying, minimum shift keying, and Gaussian minimum shift keying).

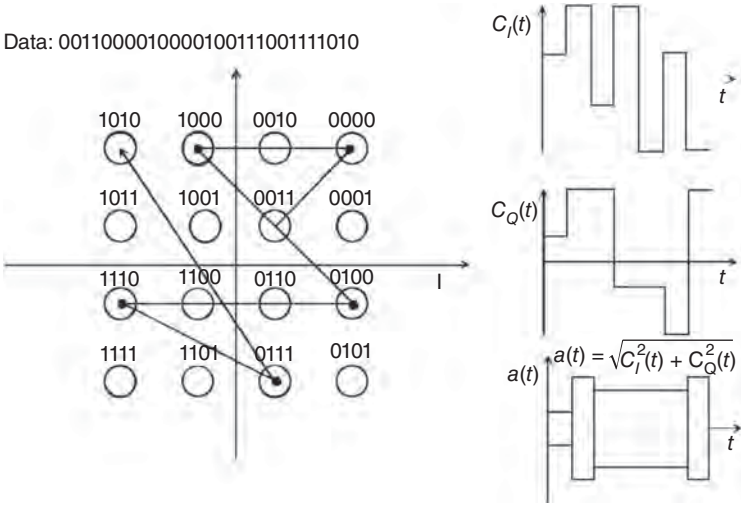

Figure 5-80 Constellation diagram, and baseband and RF signals of 16 QAM [1].

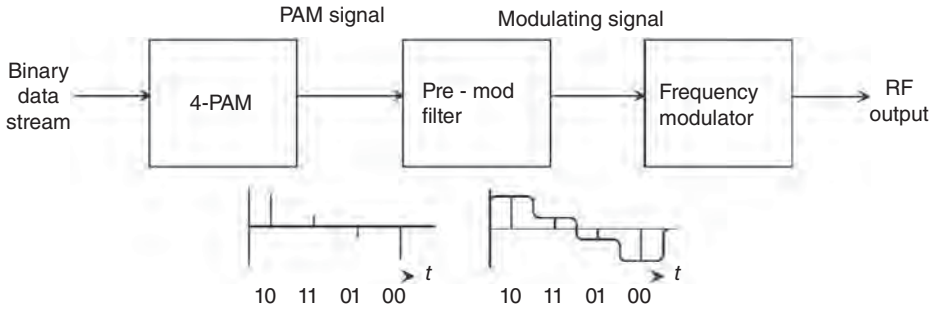

Figure 5-81 4PAM/FSK [1].

- Despite *M*-ary frequency shift keying (FSK) could be performed using *I*/*Q* modulator, for this type of modulation much simpler equipment such as a VCO is used as a frequency modulator. Figure 5-81 shows an example of quaternary frequency shift keying (4FSK), which also is known as pulse-amplitude modulation (4PAM)/FM. This term indicates that every two bits are combined to make a dibit that is mapped into a baseband pulse with an amplitude taking on one of four possible levels. The pulse than is shaped by a base band filter before being fed to the frequency modulator.

If more precise modulations are required (e.g., MSK and GMSK, which also turn out to be frequency modulations), first the instantaneous phase of the modulated RF carrier is calculated from the data. The corresponding sine and cosine values that form the modulating baseband signals $c_I(t)$ and $c_Q(t)$ are determined from a look-up table. This operation is the reason for the fact that frequency modulation is called a nonlinear modulation.

A demonstration follows of how to make sequential waveforms (see Figure 5-82).

It is the task of any transmission process to occupy as little bandwidth as possible. The absolute lower limit in the baseband is half the symbol rate of the baseband signal, where for *M*-ary modulation the symbol rate r_{Symbol} is

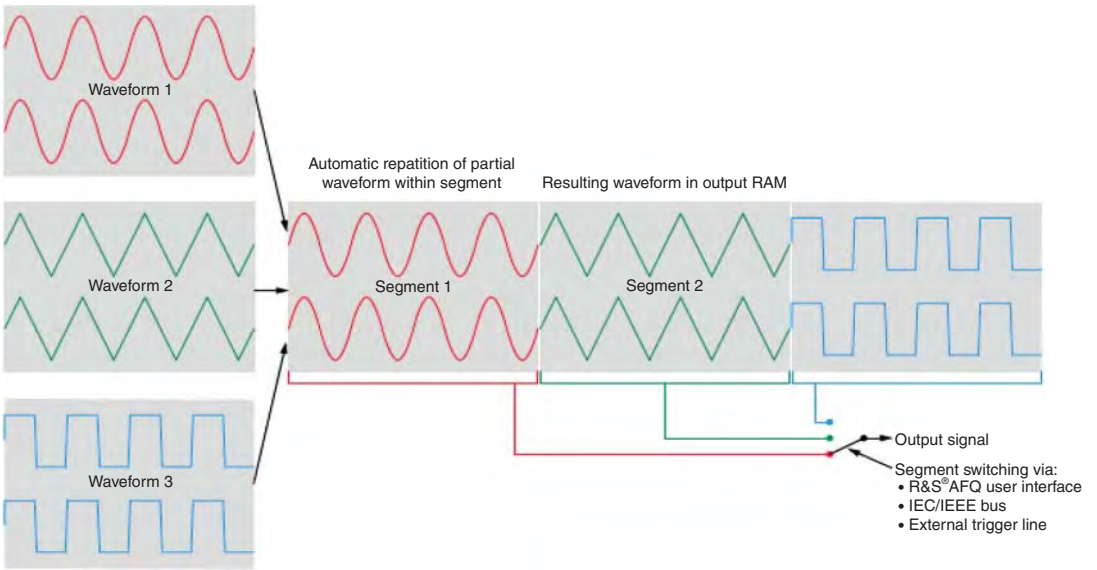

Figure 5-82 The spectrum of a digitally modulated carrier.

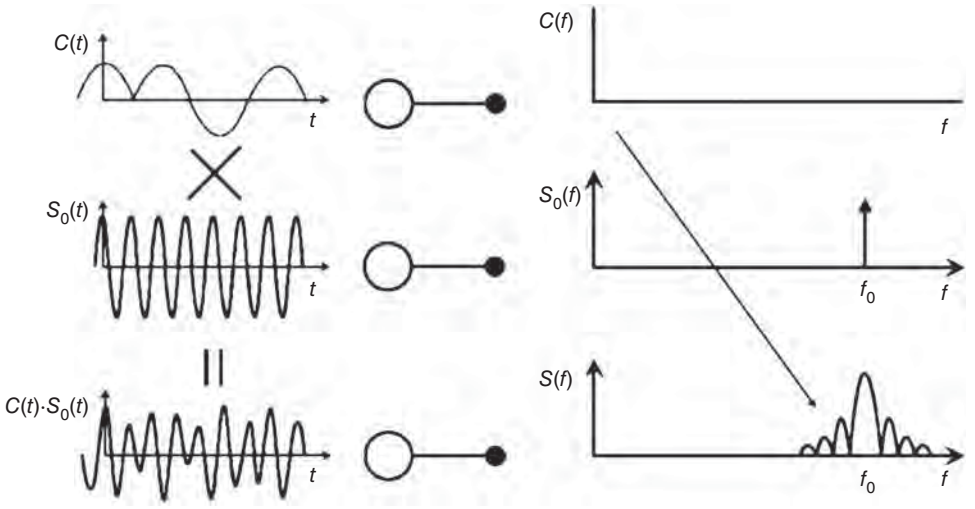

Figure 5-83 Occupied bandwidth in the baseband and the RF range [1].

equal to the bit rate divided by *ld* (*M*). This lower limit is only theoretical as ideal rectangular filters, which cannot be realized were necessary. Therefore, in practice, a minimum baseband bandwidth of about $0.75r_{\text{Symbol}}$ has to be taken into account.

With linear modulation, the occupied bandwidth in the RF-range is twice the occupied baseband bandwidth. This follows from the lag theorem, according to which the double-sided spectrum of a time function is shifted from $f = 0$ to the frequency $f = f_c$ when the time function is multiplied with $\cos(2\pi f_c t)$ (see Figure 5-83).

Expressing this with formulas, we find:

$$c(t) \quad \bigcirc\!\!-\!\!\bullet \quad C(f) \tag{5-12}$$

$$e^{j2\pi f_c t}\, c(t) \quad \bigcirc\!\!-\!\!\bullet \quad C(f - f_0) \tag{5-13}$$

Therefore, if the baseband spectrum is limited by a low-pass filter, the RF spectrum is limited as if it was filtered by an RF bandpass filter with twice the bandwidth of the baseband filter.

The following are some interesting examples (see Figure 5-84a). These different waveforms are needed to characterize the system.

The waveform shown in Figure 5-84b is a very complex signal and beyond the capabilities of standard signal generators. That's where the vector signal generator comes into the picture (Figure 5-84c).

One of the best synthesized generators for vector signals is the SMW200A Vector Signal Analyzer, two channels. A less expensive version is the SMBV100B. This is a single channel generator with 500 MHz bandwidth.

5-6-3 Putting It all Together

We started it all with an analog circuitry. The conventional recommendation is, unless a YIG oscillator is used; don't build a VCO above 6 GHz. Why? The Figure of Merit (FOM) "*Q*" of resonators and tuning diodes deteriorates rapidly, more aggressive than the 6 dB/octave noise increase. This is mostly due to the effect of the parasitic components and difficulties with the planar structure of transmission lines, maintaining 50 Ω and once an inductor is reduced to two turns, the concentration of the magnetic field is not significant and the *Q* suffers. Remember the best *Q* is obtained if length/diameter ratio is more than 3, better 5. Therefore, it is better to multiply the 6 GHz oscillator

(A)

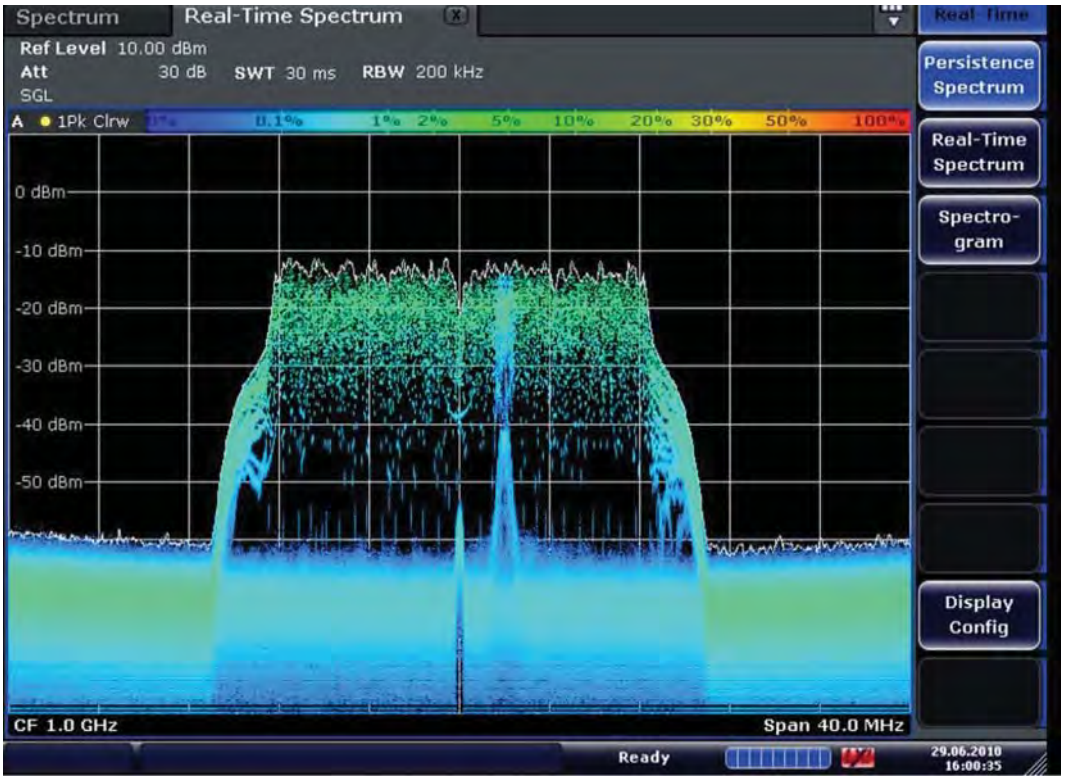

Figure 5-84a A Wi-Fi wideband signal including a discrete carrier (URL-Munich paper).

than to build one at 12 GHz. The block diagram shown in Figure 5-85 can use a mostly DDS-based synthesizer. This would require a clock frequency of 12 GHz. This is the current state-of-the-art possible in development stage.

The digital implementation requires the baseband generator, which can be part of the IC and the *I*/*Q* modulator. So far, *I*/*Q* modulators up to a bandwidth of 2 GHz and more have been implemented. Figure 5-86 shows a block diagram of such an implementation. To compensate frequency and temperature dependence and drift, a complicated compensation circuit has to be in place.

Figure 5-87a shows some block diagrams of signal generators that have been implemented.

The DDS on the lower part of Figure 5-87b is triggered by a clock generator derived from a 1000 MHz PLL. The DDS output, which allows both arbitrary resolution as well as complex waveforms, becomes the reference frequency for the PLL on its right side. Provisions for either a YIG oscillator or a VCO can be made. The switches allow choosing a suitable output frequency. This comparatively simple approach avoids the difficulties of a multi-loop synthesizer.

This approach only works well if a PLL system is available that accepts a 1 GHz reference frequency. So far, most PLLs avoid frequencies above 100 MHz, as the phase-frequency discriminators are not fast enough.

On the 6 GHz Output Unit, we pass the signal through several amplifiers to achieve the desired power levels. The signal is then feed through a variable attenuator for AM modulation and level control. Most devices offer also a

(B)

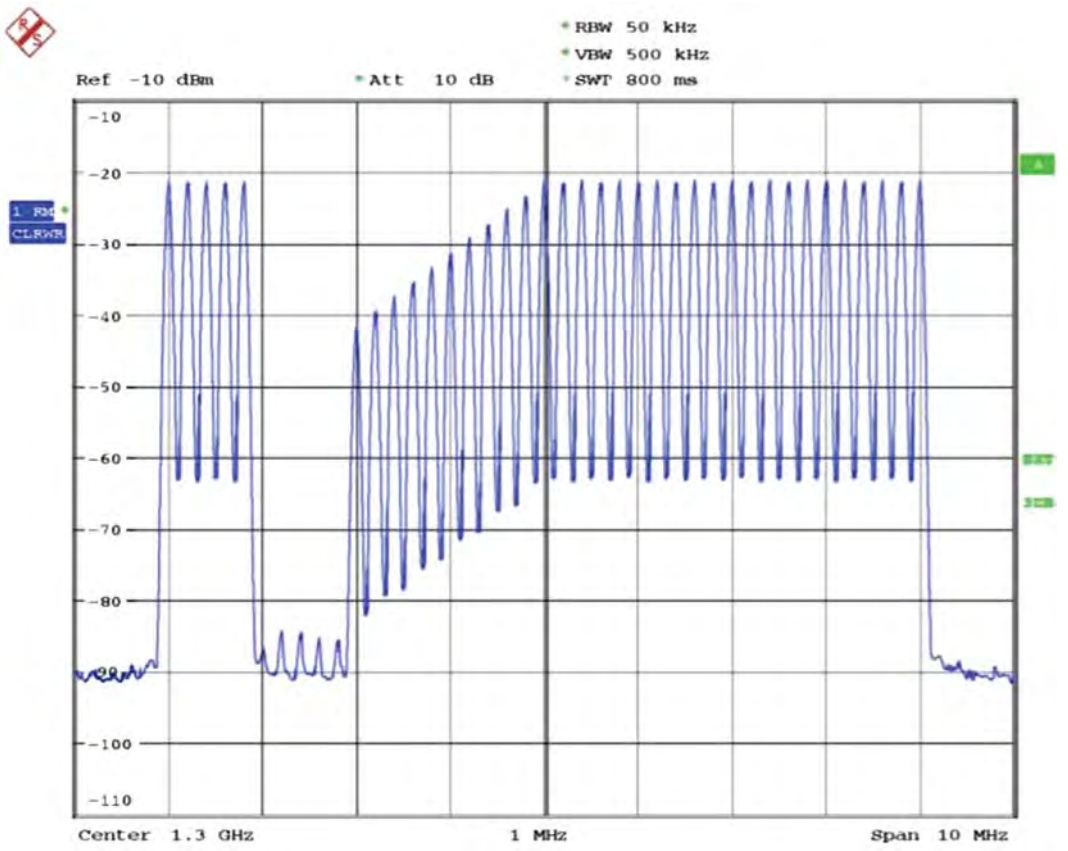

Figure 5-84b Example of multicarrier CW, with different carrier powers and some carriers switched off in the half of the spectrum.

pulse modulator which completely mutes the RF signal. The optional *I*/*Q* modulator gives the possibility for digital modulation. At the end of the signal path, we find different low pass filters for reducing the harmonic distortion and a level detector for the automatic level control (ALC) (see Figure 5-87c).

5-6-4 Combination of Techniques

Figure 5-88 shows a hybrid synthesizer for a precision clock (preliminary data). Output phase noise of AD9914 is about 5 dB higher than the residual phase noise as specified in the datasheet even when it is driven by an R&S SPREF. Most likely the clock buffer is the bottleneck. Nevertheless, the initial result looks promising. Performance curves are given in Figure 5-89a.

The top curve in Figure 5-89a shows the DRO with 300 kHz loop bandwidth, locked against the R&S SMA100A synthesized generator. The lower curve without the overshoot uses a special fixed frequency in-house synthesizer model, SPREF, which generates discrete frequencies from 100 MHz to 8 GHz. The next set of plots shows the same 12.8 GHz generated from the AD9914, the black curve again uses the R&S SMA100A (this can be recognized due

(C)

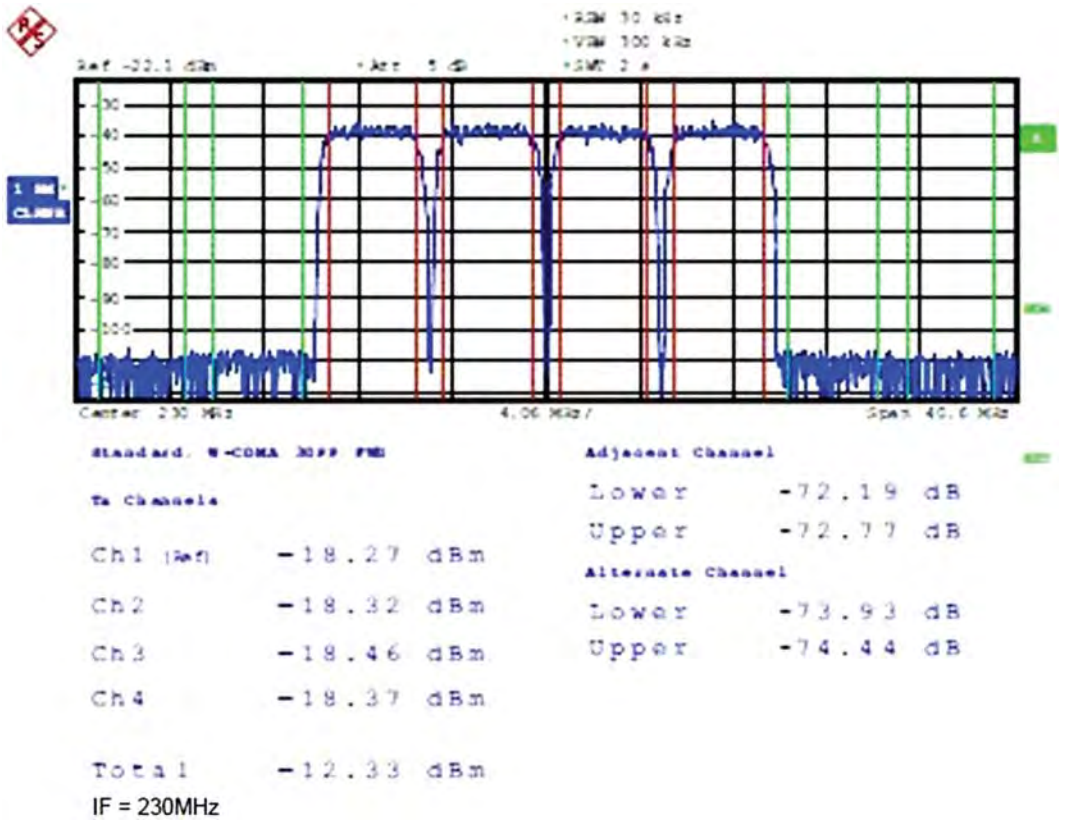

Figure 5-84c Four carrier W-CDMA test mode 1. W-CDMA, wideband code division multiple access.

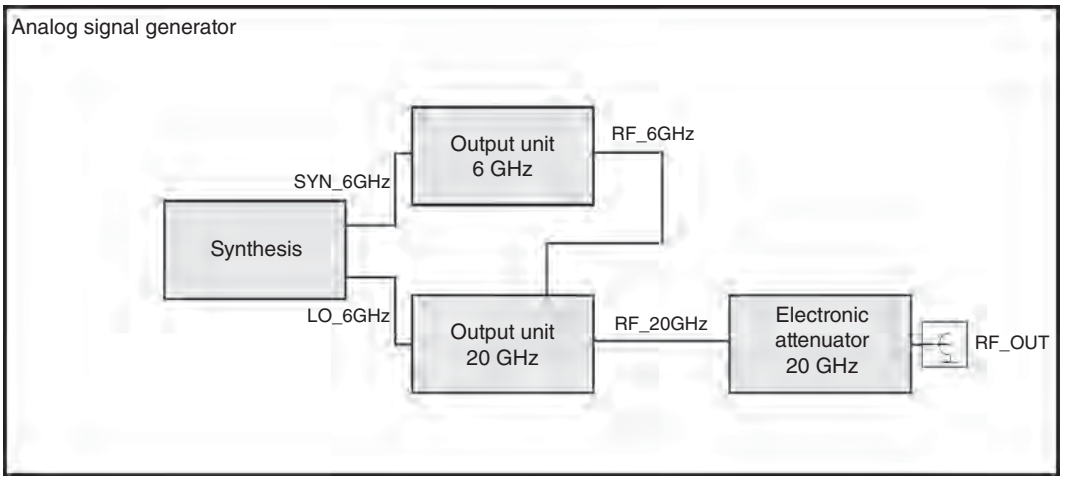

Figure 5-85 Analog signal generator (R&S).

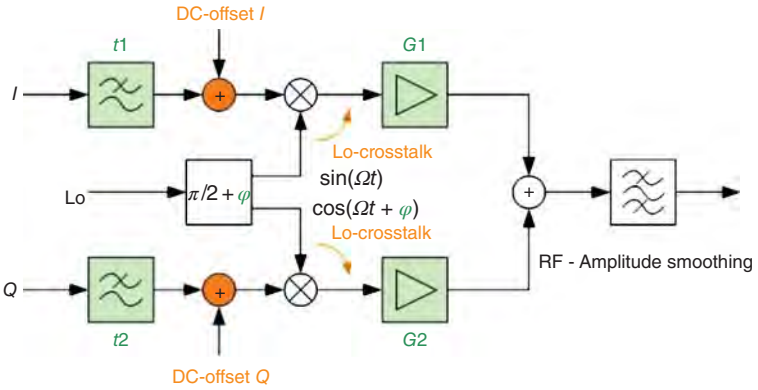

Figure 5-86 Implementation of an *I*/*Q* modulator (R&S).

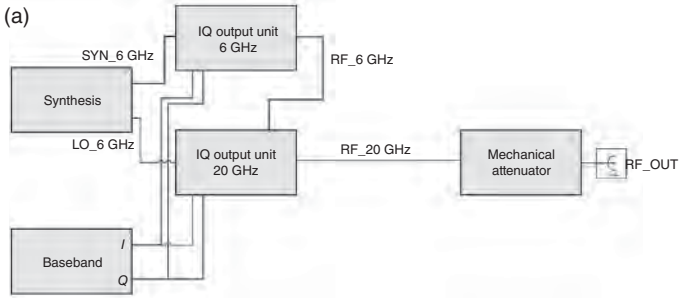

Figure 5-87a Vector signal generator (R&S).

to the PLL overshoot and the same done with the AD9914 and the R&S SPREF reference synthesizer). In about 1 MHz the phase noise is limited by the digital-to-analog converter (DAC). At frequencies close to the carrier, the AD9914 wins, but far out the DAC limits the phase noise to about −145 dBc/Hz. The DRO (top curve) has a much better far off phase noise (∼ −165 dBc/Hz). To a degree this is also limited by its buffer/isolation amplifier (Figures 5-89b and 5-89c).

The SPREF is a custom-made ultra-high performance reference generator, producing from 100 MHz to 12 GHz. A frequently used frequency in synthesizers is 640 MHz. The SPREF is based on an extremely low noise 100 MHz crystal oscillator, typically the Wenzel Golden Citrine. As the output frequencies are related to 100 MHz, a 600 MHz output frequency is close enough to use this instrument for auxiliary frequencies in a synthesizer. This synthesizer is optimized for best phase noise performance up to 12 GHz.

ACKNOWLEDGMENTS

We would like to again acknowledge the contributions of Texas Instruments, General Electric (Martin Marietta/Sanders), Rohde & Schwarz, and other industry sources, which assisted in compiling the overview of Section 5-3.

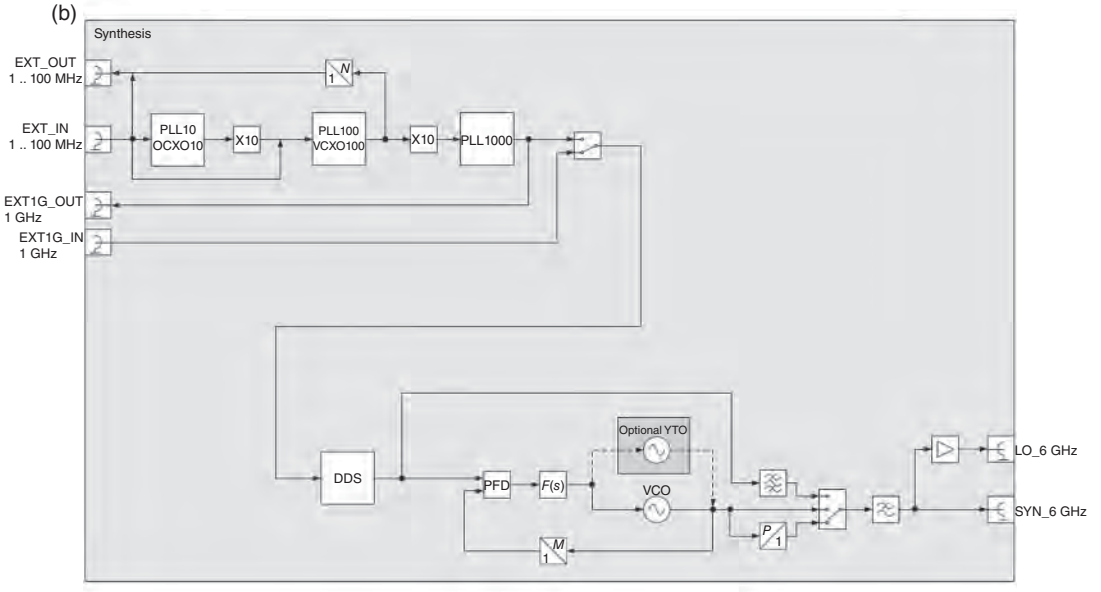

Figure 5-87b Synthesis (R&S).

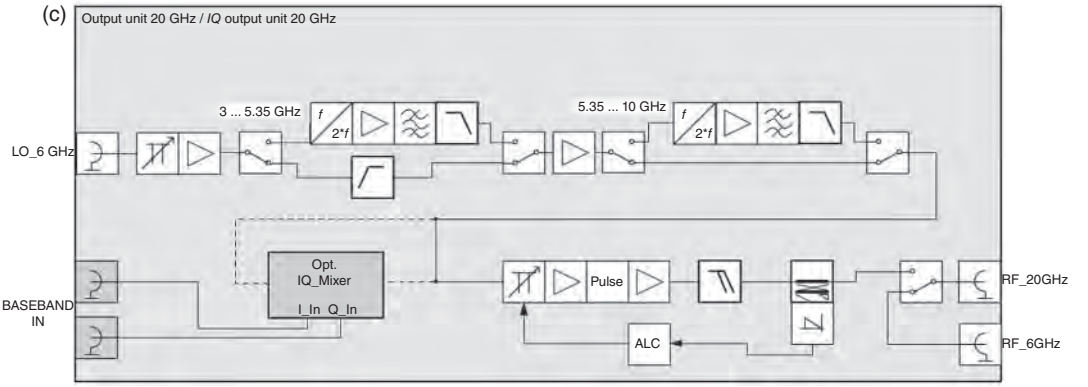

Figure 5-87c Block diagram, output unit 20 GHz/IQ (R&S).

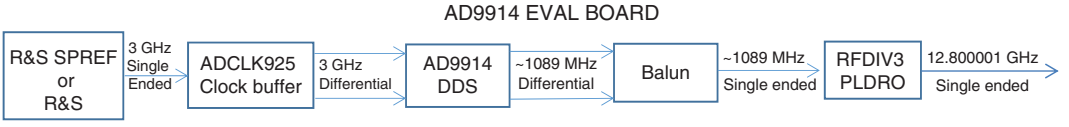

Figure 5-88 Block diagram of AD9914 evaluation board.

(a)

Figure 5-89a Experimental evaluation of a DRO based frequency reference and a DAC based frequency synthesizer.

(b)

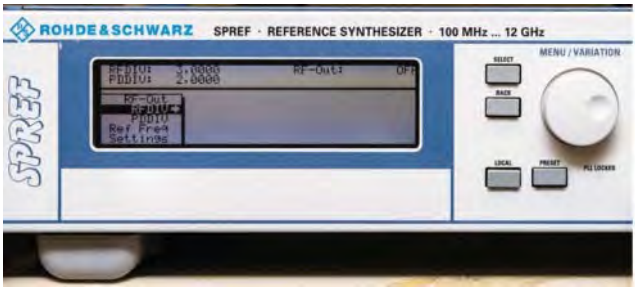

Figure 5-89b Front panel of the SPREF instrument.

(c)

Figure 5-89c SPREF instrument connection points.

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6

A HIGH-PERFORMANCE HYBRID SYNTHESIZER

6-1 INTRODUCTION

The previous chapters have dealt with the design principles of frequency synthesizers and the effect that parameters have on the loop performance. It is impossible to show all details relevant to the design of frequency synthesizers, especially regarding the selection of components, printed circuit (PC) board layouts, and which principle to use over another, as sometimes they are equally good and the choice is very difficult. Engineers typically want to reinvent everything themselves. This is not a very economical way to do research, and inasmuch as one relies on literature, it is also good to take a look at proven designs. A nonworking novel approach is more difficult to digest than looking at a reliable and working approach and trying to improve this and also to understand why it has been done the way it has been done.

In this chapter we will look at a high-performance hybrid synthesizer as a combination of most of the technologies we have analyzed thus far.

Frequency agile synthesizers can now be built easily, essentially by using off-the-shelf available integrated circuits. If very fine resolution is required, one ends up with either a multiloop synthesizer or a combination of a phase-locked loop (PLL) synthesizer and a fine-resolution loop. The two commonly used choices for fine resolution are fractional division N synthesizers and direct digital synthesizers (DDSs). Fractional division N synthesizers, as previously described, are usually found in test equipment and offer some distinct advantages due to their predictability of spurious sidebands. Also, they can be frequency modulated by a fast change of the division ratio. Conventional analog cancellation circuits, which are responsible for suppressing the unwanted sidebands, are both temperature and component sensitive. Therefore, a digital version of this is needed. For most communication circuits, where high-resolution synthesizers are required, the direct digital frequency synthesizers are attractive because all necessary components are located on the chip and a custom-tailored synthesizer using both a PLL and DDSs can easily be put together.

To demonstrate the ease of application, we would like to show a high-performance hybrid synthesizer that uses a unique combination of generally available techniques. Such an implementation, for which a patent had been issued to Qualcomm in the United States, had been done initially in 1979 in the Rohde & Schwarz XPC Synthesizer. The interpolation synthesizer portion of the overall approach, shown in detail, has two chips. However, if the application is less cost sensitive, this can be replaced by a higher integrated version.

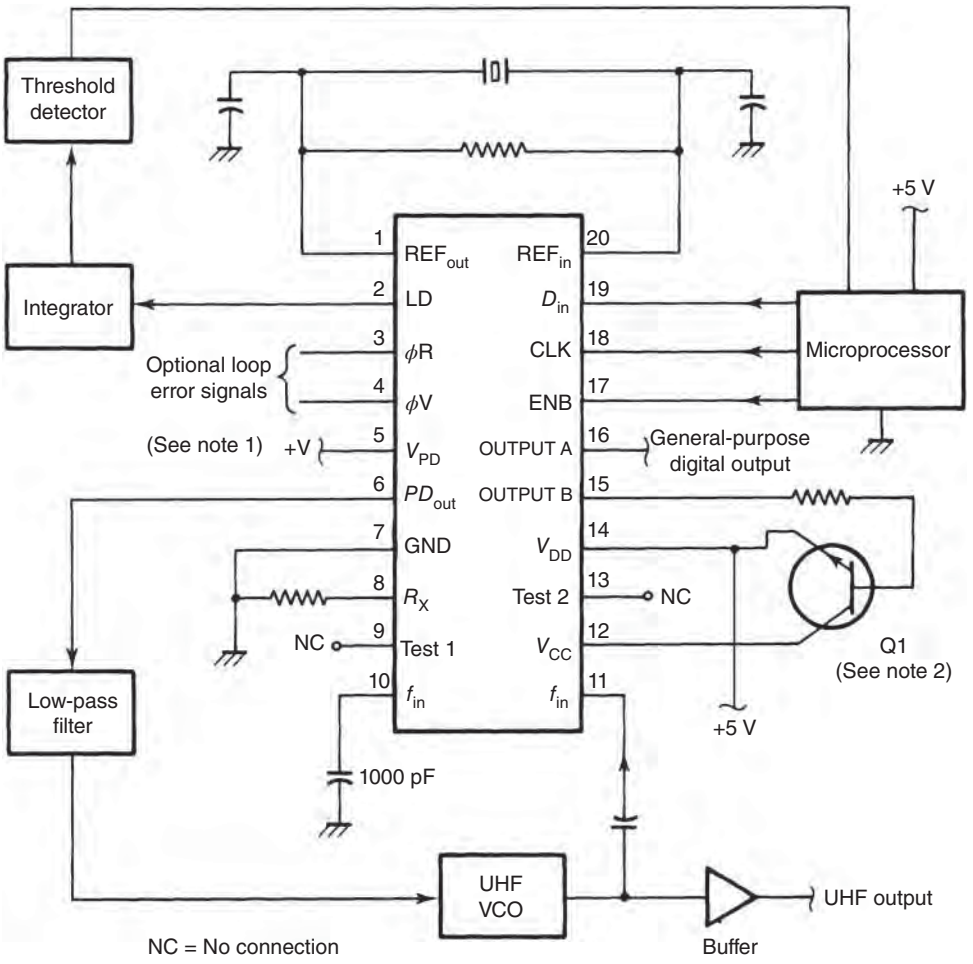


Figure 6-1 Example application. Notes: (1) When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. (2) Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general-purpose digital pin, OUTPUT B. If the standby feature is not needed, tie pin 12 directly to the power supply. (3) For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND (ground) with low-inductance capacitors. (4) The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the voltage-controlled oscillator (VCO). Also, the VCO frequency divided by $f_R - NT = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

6-2 BASIC SYNTHESIZER APPROACH

Figure 6-1 shows an application example using the Motorola Series MC1451XX. Because of their low power consumption and silent operation mode capability, these synthesizers allow the design of very powerful single-loop synthesizers. The required interface is fairly simple to handle and, of course, makes intensive use of microprocessors.

On the other hand, the required quasi-arbitrary resolution is obtained from the DDS. These DDSs are available through several sources and of various types, such as the Analog Devices model AD7008, and have a built-in digital/analog (D/A) converter to provide the necessary output.

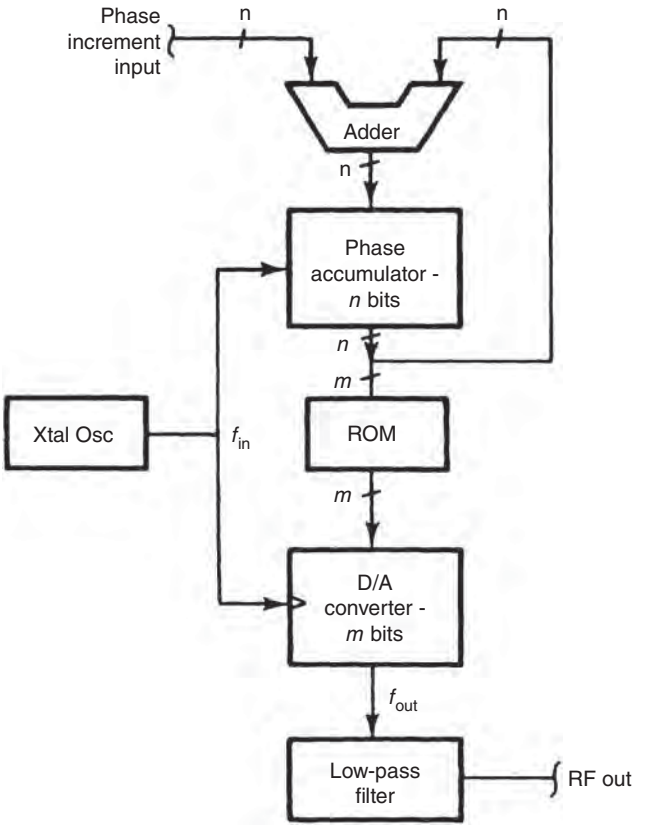


Figure 6-2 Block diagram of a DDS system.

Figure 6-2 shows the functional block diagram of a DDS system. In analyzing both the resolution and signal-to-noise ratio (or rather signal to spurious performance) of the DDS, one has to know the resolution and input frequencies. As an example, if the input frequency is approximately 35 MHz and the implementation is for a 32-bit device, the frequency resolution compared with the input frequency is $35E6 \div 2^{32} = 35E6 \div 4.294967296E9$ or $0.00815\,\text{Hz} \approx 0.01\,\text{Hz}$. Given the fact that modern shortwave radios with a first intermediate frequency (IF) of about 75 MHz will have an oscillator between 75 and 105 MHz, the resolution at the output range is more than adequate. In practice, one would use the microprocessor to round it to the next increment of 1 Hz relative to the output frequency.

As to the spurious response, the worst-case spurious response is approximately $20 \log = 2^R$, where R is the resolution of the D/A converter. For an 8-bit A/D converter, this would mean approximately 48 dB down (worst case), as the output loop would have an analog filter to suppress close-in spurious noise. In our application, we will use an 8-bit external D/A converter. However, devices such as the Analog Devices AD7008 DDS modulator have a 10-bit resolution, as shown in Figure 6-3. Ten bits of resolution can translate into $20 \log 2^{10}$ or 60 dB of suppression. The actual spurious response would be much better. The current production designs for communication applications, such as shortwave transceivers, despite the fact that they are resorting to a combination of PLLs and DDSs, still end up somewhat complicated.

Figure 6-4 shows the necessary components of a single PLL system, which are hidden in the chip approach outlined in Figure 6-1. Figure 6-5 shows the combination of a standard PLL and a DDS, as implemented in the ICOM IC 736 HF/6m transceiver. This approach uses the DDS in a frequency range between 500 kHz and 1 MHz. This frequency gets converted up to either 60 MHz at the shortwave band or 90 MHz at the 6-m ham band. The

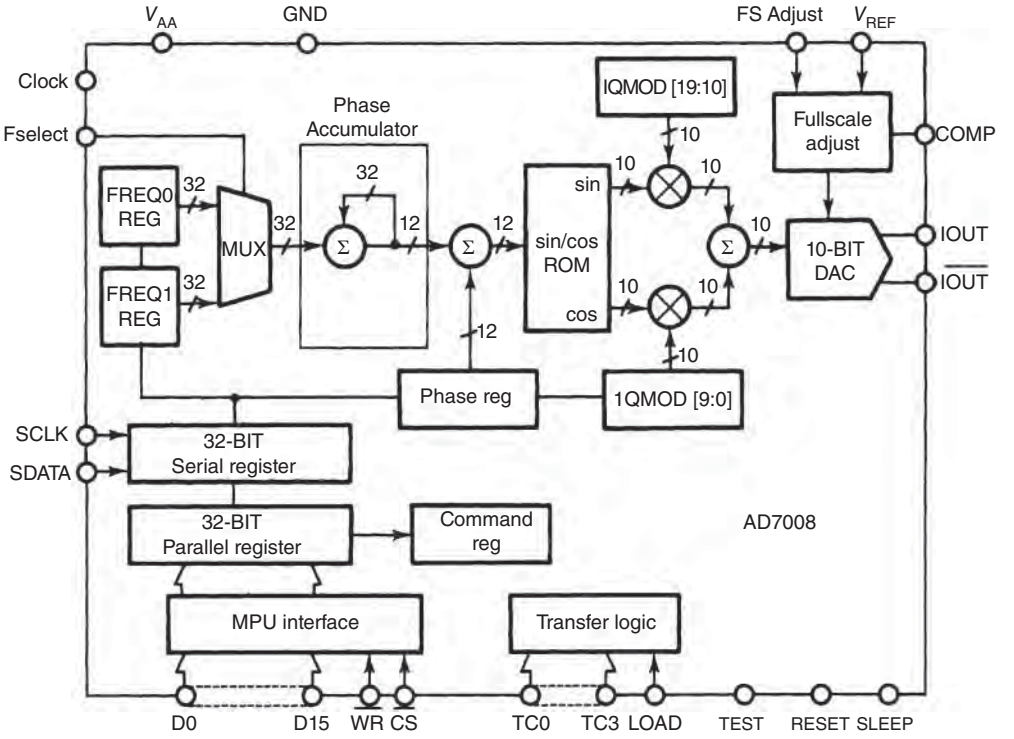


Figure 6-3 Functional block diagram of the Analog Devices AD7008 DDS modulator.

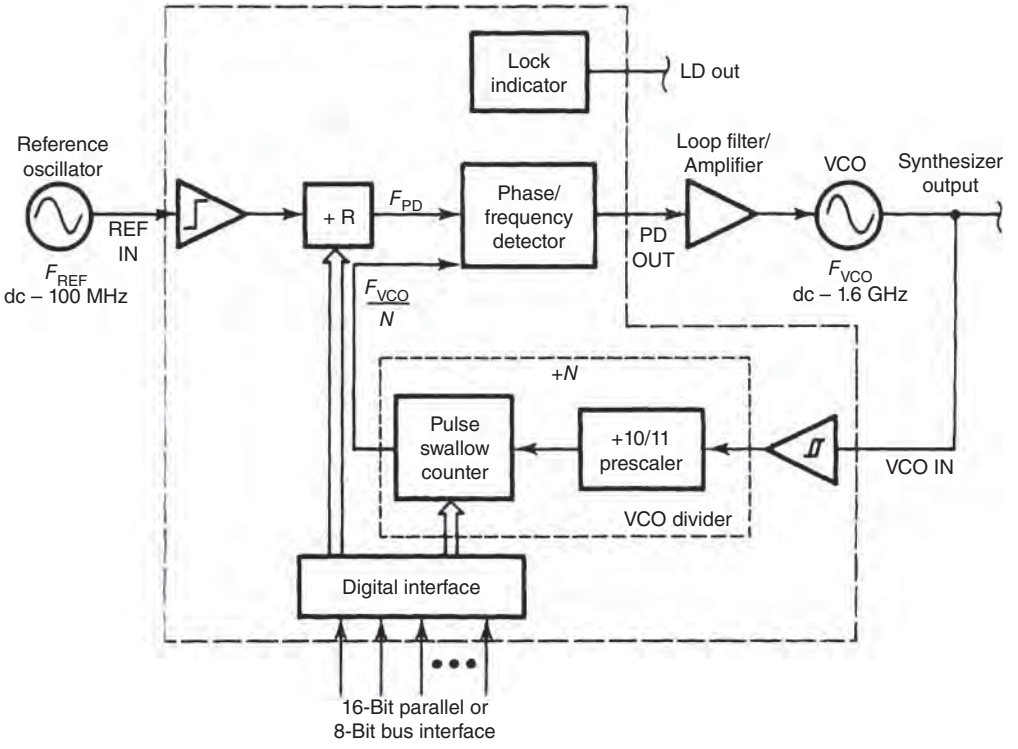


Figure 6-4 Block diagram of a single-loop PLL synthesizer showing all the necessary components for microwave and RF application.

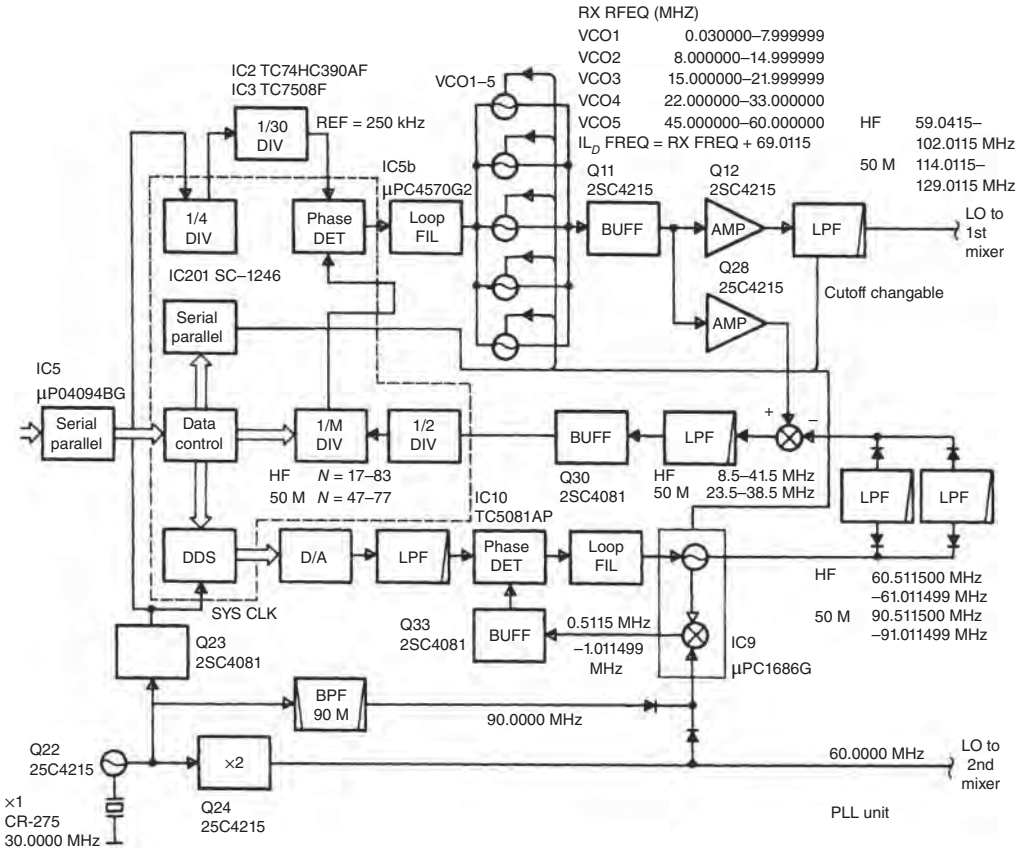


Figure 6-5 Synthesizer used in the ICOM IC 736, 6-m transceiver. The IC 736 combines both the DDS and PLL approaches.

resulting frequency is used as an auxiliary frequency to convert the frequency of the first local oscillator (LO) (69.0415– 102.0115 MHz) down to the synthesizer IF between 8.5 and 41.5 MHz. There is an additional divide-by-2 stage in the loop, which therefore requires a reference frequency of 250 kHz instead of 500 kHz. This is done to extend the operating range of the synthesizer chip, including its prescaler's capability of operating at much higher frequencies, although it does not have such a hybrid DDS incorporated (Figure 6-6). While this approach obtains a fairly small division ratio, it is still a four-loop synthesizer. One loop is the DDS itself. The second is the translator loop that mixes the DDS up to 60 MHz. The third is the main loop responsible for the desired output frequency. The fourth loop, so to speak, is the generation of the auxiliary frequencies of 60 and 90 MHz, which are derived from the 30-MHz frequency standard. For reasons of good phase noise, it employs a total of five VCOs. The fact that the division ratio varies between 80 and 17 also indicates that the loop gain will change considerably (Figure 6-7).

The 10.7-MHz signal from the crystal filter now goes to the single chip MC145170 shown in Figure 6-8, which contains all the necessary dividers and the phase/frequency discriminator. The operational amplifier is driven from a 28-V source and the negative supply of the OPA27 is connected to a voltage doubler, which receives its ac voltage from the synthesizer IC. This trick allows extension of the operating automatic gain control (AGC) voltage. The resistive filter following the op-amp is a spike suppression filter. The actual VCO consists of an arrangement of 2×6 tuning diodes BB805. The inductor is 92 nH and consists of four turns, with the taps on turns 2 and 3. The oscillator also has a clamping circuit as opposed to a diode, similar to a grid leakage current detector. This circuit provides the cleanest output from a phase noise point of view.

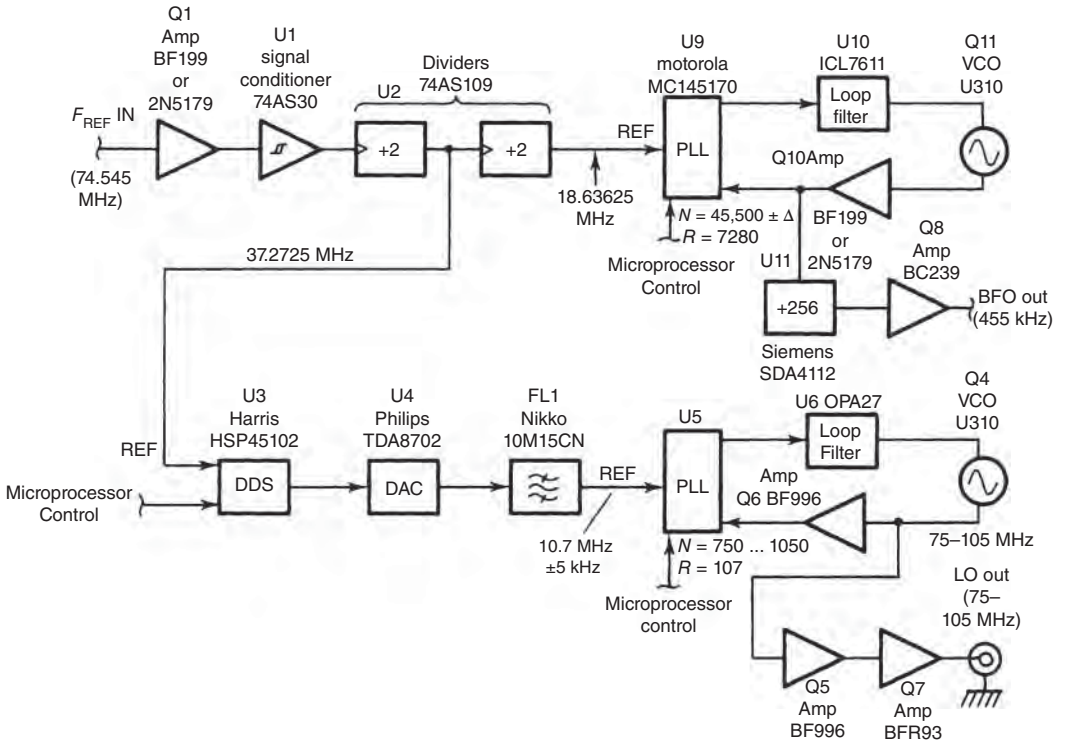


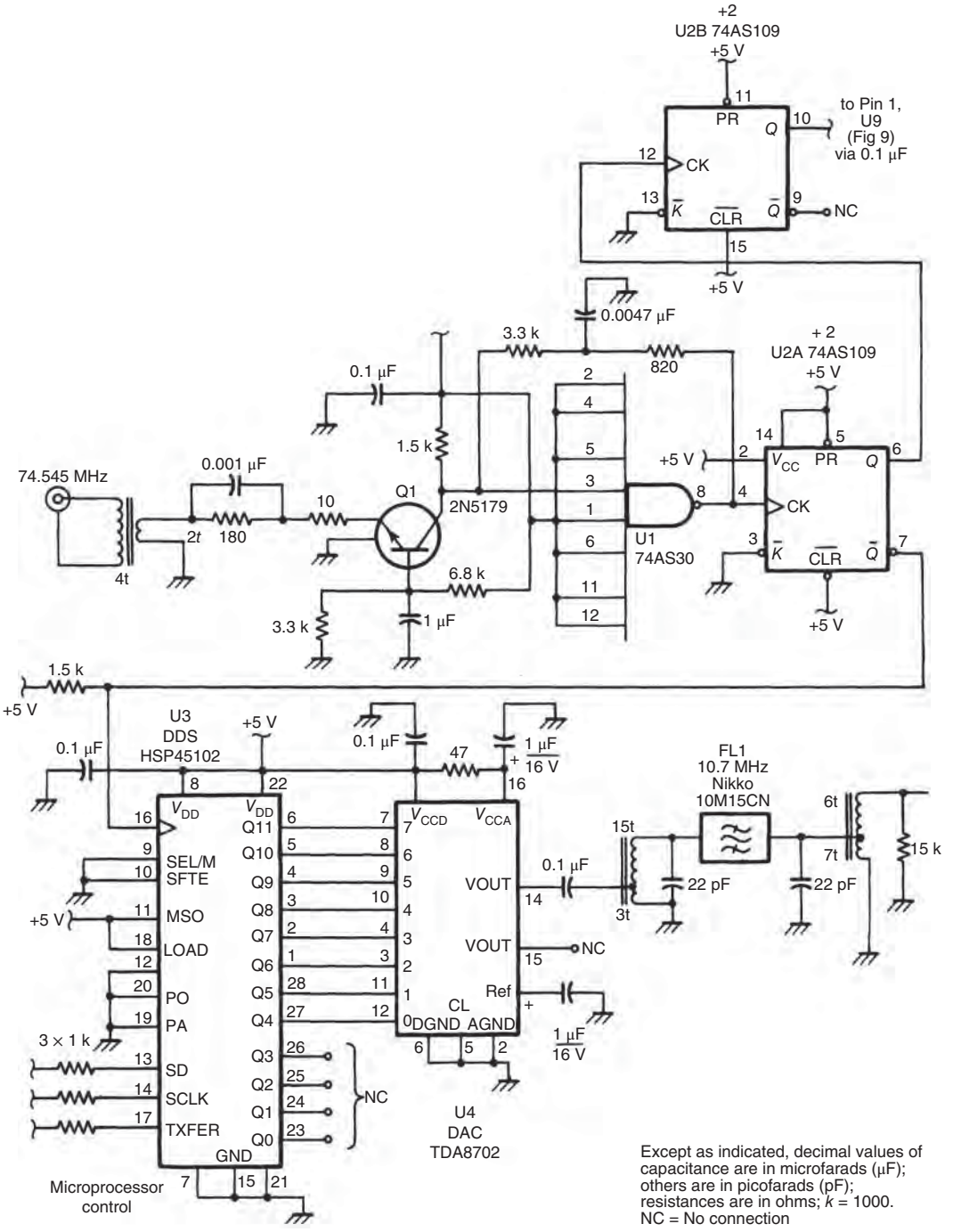
Figure 6-6 Hybrid synthesizer with output frequency of about 455 kHz, which provides the 75–105 MHz at approximately 0.01-Hz resolution. This synthesizer uses a combination of a standard PLL and DDS.

The output from this VCO is then applied to a distribution amplifier system as shown in Figure 6-9. One dual-gate metal–oxide–semiconductor field-effect transistor (MOSFET) provides the output for the PLL IC and the other dual-gate MOSFET drives a feedback stage, which, in turn, supplies 17 dBm output power for the first mixer. Both the BFO and LO synthesizer have their own regulator.

Finally, the BFO synthesizer, as shown in Figure 6-10, follows the same principal pattern since the voltage swing for the tuning diode can be much smaller: it operates off 10 V. Also, the BFO oscillator is much simpler in that its output gets divided down to 455 kHz, which is done by using a fixed divide-by-256 divider. Both the synthesizer chips and the DDS are driven by an appropriate microprocessor. The microprocessor system is then responsible for all the housekeeping activities.

6-3 LOOP FILTER DESIGN

The synthesizer uses a type 2 third-order loop, which is sufficient in both reference suppression and switching speed. In order to accomplish this, we have to look at both the free-running phase noise and the phase noise under closed-loop conditions. For the calculation of the open loop, we assume an equivalent noise resistor of R_n for the tuning diode of about 3 kΩ and a large signal-to-noise figure of the transistor of 10 dB. The definition of R_n was explained earlier. We will calculate the noise at 100-MHz frequency and assume a loaded resonator Q of 120. The flicker frequency noise, because of using an N-junction field effect transistor (FET), is assumed to be 50 Hz. The resulting phase noise is −134 dBc/Hz. Since the VCO gain is 1 MHz per volt, it can be shown that the noise contribution is mostly from the tuning diode. A change in the Q value will have no contribution because the flicker noise of the tuning diode gets modulated on the oscillator. The phase noise for the free-running oscillator is around



Except as indicated, decimal values of capacitance are in microfarads (µF); others are in picofarads (pF); resistances are in ohms; k = 1000. NC = No connection

Figure 6-7 Portion of the hybrid synthesizer's detailed schematic. It takes 74.55 MHz from the second LO and drives the beat frequency oscillator (BFO), PLL, and DDS systems.

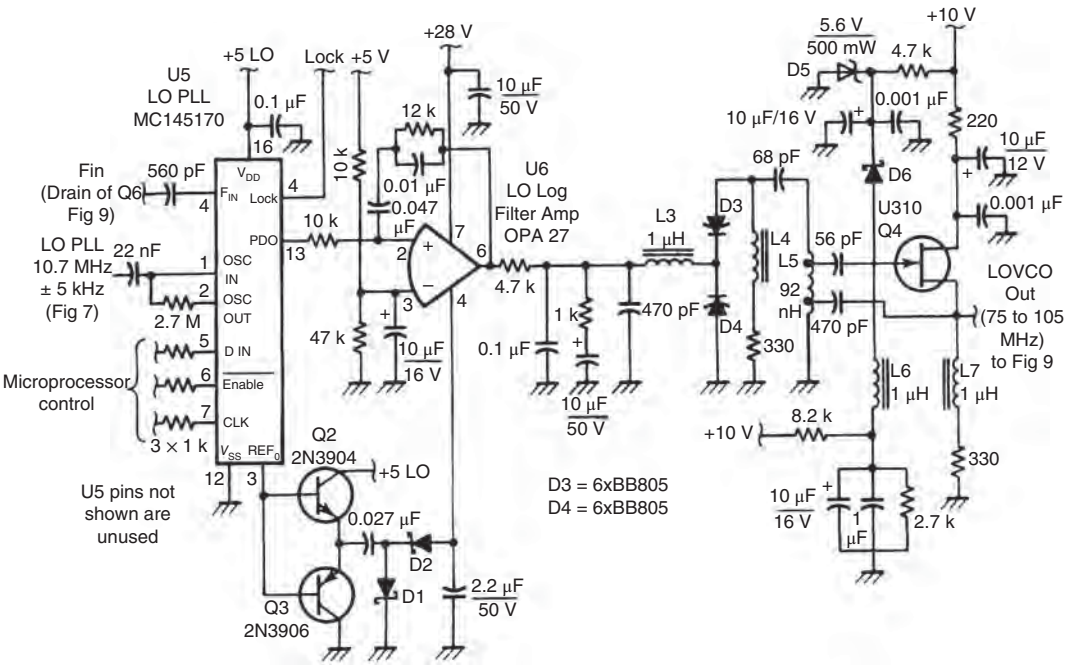


Figure 6-8 Single-loop PLL synthesizer of the main loop LO and the 75–105 MHz VCO.

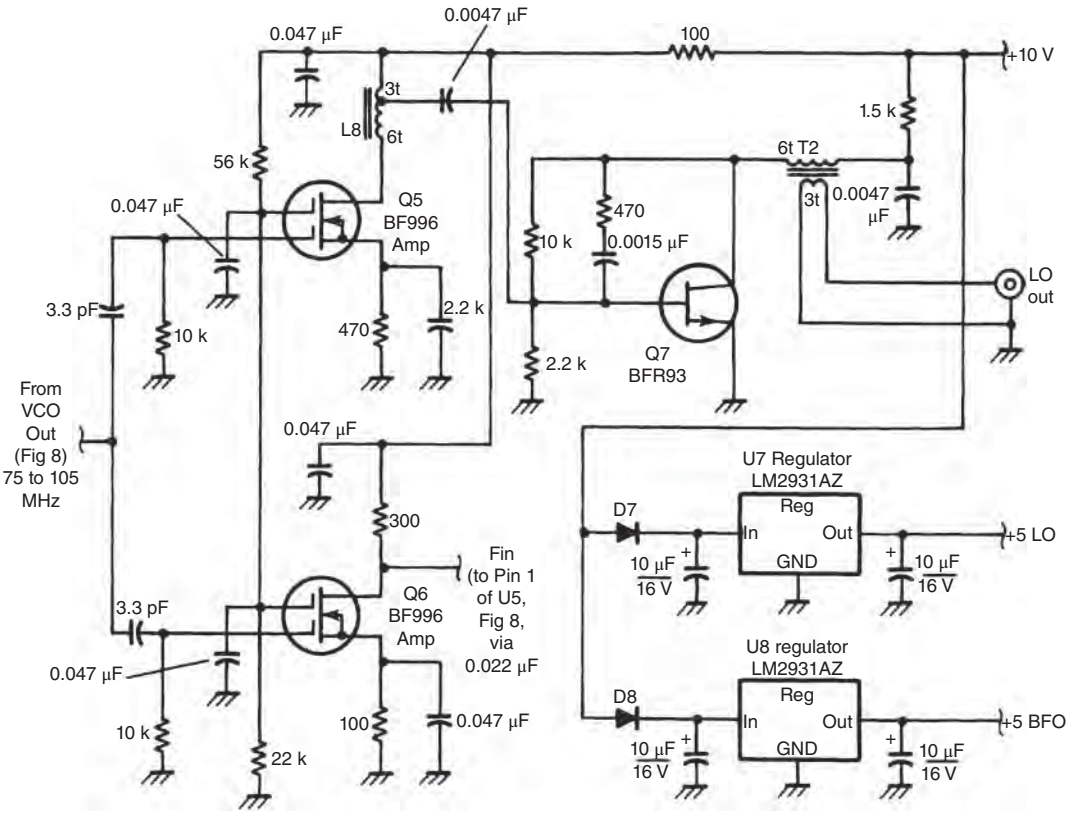


Figure 6-9 Isolation and driver for the first LO. Each synthesizer stage is driven by a separate regulated power supply.

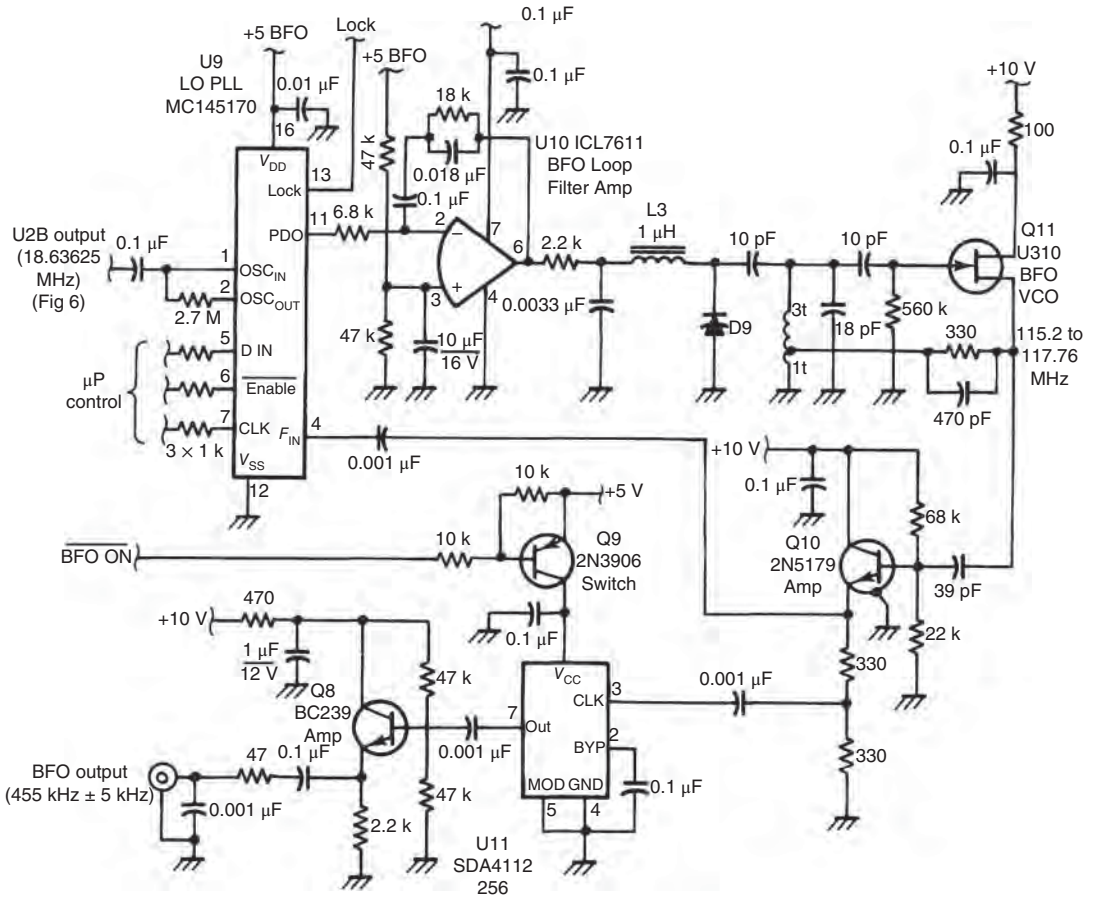


Figure 6-10 Single-loop BFO synthesizer. Note the output frequency is divided by 256 down to 455 kHz.

134 dBc/Hz at 20 kHz off the carrier. Table 6-1 shows all the values used to calculate the single sideband (SSB) phase noise of the oscillator. This was done with Compact Software's PLL Design Kit.

The next step to consider is the difference between switching time and phase noise. Also, because of the up-multiplication of the phase noise into the loop, the loop frequency has to be carefully selected. As a first example, we set the natural loop frequency at 1 kHz; this results in a phase noise deterioration from 107 dBc/Hz down to about 90 dBc/Hz. Figure 6-11 shows the comparison between open- and closed-loop phase noise prediction. Note the overshoot around 1 kHz off the carrier. Also, because of the many dividers of the loop, the phase noise below 10 Hz increases dramatically. In order to improve the single-loop synthesizer, one has to allow for a loop bandwidth at around 300 Hz. Why is this important in practical use? It is important because the continuous wave (CW) operation of a commercial receiver would be poorer in signal-to-noise ratio than with a different filter bandwidth. A re-run of the same analysis with a 300-Hz bandwidth shows a significant reduction of the phase noise compared with the previous example. Figure 6-12 shows the comparison between the open- and closed-loop phase noise predictions. Note the overshoot around 300 Hz off the carrier. This results in much less deterioration of the free-running oscillator.

The values for the active element have been computed using Compact Software's PLL Design Kit and Figure 6-13 shows the Bode diagram for the one-loop synthesizer.

Table 6-1 Values used in calculation of SSB phase noise

Equivalent tuning-diode noise resistance	3000 Ω
Transistor noise figure	10 dB
Root-mean-square (RMS) noise per signal to quantisation noise ratio (SQR) (1 Hz) bandwidth	7.04 nV
VCO gain in Hz/V	1.E6
SSB noise at frequency offset	25.e3 Hz
Enter VCO center frequency	100 MHz
Loaded resonator *Q*	120
Flicker frequency (1 Hz–100 MHz)	50
LO output power	1.0 mW
The phase noise in 25-kHz offset is −134 dBc/Hz	

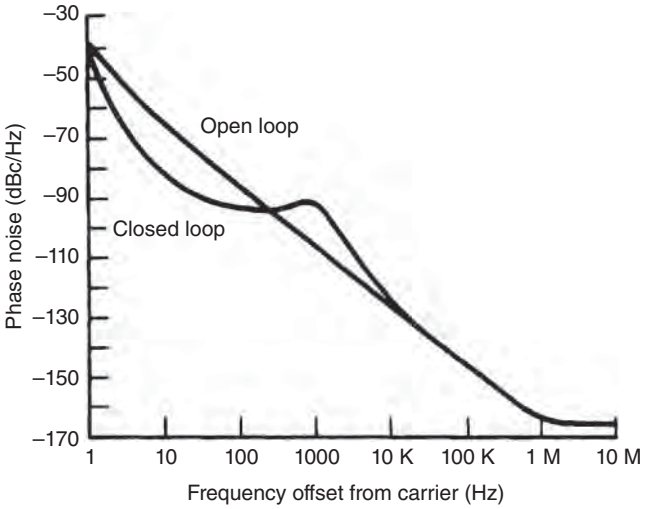


Figure 6-11 Comparison between open- and closed noise prediction. Note the overshoot of around 1 kHz off the carrier.

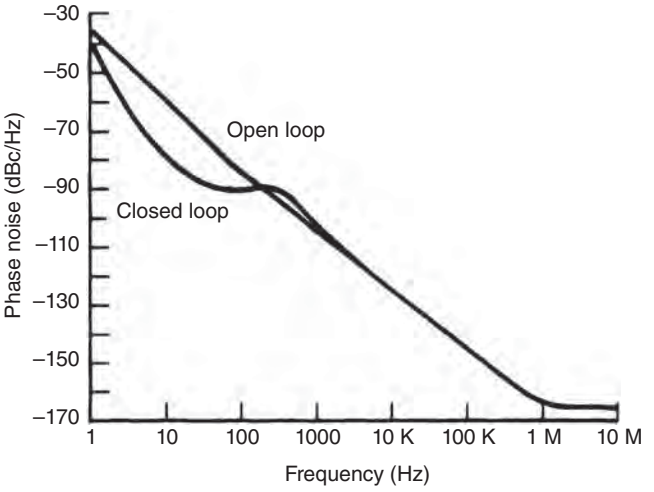


Figure 6-12 Comparison between open- and closed-loop noise predictions. Note the overshoot around 300 Hz off the carrier.

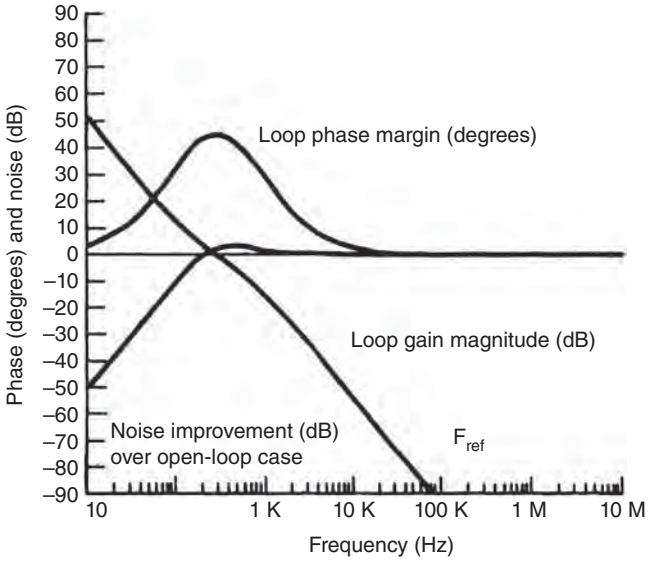


Figure 6-13 Bode diagram of a type 2 third-order loop. It is used in the main loop of our hybrid synthesizer. The predicted reference suppression is 90 dB.

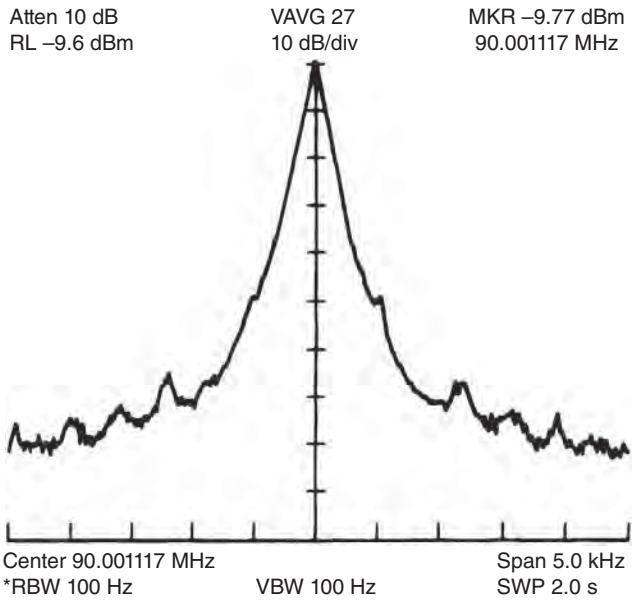


Figure 6-14 Spur analysis of the hybrid synthesizer in which there are no close-in discrete spurs within ±2 kHz.

Figures 6-14 and 6-15 show the spectral analysis plots of the first LO loop, at a speed of ±2.5 kHz. We have not found any discrete spurs close in. There are two spurs located at approximately ±32 kHz, which seem to come from radiation and not directly from the DDS. We can then calculate the transient response, which is approximately 5 ms. (This is the time it takes the synthesizer to lock.)

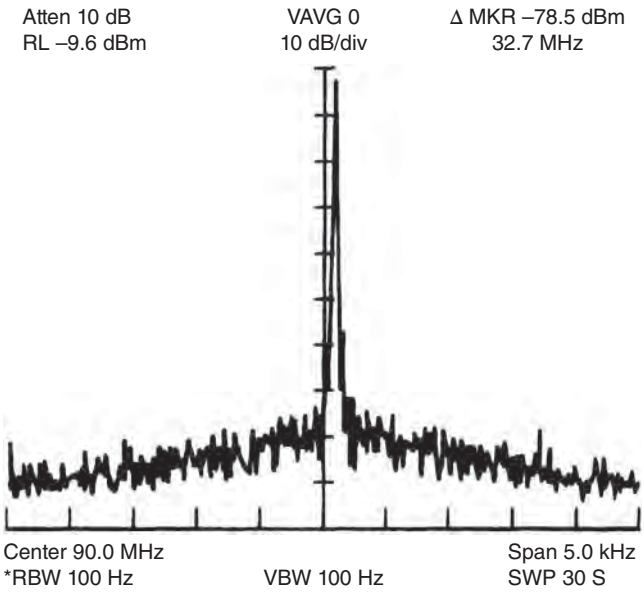


Figure 6-15 Spur analysis of the main loop synthesizer in the 100-kHz regime. Note that there are two discrete spurs approximately ±32 kHz and 78.5 dB down. These are due to the DDS contribution and other pick-ups.

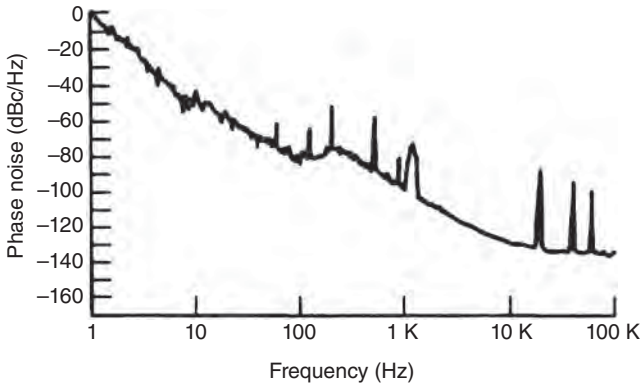


Figure 6-16 SSB phase noise of the hybrid frequency synthesizers, which is the topic of this discussion.

The measured phase noise for the system in Figure 6-16 shows quite good agreement with the prediction outside the loop bandwidth. It shows a hump between 200 and 300 Hz at about 75 dBc/Hz and a phase noise of approximately 105 dBc/Hz at 1 kHz. The reason the phase noise values on the left side between 1 and 300 Hz differ from the measurement has to do with the fact that the designer does not have enough insight into all the noise contributions, including the one provided by the DDS system. The simulation is optimistic by approximately 10 dB, but for practical operating points, the phase noise at distances of 500 Hz off the carrier are still quite acceptable and can be tweaked by changing the phase of the filter. At 1 kHz off the carrier, the simulation is off by about 5 dB, meaning that the simulation is slightly too optimistic. At 10 kHz, the simulation is too pessimistic. At 20 kHz, the simulation agrees with the measurement, and further out, the measurement was limited by the test equipment. The

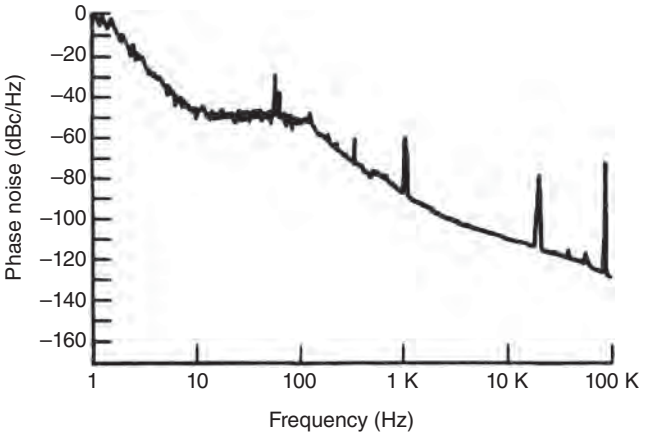


Figure 6-17 Phase noise of the English-made Lowe model HF150 single-loop synthesizer as it drives the first mixer. Its phase noise is significantly higher than the approach demonstrated here. Note that the discrete spurs below 100 Hz are small compared with previous measurements.

measured area between 1 and 10 Hz is questionable because of the 50-dB jump in one decade. This area is referred to as *random walk*. The area between 10 and 100 Hz still has 40-dB decay, which is also on the high side, while the area between 100 Hz and 10 kHz seems reasonable. It is useful to compare this with another synthesizer approach. We look at the Lowe HF150 receiver's phase noise in Figure 6-17. It is significantly worse in all areas and also uses only a single VCO design. Figure 6-18 shows a Rohde & Schwarz multiloop synthesizer model SMK. Its measured phase noise is not that far from the synthesizer approach used in the hybrid synthesizer detailed here.

After "polishing" the loop filter, Figure 6-19 shows the synthesizer phase noise of our hybrid frequency synthesizer. For those interested in the transient response of the synthesizer, Figure 6-20 shows the switching time of the synthesizer. After 5.11 ms we can estimate a locking error of less than 1°. There is also no ringing on the response curve. Finally, since the "power supply" is an important issue, Figure 6-21 shows a dc voltage supply for

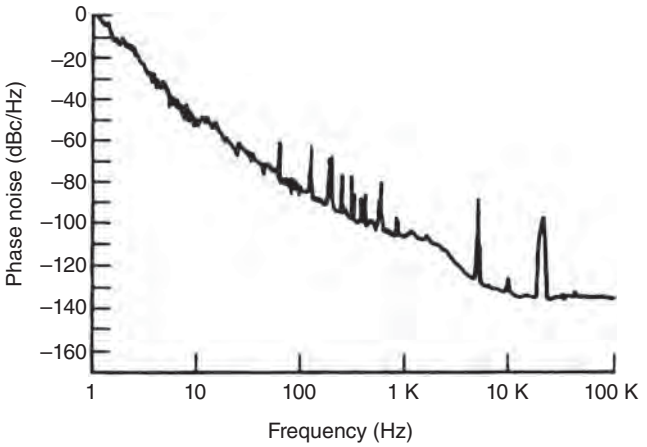


Figure 6-18 Measured SSB phase noise of the Rohde & Schwarz high-performance multiloop synthesizer model SMK. *Note:* In all cases, the reference oscillator was the Hewlett-Packard HP8662. Therefore, measurements above 20 kHz off the carrier were limited by the test setup. The actual phase noise further out may be better.

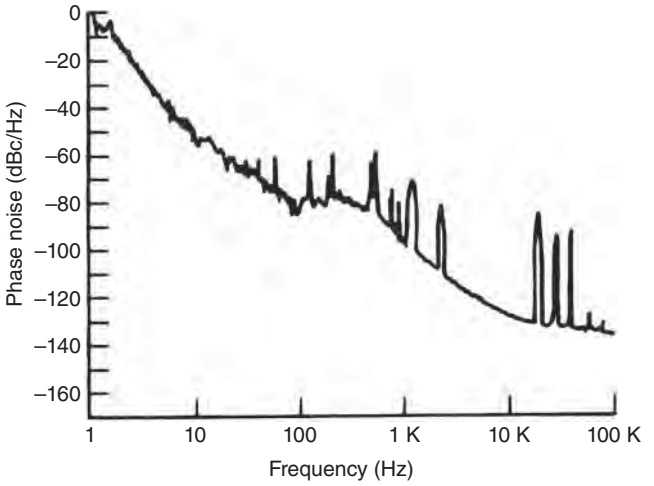


Figure 6-19 Measured phase noise of our hybrid synthesizer. The combination of the filters was optimized to reduce the overshoot, as shown in Figure 6-15. This "correction" has changed the far-out phase noise somewhat, and due to the higher VCO gain, the diodes are slightly more noisy.

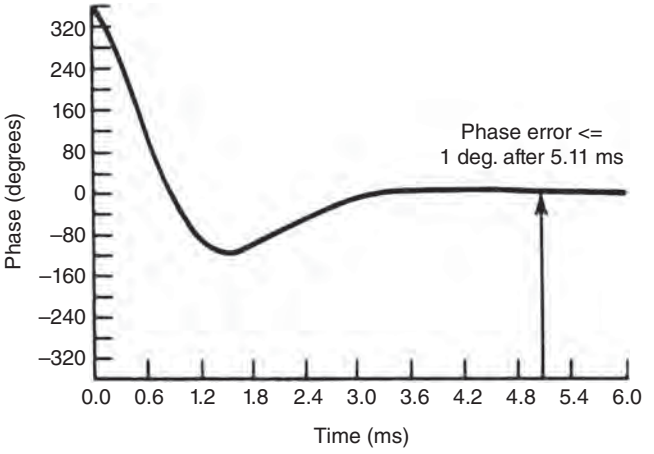


Figure 6-20 Switching time of the synthesizer. After 5.11 ms, phase/frequency error can be estimated to be less than 1°.

the synthesizer including the generation of the 28 V. It is based on an ITT TV IC, which generates a stabilized, regulated, and temperature-compensated voltage.

6-4 SUMMARY

In designing this hybrid synthesizer, a combination of two technologies has made it possible to design and build a high-performance synthesizer that meets today's requirement for purity and acceptable switching speed. The switching speed can be increased by a factor of 10–30 by going to a type 2 fifth-order loop at the expense of more components.

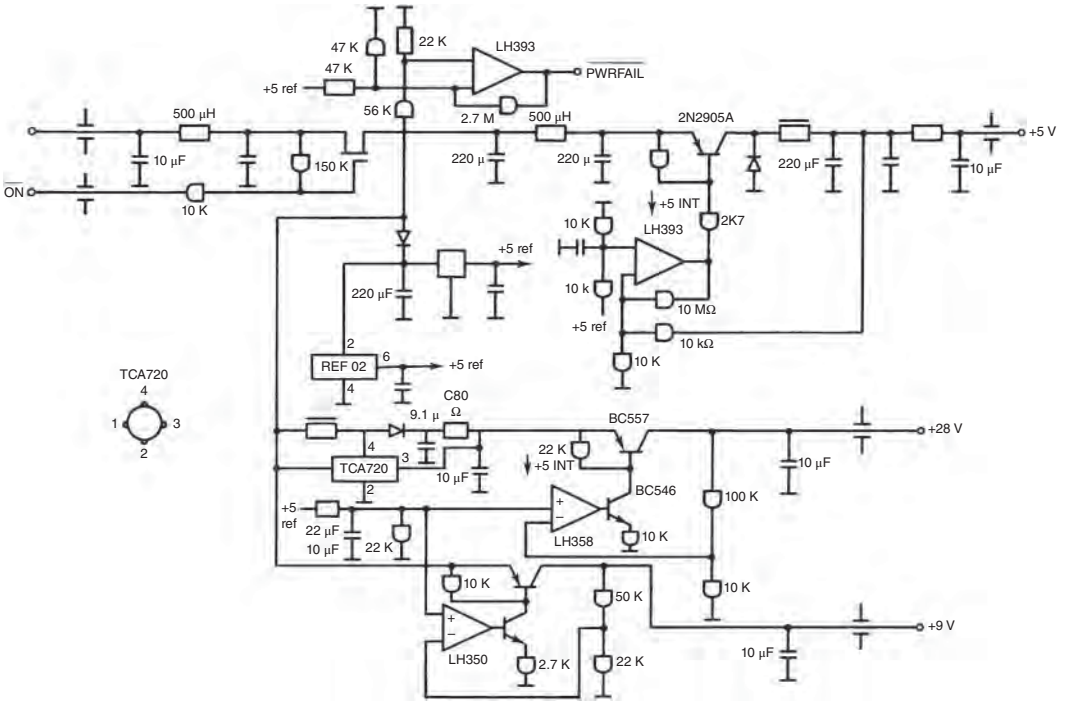


Figure 6-21 The dc power supply voltage for the synthesizer, including generation of the 28 V. It is based on an ITT TV IC, which generates a stabilized, regulated, and temperature-compensated voltage.

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Ulrich L. Rohde, Enrico Rubiola, and Jerry C. Whitaker.
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APPENDIX A

MATHEMATICAL REVIEW

A-1 FUNCTIONS OF A COMPLEX VARIABLE

Definition:

$$\sqrt{-1} = i \text{ or } j \quad i^2 = -1 \quad j^2 = -1$$

i or j is also used to indicate reactive components in electrical circuits; i is used in nonelectrical work. A complex number such as

$$p = x + j\,y \tag{A-1}$$

or

$$p = 4 + j\,5$$

can be shown in the complex plane as in Figure A-1. This is called the *rectangular form*. The magnitude M, as well as the direction or angle θ, can be computed from

$$M = \sqrt{x^2 + y^2} \tag{A-2}$$

or

$$M = \sqrt{16 + 25} = 6.40$$

and

$$\theta = \arctan \frac{y}{x} \tag{A-3}$$

or

$$\theta = \arctan \frac{5}{4} = 51.34°$$

This is called the *polar form*. The conversion from one form to the other is achieved by

$$x = M \cos \theta \tag{A-4}$$

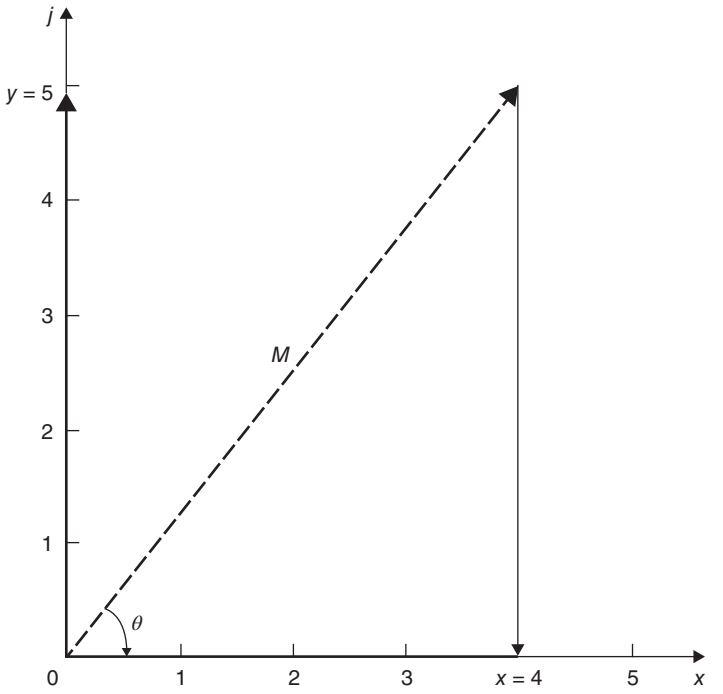

Figure A-1 Complex plane showing a complex number as the sum of two components.

$$y = M \sin\theta \tag{A-5}$$

and

$$p = M(\cos\theta + j\sin\theta) \tag{A-6}$$

This is the same as

$$p = M\exp(j\theta) \tag{A-7}$$

as

$$p = M(\cos\theta + j\sin\theta)$$

We can expand both $\sin\theta$ and $\cos\theta$ into a series.

$$\sin\theta = \theta - \frac{\theta^3}{3!} + \frac{\theta^5}{5!} - \frac{\theta^7}{7!} + \cdots \quad |x| < \infty, \quad x = \text{radians} \tag{A-8}$$

$$\cos\theta = 1 - \frac{\theta^2}{2!} + \frac{\theta^4}{4!} - \frac{\theta^6}{6!} + \cdots |x| < \infty, x = \text{radians} \tag{A-9}$$

Using Euler's theorem, it can be shown that adding the power series together results in the expansion series for e^{θ}.

Some other useful conversion equations are

$$\sin\theta = \frac{y}{\sqrt{x^2 + y^2}} = \frac{\exp(j\theta) - \exp(-j\theta)}{2j} = \text{Im}\{\exp[j(\theta)]\} \tag{A-10}$$

$$\cos\theta = \frac{x}{\sqrt{x^2 + y^2}} = \frac{\exp(j\theta) + \exp(-j\theta)}{2} = \text{Re}\{\exp[j(\theta)]\} \tag{A-11}$$

The FORTRAN computer language allows the use of complex mathematics, whereas the BASIC language does not permit such easy conversions.

Table A-1 lists operations that are useful in dealing with complex mathematics.

A-2 COMPLEX PLANES

The complex number

$$p = x + j\,y$$

was pictured as a point located x units to the right and y units up from the zero point. Any complex number whose real and imaginary parts are given can be located as a point in the xy-plane. It has become conventional in mathematics to call the variables x and y and call z the resulting complex number. As this book deals mainly with engineering problems rather than mathematics, we have substituted p for z.

Any complex number z consists of a real part x and an imaginary part y and occupies a definite point in the complex plane. The particular plane used to plot z values will therefore be called the z-plane or complex impedance plane. If we had chosen to stay with the previously used p, we could have called this the p-plane.

As we have more values of x and y as they are connected together with a mathematical function, we will see that any line in the z plane is actually a chain of connective points. If the function $F(x,y)$ is known, the graph of the function can be presented.

In generating maps, several methods of projection are used, some of which are to show the real distance between any given points and some of which are chosen to give the correct surface of an area. Depending on the projection used, the resulting image looks different while still providing the same basic information. If one is not familiar with a particular area because of the difference in projection methods, it will seem that there is no similarity, and the same area can look so different that it is hard to think of the two projections as being the same.

Apparently, it is desirable to have more than one particular projection or plane. We can now use this assumption in mathematics, and we will create an additional plane, the s-plane. The s-plane will be drawn with vertical and horizontal lines in the same way as is done for the z-plane, but the coordinates of the point locations will be given as σ units to the right or left and ω units up or down from the zero reference. In mathematics, the letters u and v are used at times, but since we want to solve engineering problems rather than mathematics, and since this is only a question of whether or not one agrees to a certain abbreviation, we will use the term "s-plane" and stay with the nomenclature, since this technique will be used for the Laplace transformation, where it is used this way. We therefore define

$$s = \sigma + j\,\omega \tag{A-12}$$

By using the identity

$$s = f(z) \tag{A-13}$$

we can transform one plane to the other once we know the particular function.

Let us try a simple example. If

$$s = \frac{1}{z} \tag{A-14}$$

or

$$s = \frac{1}{x + j\,y} = \frac{x - j\,y}{(x + j\,y)(x - j\,y)} \tag{A-15}$$

and

$$s = \sigma + j\,\omega = \frac{x - j\,y}{x^2 + y^2} \tag{A-16}$$

Table A-1 Operations for complex mathematics.

Rectangular to Polar

```
100 R = SQR(A*A + B*B)
110 S=0
120 IF R = 0 Then 170
130 S = ACS(A/R)
140 IF B < 0 Then 170
150 B = S
160 Go to 180
170 B = –S
180 A = R
190 Return
```

Note: X,Y are positional parameters
X – A
Y - B
A/B → Input
R/S → Output → A/B

Polar to Rectangular

```
100 A = R*COS(S)
110 B = R*SIN(S)
120 R = A
130 S = B
140 Return
```

Note: R,S are positional parameters

R – R
S - S

Multiplication

```
100 A3 = Al * A2 – Bl * B2
110 B3 = Al * B2 + A2 * B1
120 Return
```

Arrays A(l,2)B(l,2)C(l,2)

Note: A, B, C are positional parameters
A(l,1)- Al R
A(l,2) - Bl I rectangular
B(l,1) - A2 R
B(l,2) - B2 I rectangular
C(1,1) - A3 Real | Product rectangular
C(l,2) - B3 Imag |

Division

```
100 B3 = A2 * A2 + B2 * B2
110 IF B3 <>Then 140
120 Print "Error - Denominator = O"
130 End
140 A3 =(Al * A2 + Bl * B2)/B3
150 B3 = (A 2 *B1 - Al * B2)/B3
160 Return
```

Arrays A(l,2)B(l,2)C(l,2)

Note: A, B, C are positional parameters

A(l,1) - Al) | Both inputs rectangular
A(l,2) - Bl |
B(l,l) - A2 |
B(l,2) - B2 |
C(l,1) - A3 | Output rectangular
C(l,2) - B3 |

Complex Number Raised to a Complex Power

```
100 A = Al
110 B = Bl
120 GOSUB 240
130 IF R = 0 Then 210
140 R = LOG(R)
150 Zl = A2 * R - B2 * S
160 Z2 = A2 * S + B2 * R
170 Zl = Exp(Zl)
180 A3 = Zl * COS(Z2)
190 B3 = Zl * SIN(Z2)
200 Return
```

Arrays A(l,2) B(l,2) C(l,2)

Note: A, B, C are positional parameters

A(l,1) - Al) | both inputs rectangular
A(l,2) - Bl |
B(l,1) - A2 |
B(l,2) - B2 |
C(l,1) - A3} | output rectangular
C(l,2) - B3 |

Table A-1 (*Continued*)

```
210 A3 = 0
220 B3 = 0
230 Return
240 R = SQR(A * A + B & B)
250 S = 0
260 IF R = 0 Then 300
270 S = ACS(A/R)
280 IF > B = > 0 Then 300
290 S = -S
300 Return
```

Logarithm of a Complex Number to a Complex Base

```
100 GOSUB 190                                   Arrays A(l,2) B(l,2)
110 IF Rl < > 0 or R2 < > 0 Then 140
120 Print "Error - Complex No. = 0"
130 End                                 Note:   A, B, X, Y are positional parameters
140 Rl = LOG(Rl)
150 R2 = LOG(R2)                                A(l,1) - Al     X - R3
160 R3 = Rl/R2                                  A(l,2) - Bl     Y- S3
170 S3 = Sl - S2                                B(l,1) - A2
180 Return                                      B(l,2) - B2
190 Rl = SQR(Al * Al + Bl * B1)
200 R2 = SQR(A2 * A2 + B2 * B2)                 Both inputs:    rectangular
210 Sl = 0                                      Output:         polar
220 S2 = 0
230 IF Rl = 0 or R2 = 0 Then 290
240 Sl = ACS(Al/Rl)
250 S2 = ACS(A2/R2)
260 IF Bl = >0 or B2 = >0 Then 290
270 Sl = -Sl
280 S2 = -S2
290 Return
```

Sinh

```
100 B2 = Exp(-Al)                               Arrays A(l,2) B(l,2)
110 A2 = -0.5 * COS(Bl) * (B2 - 1/82
120 B2 = 0.5 * SIN(Bl) * (B2 + 1/82)
130 Return                              Note:   A, B are positional parameters
                                                A(l,l} - Al
                                                A(l,2) - Bl
                                                B(l,1) - A2
                                                B(l,2) - B2
```

Cosh

```
100 B2 = Esp (Al)                               Arrays A(l,2) B(l,2)
110 A2 = 0.5 * COS(Bl} * (l/82 + B2)
120 B2 = -0.5 * SIN(B1) * (1/B2 - 82)
130 Return                              Note:   A, B are positional parameters
                                                A(l,1) - Al
                                                A(l,2) - Bl
                                                B(l,l) - A2
                                                B(l,2) - B2
```

Table A-1 (*Continued*)

Tanh

```
100 Zl = Exp(2 * Al)                                  Arrays A(l,2) B(l,2)
110 Z2 = 1/Zl
120 B2 = (Zl + 22) * 0.5 + COS(2 * B1)
130 IF ABS(B2) > l.0E-12 Then 160
140 Print "Error - TANH is infi-
  nite"
150 End                                  Note:        A, B are positional parameters
160 A2 = (Zl - 22)4 * 0.5/B2
170 B2 = SIN(2 * Bl)/B2                               A(l,l) - Al Input
180 Return                                            A(l,2) - Bl rectangular
                                                      B(l,l} - A2 Output
                                                      B(l,2) - B2 rectangular
```

Arc sinh

```
100 A2 = (1 - B1) * (1 - Bl) + Al * Al                Arrays A(l,2) B(l,2)
110 B2 = SQR(A2 + 4 * B1)
120 A2 = SQR(A2)                         Note:        A, B are positional parameters
130 21 = 0.5 * (A2 + B2)
140 22 = 0.5*(A2 - B2)                                A(l,1) - Al
150 B2 = -ASN(Z2)                                     A(l,2) - Bl
160 A2 = WG(Z1 + SQR(ABS(Z1 * Zl - 1)))               B(l,1) - A2
170 Return                                            B(l,2) - B2
```

Arc cosh

```
100 GOSUB 150                                         Arrays A(l,2) B(l,2)
110 Z2 = A2
120 A2 = -B2                             Note:        A, B are positional parameters
130 B2 = Z2
140 Return                                            A(l,1) - Al
150 A2 =(Al + l) * (Al + 1) + Bl * B1                 A(l,2) - Bl
160 B2 = SQR(A2 - 4*Al)                               B(l,l} - A2
170 A2 = SQR(A2)                                      B(l,2) - B2
180 Zl = 0.5 * (A2 + B2)
190 Z2 = 0.5 * (A2 - B2)
200 A2 = ACS(Z2)
210 B2 = - LOG(Zl + SQR(ABS(Zl * Z4 - 1)))
220 Return
```

Arc tanh

```
100 A2 = Al* Al + Bl * Bl                             Arrays A(l,2) B(l,2)
110 IF A2 < > 1 Then 170
120 IF ABS(Al) < >Then 150               Note:        A, B are positional parameters
130 Print "Error -ARCTANH not defined for Com-        A(l,1) - Al
  plex No. =1 or -1"
                                                      A(l,2) - B1
140 End                                               B(1,1) - A2
150 B2 = PI/4                                         B(l,2) - B2
160 Go to 180
170 B2 = 0.5 * ATN(2 * B1/(1 - A2))
180 A2 = -0.25 * LOG((A2 – 2 * Al + 1)/ (A2 + 2 * Al + 1))
190 Return
```

then

$$\sigma = \frac{x}{x^2 + y^2}\omega = \frac{-y}{x^2 + y^2} \tag{A-17}$$

This transform was fairly simple and straightforward and for any given pair of values for x and y we can find the corresponding σ and ω values.

An example using an inductor-capacitor (LC) oscillator is given in the following text.

A-2-1 Functions in the Complex Frequency Plane

The frequency response of a network or the steady-state response to a sinusoidal input is directly related to the transfer function of the network. It is important to make sure that the waveform of the signal applied to the electrical circuit is really sinusoidal. The steady-state response assumes sinusoidal waveforms, and an analysis of the response to a nonsinusoidal waveform is better analyzed with the mathematical aid of the Fourier series and integral, which then leads to the Laplace transformation and the inverse Laplace transformation. The following discussion covers the transfer functions of several useful networks with $s = j\omega$ and $\sigma = 0$. Probably the most interesting transfer characteristics for our phase-locked loop applications are the ones for the simple resistor-capacitor (RC) network and the ones for the compensated RC network. The simple RC network shown in Figure A-2 is described by

$$F(s) = \frac{1}{sCR + 1} \tag{A-18}$$

The magnitude of the frequency response is

$$|F(j\omega)| = \frac{1}{\sqrt{(1 + \omega^2 R^2 C^2)}} \tag{A-19}$$

and the phase is

$$\theta(\omega) = -\arctan(\omega CR) \tag{A-20}$$

For the type 2 second-order loop with an active filter, *RC* lag network shown in Figure A-3 is commonly used. Its frequency response is

$$F(j\omega) = \frac{1 + j\omega R_2 C}{1 + j\omega C(R_1 + R_2)} \tag{A-21}$$

and the magnitude of the frequency response is

$$|F(j\omega)|^2 = \frac{1 + \omega^2 R_2^2 C^2}{1 + \omega^2 C^2 (R_1 + R_2)^2} \tag{A-22}$$

The phase is

$$\theta(\omega) = \arctan(\omega R_2 C) - \arctan[\omega C(R_1 + R_2)] \tag{A-23}$$

The phase and frequency response are sketched in Figure A-4.

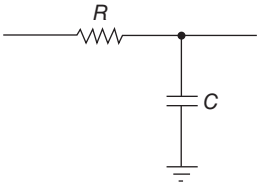

Figure A-2 Simple RC network.

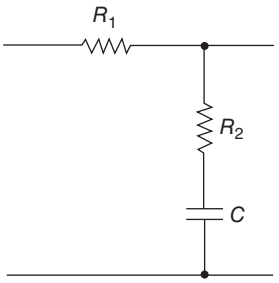

Figure A-3 RC lag filter.

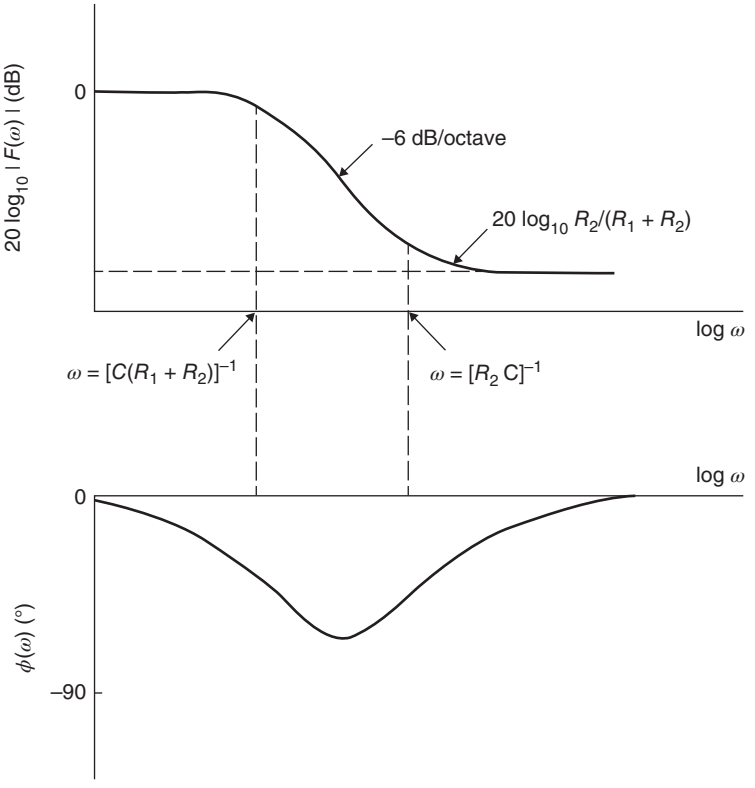

Figure A-4 Phase and frequency response of the lag filter in Figure A-3.

The general transfer characteristics of the networks we are dealing with are defined as

$$F(s) = \frac{A(s)}{B(s)} \tag{A-24}$$

and $F(s)$ is the ratio of two polynomials in s. In an expanded form this reads

$$F(s) = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0} \tag{A-25}$$

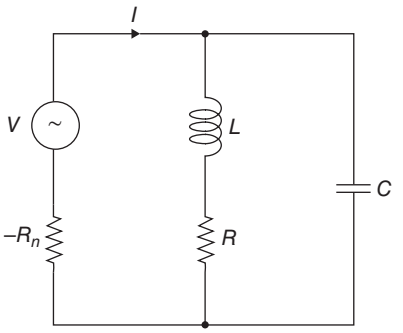

Figure A-5 Tuned circuit with negative resistor.

$m < n$ is a practical network. A polynomial may be factored and expressed as a product of binomials.

$$F(s) = \frac{a_m(s - z_m)(s - z_{m-1}) \cdots (s - z_1)}{b_n(s - p_n)(s - p_{n-1}) \cdots (s - p_1)} \tag{A-26}$$

Roots of the numerator are called *zeros*, whereas roots of the denominator are called *poles*. A zero occurs at a frequency where no power is transmitted through the complex network; a pole occurs at a frequency where no power is absorbed by the network. There are m zeros and n poles. The network is said to be of nth *order*; the order is equal to the number of poles, which is the same as the degree of the denominator.

Now let us try an example. Figure A-5 shows a tuned parallel circuit consisting of the capacitor C, the inductance L, the loss resistor R, and the negative resistor R_n, which is generated by an amplifier as dealt with in Chapter 4. The equation for this can be written

$$I = V\frac{1 + sCR + s^2LC}{R - R_n + s(L - CRR_n) - s^2R_nCL} \tag{A-27}$$

The denominator provides us with the characteristic equation, which will be set to zero.

$$R - R_n + s(L - CRR_n) - s^2R_nCL = 0 \tag{A-28}$$

This is a quadratic equation, and its roots are

$$p_{1,2} = \frac{L - CRR_n}{2R_nCL} \pm \sqrt{\left(\frac{L - CRR_n}{2R_nCL}\right)^2 + \frac{R - R_n}{R_nCL}} \tag{A-29}$$

and as $s = \sigma \pm j\omega$, we finally obtain

$$\sigma = -\frac{R}{2L} + \frac{1}{2R_nC} \tag{A-30}$$

and

$$\omega_0 = \sqrt{\frac{1}{LC} - \frac{R}{R_nLC} + \sigma^2} \tag{A-31}$$

We can define this result in three cases:

(1) $\sigma > 1$; any initial oscillation will cease rapidly.
(2) $\sigma = 0$; this is the case of a lossless circuit, in which the losses generated by R are exactly compensated by R_n.

(3) $\sigma < 1$; in this case we have oscillation that will grow in amplitude until some saturation or limiting effect occurs in the device that produces the negative resistance. Circuits of this kind are called *negative resistance oscillators*.

Let us return now to the general transfer characteristic of the system and determine the stability from the Bode diagram as a graphical method rather than from the characteristic equation of the system under closed-loop conditions, because in complicated systems this will become very difficult. In Chapter 1 we analyzed higher-order loops. However, we will now think what the transfer characteristic of a network in the form of a polynomial expression can be. For phase-locked-loop circuits, this function would describe an *n*th-order phase-locked loop (PLL).

To review: roots of the numerator are called zeros and roots of the denominator are called poles. There are m zeros and n poles. The network is said to be of *n*th order. The order is equal to the number of poles, which is the same as the degree of the denominator. What does this mean for phase-locked-loop circuits? Phase-locked-loop circuits are generally categorized into systems of a certain type and of a certain order. The type of phase-locked loop indicates the number of integrators, and as we have seen before, a type 1 first-order loop is a loop in which the filter is omitted and the loop therefore has only one integrator, the voltage-controlled oscillator (VCO). For good tracking, a large dc gain is needed and as the type 1 first-order loop has no filter, the bandwidth also must be large. It is apparent that narrow bandwidth and good tracking are incompatible for first-order loops—the principal reason why they are not used very often.

This network has only one pole. If we use a phase-locked loop with an active integrator, we now cascade two integrators, the VCO and the active integrator, and the loop automatically becomes a type 2 loop. Depending on the filter, we will have a type 2 second-order, third-order, or up to *n*th-order system. The consequences of the higher order are explained in Section A-3, where we deal with stability and use the Bode diagram to analyze the stability. On very rare occasions, loops with three integrators have been built, but since they find no application in frequency synthesizers, they are not dealt with here.

A-3 BODE DIAGRAM

In Chapter 1, in dealing with the question of stability, the Bode diagram was used. It is an aid to determining loop stability by plotting the amplitude and phase characteristic of the transfer function of a system and applying several criteria.

There are several ways in which stability can be analyzed. The Nyquist stability analysis requires a fairly large amount of calculation, and as most of the information available about phase-locked loops is based on an approximation, it is difficult to obtain all the necessary information.

Considerable information about the behavior of a phase lock can be obtained by determining the location of poles in the closed-loop response. These poles change their locations as the loop gain changes. The path that the pole traces in its migrations in the s-plane is known as the root-locus plot. This method again requires substantial mathematical effort because the roots of the denominator have to be determined with a computer. We will see that applying the Bode diagram is a fairly easy and convenient way of forecasting the stability of a loop by analyzing the open-loop gain.

First let us take a look at Figure A-6, which contains all the necessary loop components.

The loop, according to this block diagram, consists of the VCO, a dc amplifier with gain K_2, two lag filters called F_3 and F_4, which are determining τ_1 and τ_2, and the two cutoff frequencies F_6 and F_7. F_6 refers to the cutoff frequency of the operational amplifier used for the active filter, and F_7 is the 3-dB bandwidth that is generated by possible series resistors and bypass capacitors in the system. These various frequencies allow the simulation of influences as they actually occur. In addition, we saw in Chapter 1 that it is possible to use elliptic LC filters for high attenuation, and we also dealt with them in Sections A-4–A-7. The Cauer or elliptic low-pass filter can be described by providing the poles and zeros, the order, and the cutoff frequency of the filter. M refers to the order, F_5 refers to the cutoff frequency, and ω and σ refer to the transfer function of the filter. In order to be able to describe a complex system, we will allow for a mixer, and we also have the divider and the phase detector included.

In our first example, we are trying to simulate a first-order loop. The first-order loop has no active integrator and the loop bandwidth is determined by K_0K_θ/N; all other values, F_1 and F_7 are set so high that they will have no influence. Therefore, our next drawing, Figure A-7, shows the ideal first-order open-loop frequency response. The phase is $-90°$ and constant as a function of frequency, the gain marked V on the plot has a slope of -6 dB/octave,

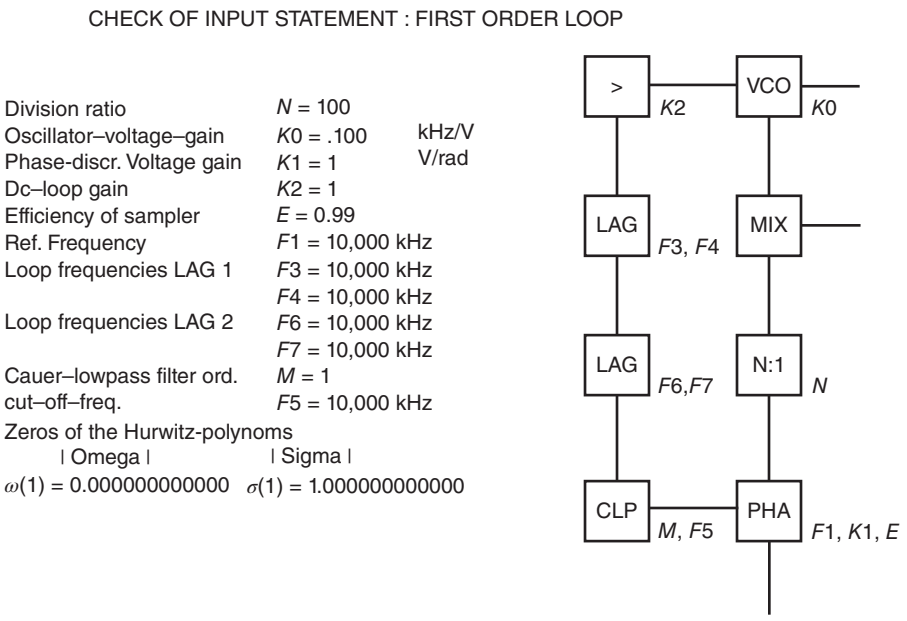

Figure A-6 Block diagram of a universal phase-locked loop system used in the computer program for high-order phase-locked loops.

and our open-loop bandwidth is 1 kHz. Note that the frequency display on the x-axis is logarithmic, and the gain is expressed in decibels. This is an ideal situation, and there is no question of stability, as there is only 90° phase shift. The very moment we add a simple filter to the first-order loop, it becomes a type 1 second-order loop, which refers to one integrator and a simple RC network. As long as the following requirements are fulfilled, there is no problem with stability.

Referring to Figure A-7:

(1) The open-loop gain $A(s)$ as plotted must fall below 0 dB before the phase shift reaches 180°. A typical gain margin of +10 dB is desirable for −180°.

(2) A phase shift of less than 180° must be provided at the gain crossover frequency for $A(s)$. This is called *phase margin*. A typical phase margin of 45° is desirable.

It is possible that a loop is conditionally stable and violates the Bode criteria. However, once it meets the Bode criteria, the loop is unconditionally stable. As the type 1 first-order loop phase stays at −90°, it will always remain stable. The type 1 second-order loop has only one element for phase shifting, as seen in Figure A-8, and the phase margin at $A(s) = 0$ is sufficient. The gain margin at −180° phase is about 35 dB. Therefore, the type 1 second-order loop, as plotted, is unconditionally stable.

Next, we look at a type 1 second-order loop that has phase compensation. In the block diagram of the loop, we made allowance to indicate the phase shift introduced by various components. Rather than use the simple RC network, we now use a lag filter corresponding to the two time constants τ_1 and τ_2. The cutoff frequency determined by F_3 is set below the open-loop bandwidth of 10 kHz, and it is evident that the phase is being compensated by the introduction of the time constant calculated from F_4. This lag filter therefore increases the phase margin. At the point of 0-dB gain, we have sufficient phase margin, and even at −40-dB gain, the phase is still at about −130°. This is equal to a phase margin of about 50° (see Figure A-9).

Next, we take into consideration the finite cutoff frequency of the operational amplifier. Figure A-10 shows the Bode diagram in which the operational amplifier, used as a dc amplifier (gain $K_2 = 1$), introduces considerable phase shift. The system is still stable, and for −180° phase, the gain is about −20 dB, resulting in a 20-dB gain margin. At 0 dB, about 45° phase margin is available. The operational amplifier is responsible for a 180° phase shift.

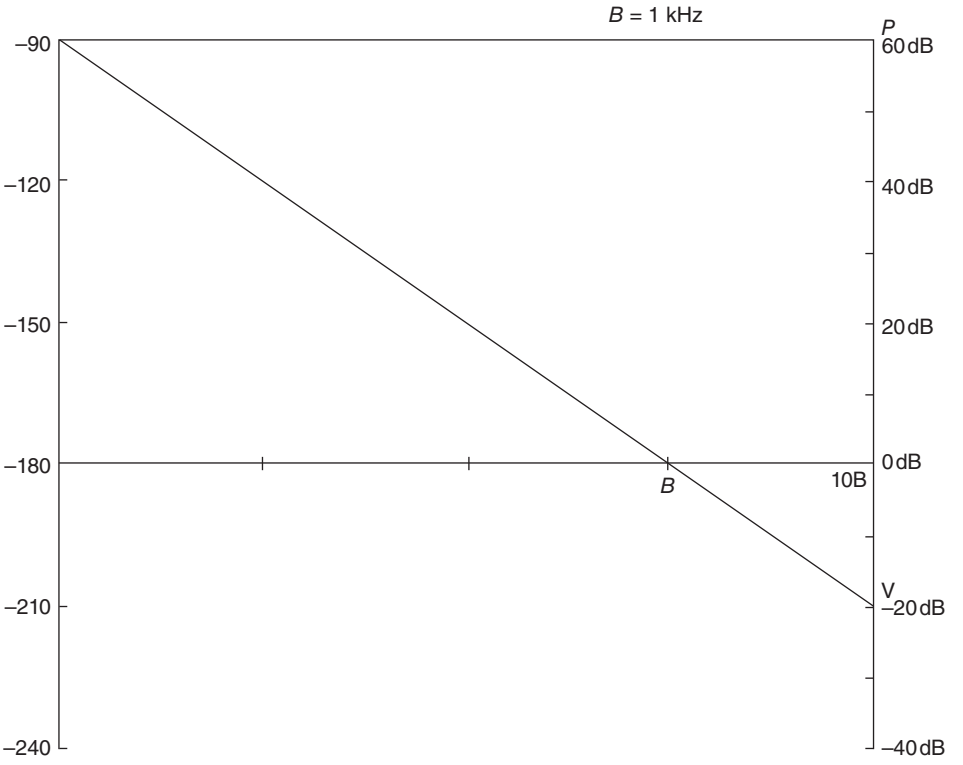

Figure A-7 Bode plot of a first-order loop; P is for phase V is for gain.

We will now look at the influence of more parameters and will plot a type 2 second-order loop. Figure A-11 shows a type 2 high-order loop with an open-loop bandwidth of 200 kHz using the lag filter with the two cutoff frequencies F_3 and F_4 (note that F_4 is smaller than F_3). F_6 describes the cutoff frequency of the operational amplifier used for the active filter.

The gain curve marked *V* starts off with 12 dB/octave due to two integrators and then, because of the effect of the lag filter, decays with 6 dB/octave. The phase margin at 0 dB gain is about 30°, and the gain margin at −180° of phase is about 7 or 8 dB. This is a stable loop.

Next, we make allowance for the low-pass filter action of the RC network generated by bypass capacitors, cutoff frequency F_7. This loop, by choosing the right F_3 and F_4 values, is stable as the phase margin at 0 dB gain is 60° and the gain margin at −180° of phase is about 40 dB (see Figure A-12).

Finally, let us take a look at Figure A-13, which shows the open-loop performance of a type 2 *n*th-order loop that contains allowance for the phase shift of the operational amplifier *RC* filtering and shows the effect of a first-order elliptic filter. This loop is no longer stable, as the gain does not fall to 0 dB while the phase is still less than −180°. It is very convenient to use a computer to generate these plots because once all the parameters are known, the Bode diagram instantaneously reveals whether a loop is stable and what parameters have to be changed to obtain the necessary phase and gain margins.

The following three traces (Figures A-14–A-16) show some in-house tools, which were generated in May 2000. Similar tools are now offered by Analog Devices, found at https://www.analog.com/adisimpll.html, and also by Texas Instruments and others.

An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops

National Semiconductor
Application Note 1001
William O. Keese
May 1996

The high performance of today's digital phase-lock loop makes it the preferred choice for generation of stable, low noise, tunable local oscillators in wireless communications applications. This paper investigates the design of passive loop filters for Frequency Synthesizers utilizing a Phase-Frequency Detector and a current switch charge pump such as National Semiconductor's PLLatinum™ Series. Passive filter design for a TYPE II third order phase-lock loop is discussed in depth, with some discussion of higher order filters included. Specific test results are presented for a GSM synthesizer design. Optimization of phase-lock loop performance with respect to different parameters is discussed.

The basic phase-lock-loop configuration we will be considering is shown in *Figure 1*. The PLL consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2315TM, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, and programmable frequency dividers. A passive filter is desirable for its simplicity, low cost, and low phase noise.

In most standard PLL's there are several design parameters which can be treated as constant values. This linear approximation provides a good estimation of loop performance. The values of the PLL filter design constants depend on the specific application. For example, Kϕ is determined by the synthesizer charge pump output current magnitude. The notation and definitions for these values along with standard units used throughout this paper are given in Table I below.

TABLE I. PLL Filter Design Constants

Kvco - (MHz/Volt)

Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

Kϕ - (mA/2πrad)

Phase detector/charge pump constant. The ratio of the current output to the input phase differential.

RFopt - (MHz)

Radio Frequency output of the VCO at which the loop filter is optimized.

Fref - (kHz)

Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

N

Main divider ratio. Equal to RFopt/Fref.

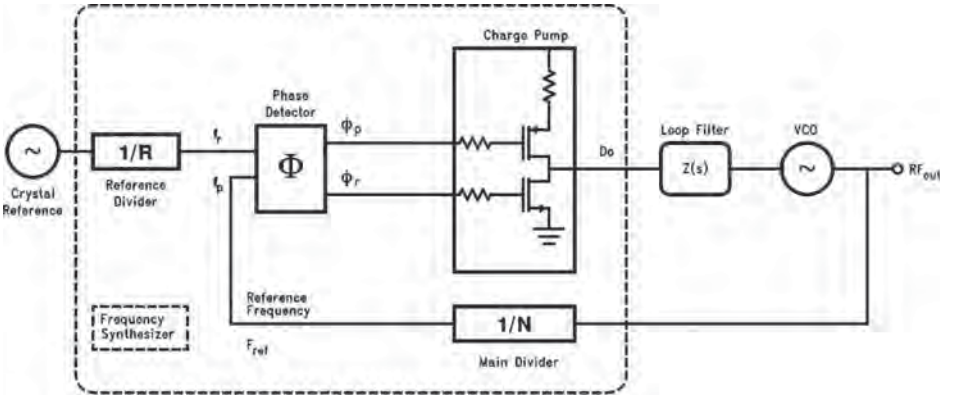

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FIGURE 1. Basic Charge Pump Phase Locked Loop

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An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops

AN-1001

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Some basic knowledge of control loop theory is necessary in order to understand PLL filter dynamics. For a more thorough treatment consult references [1] through [6]. A linear mathematical model representing the phase of the PLL in the locked state is presented in *Figure 2*. An additional integrator is needed in the transfer function for the forward gain and is usually lumped together with the VCO in the literature, references [1-4]. Using the simplified diagram in *Figure 2*, and feedback theory, one may obtain the equations for the phase transfer functions presented in Table II.

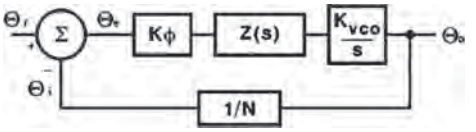

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FIGURE 2. PLL Linear Model

TABLE II. PLL Phase Transfer Functions

Forward loop gain	$G(s) = \Theta o/\Theta e$
	$= \mathbf{K\phi\ Z(s)\ Kvco/s}$
Reverse loop gain	$H(s) = \Theta i/\Theta o = \mathbf{1/N}$
Open loop gain	$H(s)\ G(s) = \Theta i/\Theta e$
	$= \mathbf{K\phi\ Z(s) Kvco/Ns}$
Closed loop gain	$\Theta o/\Theta r = \mathbf{G(s)/\ [1 + H(s)\ G(s)]}$

The standard passive loop filter configuration for a type II current mode charge pump PLL is shown in *Figure 3*. The loop filter is a complex impedance in parallel with the input capacitance of the VCO, or in other words, a driving point immitance.

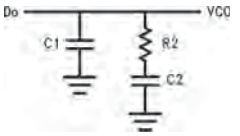

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FIGURE 3. 2nd Order Passive Filter

The phase detector's current source outputs pump charge into the loop filter, which then converts the charge into the VCO's control voltage. The shunt capacitor C1 is recommended to avoid discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. A low pass filter section may be needed for some high performance synthesizer applications that require additional rejection of the reference sidebands, known as spurs.

One method of filter design uses the open loop gain bandwidth and phase margin to determine the component values. Locating the point of minimum phase shift at the unity gain frequency of the open loop response as shown in *Figure 4* ensures loop stability. The phase relationship between the pole and zero also allows easy determination of the loop filter component values. The phase margin, ϕ_p, is defined as the difference between 180° and the phase of the open loop transfer function at the frequency, ω_p, corresponding to 0-dB gain. The phase margin is chosen between 30° and 70°. When designing for a higher phase margin you trade off higher stability for a slower loop response time and less attenuation of Fref. A common rule of thumb is to begin your design with a 45° phase margin.

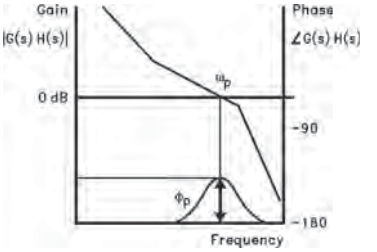

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FIGURE 4. Open Loop Response Bode Plot

The impedance of the second order filter in *Figure 3* is

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2 (C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (1)$$

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (2a) \qquad T2 = R2 \bullet C2 \quad (2b)$$

Thus the 3rd order PLL Open Loop Gain in Table II can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants Kϕ, Kvco, and N.

$$G(s) \bullet H(s)\Big|_{s=j\bullet\omega} = \frac{-Kpd \bullet Kvco\ (1 + j\omega \bullet T2)}{\omega^2\, C1 \bullet N\ (1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (3)$$

From equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in equation 4. The available phase margin therefore is proportional to the ratio of C1 and C2.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \quad (4)$$

By setting the derivative of the phase margin equal to zero as shown in equation 5,

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \quad (5)$$

the frequency point corresponding to the phase inflection point is found in terms of the filter time constants T1 and T2. This relationship is given in equation 6.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \quad (6)$$

To insure loop stability, we want the phase margin to be maximum when the magnitude of the open loop gain equals 1. Equation 3 then gives

$$C1 = \frac{Kpd \bullet Kvco \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \quad (7)$$

Therefore, if the loop bandwidth, ω_p, and the phase margin, ϕ_p, are specified, equations 1 through 7 allow us to calculate the two time constants, T1 and T2.

The formulas for T1 and T2 are shown in equations 8 and 9.

$$T1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p} \quad (8)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (9)$$

From the time constants, T1, T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 10 to 12.

$$C1 = \frac{T1}{T2} \bullet \frac{Kpd \bullet Kvco}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (10)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right) \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

Current switching noise in the dividers and the charge pump at the reference rate, Fref, may cause unwanted FM sidebands at the RF output. In wireless communications, the phase detector comparison frequency is generally a multiple of the RF channel spacing. These spurious sidebands can cause noise in adjacent channels. Additional filtering of the reference spurs is often times necessary, depending on how narrow your loop filter is. This is usually the case in today's TDMA digital cellular standards, such as GSM, PDC, PHS, or IS-54. The sub-millisecond lock times necessary for switching between channel frequencies makes a relatively wide loop filter mandatory. For these performance critical synthesizer applications placing a series resistor and a shunt capacitor prior to the VCO provides a low pass pole for more attenuation of unwanted spurs. The use of a passive loop filter eliminates the noise contributions from an op amp in an active filter. This is critical due to the strict RMS. phase error, and integrated phase noise requirements. The recommended filter configuration is shown in *Figure 5*.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log [(2\pi Fref \bullet R3 \bullet C3)^2 + 1] \quad (13)$$

Defining the additional filter time constant as

$$T3 = R3 \bullet C3 \quad (14)$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{(ATTN/20)} - 1}{(2\pi \bullet Fref)^2}} \quad (15)$$

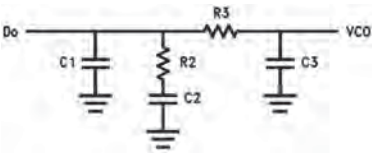

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FIGURE 5. 3rd Order Lowpass Filter

The additional pole must be lower than the reference frequency, in order to significantly attenuate the spurs, but must be at least 5 times higher than the loop bandwidth, or the loop will almost assuredly become unstable. In order to compensate for the added low pass section, the filter component values are recalculated using the new open loop unity gain frequency, ω_c, as in equation 17. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2. Note that ω_c is slightly $< \omega_p$, therefore the frequency jump lock time will increase. Although not exact, the linear assumptions used in this design technique provide suprisingly good results for loop filter bandwidths of up to 1/5 of the reference rate. The derivation of ω_c is included in the appendix.

$$T2 = 1/[\omega_c^2 \bullet (T1 + T3)] \quad (16)$$

$$\omega_c = \frac{\tan \phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \times \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan \phi \bullet (T1 + T3)]^2}} - 1 \right] \quad (17)$$

$$C1 = \frac{T1}{T2} \frac{Kpd \bullet Kvco}{\omega_c^2 \bullet N} \times \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)} \right]^{1/2} \quad (18)$$

Similar to the 2nd Order filter we have

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1 \right); \quad (11)$$

$$R2 = \frac{T2}{C2} \quad (12)$$

The only component values that need to be determined comprise the added low pass pole. Since these values are solely determined from equations 13 and 14, their values are somewhat arbitrary. It is not prudent, however to have a capacitor value for C3 which is equal to or greater than the other capacitors. As rule of thumb choose C3 $\leq$ C1/10, otherwise T3 will interact with the primary poles of the filter. Likewise, choose R3 at least twice the value of R2. When selecting C3 you must also take into account the input capacitance of the VCO tuning varactor diode which will add in parallel.

The following example is a typical synthesizer developed for the Global System Mobile (GSM) digital cellular standard using the described filter design technique. The RF channel spacing is 200 kHz, and a typical synthesizer frequency range is from 865 MHz–915 MHz. Since the addition of a low pass filter will reduce the closed loop bandwidth slightly, select an initial design value which is slightly larger than desired.

Example

$$\mathbf{Kvco} = 20\ \text{MHz/V}.$$

$$\mathbf{Kphi} = 5\ \text{mA}$$

$$\mathbf{RFopt} = 900\ \text{MHz}$$

$$\mathbf{Fref} = 200\ \text{kHz}$$

$$\mathbf{N} = \mathbf{RFopt/Fref} = 4500$$

$$\omega_{\mathbf{p}} = 2\pi * 20\ \text{kHz} = 1.256e5$$

$$\phi_{\mathbf{p}} = 45°$$

$$\mathbf{ATTEN} = 20\ \text{dB}$$

$$T1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p} = 3.29e-6$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \bullet 200e3)^2}} = 2.387e-6$$

$$\omega_c = \frac{(3.29e-6 + 2.387e-6)}{[(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6]} \times \left[\sqrt{1 + \frac{(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6}{[(3.29e-6 + 2.387e-6)]^2}} - 1\right]$$

$$\omega_c = 7.045e4$$

$$T2 = \frac{1}{(7.045e4)^2 \bullet (3.29e-6 + 2.387e-6)} = 3.549e-5$$

$$C1 = \frac{3.29e-6}{3.549e-5} \frac{(5.0e-3) \bullet 20e+6}{(7.045e4)^2 \bullet 4500} \times \left[\frac{[1 + (7.045e4)^2 \bullet (3.549e-5)^2]}{[1 + (7.045e4)^2 \bullet (3.29e-6)^2 \parallel 1 + (7.045e)^2 \bullet (2.39e-6)^2]}\right]^{1/2}$$

$$C1 = 1.085\ \text{nF}$$

$$C2 = 1.085\ \text{nF} \bullet \left(\frac{3.55e-5}{3.29e-6} - 1\right) = 10.6\ \text{nF};$$

$$R2 = \frac{3.55e-5}{10.6e-9} = 3.35\ \text{k}\Omega;$$

if we choose $R3 = 22\ \text{k}\Omega$;

then $$C3 = \frac{2.34e-6}{22e3} = 106\ \text{pF}$$

Converting the calculated numbers to standard component values gives the filter shown in the test board schematic for the synthesizer implementation, *Figure 6*.

Test results for the PLL loop filter design using a National Semiconductor LMX2315 Frequency Synthesizer are shown in the following pages. A 10 MHz crystal oscillator was used as the reference oscillator input signal. The supply voltage was 5V, and the entire current consumption, including the VCO, was <15 mA.

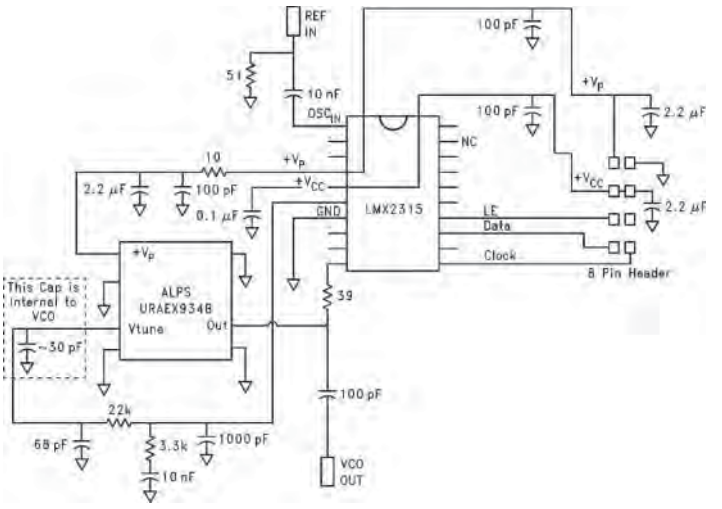

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FIGURE 6. Test Fixture Schematic

Figures 7 to *9* show HP8566 Spectrum Analyzer measurements of the RF output. The measured closed loop filter bandwidth is between 15 kHz and 17.5 kHz. The reference spurious level is ≤70 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2315. The phase noise level at 1 kHz offset in *Figure 9* is −79.5 dBc/Hz. This correlates to a phase noise floor of ≤150 dBc/Hz. The relatively flat PLL closed loop characteristics gives a measured RMS. phase error of <2°, and is also an indicator of good loop stability.

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. The HP53310A Modulation Domain Analyzer plots in *Figures 10* and *11* show the positive and negative switching waveforms for a frequency jump of 865 MHz–915 MHz. The well balanced charge pump of the LMX2315 frequency synthesizer causes the waveforms to be nearly inverted replicas of each other. Narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±500 Hz. The lock time is seen in *Figure 12* to be <500 μs for a frequency jump of 50 MHz.

CONCLUSION

An analysis of a frequency domain design technique for passive filters in charge pump phase-locked loops was presented. Measurements of a PLL designed using this method show good results in a practical synthesizer realization. The results demonstrate a high performance synthesizer in conjunction with a passive loop filter provide a fast switching, low noise frequency source for today's challenging digital wireless telecommunications standards.

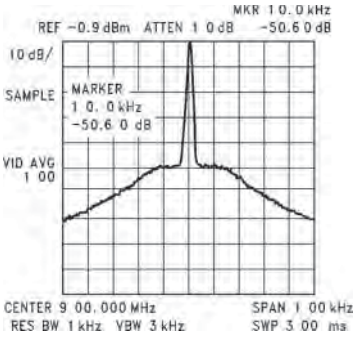

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FIGURE 7. PLL Output Spectrum 100 kHz span

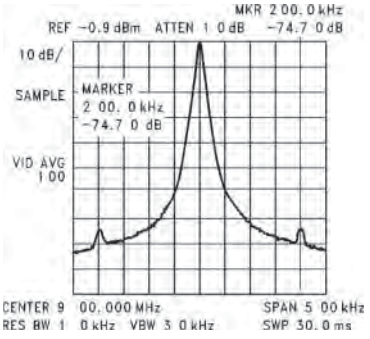

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FIGURE 8. PLL 200 kHz Reference spurs

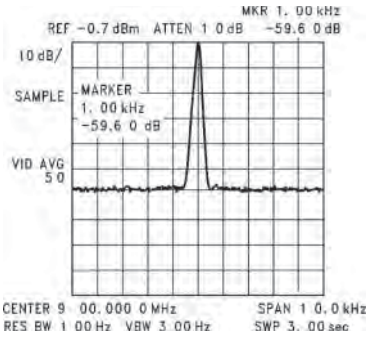

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FIGURE 9. PLL Close in Phase Noise

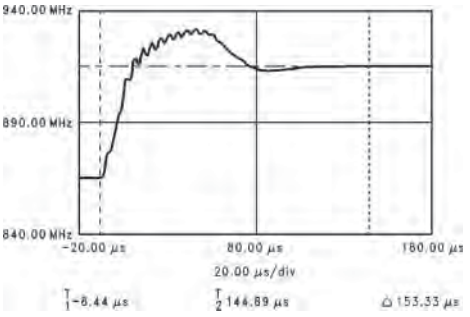

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FIGURE 10. PLL Positive Frequency Jump Waveform

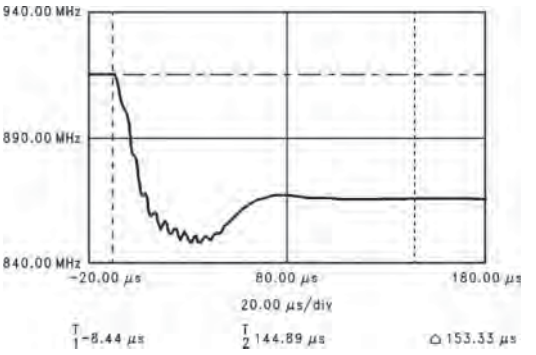

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FIGURE 11. PLL Negative Frequency Jump Waveform

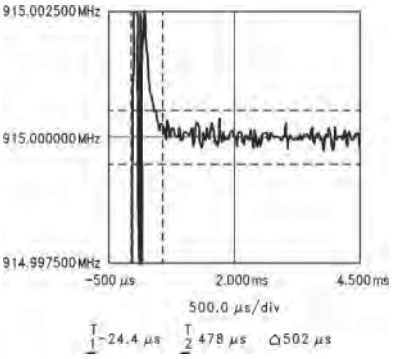

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FIGURE 12. PLL Frequency Jump Lock Time

APPENDIX

Derivation of ωc

The impedance of the loop filter shown in *Figure* 5 is

$$Z_T(s) = \frac{Z(s) \bullet \left(\frac{1}{s\,C3}\right)}{Z(s) + R3 + \left(\frac{1}{s\,C3}\right)} \tag{19}$$

where Z(s) is given by equation 1.

Knowing that $C1 \geq 10\,C3;$

and by substituting $T3 = R3 \bullet C3$

along with equations 2a, 2b.

simplifies the third order equation for the open loop gain to

$$G(s) \bullet H(s)\Big|_{s = j\bullet\omega} = \frac{-Kpd \bullet Kvco\,(1 + j\omega \bullet T2)}{\omega^2\,C1 \bullet N\,(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \bullet \frac{1}{(1 + j\omega \bullet T3)} \tag{20}$$

$$\phi(\omega) \propto (1 + \omega \bullet T2) \bullet (1 - \omega \bullet T1) \bullet (1 - \omega \bullet T3) \tag{21}$$

Similar to equation 9

$$T2 = \frac{1}{\omega^2\,(T1 + T3)} \tag{22}$$

Substituting (22) into (21) gives

$$\phi(\omega) \propto 2 - \omega^2 \bullet T1 \bullet T3 - j\omega \bullet (T1 + T3) + \frac{j}{\omega \bullet (T1 + T3)} - \frac{j\omega \bullet T1 \bullet T3}{(T1 + T3)} \tag{23}$$

Thus

$$\tan\phi = \frac{-\omega \bullet (T1 + T3) - \dfrac{\omega \bullet T1 \bullet T3}{(T1 + T3)} + \dfrac{1}{\omega \bullet (T1 + T3)}}{2 - \omega^2 \bullet T1 \bullet T3} \tag{24}$$

Assuming $$\omega^2 \bullet T1 \bullet T2 \ll 2 \tag{25}$$

After some manipulation we arrive at the characteristic equation

$$\omega^2 + \omega \frac{2 \tan\phi \bullet (T1 + T2)}{[(T1 + T3)^2 + T1 \bullet T3]} - \frac{1}{(T1 + T3)^2 + T1 \bullet T3} = 0 \tag{26}$$

Taking the negative root, and multiplying through gives the expression for the closed loop bandwidth, ω_c, equation (20).

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right]$$

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[1] Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design,* Prentice-Hall, 1983

[2] Egan, W.F., *Frequency Synthesis by Phase Lock,* John Wiley & Sons, 1981.

[3] Best, Roland E., *Phase-Locked Loops Theory, Design, and Applications,* 2nd ed., McGraw-Hill Inc, 1993.

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[5] Gardner, F.M., *Charge-Pump Phase-Lock Loops,* IEEE Trans. Commun., vol. COM-28, pp 1849–1858, Nov 1980

[6] Barker, Cynthia, *Introduction to Single Chip Microwave PLLs,* National Semiconductor Application Note, AN885, March 1993

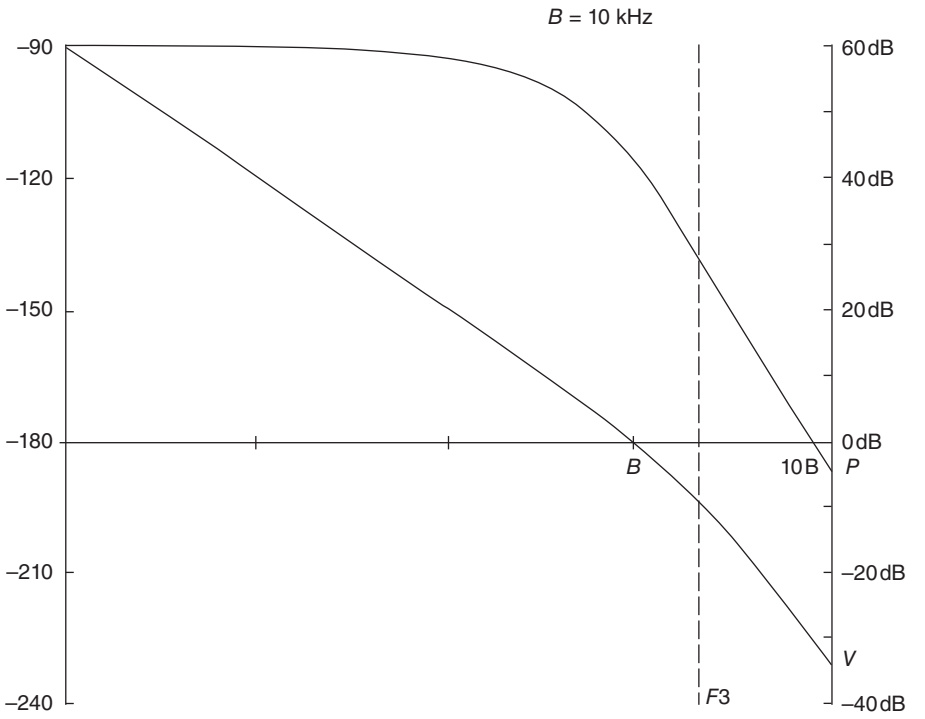


Figure A-8 Type 1 second-order loop with simple RC filter.

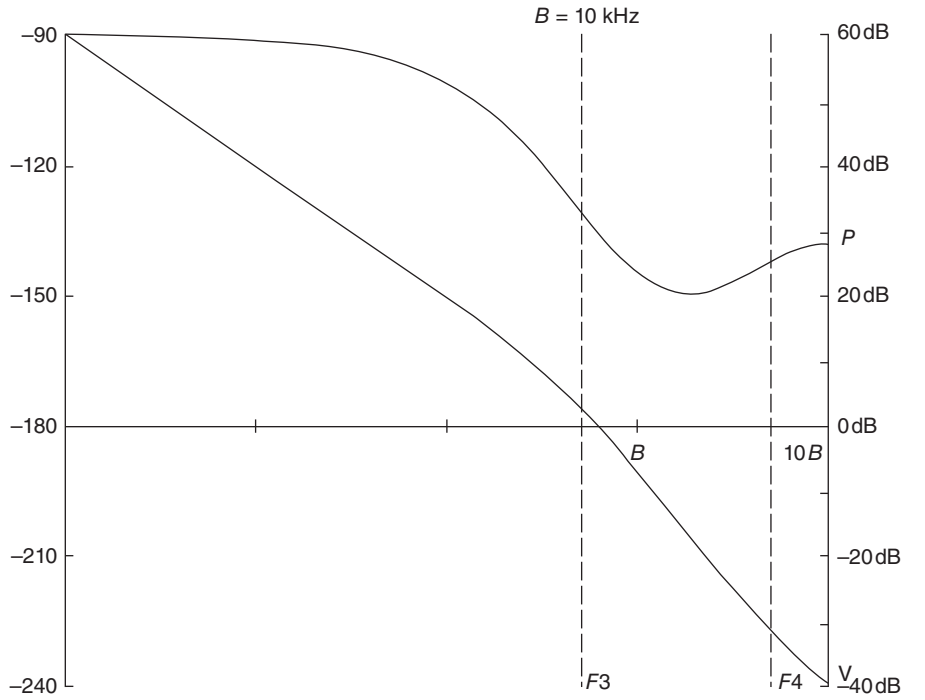


Figure A-9 Type 1 second-order loop taking the phase shift of an operational amplifier into consideration.

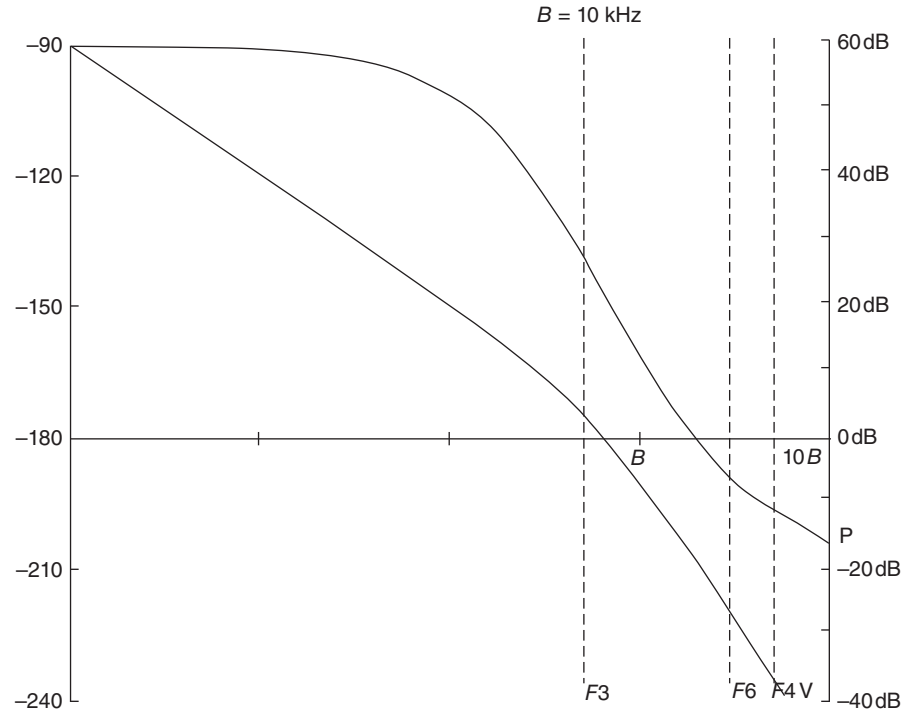


Figure A-10 Type 1 second-order loop with the time constants expressed in frequencies F_3 and F_4, as well as the additional phase shift caused by an operational amplifier.

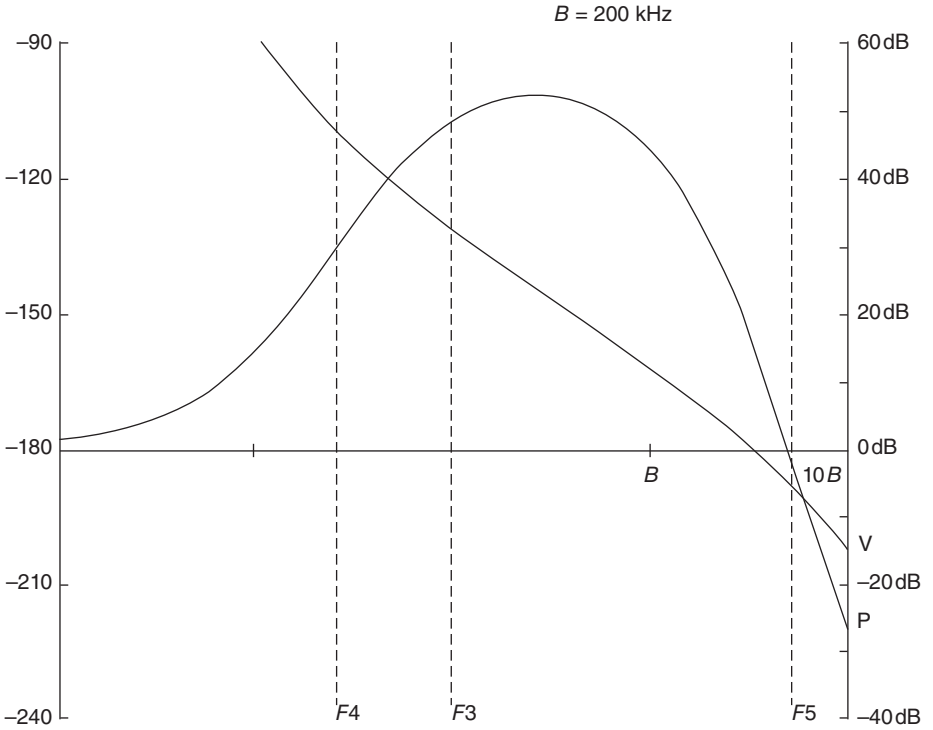


Figure A-11 Type 2 second-order loop showing the influence of the operational amplifier (F_6).

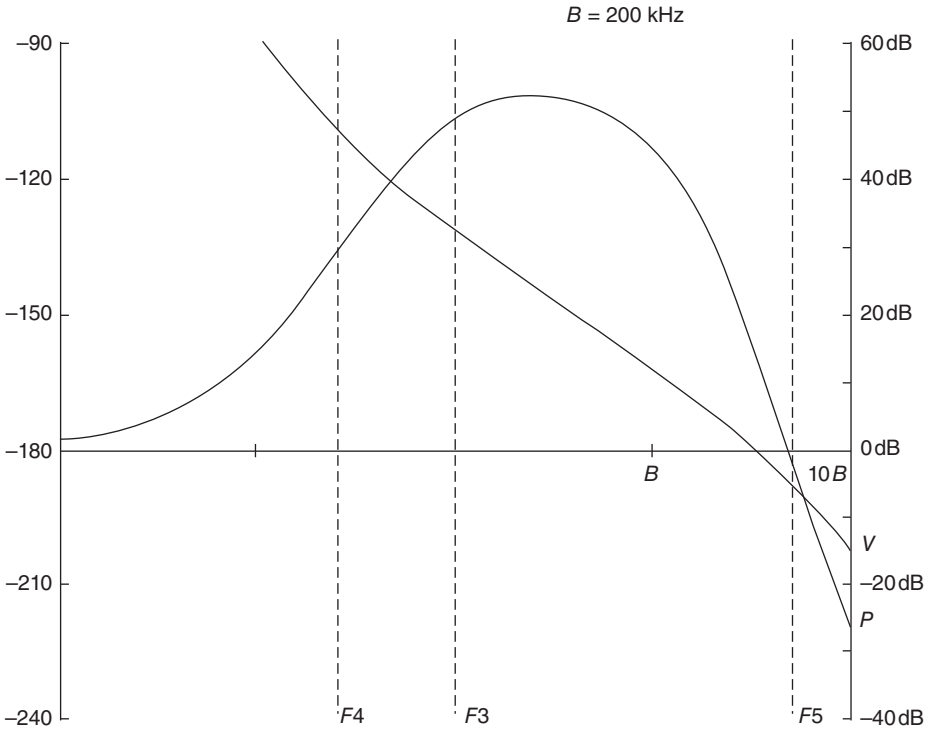


Figure A-12 Type 2 second-order loop in which the two cutoff frequencies F_3 and F_4, the phase shift and cutoff frequencies of the operational amplifier F_6, and an additional *RC* network (F_7) are incorporated.

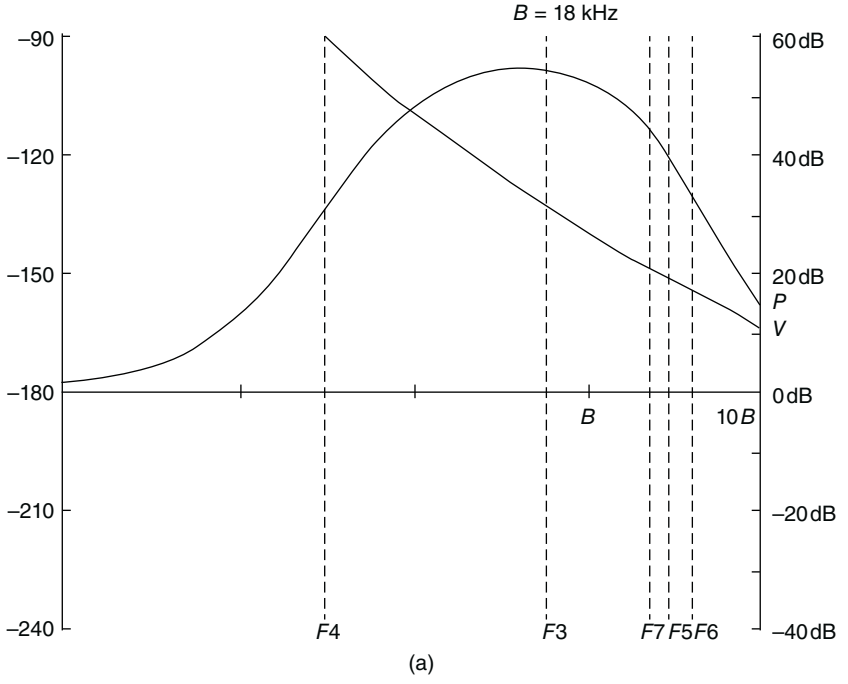
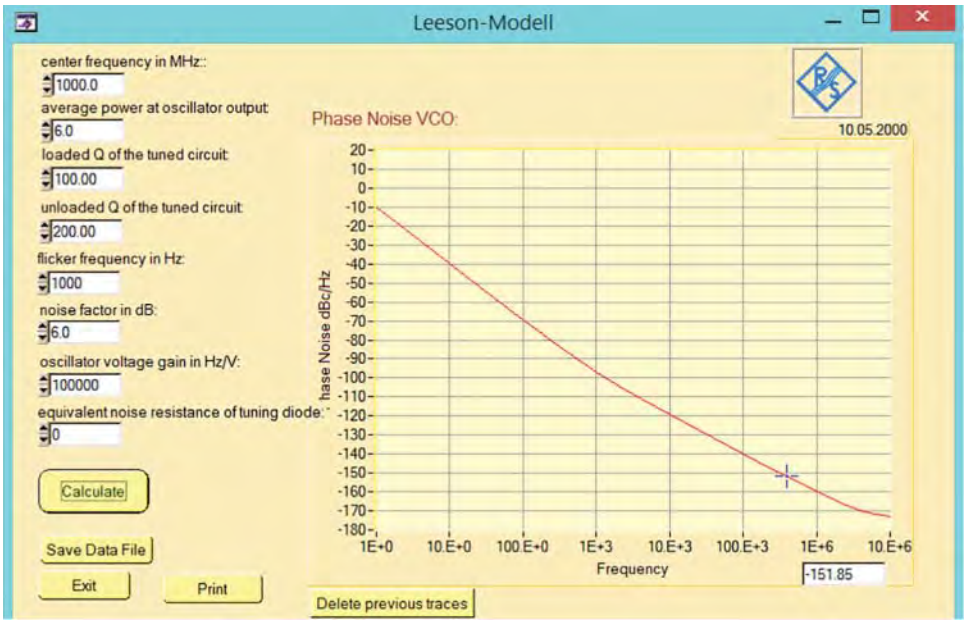
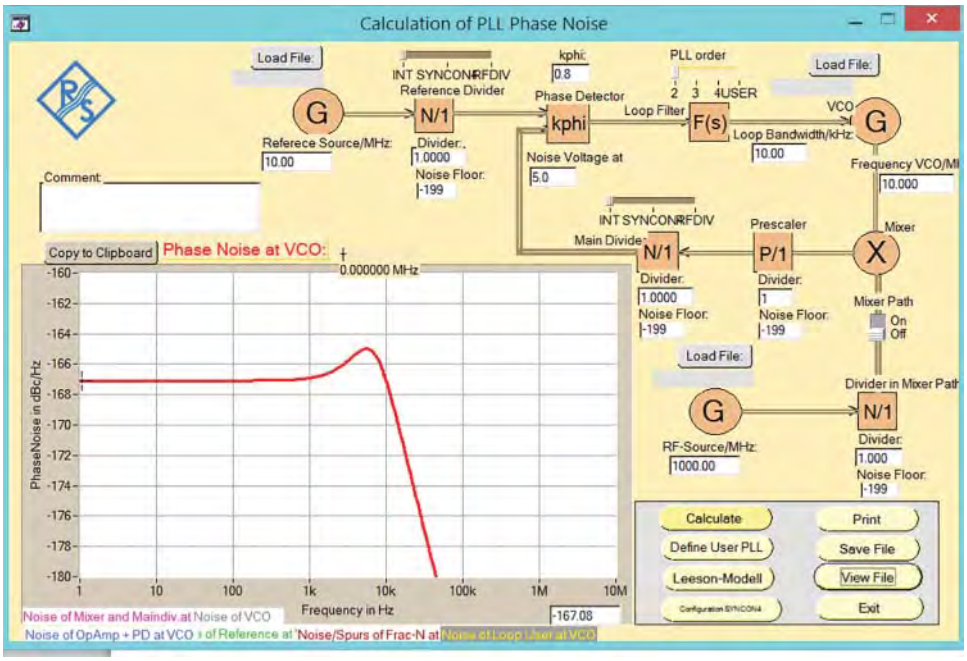


Figure A-13a Type 2 *n*th-order loop in which several elements are incorporated. This is an unstable loop.



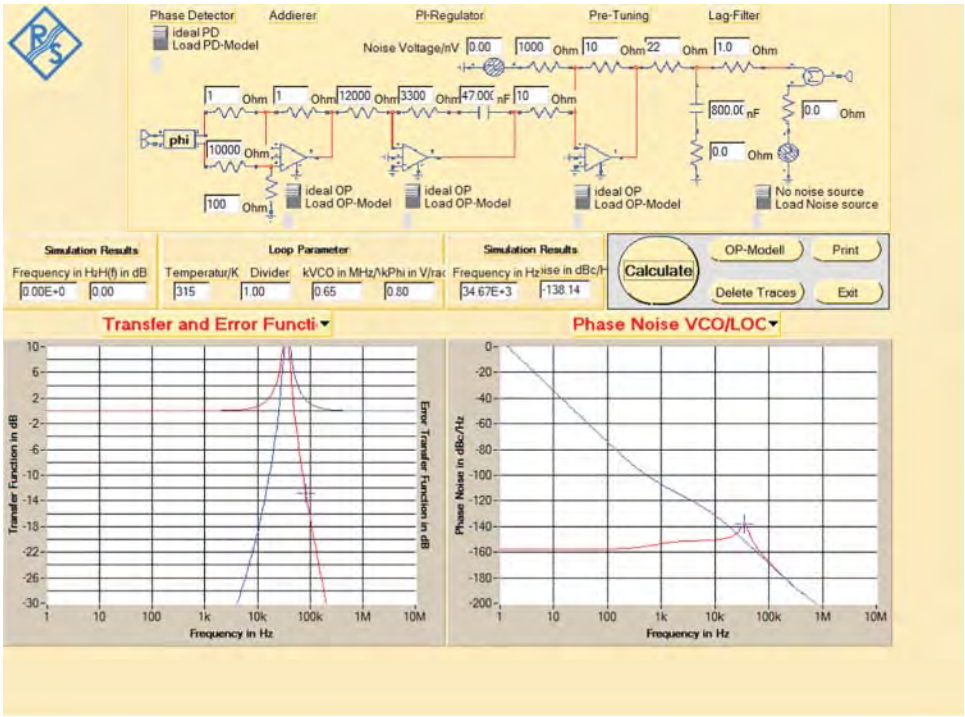
(b)

Figure A-13b Phase-noise plot calculated with the modified Leeson equation.



(c)

Figure A-13c Calculation of the open loop gain of the PLL system.



(d)

Figure A-13d Loop performance with added circuitry.

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A-4 LAPLACE TRANSFORM

The Laplace transformation is a convenient mathematical way to analyze and synthesize electronic circuitry with much less effort and far more accuracy than the conventional method by solving differential equations. The Laplace transformation is based on a method described by Pierre-Simon de Laplace, the French mathematician who developed the foundation of potential theory and made important contributions to celestial mechanics and probability theory. The word "transformation" in this case means that functions in time are converted to functions in frequency, and vice versa. Let us look at Figure A-14.

Figure A-14 shows a square wave generated by a suitable generator. We all know that square waves contain harmonics up to very high orders and that the Fourier analysis can be used to synthesize the square waveform. The Laplace transformation allows the direct transformation of the square wave into the Fourier spectrum. This method is used in engineering to analyze the performance of an electrical circuit where an electrical short pulse, a single event, or a periodic event that is not merely a sine or cosine function excites this circuit. Therefore, the Laplace transformation is used as a final method of solving differential equations and will provide an algebraic method of obtaining a *particular* solution of a differential equation from stated initial conditions. Since this is often what is desired in practice, the Laplace transformation is preferred for the solution of differential equations for electronic engineering.

Let us assume that $f(t)$ is a given function like the one shown in Figure A-15 and is defined for all $t \geq 0$. This function $f(t)$ is multiplied by e^{-st} and integrated with respect to t from 0 to infinity. Provided that the resulting integral exists, we can write

$$F(s) = \int_0^\infty e^{-st} f(t) dt \tag{A-32}$$

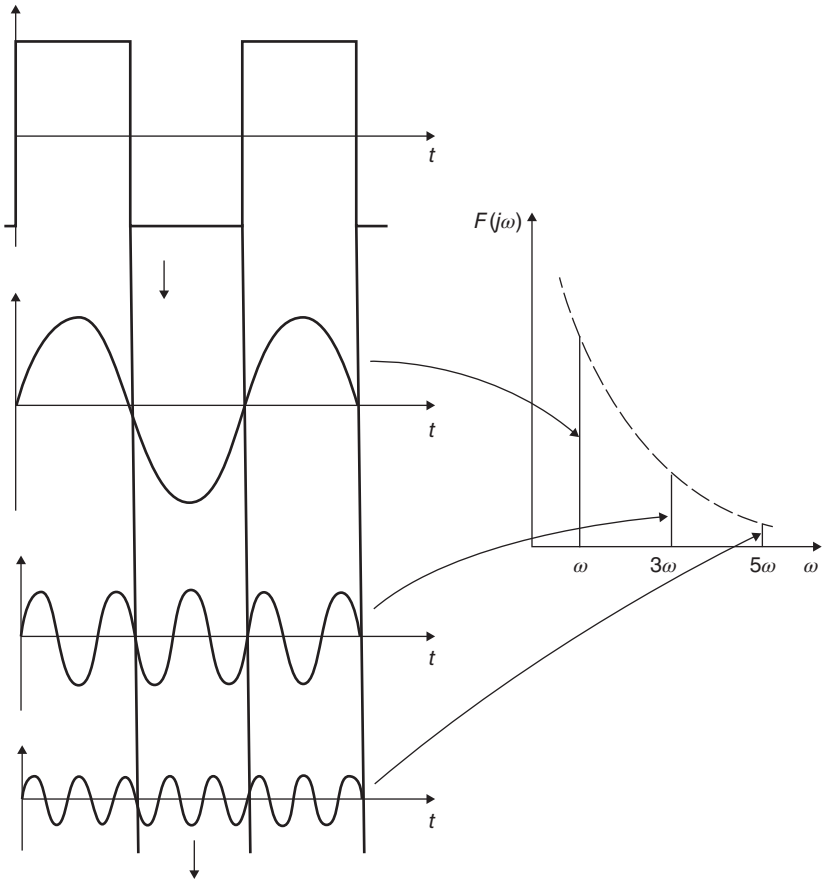


Figure A-14 Square wave showing its sine-wave contents.

The function $F(s)$ is called the *Laplace transform* of the original function $F(s)$ and will be written

$$F(s) = \mathscr{L}(f) = \int_0^\infty e^{-st} f(t)dt \tag{A-33}$$

Let us assume that we start with the Laplace transform and want to get the resulting time function. Mathematically this would be done with the inverse Laplace transformation and will be denoted by $\mathscr{L}^{-1}\{F(s)\}$. We shall write

$$f(t) = \mathscr{L}^{-1}[F(s)] \tag{A-34}$$

Rather than get scared, it may be nice to use it.

A-4-1 The Step Function

Let us assume that we have a step function

$$f(t) = 0 \quad \text{for } t < 1$$

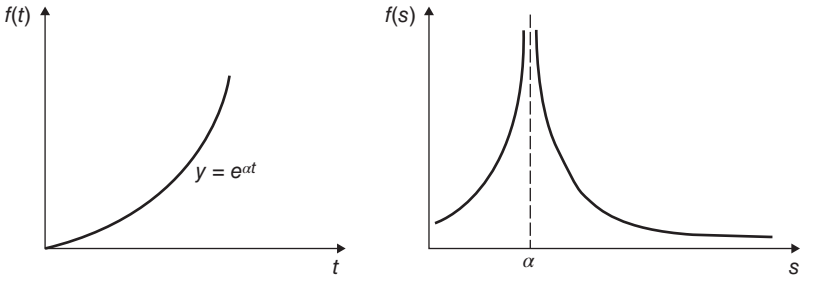


Figure A-15 Function $f(t)$ to be transformed into $F(s)$.

and

$$f(t) = 1 \quad \text{for } t \geq 0$$

We want to determine $F(s)$.

We obtain by integration

$$\mathscr{L}(f) = \mathscr{L}(1) = \int_0^\infty e^{-st} dt = -\frac{1}{s} e^{-st} \Big|_0^\infty \tag{A-35}$$

Hence, when $s > 0$,

$$\mathscr{L}(1) = \frac{1}{s} \tag{A-36}$$

A-4-2 The Ramp

Accordingly, for a ramp

$$\begin{aligned} \mathscr{L}(f') &= \int_0^\infty te^{-st} dt = \lim_{c \to \infty} \int_0^c te^{-st} dt \\ &= \lim_{c \to \infty} \frac{e^{-st}(-st - 1)}{s^2} \Big|_0^c = \frac{1}{s^2} \end{aligned} \tag{A-37}$$

We will use the ramp function as well as the step function in analyzing the loop performance of initial disturbance. In using actual Laplace transformation, the linearity theorem is important.

A-4-3 Linearity Theorem

Because the Laplace transformation is a linear operation, we can state that for any given functions $f(t)$ and $g(t)$ whose Laplace transforms exist, and any constants a and b, we have

$$\mathscr{L}[af(t) + bg(t)] = a\mathscr{L}[f(t)] + b\mathscr{L}[g(t)] \tag{A-38}$$

In addition, we have to know about the derivatives and integrals.

A-4-4 Differentiation and Integration

The differentiation is made very simple by the fact that differentiation of a function $f(t)$ corresponds simply to multiplication of the transform $F(s)$ by s. This permits replacing operations of calculus by simple algebraic operations on transforms. Furthermore, since integration is the inverse operation of differentiation, we expect it to correspond to division of transforms by s. This means that

$$\mathscr{L}(f') = s\mathscr{L}(f) - f(0) \tag{A-39}$$

and

$$\mathscr{L}\left[\int_0^t f(\tau)d\tau\right] = \frac{1}{s}\mathscr{L}[f(t)] \tag{A-40}$$

Table A-2 shows some functions $f(t)$ and their Laplace transforms.

A-4-5 Initial Value Theorem

If we apply a nonsinusoidal signal to an electrical circuit, we are interested in obtaining the value of $f(t)$ at the time $t = 0$, and this can be determined from the Laplace transform by

$$\lim f(t)_{t\to 0} = \lim sF(s)_{s\to\infty} \tag{A-41}$$

After the initial start condition, we are interested in determining the final value.

A-4-6 Final Value Theorem

The final value can be determined accordingly,

$$\lim f(t)_{t\to\infty} = \lim sF(s)_{s\to 0} \quad \text{(Provided that such a limit exists)}$$

Let us now use our knowledge and the integration table for one particular case, the active integrator.

A-4-7 The Active Integrator

Figure A-16 shows the circuit of an active RC integrator being driven with a step; because of the integration, the output voltage has to be a ramp. Let us prove this. The differential equation can be written

$$v_2(t) = -\frac{1}{C}\int_0^t i\ dt = \frac{-1}{RC}\int_0^t v_1 dt \tag{A-42}$$

Using $\tau = RC$, we obtain in Laplace notation

$$V_2(s) = \frac{-1}{st}V_1(s) \tag{A-43}$$

We assume that the capacitor at $t = 0$ has no charge. The step function $v_1(t)$ rises to the value v_0 and

$$V_1(s) = \frac{v_0}{s} \tag{A-44}$$

Therefore,

$$V_2(s) = \frac{-v_0}{\tau}\frac{1}{s^2} \tag{A-45}$$

Table A-2 Functions *f*(*t*) and their Laplace transforms *F*(*s*).

	$F(s)$	$f(t)$
(1)	$sF(s)-f(0)$	$\frac{df(t)}{dt}$
(2)	$\frac{F(s)}{s}+\frac{f^{(-1)}(0)}{s}$	$\int_0^t f(t)dt$
(3)	$F(s)c^{-s\tau}$	$f(t-\tau)$
(4)	$kF(s)$	$kf(t)$
(5)	$F_1(s)F_2(s)$	$f_1(t)f_2(t)$
(6)	$F_1(s)F_2(s)$	$f_1(t)f_2(t)$
(7)	0	0
(8)	$\frac{1}{s}$	$u(t)$
(9)	1	$\delta(t)$
(10)	$\frac{1}{s^2}$	t
(11)	$\frac{1}{s^3}$	$\frac{t^2}{2}$
(12)	$\frac{1}{s^n} n>0$	$\frac{t^{n-1}}{(n-1)!}$
(13)	$\frac{1}{s-\alpha}$	$e^{\alpha t}$
(14)	$\frac{1}{s(s-\alpha)}$	$\frac{1}{\alpha}\frac{1}{e^{\alpha t}-1}$
(15)	$\frac{1}{s(s+\alpha)}$	$\frac{1}{\alpha}(1-e^{\alpha t})$
(16)	$\frac{1}{(s-\alpha)^n} n>0$	$\frac{t^n-1}{(n-1)!e^{\alpha t}}$
(17)	$\frac{1}{s^2+\alpha^2}$	$\frac{1}{\alpha}\sin\alpha t$
(18)	$\frac{s}{s^2+\alpha^2}$	$\cos\alpha t$
(19)	$\frac{1}{s(s^2+\alpha^2)}$	$\frac{1}{\alpha^2}(1-\cos\alpha t)$
(20)	$\frac{1}{s^2-\alpha^2}$	$\frac{1}{\alpha}\sinh\alpha t$
(21)	$\frac{s}{s^2-\alpha^2}$	$\cosh\alpha t$
(22)	$\frac{1}{s(s^2-\alpha^2)}$	$\frac{1}{\alpha^2}(\cosh\alpha t-1)$
(23)	$\frac{1}{(s-\alpha)(s-\beta)}$	$\frac{e^{\beta t}-e^{\alpha t}}{\beta-\alpha}$
(24)	$\frac{s}{(s-\alpha)(s-\beta)}$	$\frac{\beta e^{\beta t}-\alpha e^{\alpha t}}{\beta-\alpha}$
(25)	$\frac{1}{s(s-\alpha)(s-\beta)}$	$\frac{\beta e^{\alpha t}-\alpha e^{\beta t}}{\alpha\beta(\alpha-\beta)}+\frac{1}{\alpha\beta}$
(26)	$\frac{1}{s^2+2s\varsigma\omega_n+\omega_n^2}$	$\frac{e^{-\varsigma\omega}n^t\sin\sqrt{1-\varsigma^2\omega_n}}{\sqrt{1-\varsigma^2\omega_n}}$
(27)	$\frac{s}{s^2+2s\varsigma\omega_n+\omega_n^2}$	$\left[\cos\sqrt{1-\varsigma^2}\omega_n t-\frac{\varsigma}{\sqrt{1-\varsigma^2}}\sin\sqrt{1-\varsigma^2}\omega_n t\right]e^{-\varsigma\omega_n t}$
(28)	$\frac{1}{s(s^2+2s\varsigma\omega_n+\omega_n^2)}$	$\frac{1}{\omega_n^2}\left[1-\left(\cos\sqrt{1-\varsigma^2}\omega_n t+\frac{\varsigma}{\sqrt{1-\varsigma^2}}\sin\sqrt{1-\varsigma^2\omega_n}t\right)e^{-\varsigma\omega_n t}\right]$
(29)	$\frac{1}{(a-\alpha)(s-\beta)^2}$	$\frac{e^{\alpha t}-[1+(\alpha-\beta)t]e\beta t}{(\alpha-\beta)^2}$

Table A-2 (*Continued*)

	$F(s)$	$f(t)$
(30)	$\frac{s}{(s-\alpha)(s-\beta)^2}$	$\frac{\alpha e^{\alpha t} - [\alpha + \beta(\alpha - \beta)t]e^{\beta t}}{(\alpha - \beta)^2}$
(31)	$\frac{s^2}{(s-\alpha)(s-\beta)^2}$	$\frac{\alpha^2 e^{\alpha t} - [2\alpha - \beta + \beta(\alpha - \beta)t]\beta e^{\beta t}}{(\alpha - \beta)^2}$
(32)	$\frac{1}{(s-\alpha)(s-\beta)(s-\gamma)}$	$\frac{(\beta - \gamma)e^{\alpha t} + (\gamma - \alpha)e^{\beta t} + (\alpha - \beta)e^{\gamma t}}{(\alpha - \beta)(\beta - \gamma)(\gamma - \alpha)}$
(33)	$\frac{1}{(s^2 + \alpha^2)(s^2 + \beta^2)}$	$\frac{\alpha \sin \beta t - \beta \sin \alpha t}{\alpha\beta(\alpha^2 - \beta^2)}$
(34)	$\frac{s}{(s^2 + \alpha^2)(s^2 + \beta^2)}$	$\frac{\cos \beta t - \cos \alpha t}{\alpha^2 - \beta^2}$
(35)	$\frac{1}{\sqrt{s}}$	$\frac{1}{\sqrt{\pi t}}$
(36)	$\frac{1}{s\sqrt{s}}$	$2\sqrt{\frac{t}{\pi}}$
(37)	$\frac{1}{s^n\sqrt{s}}$	$\frac{n!}{(2n)!}\frac{4\pi}{\sqrt{\pi}}t^{n-1/2}$
(38)	$\frac{1}{\sqrt{s-\alpha}}$	$\frac{1}{\sqrt{\pi t}}e^{\alpha t}$
(39)	$\frac{1}{s\sqrt{s-\alpha}}$	$\frac{2}{\sqrt{\alpha\pi}}\int_0^{\sqrt{\alpha t}} e^{-\varsigma^2} d\xi$
(40)	$\frac{1}{(s+\alpha)\sqrt{s+\beta}}$	$\frac{2e^{-\alpha t}}{\sqrt{\pi(\beta - \alpha)}}\int_0^{\sqrt{(\beta-\alpha)t}} e^{-s^2} d\xi$
(41)	$\frac{\sqrt{s+a}}{s}$	$\frac{e^{-\alpha t}}{\sqrt{\pi t}} + 2\sqrt{\frac{\alpha}{\pi}}\int_0^{\sqrt{\alpha t}} e^{-s^2} d\xi$
(42)	$\frac{1}{\sqrt{s^2 + \alpha^2}}$	$I_0(\alpha t)$
(43)	$\frac{1}{\sqrt{s^2 - \alpha^2}}$	$J_0(\alpha t)$

According to Table A-2,

$$v_2(t) = \mathscr{L}^{-1}[V_2(s)] = -v_0\frac{t}{\tau} \tag{A-46}$$

This is the equation of a linear ramp.

Let us now become more challenging and determine the locking behavior of a phase-locked loop, using a lag filter as shown in Figure A-17.

A-4-8 Locking Behavior of the PLL

The transfer function of the lag filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{A-47}$$

and the phase detector voltage is

$$v_\phi(t) = K_\theta\theta \tag{A-48}$$

and in Laplace notation

$$V_\phi(s) = k_\theta\theta(s) \tag{A-49}$$

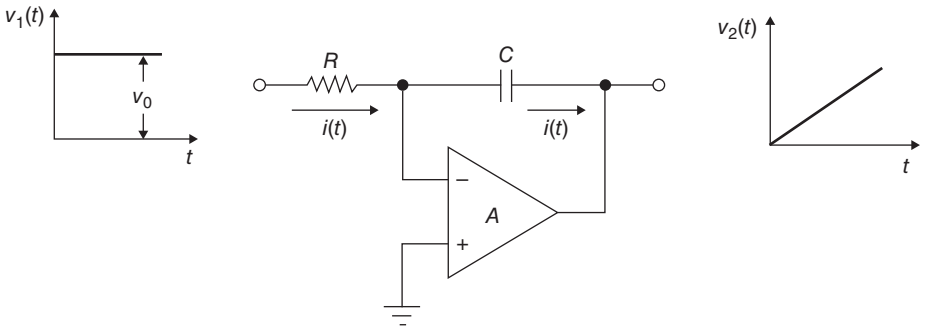


Figure A-16 Active *RC* integrator being driven with a step function.

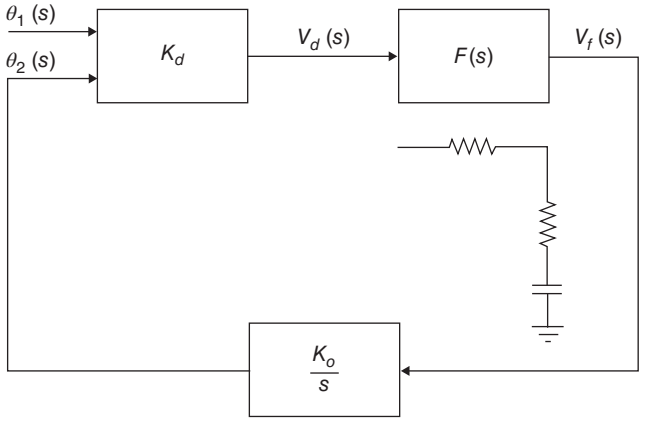


Figure A-17 PLL with lag filter.

The output frequency of the VCO is

$$\omega_o = K_o v(t) \tag{A-50}$$

$$\theta_O = K_O \int_0^t v(t)dt \tag{A-51}$$

and in Laplace notation

$$\theta(s) = K_o \frac{V(s)}{s} \tag{A-52}$$

There are three building blocks for which we define the following functions:

(1) Phase comparator:

$$\frac{v_\phi(s)}{\theta_e(s)} = K_o \tag{A-53}$$

(2) Low-pass filter:

$$\frac{V(s)}{\theta(s)} = F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{A-54}$$

(3) VCO:

$$\theta_2(s) = \theta_1(s) - \theta_e(s) = K_o \frac{V(s)}{s} \tag{A-55}$$

This can be rearranged to give

$$\theta_2(s) = \theta_1(s) \frac{s^2}{s^2 + sK_oK_\theta(\tau_2/\tau_1) + (K_oK_\theta/\tau_1)} \tag{A-56}$$

Using similar abbreviations,

$$\omega_n = \left(\frac{K_oK_\theta}{\tau_1}\right)^{1/2} \tag{A-57}$$

$$\zeta = \frac{\tau_2}{2}\left(\frac{K_oK_\theta}{\tau_1}\right)^{1/2} \tag{A-58}$$

we can rearrange the equation earlier in the form

$$\theta_e(s) = \theta_1(s) \frac{s^2}{s^2 + 2s\varsigma\omega_n + \omega_n^2} \tag{A-59}$$

Applying a step to the input,

$$\theta_1(s) = \frac{\Delta\phi}{s} \tag{A-60}$$

we obtain

$$\theta_e(s) = \frac{s\Delta\phi}{s^2 + 2s\zeta\omega_n + \omega_n^2} \tag{A-61}$$

We apply the initial value theorem,

$$\lim_{t\to 0} \theta_e(t) = \lim_{s\to\infty} s\theta_e(s) = \frac{s^2\Delta\phi}{s^2 + 2s\zeta\omega_n + \omega_n^2} = \Delta\phi \tag{A-62}$$

This means that the initial phase error is equal to the step in phase $\Delta\phi$.

Using the final value theorem, we find

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\theta_e(s) = \frac{s^2\Delta\phi}{s^2 + 2s\zeta\omega_n + \omega_n^2} = 0 \tag{A-63}$$

This means that, if we wait long enough, the phase error will be zero. The final remaining task is to look up the equation earlier in our table of Laplace transform functions, and we find the required transform in No. 27:

$$\begin{aligned} f(t) &= \theta_e(t) \\ &= \Delta\phi \left[\cos\sqrt{1-\zeta^2}\omega_n t - \frac{\zeta}{\sqrt{1-\zeta^2}} \sin\sqrt{1-\zeta^2}\omega_n t\right] e^{-\zeta\omega_n t} \end{aligned} \tag{A-64}$$

A-5 LOW-NOISE OSCILLATOR DESIGN

The design of low-noise oscillators is based on various principles.

(1) We have learned that one way of reducing the noise is to keep as much energy storage in the capacitor as possible. We can assign for any tuned circuit an equivalent transmission impedance $C_o = \sqrt{L/C}$. This would indicate that the larger the C, the lower the transmission impedance. In addition, such a circuit is less sensitive to circuit board capacitance and should provide better performance.

(2) We have learned that the noise outside the loop bandwidth of an oscillator is determined by the Q of the LC network—the highest possible Q that can be obtained in an LC circuit when the losses are minimized. High-Q tuned circuits can be built with transmission lines, and quarter-wavelength transmission lines are specifically used for this purpose. The easiest way of accomplishing this is to take a mechanical cavity that is adjusted to odd numbers of quarter-wavelengths, whereby any material inside the cavity has to be taken into consideration. The wavelengths of a quarter-wave transmission line can be determined from $\lambda_o = 300/f_o$. If the frequency is inserted in megahertz, the resulting wavelength is in meters. In the event that a dielectric material is used, as in the case of coaxial cable as a cavity oscillator, the wavelengths electrically and mechanically differ:

$$\lambda = \frac{\lambda_o}{\sqrt{\varepsilon_\tau}} \tag{A-65}$$

For Teflon, $\varepsilon_\tau = 2$.

This second principle is used in the Hewlett-Packard HP8940 signal generator, where a cavity is mechanically tuned. This cavity has a high Q of about 600–800, and therefore the noise sideband is very low.

Let us design such an oscillator.

A-5-1 Example Implementation

A quarter-wavelength oscillator using a rigid coaxial line will be built covering the frequency range from 250 to 450 MHz. We have to use the equation

$$\frac{dz}{\lambda} = \frac{1}{2\pi} \arctan \omega C Z \tag{A-66}$$

where dz is the amount by which the cavity is reduced in size relative to quarter-wavelength. The highest frequency of our oscillator is 450 MHz, and therefore $\lambda_o = 66.6$ cm. Quarter-wavelength is $\lambda_o/4 = 16.66$ cm. For reasons of available mechanical space, we have decided to make the transmission line quarter-wavelength cable 5 cm long. Therefore,

$$L = \frac{\lambda_O}{4} - dz = 16.66 - 5 = 11.66$$

We now rearrange the equation earlier and solve it for C.

$$C = \frac{1}{\omega Z} \tan \frac{2\pi dz}{\lambda_0} \tag{A-67}$$

or

$$\begin{aligned} C_1 &= \frac{1}{2\pi \times 450 \times 10^6 \times 50} \tan \frac{2\pi \times 11.66}{66.6} \\ &= 7.736 \times 10^{-12} \times \tan 1.1 \ \text{(rad)} \\ &= 7.736 \times 10^{-12} \times 1.9649 \\ &= 13.899 \times 10^{-12} = 13.899 \ \text{pF} \end{aligned}$$

Electrically, the transmission line, which is now operating as a quarter-wavelength resonator, is an inductance that requires an external capacitor of about 14 pF to be in resonance for 450 MHz. For 250 MHz we will get a new value for the capacitance. First, we determine λ. $\lambda_o = 1.2$ m and $\lambda_o/4 = 30$ cm. Because the mechanical length of our quarter-wavelength is 5 cm,

$$L = \frac{\lambda_O}{4} - dz = 30^{-5} = 25\text{cm}$$

We now compute

$$C_2 = \frac{1}{2\pi \times 250 \times 10^6 \times 50} \tan \frac{2\pi \times 25}{120}$$

$$C_1 = 12.732 \times 10^{-12} \tan 1.309$$

$$= 12.732 \times 10^{12} \times 3.7321 = 47.156 \text{ pF}$$

These are the two values required for the oscillator to cover the frequency range. If one compares these two capacitance values with values obtained with conventional high-Q inductors, it is apparent that those values are substantially larger. This is due to the fact that we have chosen a 50-Ω transmission line. The use of a low-impedance transmission line has several advantages.

(1) It can be shown mathematically that the optimum Q of a coaxial transmission line occurs at about 70 Ω. All higher impedances exhibit more losses and lower Q.
(2) If a rigid line or its equivalent mechanical arrangement is used, the low-impedance version transmission line and is therefore electrically much more stable will have fewer microphonic effects due to mechanical vibration than a high-impedance transmission line and is therefore electrically much more stable.

Figure A-18 shows an analysis of this done on a digital computer. We find that, as the impedance increases, the external shunt capacitance goes down in value. In this figure, the computer has plotted the curves from 50 to 300 Ω, and the necessary capacitance can be read from this drawing as a function of frequency and characteristic impedance. For a 300-Ω transmission line and 500 MHz, an external capacitance of about 2.5 pF is required. Most likely, circuit board and other stray capacitances will be around that magnitude. For a 100-Ω oscillator, about 7 pF is required. It is evident that the oscillator we have just calculated, which requires about 14 pF, is a better choice. Another interesting relationship is the required capacitance as a function of increase of resonator length.

Figure A-19 shows a diagram in which the capacitance is plotted as a function of frequency and resonator length with a 50-Ω transmission line. If we use a 10-cm resonator, we need about 3.5 pF at 500 MHz and about 25 pF at 250 MHz. Again, this gives some interesting insight into the mechanism. Conventional LC circuits theoretically could be built using such low inductances. However, the stray field of this unconfined resonator would result in losses, consequently lowering the magnetic Q of the circuit. A similar principle is used in helical resonators, and the Rohde & Schwarz SMDU signal generator uses this principle. There is really no difference between the two approaches. In the case of Hewlett-Packard, the quarter-wave transmission line is mechanically adjusted in its length. As a result of this, a mechanically more elaborate system is required, whereas in the Rohde & Schwarz SMDU signal generator the helical resonator is loaded with a very large, low microphonic air-variable capacitor of large diameter. Both arrangements are electrically excellent. The air-variable capacitor has the advantage that there is no mechanical abrasion, and therefore the lifetime will be longer. The cavity, on the other hand, provides a somewhat more linear frequency versus tuning curve.

Figure A-20 shows the schematic of such an oscillator. It becomes apparent that a switching technique is used to coarse steer the oscillator within certain ranges. Since we have learned that the tuning diodes will introduce more noise than fixed capacitors switched in by diodes that are not sensitive to noise pickup and other radiation effects, this technique is used. Let us take a look at the possible resolution. The minimum additional capacitor that can be added is 1 pF. At 450 MHz, 1 pF will result in the following detuning:

$$\frac{f_1}{f_2} = \sqrt{\frac{13.951}{14.951} = \frac{450}{434.69}}$$

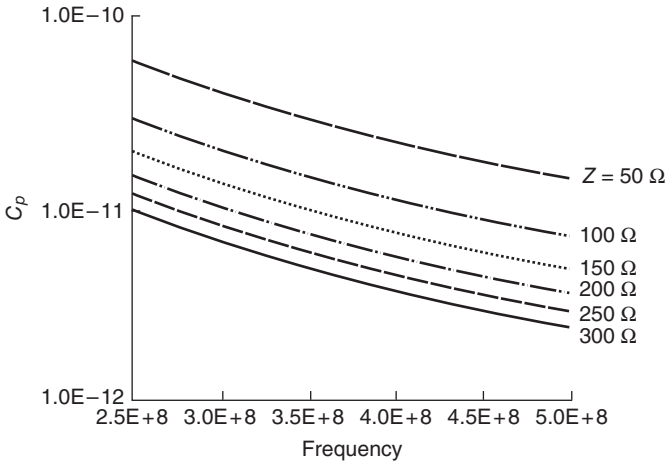


Figure A-18 Capacitance required to tune a quarter-wavelength resonator oscillator from 250 to 500 MHz as a function of the impedance of the quarter-wavelength.

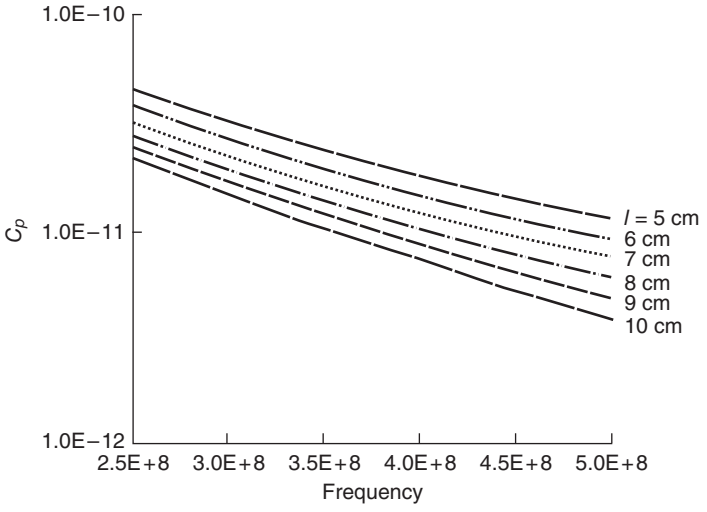


Figure A-19 Rigid cable used as a quarter-wave resonator at various lengths showing the external capacitance value required to tune it from 250 to 500 MHz as a function of length.

or a change of 15.3 MHz. At the low end of 225 MHz, this will result in

$$\frac{f_1}{f_2} = \sqrt{\frac{47.517}{48.517} = \frac{250}{247.47}}$$

or we obtain a frequency shift of 2.6 MHz.

Our highest resolution at the top is therefore about 15 MHz, with 2.6 MHz at the low-frequency end. Thus, we have to use a decoding circuit that selects the proper capacitor for the same step at the lower frequency range. In order to get 15.3 MHz, we calculate

$$\sqrt{\frac{265}{250}} = 1.0296$$

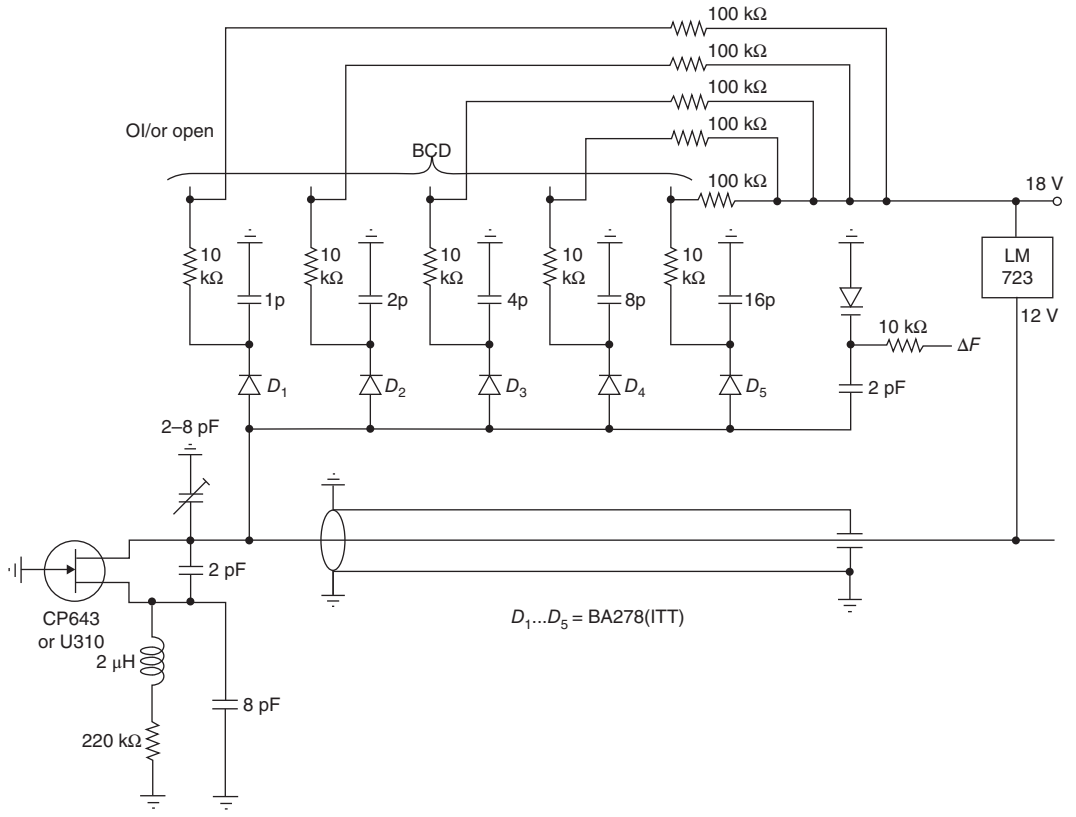


Figure A-20 Schematic of a quarter-wavelength oscillator, including switching diodes. With the availability of very low noise bipolar transistors such as the BFP 620/640, a much improved design is now possible. The design will be shown later.

or

$$\frac{C_1^*}{C_1} = 1.06$$

Our starting value at the low end is 47.517 pF, which has to be reduced to 44.827 for a 15-MHz shift. The difference is about 2.7 pF. Therefore, following the first 1-pF capacitor, we must be able to switch in 2 pF, resulting in a total of 3 pF, which is a close approximation to the required 2.7 pF for the required 15-MHz step. We now follow this binary system, and therefore our next capacitances are 4, 8, and 16 pF.

Our binary switch requires a 5-bit data command. If we add all the capacitors together, we obtain a total capacitance of 31 pF. Since the initial starting capacitance at 500 MHz was set to be about 14 pF, which is found by the feedback network as well as the stray capacitance and a coarse-tuning capacitor, the additional 30 pF, if all five capacitors are switched in, will result in 43 pF. We have to take into consideration the fact that these capacitors have some tolerances and therefore, by selecting the proper values with slightly larger amounts, we can easily make the total 33 pF to obtain the 47.5 pF required. This oscillator exhibits superior performance relative to the normal *LC* oscillator.

Some authors have found it useful to build a $\lambda/2$ oscillator, which then has twice the mechanical length we have currently used, and this may be helpful at higher frequencies. In addition, because of the transmission properties of a half-wavelength cable, a capacitor used at the output of the cable is transformed into an inductor. The drawback of this method, however, is that the resonant impedance for constant Q at the transistor varies as a function of frequency, whereby for higher frequencies where the gain is lower, the impedance gets lower.

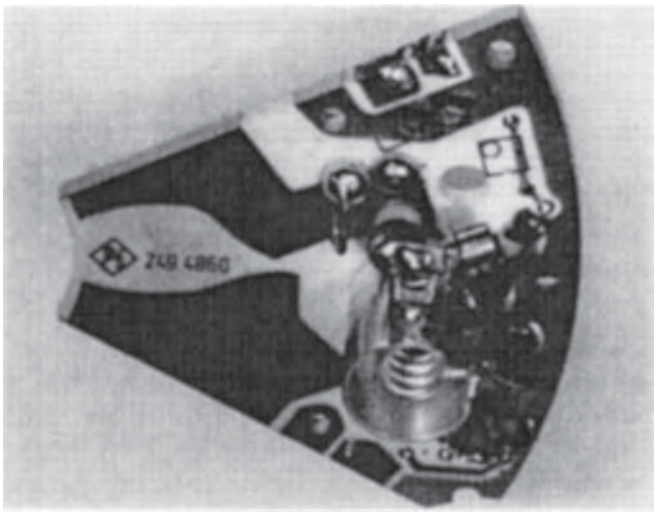


Figure A-21 Photograph of the Rohde & Schwarz SMDU oscillator.

This is opposite to the quarter-wavelength system and, in our opinion, less desirable.

The tuning diode in the quarter-wave oscillator is responsible for the fine tuning and will cover about 20 MHz of range. At 250 MHz, this is less than 10%, and as we have seen previously, the noise influence under these circumstances is extremely small.

As this oscillator is highly useful, in Section A-6 we will analyze the feedback circuit to determine the amplitude stabilization and harmonic contents with the aid of some nonlinear analysis. Figure A-21 shows a picture of the Rohde & Schwarz SMDU oscillator.

A-6 OSCILLATOR AMPLITUDE STABILIZATION

In Chapter 4 we mentioned briefly that the oscillator amplitude stabilizes due to some nonlinear performance of the transistor. There are various mechanisms involved and, depending on the circuit, several of them are simultaneously responsible for the performance of an oscillator. Under most circumstances, the transistor is operated in an area where the dc bias voltages are substantially larger than the ac voltages. Therefore, the theory describing the transistor performance under these conditions is called *small-signal theory*. In a transistor oscillator, however, we are dealing with a feedback circuit that applies positive feedback. The energy that is being generated by the initial switch-on of the circuit is being fed back to the input of the circuit, amplified, and returned to the input again until oscillation starts. The oscillation would theoretically increase in value indefinitely unless some limiting or stabilization occurs. In transistor circuits, we have two basic phenomena responsible for limiting the amplitude of oscillation.

(1) Limiting because of gain saturation and reduction of open-loop gain.

(2) Automatic bias generated by the rectifying mechanism of either the diode in the bipolar transistor or in the junction field-effect transistor. In metal–oxide–semiconductor field-effect transistors (MOSFETs) an external diode is sometimes used for this biasing.

A third phenomenon would be external automatic gain control (AGC), but it will not be considered here.

The oscillators we discuss here are self-limiting oscillators.

The self-limiting process, which by generating a dc offset bias moves the operating point into a region of less gain, is generally noisy. For very low noise oscillators, this operation is not recommended. After dealing with the quarter-wavelength oscillator in the preceding section, we will deal here only with the negative resistance oscillator, in which, through a mechanism explained in Chapter 4, a negative resistance is generated due to feedback and is used to start oscillation with the passive device. Here we look at what is happening inside the transistor that is responsible for amplitude stabilization, and we will thus be in a position to make a prediction regarding the available energy and the harmonic contents.

Figure A-22 shows the quarter-wavelength oscillator redrawn in such a way that the source electrode is now at ground potential while the gate and drain electrode are electrically hot. The reason for doing this is because we will look at the gate-to-source transfer characteristic and use its nonlinearities as a tool to describe what is happening. The same analysis can be applied to a transistor circuit, provided that the resistors used for dc bias are small enough not to cause any dc offset. The field-effect transistor characteristic follows a square law and therefore can be expressed as

$$i_2 = I_{\text{DSS}}\left(1 - \frac{v_1}{v_p}\right)^2 \tag{A-68}$$

For any other device, we have to take the necessary transfer characteristic into consideration, and this could theoretically be done by changing the square law into nth order. The voltage v_1 will be in the form

$$v_1 = V_b + V_1 \cos \omega t \tag{A-69}$$

This is the voltage that is being generated due to the selectivity of the tuned circuit at which there is a resonant frequency. Inserting this into the above equation and using

$$V_x = V_p - V_b \tag{A-70}$$

we obtain

$$i_2 = \frac{I_{\text{DSS}}}{V_p^2}(V_x^2 - 2V_x\ V_1 \cos \omega t + V_1^2 \cos^2 \omega t) \tag{A-71}$$

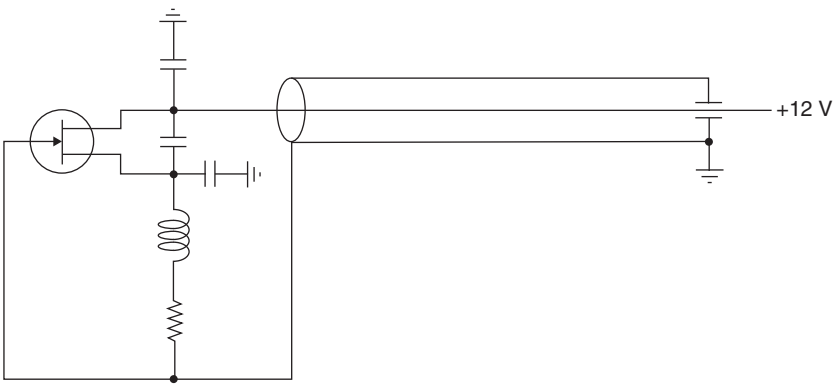


Figure A-22 Quarter-wavelength oscillator with grounded source electrode.

Once we know the peak value of i_2, we can expand this into a Fourier series. In this case a Fourier series expansion for i_2 has only three terms; that is,

$$i_2(t) = I_o + I_1 \cos \omega t + I_2 \cos 2\omega t \tag{A-72}$$

$$I_o = \frac{I_{\text{DSS}}}{V_p^2} V_x^2 + \frac{V_1^2}{2} \tag{A-73}$$

$$I_1 = -2\frac{I_{\text{DSS}}}{V^2} V_x V_1 \tag{A-74}$$

$$I_2 = \frac{I_{\text{DSS}}}{V_p^2} \frac{V_1^2}{2} \tag{A-75}$$

Because of the square-law characteristic, I_1 is a linear function of V_1 and we can define a large-signal average transconductance G_m:

$$G_m = \frac{I_1}{V_1} = -2\frac{I_{\text{DSS}}}{V_p^2} V_x \tag{A-76}$$

In the case of the square-law characteristic, we find the interesting property that the small-signal transconductance g_m at any particular point is equal to the large-signal average transconductance G_m at the same point. The second harmonic distortion in the output current is given by

$$\frac{I_2}{I_1} = \frac{V_1}{4V_x} = \frac{V_1}{4V_p} \frac{g_{mo}}{g_m} \tag{A-77}$$

The transconductance G_m can be defined in such a way that it indicates the gain for a particular frequency relative to the fundamental, which means that there is a certain G_m for the fundamental frequency and one for the second harmonic, and in the general case, a G_{mn} for the nth-order harmonic. In the more general form, we rewrite our equation

$$i_d = C_n(-V_b + V_1 \cos x)^n \tag{A-78}$$

As this will exist only during the period from $-\alpha$ to $+\alpha$, the equation

$$-\alpha < x < +\alpha$$

exists only for

$$i_2 = 0$$

$$x = \pm\alpha$$

$$\cos \alpha = \frac{V_b}{V_1}$$

We can rewrite our equation for the drain current or collector current of a transistor:

$$i_d = C_n V_1^n (\cos x - \cos \omega)^n \tag{A-79}$$

The dc value of the current is

$$I_d = \frac{1}{\pi} \int_0^{\alpha} i_d \, dx \tag{A-80}$$

or

$$I_d = \frac{C_n V_1}{\pi} \int_0^{\alpha} (\cos x - \cos \alpha)^n dx \tag{A-81}$$

The amplitude of the fundamental frequency is

$$I_1 = \frac{2}{\pi} \int_0^{\alpha} i_d \cos x \; dx \tag{A-82}$$

or

$$I_1 = \frac{2C_n V_1^n}{\pi} \int_0^{\alpha} (\cos x - \cos \alpha)^n \cos x \; dx \tag{A-83}$$

For $n = 1$, the collector current is

$$I_d = C_1 V_1 A_1 \tag{A-84}$$

and the amplitude of the fundamental frequency is

$$I_1 = C_1 V_1 B_1 \tag{A-85}$$

For $n = 2$, the collector current is therefore

$$I_d = C_2 V_1^2 A_2 \tag{A-86}$$

and the amplitude of the fundamental frequency is

$$I_1 = C_2 V_1^2 B_2 \tag{A-87}$$

With the definition of the conduction angle, we find

$$\alpha = \text{arc} \frac{V_b}{V_1} \tag{A-88}$$

These values are listed in Table A-3.

These are the normalized Fourier coefficients as a function of n and the conduction angle. Theoretically, this has to be expanded to the order n of 3 or 4, depending on the particular device, and can be found from tables or by a computer.

Table A-3 Normalized Fourier coefficients.

$\frac{V_b}{V_1}$	A_1	B_1	$\frac{B_1}{A_1}$	A_2	B_2	$\frac{B_2}{A_2}$
0	0.318	0.500	1.57	0.250	0.425	1.7
0.1	0.269	0.436	1.62	0.191	0.331	1.73
0.2	0.225	0.373	1.66	0.141	0.251	1.78
0.3	0.185	0.312	1.69	0.101	0.181	1.79
0.4	0.144	0.251	1.74	0.0674	0.126	1.87
0.5	0.109	0.195	1.79	0.0422	0.0802	1.90
0.6	0.077	0.141	1.83	0.0244	0.0458	~1.95
0.7	0.050	0.093	1.86	0.0118	0.0236	~2
0.8	0.027	0.052	1.92	0.0043	0.0082	~2
0.9	0.010	0.020	2	0.00074	0.00148	2
1.0	0	0	2	0	0	2

For simplifications, let us go back to the case of our square-law device, where our transconductance is

$$G_m = \frac{I_1}{V_1} = -2\frac{I_{\text{DSS}}}{V_p^2}V_x \tag{A-89}$$

This can be rewritten in the form

$$G_m = -\frac{2I_{\text{DSS}}}{V_p^2}(V_p - V_b + V_1 \cos \omega t) \tag{A-90}$$

V_p is the pinch-off voltage of the field-effect transistor, V_b is the bias voltage that is measured between source and ground, and V_1 is the peak value of the voltage of the fundamental frequency. Figure A-23 shows the effect where the sine wave is driving the transfer characteristic, and the resulting output currents are narrow pulses. Based on the duration, the mutual conductance g_m becomes a fraction of the dc transconductance G_m, and therefore the gain is reduced. For small conduction angles I_n/I_d, the mutual conductance can take very small values, and therefore the gain gets very small; this is the cause for stabilizing the amplitude in the oscillator. We note that the gain is being reduced as the amplitude causing the small conduction angle is increased.

Fourier analysis indicates that, for a small harmonic distortion, the radio frequency (*RF*) voltage at the source or gate (depending on where it is grounded) has to be less than 80 mV. Now we can design the oscillator performance.

Let us assume that the saturation voltage of the active device is 2 V, battery voltage applied to the transistor is 12 V, and the transistor starts at a dc current of 10 mA with a source resistor of 200 Ω. This results in a voltage drop of 1 V at the source and 2 V in the device; therefore, 9 V is available. It can be assumed that the maximum voltage at the drain will be $9 \times \sqrt{2}$. The capacitor voltage divider from drain to voltage now depends on the gain. If we assume an I_n/I_d of 0.15 for about 50° conduction angle, 2α, and the dc conductance of the transistor at the starting dc operating point is 20 mA/V, the resulting transconductance is 3 mA/V.

Next, we need the output impedance provided by the quarter-wave resonator:

$$R_L = Q\frac{1}{\omega C}(250\ \text{MHz})$$

or

$$R_L = 600\frac{1}{2\pi \times 47 \times 10^{-12} \times 250 \times 10^6} = 8127\ \Omega$$

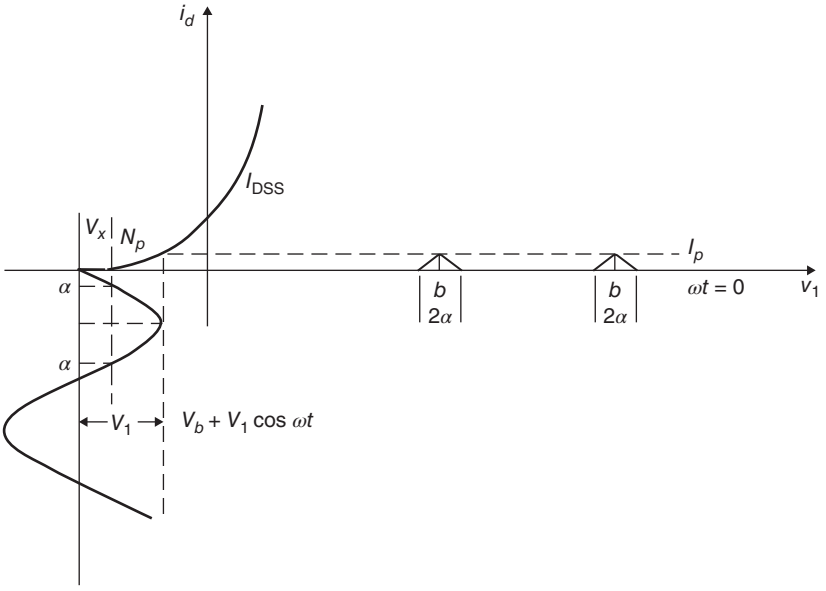


Figure A-23 Current tips as a function of narrow conduction angles in a square-wave transfer characteristic.

As we want 9 V rms at the output, we have to use the equation

$$\frac{V_{\text{out}}}{V_{\text{in}}} = A(\text{voltage gain}) = g_m R_L = 3 \times 10^{-3} \times 8.127 \times 10^3$$

$$A = 24.38$$

or

$$V_{\text{in}} = \frac{8\text{V}}{A} = 328 \text{ mV}$$

This would mean that the capacitance ratio of the feedback capacitors C_1 and C_2 would be 1:24.38. In practice, we will find that this is incorrect, and we need a 1:4 or 1:5 ratio. The reason for this is that the equations we have used so far are not accurate enough to represent the actual dc shifts and harmonic occurrences. As mentioned in Sections A-4-1 and A-5, a certain amount of experimentation is required to obtain the proper value. To determine the actual ratio, it is recommended that one obtain from the transistor manufacturer the device with the lowest gain and build an oscillator testing it over the necessary temperature range. As the gain of the transistor changes as a function of temperature (gain increases as temperature decreases for field-effect transistors and acts in reverse for bipolar transistors), a voltage divider has to be chosen that is, on the one hand, high enough to prevent the device from going into saturation, which will cause noise, and, on the other hand, small enough to allow oscillation under worst-case conditions.

The simulation using a bipolar transistor-type BFP 620 uses as lossless cable as a resonator very loosely coupled to the transistor (see Figure A-24). Predicted performance is shown in Figures A-25–A-28.

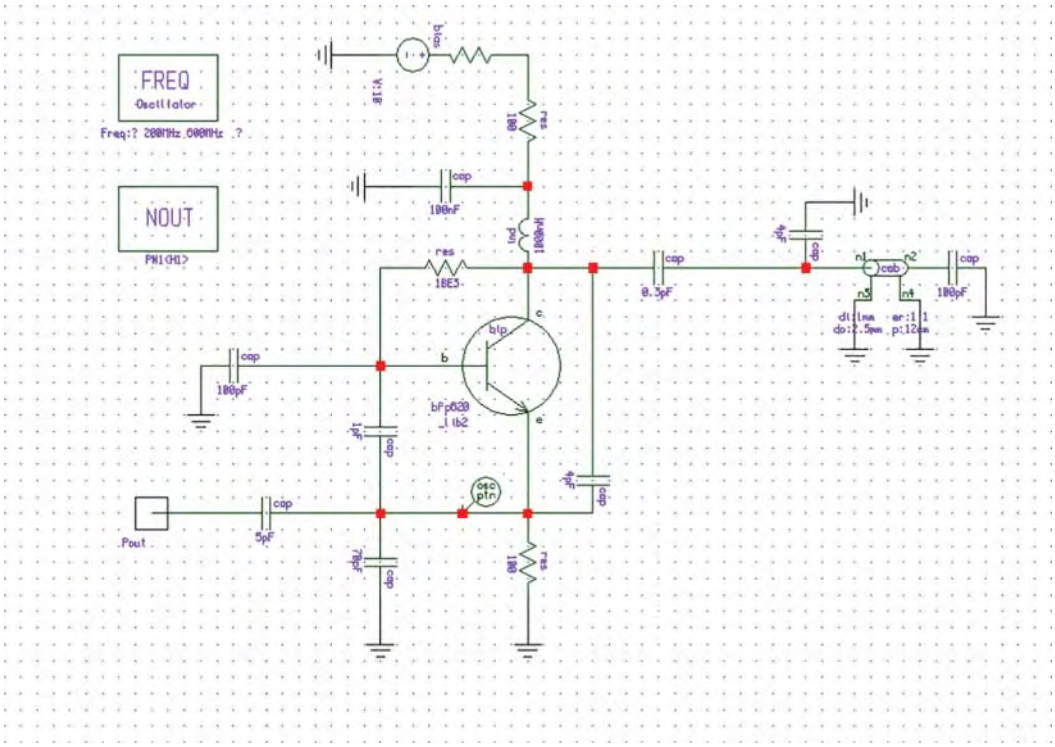


Figure A-24 Schematic of the quarter wave resonator UHF oscillator.

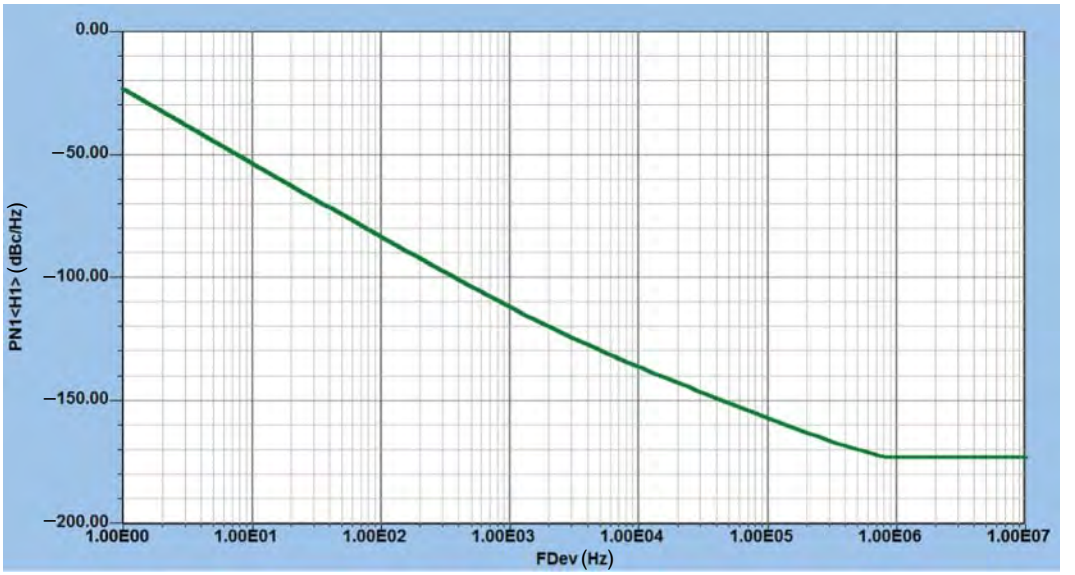


Figure A-25 Predicted phase noise; the noise break point is at about 1 kHz.

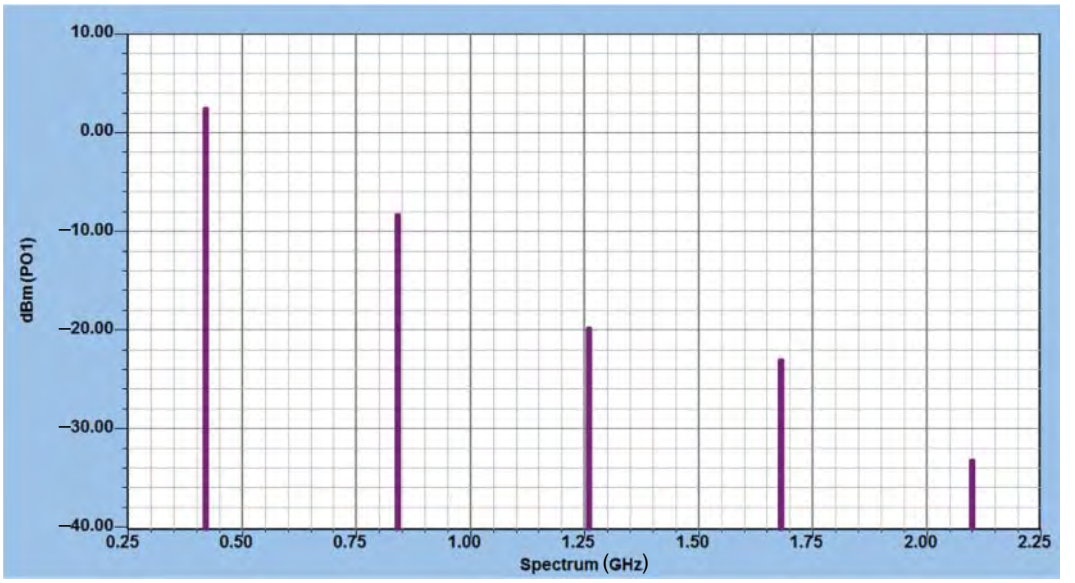


Figure A-26 Predicted output power of the oscillator.

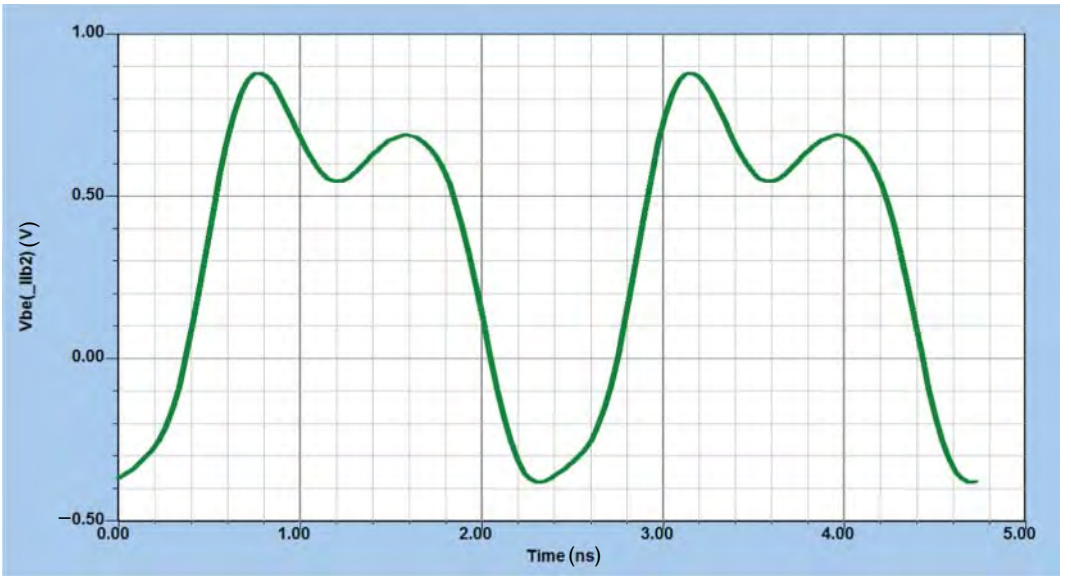


Figure A-27 Base-emitter RF voltage.

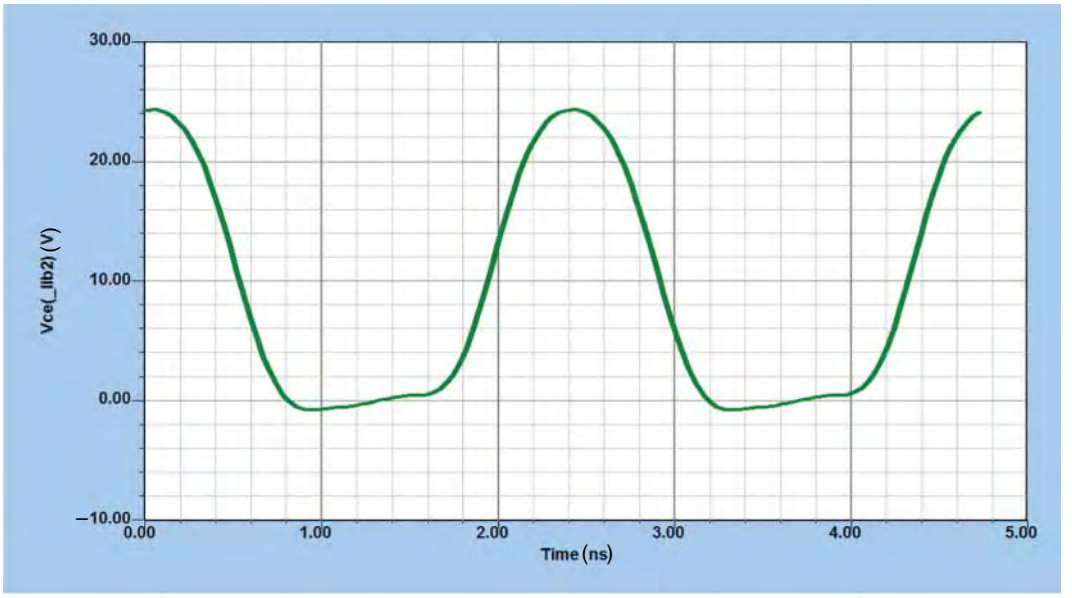


Figure A-28 Collector-emitter RF voltage.

A-7 VERY LOW PHASE NOISE VCO FOR 800 MHZ

The quarter-wavelength resonator-based oscillator (described previously), while covering a large frequency range, is subject to switching noise while moving from one frequency range to another. The circuit shown in Figure A-29 is a high-performance VCO in which the transmission line is part of the layout. While the circuit is not too different from previously described circuits, a constant-current generator is used in the emitter of the oscillator's transistor. This feedback, along with flicker noise feedback obtained by the 27-Ω resistor labeled R444, results in overall smaller phase noise than one would obtain in a conventional oscillator, eliminating the constant-current generator V436 by using a fixed resistor. The other transistors, V438 and V440, only serve as dc switches and are part of the power supply circuit. In the selection of this particular oscillator transistor, a high-dissipation device was used and is also operating at fairly high currents. However, the maximum current of the device is significantly higher and therefore, compared to this maximum value, the operating value is still smaller.

To minimize the noise in the tuning diodes, the series loss resistors are kept to 3.3 Ω, which reduces the Q of the inductors to the point where one does not observe spurious resistant frequencies and has a minimal noise contribution of its own.

Figure A-30 shows the measured phase noise for this oscillator.

A voltage-controlled "push–push" oscillator using a hair pin resonator was described by Yabucki et al. [1]. Figure A-31 shows the layout of the stepped impedance hair pin resonator with parallel coupled lines. To calculate such a structure, one needs to use a circuit simulator with electromagnetic models such as Super-Compact or an electromagnetic simulator such as Microwave Explorer, both made by Compact Software, Inc., Paterson, NJ.

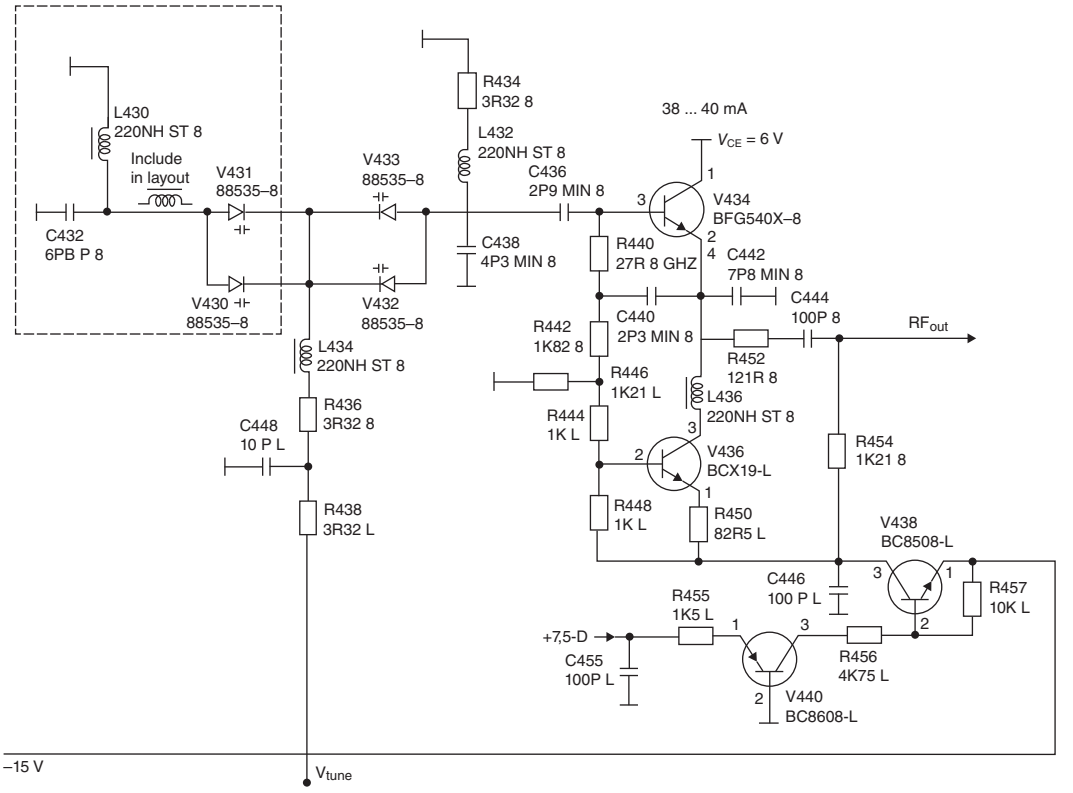


Figure A-29 Very low phase noise VCO for high-performance synthesizer application operating at 800 MHz.

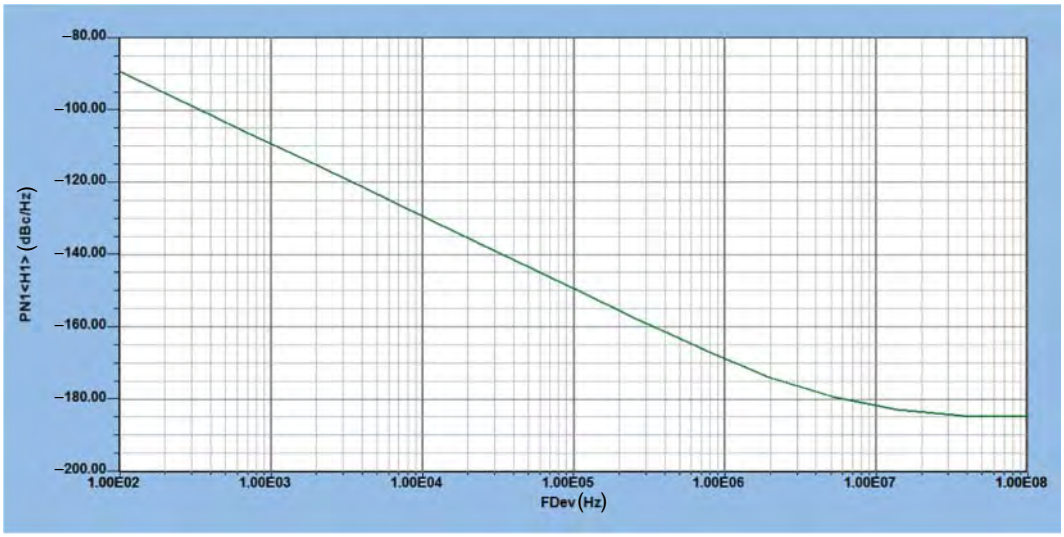
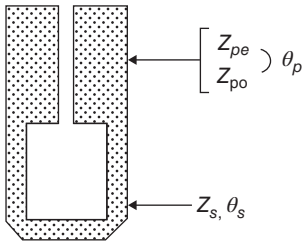


Figure A-30 Simulated phase noise of the oscillator show in Figure A-24.



Z_s	Characteristic impedence of the single line
θ_s	Electrical length of the single line
Z_{pe}, Z_{po}	Even-and odd-mode impedence of the parallel coupled lines
θ_p	Electrical length of the parallel coupled lines

Figure A-31 Layout of the stepped impedance hair pin resonator with parallel coupled lines.

Figure A-32 shows the frequency response of the resonator as a function of mode capacitor and Figure A-33 shows the voltage distribution of the hair pin resonator. One can build a push–push oscillator using this symmetrical resonator. This oscillator has certain similarities to a tuning fork oscillator using ceramic material described by Lothar Rohde around 1940 when he designed the world's first portable time/frequency standard. In the case of the time standard, the material chosen had a ±0 temperature coefficient and therefore did not require a proportional oven for maintaining constant temperature. In the case of the printed symmetrical hair pin resonator, the Q of the resonator depends solely on the chip material on which the circuit is assembled.

A push–push oscillator consists of two identical oscillators with one common resonator, where the two sides are 180° out of phase. This is applicable to the hair pin resonator and the authors [1] have shown that such an arrangement has 40-dB suppression of the second harmonic. While the third harmonic is only suppressed by about 10 dB, this is specifically due to the fact that the oscillator shows higher modes. When comparing the phase noise of a signal versus a push-push configuration (as shown in Figure A-34), an improvement of about 10 dB can be realized. A

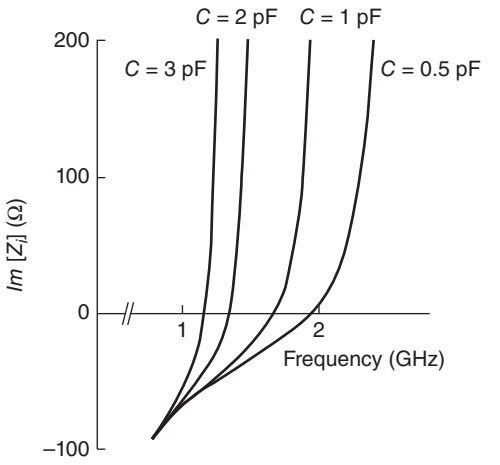


Figure A-32 Frequency response of the resonator.

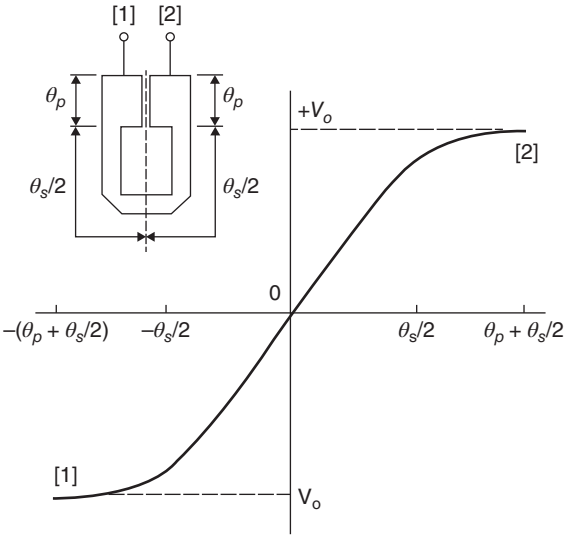


Figure A-33 Voltage distribution of the hair pin resonator.

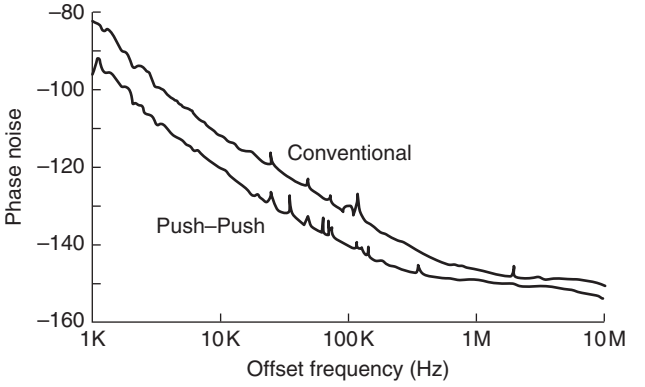


Figure A-34 Comparison between single sideband (SSB) phase noise of the conventional and push–push oscillators.

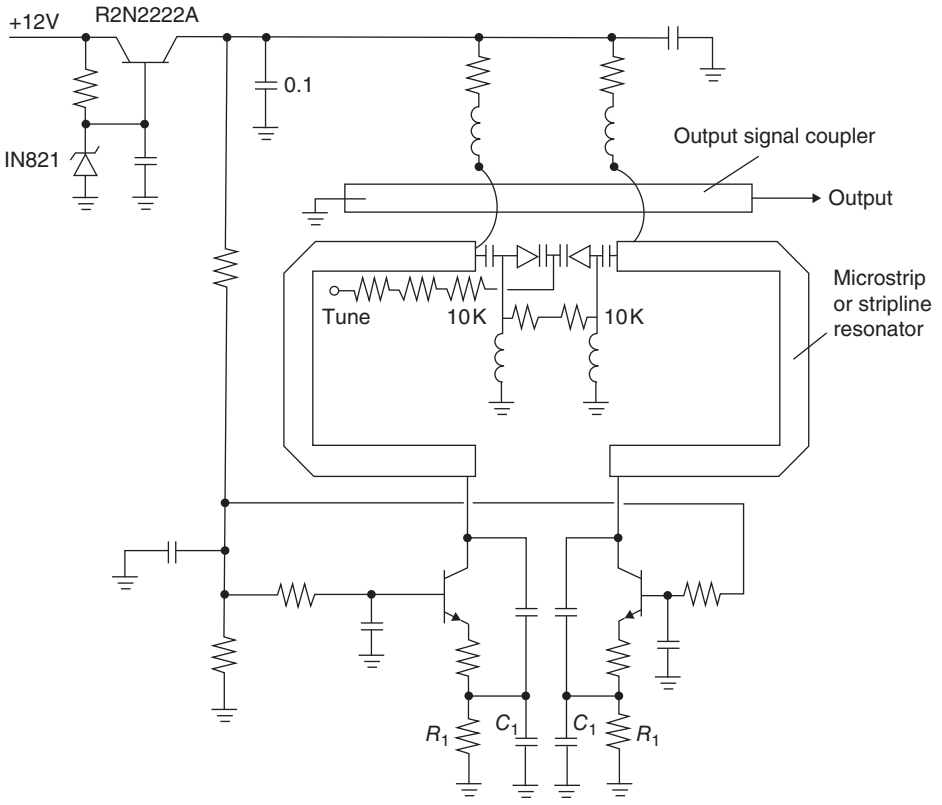


Figure A-35 Push–push VCO, based on the original [1] but modified and improved by James A. Crawford [2].

push–push arrangement helps to cancel noise from external devices; since the oscillators are also interface locked to each other, the overall performance is improved.

The actual circuit diagram is shown in Figure A-35. It is based on the original publication [1] as improved by James A. Crawford [2]. As shown in the original, the push–push arrangement has reduced the phase noise by at least 10 dB.

There are other circuits, such as feedback circuits, available, which reduce the phase noise by 10 dB or more. This is an important area where we expect to see more interesting contributions.

REFERENCES

1. Yabucki, H. et al. (1991/1992). VCOs for mobile communications. *Applied Microwave*, Winter.
2. Crawford, J.A. (1994). *Frequency Synthesizer Design Handbook*. Boston, MA: Artech House.

Microwave and Wireless Synthesizers: Theory and Design, Second Edition.
Ulrich L. Rohde, Enrico Rubiola, and Jerry C. Whitaker.
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APPENDIX B

A GENERAL-PURPOSE NONLINEAR APPROACH TO THE COMPUTATION OF SIDEBAND PHASE NOISE IN FREE-RUNNING MICROWAVE AND RF OSCILLATORS

B-1 INTRODUCTION

The harmonic balance method, used in calculating phase noise in nonlinear circuits, has some magic to it for most of us. Here is a look at our magic-lady (Figure B-1).

The amplifier shown in Figure B-2 was the world's first validation of the Compact Software Harmonic Balance Simulator, being able to correctly calculate the noise and gain of this 10 GHz amplifier. It uses measured Spice parameters. The success of the harmonic balance method was written up amongst others in *Communications Quarterly*, shown in Figure B-3, covering both amplifiers and oscillators.

We want to look at the contribution of active devices like field effect transistors (FETs) and BIPs as well as a novel algorithm for the computation of near-carrier noise in free-running microwave oscillators by the nonlinear harmonic-balance (HB) technique [1].

The application of the HB methodology to nonlinear noise analysis is very effective, because frequency-domain analysis is well suited for describing the mechanism of noise generation in nonlinear circuits. This topic has received the interest of several research teams; however, until the first edition of this book, a rigorous treatment of noise analysis in autonomous circuits had not appeared in the technical literature.

The usual approach, relying on a simple noise model of the active device and the frequency-conversion analysis, is not sufficient to describe the complex physical behavior of a noisy oscillator. Instead, we apply the following approach:

- A complete bias-dependent noise model for bipolar transistors and FETs is developed.
- The frequency-conversion approach is reviewed, and its limitations are pointed out.
- It is shown how the analysis procedure can be extended to include the case of autonomous circuits.
- The capabilities of the proposed algorithm are demonstrated by means of some application examples.

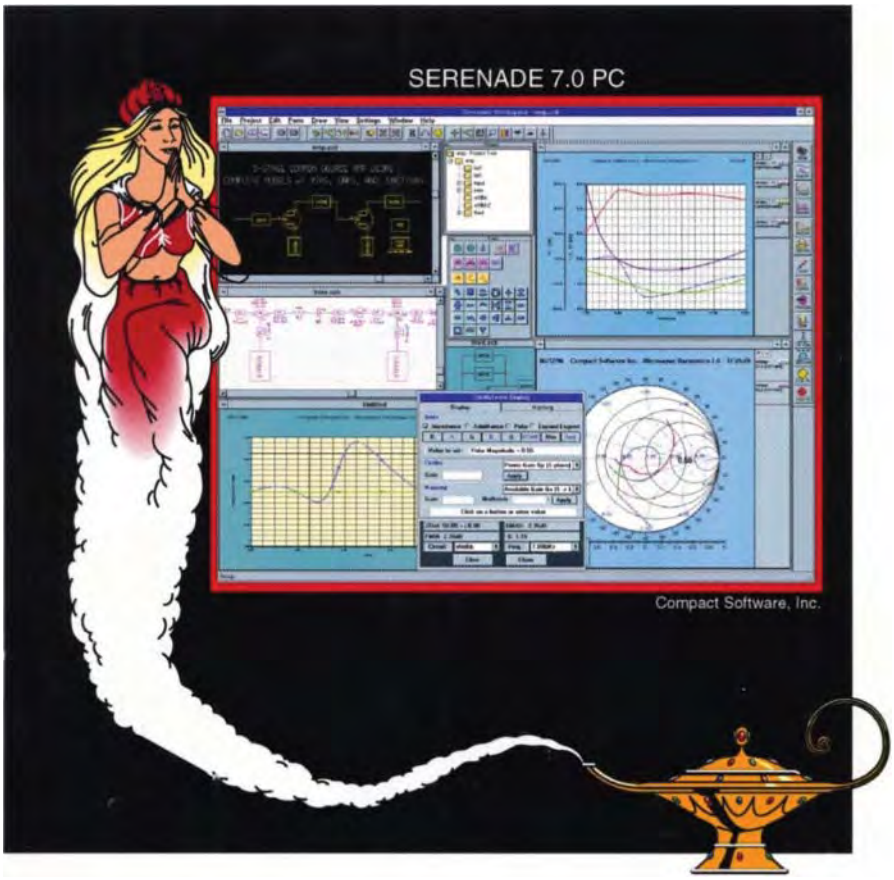

Figure B-1 Harmonic balance serenade program.

B-2 NOISE GENERATION IN OSCILLATORS

The qualitative picture of noise generation in oscillators is well known. As previously outlined, Lesson had developed a linear model,

$$\mathcal{L}(f_{\mathrm{m}}) = \frac{1}{2}\left[1 + \frac{1}{\omega_m^2}\left(\frac{\omega_o}{2Q_{\mathrm{load}}}\right)^2\right]\frac{FkT}{P_{\mathrm{sav}}}\left(1 + \frac{f_c}{f_m}\right)$$

which requires the following input parameters: (1) RF output power, (2) large signal noise figure, (3) loaded Q, and (4) flicker component. The harmonic-balance method is used to calculate the RF output power of the oscillator and at the same time calculate the loading of the tuned circuit as a function of the large-signal condition. The flicker frequency (flicker frequency corner) is a device-dependent parameter that has to be entered. A more complete expression is as follows:

$$\begin{aligned} S_\phi(f_m) = {} & [\alpha_R F_0^4 + \alpha_E (F_0/(2Q_L))^2]/f_m^3 \\ & + [(2GFKT/P_0)(F_0/(2Q_L))^2]/f_m^2 \\ & + (2\alpha_R Q_L F_0^3)/f_m^2 \\ & + \alpha_E/f_m + 2GFKT/P_0 \end{aligned}$$

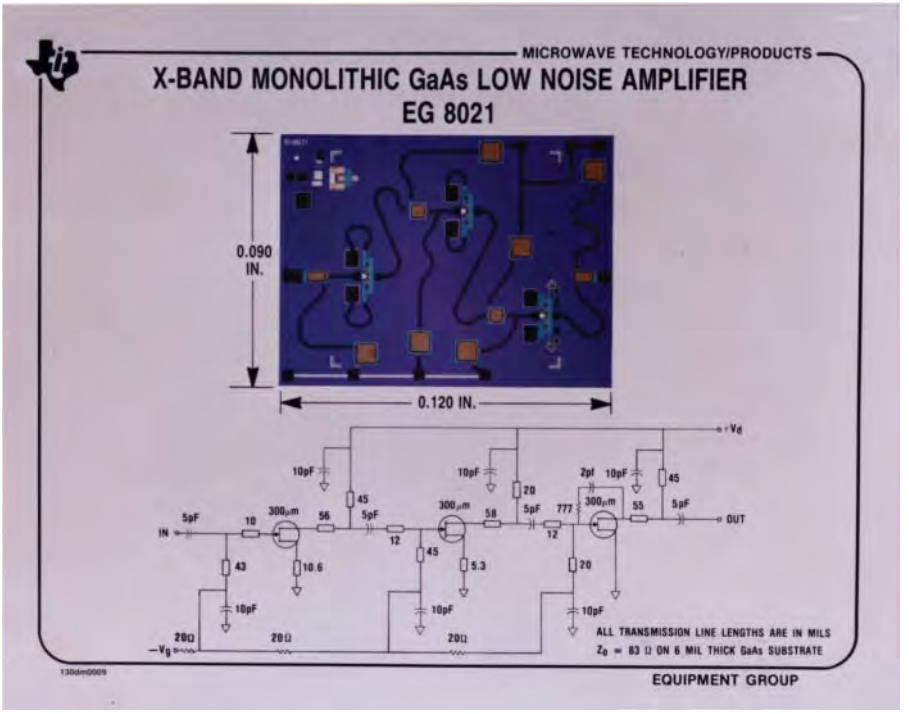

Figure B-2 Schematic of the X-band GaAs monolithic low noise amplifier (Texas Instruments).

where

G	=	Compressed power gain of the loop amplifier
F	=	Noise factor of the loop amplifier
K	=	Boltzmann's constant
T	=	Temperature (K)
P_0	=	Carrier power level (in Watts) at the output of the loop amplifier
F_0	=	Carrier frequency in Hz
f_m	=	Carrier offset frequency in Hz
$Q_L(=\pi F_0 \tau_g)$	=	Loaded Q of the resonator in the feedback loop
α_R and α_E	=	Flicker noise constants for the resonator and loop amplifier, respectively

B-3 BIAS-DEPENDENT NOISE MODEL

Figure B-4 shows the traditional Gummel–Poon [1] model for bipolar transistors. For microwave applications, the model has to be transformed into a T-equivalent circuit, as shown in Figure B-5.

To be compatible, the equivalent circuit had to be updated by adding the appropriate resistor R_{CE} to it. For the bipolar transistor, a convenient starting solution to determine the intrinsic values of R_{bb}, R_e, and C_e is a set of equations that calculate the four noise parameters F_{min}, Γ_{opt}, and R_n.

$$F_{\min} = a\frac{R_b + R_{\text{opt}}}{r_e} + \left(1 + \frac{f^2}{f_b^2}\right)\frac{1}{\alpha_0} \tag{B-1}$$

Figure B-3 Front page of *Communications Quarterly*, Spring 1995.

The optimum source resistance is

$$R_{\text{opt}} = \left\{ R_b^2 - X_{\text{opt}}^2 + \left(1 + \frac{f^2}{f_b^2}\right) \frac{r_e(2R_b + R_e)}{\alpha_0 a} \right\}^{1/2} \tag{B-2}$$

and optimum source reactance is

$$X_{\text{opt}} = \left(1 + \frac{f^2}{f_b^2}\right) \frac{2\pi f \ C_{\text{Te}} R_e^2}{\alpha_0 a}$$

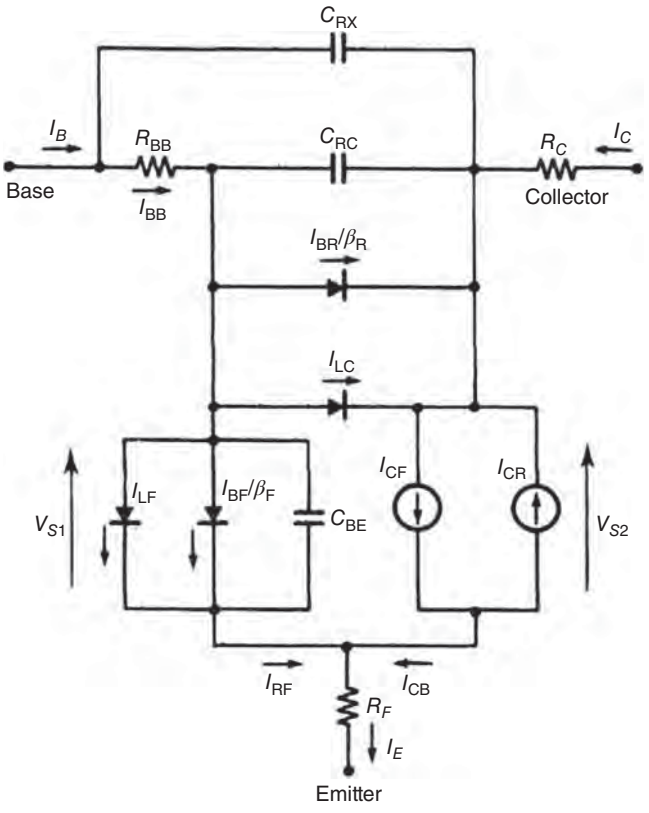

Figure B-4 Gummel–Poon bipolar transistor model.

where

$$a = \left[\left(1+\frac{f^2}{f_b^2}\right)\left(1+\frac{f^2}{f_e^2}\right)-\alpha_0\right]\frac{1}{\alpha_0} \tag{B-3}$$

$$R_n = R_b\left(A-\frac{1}{\beta_0}\right)+\frac{R_e}{2}\left(A+\left(\frac{R_b}{R_e}\right)^2\left\{1-\alpha_0+\left(\frac{f}{f_b}\right)^2+\left(\frac{f}{f_e}\right)^2+\left[\frac{1}{\beta_0}-\left(\frac{f}{f_b}\right)\left(\frac{f}{f_e}\right)\right]^2\right\}\right) \tag{B-4}$$

where

$$A = \frac{1+\left(\frac{f}{f_b}\right)^2}{a_0^2}$$

and f_b denotes the *cutoff* frequency of the common base current gain $\alpha(f)$. The aforementioned provides a convenient set of equations for representing the low-frequency noise performance of a bipolar transistor. Unlike Fukui's formula, the new expression does not involve the unity current gain frequency f_T.

These equations are based on Refs. [2, 3] and have been modified by us to reflect the modern geometry. These results have been published in the *IEEE-MTT Transactions* [4]. Further information can be found in Ref. [5]. Based on actual noise measurements, they predict the starting values for the base spreading resistor R_{bb} and the input capacitor C_e in schematic, while the emitter diffusion resistor can be calculated directly from the dc bias point. These values have better accuracy than the traditional Gummel–Poon parameter extraction for the large-signal bipolar model. A typical set of parameters for a microwave resistor is shown in Table B-1. These are the results of

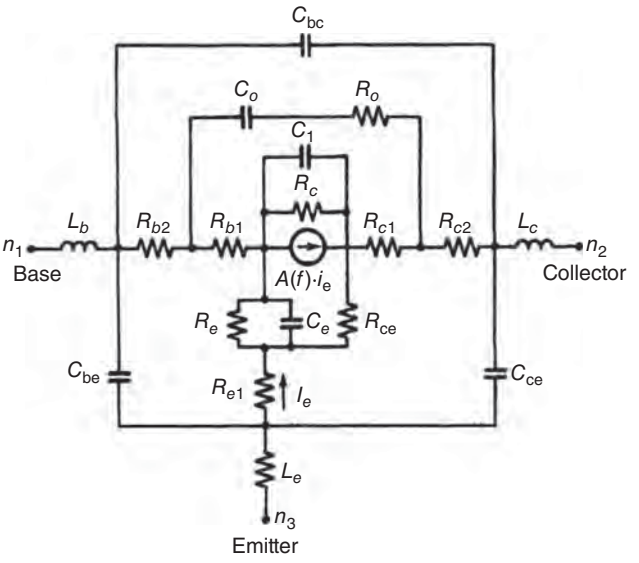

Figure B-5 Small-signal T-model derived from linear hybrid π model. Note the additional resistor R_{CE}, which is necessary for modeling reasons.

a parameter extraction method using different dc bias points and ensuring that the noise measurements agree with the predictions. Subsequently, by invoking the transformation from the hybrid π to the T model, one obtains the dc or small-signal equivalent circuit for the transistor under the bias point chosen. The calculation of the four noise parameters, which is now based on the various dc bias points, generates a table that can be used for interpolation and can be translated into the equivalent noise correlation matrix.

Figure B-6 shows the measured and modeled noise based on the parameter extraction.

A similar approach is possible with GaAs FETs. Figure B-7 shows the linear equivalent circuit for GaAs FETs, and Figure B-8 shows the large-signal equivalent circuit for which we have used the Materka model. An important feature is that the large-signal model using small-signal conditions generates the same set of *S*-parameters from the equivalent small-signal circuit.

Noise performance of microwave circuits is one of the major concerns of circuit design engineers. It is an important determining factor of receiver system sensitivity and dynamic range. Since the noise correlation matrix has been introduced, noise analysis of microwave linear circuits has been available and implemented in general-purpose computer-aided design (CAD) tools. However, in the practical world, most microwave circuits need to be analyzed using nonlinear analysis techniques.

This section illustrates how the noise performance of general mixer circuits can be simulated by using the harmonic-balance technique implemented in Microwave Harmonica v4.0, a workstation product made by Compact Software, Inc.

Noise in a microwave FET is produced by sources intrinsic to the device. If the equivalent noisy circuit of an intrinsic FET device is represented as in Figure B-9, the correlations of the gate and drain noise current sources are

$$\langle |I_c|^2 \rangle = 4K_B T \Delta f g_m P \tag{B-5}$$

$$\langle |I_g|^2 \rangle = 4K_B T \Delta f \frac{\omega^2 c_{gs}^2}{g_m} R \tag{B-6}$$

$$\langle I_g I_c^* \rangle = 4K_B T \Delta f j \omega_{gs} \sqrt{PRC} \tag{B-7}$$

Table B-1 Small- and large-signal parameters of an intrinsic transistor[a].

MICROWAVE HARMONICA PC V5.0			
File: bfr965s.ckt			
*	Linear/NON Linear BIP description:		
*			
	BIP 53 56 58		
+	; LINEAR parameters:		
+	LB = 0	LC = 0	LE = 0
+	RB2 = 0	RC2 = 0.931	CBE = 0
+	CCE = 0	CBC = 0	LBT = 0
+	ZBT = 50	LCT = 0	ZCT = 50
+	LET = 0	ZET = 50	CBEP = 0
+	CBCP = 0	CCEP = 0	RE1 = 0.53
+	RC1 = 0	RO = 0	T = 0
+	F = 8.868E+009	CO = 9.452E-013	RB1 = 7.869
+	A = 0.9686	RC = 1E+030	CI = 1.667E-013
+	RE = 0.4097	CE = 2.331E-010	RCE = 2337
+	TJ = 293		
+	{		
+	; NONLINEAR parameters:		
+	BF = 169	BR = 16.43	NF = 0.975
+	NE = 1.527	NR = 1.007	NC = 1.097
+	IS = 1.6E=016	ISE = 1.645E-014	ISC = 2.252E-015
+	VA = 117	VB = 1.782	IKR = 0.05949
+	IKF = 0.157	RE1 = 0.53	RC2 = 0.931
+	RBM = 0.025	RB = 10.24	IRB = 0.01051
+	TR = 0	TF = 1.8E-011	ITF = 1
+	XTF = 84	VTF = 0.7	FCC = 0.5
+	VJE = 1.079	MJE = 0.471	CJE = 5.46E-012
+	XCJC = 0.15	CJC = 2.631E-012	VJC = 0.106
+	MJC = 0.21	TJ = 293	XTB = 0
+	XTI = 3	TRE1 = 0	TRE2 = 0
+	TRB1 = 0	TRB2 = 0	TRM1 = 0
+	TRM2 = 0	TRC1 = 0	TRC2 = 0
+	TNOM = 293	VCMX = 11	IBMX = 9.973E+011
+	IBMN = 0	NPLT = 6	NAME = BIP_NPN
+	ANA = OFF	MODEL = NPN	RB2 = 0
+	LB = 0	LC = 0	LE = 0
+	CBE = 0	CCE = 0	CBC = 0
+	LBT = 0	ZBT = 50	LCT = 0
+	ZCT = 50	LET = 0	ZET = 50
+	CBEP = 0	CBCP = 0	CCEP = 0
+	}		

[a]The small-signal parameters were generated from the large-signal model at the dc operating point of 90 mA.

and the correlation matrix of the noise current sources is

$$C_{\mathrm{dc}}(\omega) = \frac{2}{\pi} K_B T d\omega \begin{bmatrix} \dfrac{\omega^2 C_{\mathrm{gs}}}{g_m} R & -j\omega C_{\mathrm{gs}} \sqrt{PRC} \\ j\omega C_{\mathrm{gs}} \sqrt{PRC} & g_m P \end{bmatrix} \tag{B-8}$$

The gate and drain noise parameters R and P and the correlation coefficient C are related to the physical noise sources acting in the channel and are thus functions of the device structure and bias point. These noise parameters at

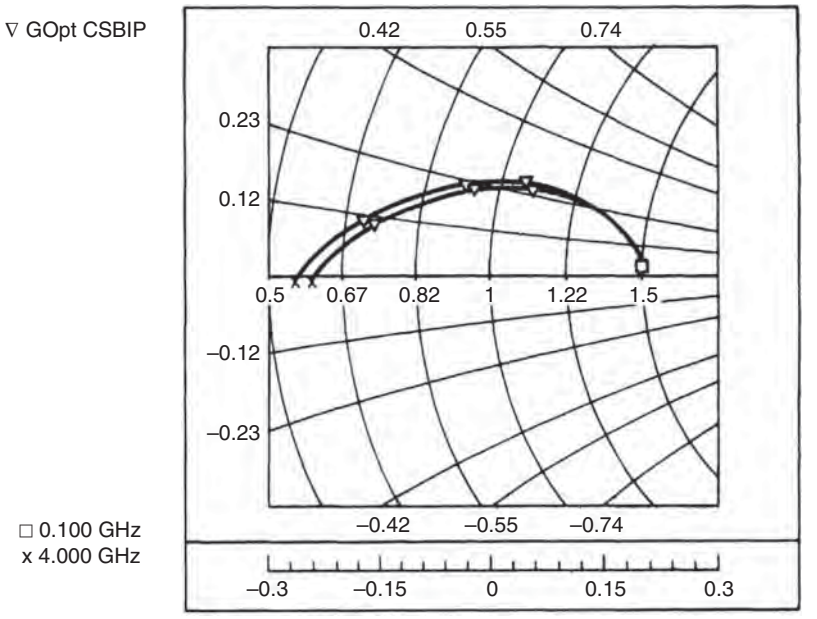

Figure B-6 Measured and modeled noise based on the parameter extraction.

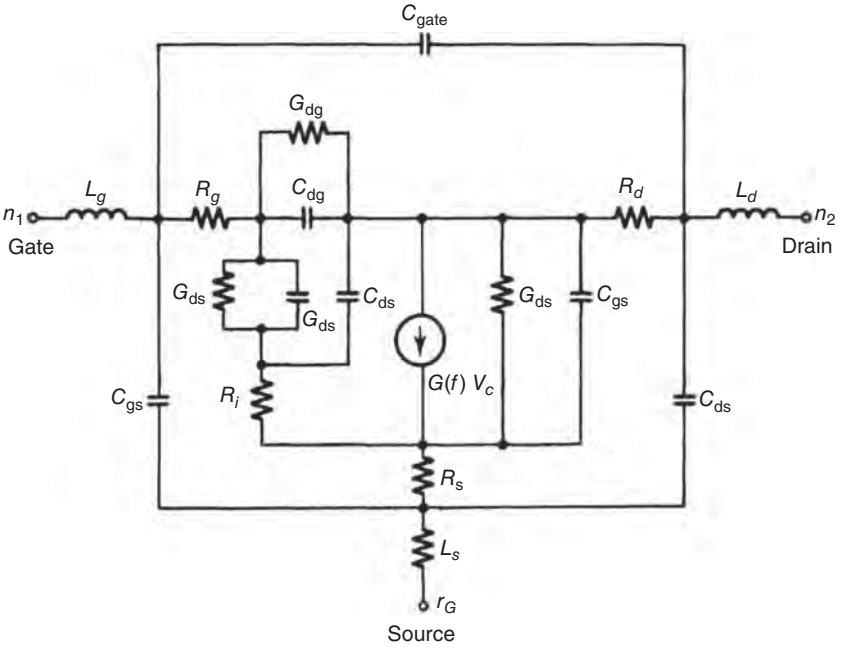

Figure B-7 Linear equivalent circuit of FET, which can be derived from Figure B-8, the large-signal equivalent circuit.

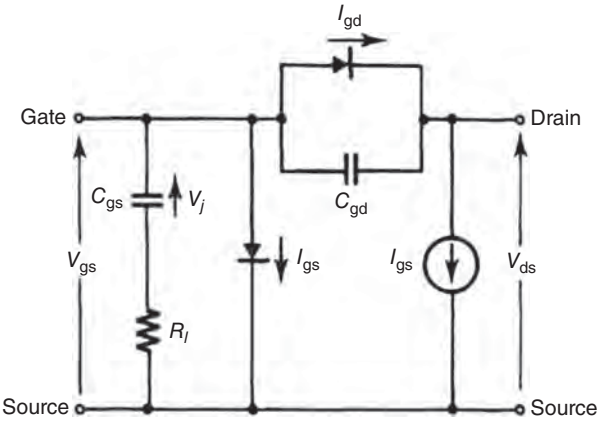

Figure B-8 Intrinsic Curtice–Ettenberg model for the MESFET. Other useful models are the Materka–Kacprzak model for the MESFET (best for millimeter-wave applications), the Statz model, and the Triquint's own model (TOM).

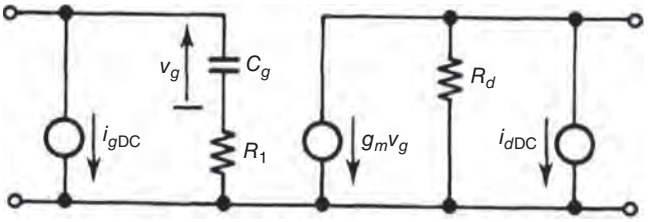

Figure B-9 Equivalent noise circuit of an intrinsic FET device.

a certain bias point can be calculated explicitly from measured device noise parameters using a noise de-embedding procedure. That is, by defining measured noise parameters, $F_{\min}$, R_n, and Γ_{opt}, and using the Super-Compact noise de-embedding procedure, the noise correlation matrix of an FET device can be determined.

The next step is to develop a bias-dependent model. This is necessary because one has to develop an analysis program that can handle the noise effect in conjunction with a general-purpose harmonic-balance simulator. The method to be used is concerned with an extension of the usual linearization adopted to apply the piecewise linear balance technique. For our purposes, the nonlinear subnetwork is a collection of intrinsic FET chips with all (linear) parasitic elements included in the linear subnetwork. These linear components are the time-averaged values as a function of the local oscillator (LO) pumping and the dc bias. It is therefore necessary to develop a bias-dependent model that can be used to obtain the necessary foundry coefficients. Using the noise correlation technique, they have been based on a de-embedding technique using measurements of the four noise parameters at a test frequency like 10 GHz. This de-embedding technique is the subject of another paper [6], while the general treatment of this had already been published [7].

This method is accurate enough that measured data and predicted data agree quite well. Table B-2 shows the corresponding correlation between the two. In the case of the bipolar transistor, the novel approach in generating the starting values for the Gummel–Poon model is using small-signal noise data as seed values first and then refining the values for different bias points. This is somewhat easier because the bipolar transistor in the Gummel–Poon approach is a physics-based model, while the Materka model is the result of a curve fit and has no physical equivalent.

Table B-3 shows the R, P, and C values of a MESFET as a function of bias, which are a result of calculation and measurement.

Table B-2 Corresponding correlation between the Gummel–Poon model predictions and the measurements of the chip: V_c = 10 V at 4 mA.

Frequency (GHz)	F_{min} (dB) CSBIP	MG_{opt} (mag) CSBIP	PG_{opt} (°) CSBIP	Run (Ω) CSBIP
		Gummel–Poon model predictions		
0.500	1.16	0.138	41.7	8.363
1.000	1.30	0.165	79.8	8.381
1.500	1.49	0.214	106.8	8.411
2.000	1.72	0.272	123.8	8.454
2.500	1.97	0.329	134.8	8.510
3.000	2.23	0.379	142.2	8.578
3.500	2.50	0.423	147.6	8.660
4.000	2.77	0.461	151.6	8.756
Frequency (GHz)	F_{min} (dB) HPBIP	MG_{opt} (mag) HPBIP	PG_{opt} (°) HPBIP	Run (Ω) HPBIP
		Gummel–Poon model predictions		
0.500	1.20	0.148	37.2	8.886
1.000	1.34	0.164	74.5	8.907
1.500	1.54	0.205	103.4	8.943
2.000	1.78	0.259	122.0	8.993
2.500	2.05	0.314	133.7	9.057
3.000	2.32	0.364	141.6	9.137
3.500	2.60	0.408	147.2	9.232
4.000	2.88	0.446	151.4	9.343

Table B-3 The *R*, *P*, and *C* values of an MESFET as a function of bias.

			P values				
I_{ds}/I_{dss}							
0.85	2.742	2.850	2.860	2.851	2.846	2.857	
0.70	2.181	2.482	2.556	2.569	2.571	2.581	
0.50	1.576	1.939	2.051	2.078	2.083	2.089	
0.30	1.307	1.460	1.527	1.541	1.540	1.541	
0.15	1.358	1.263	1.254	1.246	1.240	1.242	
0.05	1.358	1.390	1.339	1.321	1.317	1.327	
	0.25 V	0.70 V	1.10 V	1.50 V	2.10 V	2.70 V	V_{ds}
			R values				
I_{ds}/I_{dss}							
0.85	0.122	0.173	0.152	0.175	0.259	0.238	
0.70	0.131	0.193	0.180	0.211	0.306	0.294	
0.50	0.146	0.194	0.178	0.210	0.302	0.299	
0.30	0.192	0.215	0.200	0.231	0.315	0.332	
0.15	0.236	0.265	0.274	0.315	0.400	0.450	
0.05	0.236	0.283	0.328	0.380	0.464	0.538	
	0.25 V	0.70 V	1.10 V	1.50 V	2.10 V	2.70 V	V_{ds}
			C values				
I_{ds}/I_{dss}							
0.85	0.211	0.430	0.537	0.592	0.621	0.650	
0.70	0.217	0.441	0.552	0.608	0.639	0.668	
0.50	0.230	0.456	0.570	0.628	0.661	0.691	
0.30	0.253	0.485	0.603	0.665	0.700	0.732	
0.15	0.279	0.535	0.665	0.735	0.775	0.810	
0.05	0.279	0.612	0.768	0.852	0.901	0.943	
	0.25 V	0.70 V	1.10 V	1.50 V	2.10 V	2.70 V	V_{ds}

In generating large-signal models, a set of starting values is required. In the case of bipolar transistors, we use the values that are supported by the noise calculation. The standard parameter extraction programs, like in the HP TCAP program or the IC-CAP, are insufficient to obtain some of the microwave properties. In particular, the intrinsic delay times and, in the case of the bipolar transistors, the base-spreading resistor parameter extraction do not show enough sensitivity. We have seen variations of 5:1. In some cases, the standard large-signal parameter extraction program has provided a base-spreading resistor of 50 Ω, while the noise modeling approach has calculated 10 Ω with the correct value being 8 Ω. As an example, $R_n = 0.2$ transforms into $0.2 \times 50 = 10\ \Omega$. The equivalent circuit generation of the FET parameters, particularly the parasitics, is summarized in Ref. [7]. The intrinsic value of the devices, however, can be obtained by the method shown.

B-3-1 Bias-Dependent Model

We now describe our bias-dependent small-signal FET model, which is used for the piecewise linear harmonic-balance technique. We stress the word "small" since the model is not a nonlinear one, but a linear one. A bias-dependent small-signal model serves two purposes: (1) it permits "tweaking" of the monolithic microwave integrated circuit (MMIC) by external (bias voltage) means and (2) it introduces another degree of freedom in "noise matching." The first application is important since MMICs, by their very nature, do not permit on-chip adjustments: indeed, this would be counter to the whole purpose of the MMIC approach. Therefore, only external means of adjustment are allowed. The second application is important because it allows one to achieve a better compromise between a noise match and a power-gain match than one could possibly reach by a matching circuit technique alone.

We believe very strongly that one cannot derive a bias-dependent linear FET model from a nonlinear FET model that would be sufficiently accurate to satisfy the critical MMIC designer. The reason for our belief is that whereas a nonlinear nonphysical based model is obtained by some "curve-fitting" technique, which will be adequate for large-signal excursions, this fitting procedure makes no attempt to match the *derivative* of the nonlinear function that one is fitting. But small-signal parameters are derivatives of a nonlinear function; therefore, one cannot ensure accuracy by this method by deriving the small-signal parameters. Rather, we believe that the required accuracy can be obtained by directly measuring the small-signal performance as a function of bias voltages and then *fitting* this dependence by some simple function. This simple function is no more complicated than a second-degree polynomial, that is, a quadratic function.

We restrict the model to "above the knee" operations, since it is a rare occasion that one would operate the FET as a linear device below the knee. We recognize, also, that the greatest dependence of the model parameters is on the gate-source voltage. The drain-source voltage plays a secondary role. Indeed, the dependence on the latter voltage is in most cases simply a linear one.

B-3-2 Derivation of the Model

For a selected set of drain-source bias voltages, one may represent any small-signal FET parameter in one of the following forms:

$$P(V_{\text{gs}}) = a + b(V_{\text{gs}} - V_p) + c(V_{\text{gs}} - V_p)^2 \tag{B-9}$$

or

$$P(I_{\text{ds}}) = a' + bI_{\text{ds}}^{0.5} + c'I_{\text{fs}} \tag{B-10}$$

where P represents any of the small-signal equivalent circuit parameters and the desired expansion coefficients. Here V_{gs}, V_p, and I_{ds} denote the gate-source bias voltage, the pinch-off voltage, and the drain-source bias current, respectively. Since the parameter P is temperature dependent, the expansion coefficients also are a function of temperature, albeit mild ones and most probably negligible. This has been verified, however, by analysis of the data taken on a group of devices.

Note that Eq. (B-10) is in reality a quadratic polynomial in the square root of I_{ds}. This form follows directly from Eq. (B-9) because of the nearly quadratic dependence of drain current on gate-source bias that we have observed with many devices. We shall show samples of this dependence for a small pinch-off device ($V_p = 1.8$ V).

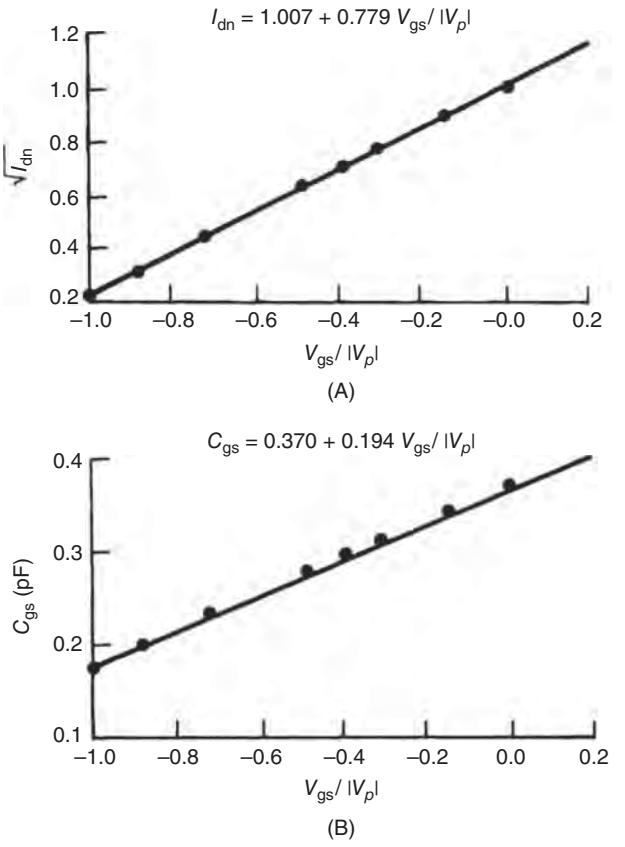

Figure B-10 Linear dependence of (A) normalized drain current and (B) gate-source capacitance on gate-source bias voltage.

Figure B-10 illustrates the quadratic dependence of I_{ds} on V_{gs} and the linear dependence of C_{gs} on V_{gs}. The fits are "perfect," as evidenced by the fact that the coefficients of the quadratic terms are zero. Figure B-11 shows, however, that in some cases quadratic terms are necessary. Although we have found that g_m usually can be fitted with a linear function for small pinch-off devices (this example being an exception), a quadratic term is usually necessary for large pinch-off devices (V on the order of 3–6 V). A quadratic term is always required for g_{ds}, however, regardless of pinch-off voltages. Some of the other model parameters such as the delay times usually require a quadratic term, although a linear approximation will probably suffice because of the insensitivity of the device performance to this quantity.

In a mixer or oscillator, the active device is not only dc biased but also pumped by the LO. At the dc bias point of the device, the nonlinear noise sidebands are uncorrelated and are dependent on the bias point. When the device is pumped by the LO, the nonlinear noise sidebands are modulated accordingly and are partially correlated because each sideband is a combination of the original uncorrelated dc sidebands. During mixing, each sideband generates a correlated component in the vicinity of the intermediate frequency (IF). To determine the correct nonlinear noise power contribution, the correlation of the sidebands must be considered in the analysis. Similarly, contributions to the noise power at the IF load are made by the thermal noise generated by the linear network through frequency conversion in the mixer. The thermal noise is not dependent on the LO excitation and, because it is uncorrelated, its noise power contribution is additive.

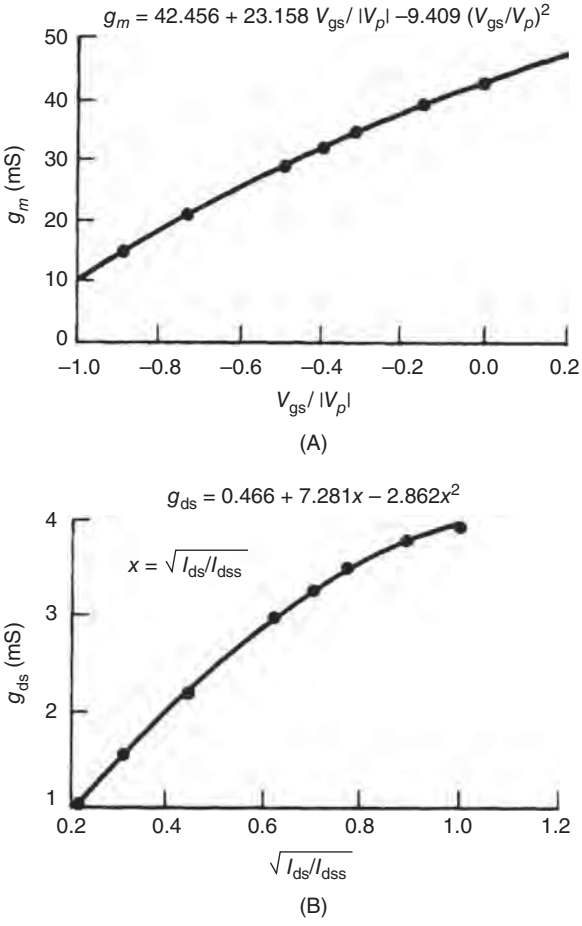

Figure B-11 Quadratic dependence of transconductance on gate-source voltage (A) and drain-source conductance on the square root of the normalized drain current (B).

B-4 GENERAL CONCEPT OF NOISY CIRCUITS

In the evaluation of a two-port, it is important to know the amount of noise added to a signal passing through a network.

$$\frac{S_{\text{in}}}{N_{\text{in}}} \rightarrow \text{Network} \rightarrow \frac{S_{\text{out}}}{N_{\text{out}}} \tag{B-11}$$

An important parameter for expressing this characteristic is the noise factor (or noise figure).

$$\text{Noise factor} = F = \frac{S_{\text{in}}/N_{\text{in}}}{S_{\text{out}}/N_{\text{out}}}$$

$$\text{Noise figure} = \text{NF} = 10\ \log(F) \tag{B-12}$$

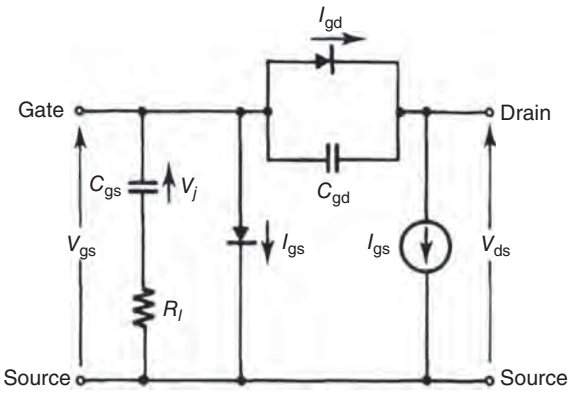

Figure B-12 Chain of amplifiers.

The noise figure of cascaded networks can be calculated by the following approximations shown in Figure B-12. The approximation assumes a 50-Ω resistive termination. The correct and frequently overlooked method for this, of course, is the noise correlation matrix.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots \tag{B-13}$$

The sources of the internal noise in a general circuit are described next.

B-4-1 Noise from Linear Elements

Thermal noise is related to the admittance of the elements:

$$C_n(\omega) = \frac{1}{\pi} K_B T \delta\omega [Y(\omega) + Y^*(\omega)] \tag{B-14}$$

A noise network can be treated as a noiseless network with equivalent noise current source at each external port.

The correlation of the noise current sources of a linear network is related to the Y matrix of this network. This is shown in Figure B-13.

The intrinsic noise sources of an active device (e.g., metal–semiconductor field-effect transistor (MESFET), bipolar junction transistor (BJT)) are at the input and the output as shown in Figure B-14. The intrinsic noise model can be expressed by four measured parameters:

$F_{\min}$	Minimum noise figure
R_n	Equivalent normalized noise resistance
MG_o	Magnitude of the optimal noise reflection coefficient
PG_o	Phase of the optimal noise reflection coefficient

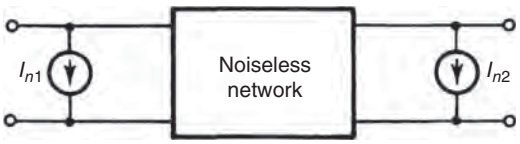

Figure B-13 Noiseless circuit noise sources at the input and output.

Figure B-14 Noiseless FET with noise sources at the input and output.

From these four parameters, the Van der Ziel noise model can be derived as

$$C_n(\omega) = \frac{2}{\pi} K_B T \delta\omega \begin{bmatrix} \dfrac{\omega^2 C_{gs}^2}{g_m} R & -j\omega C_{gs}\sqrt{PR}C \\ j\omega C_{gs}\sqrt{PR}C & g_m P \end{bmatrix} \tag{B-15}$$

This conversion, shown in Figure B-14 for all active devices, has been implemented in both Super-Compact and Microwave Harmonica.

In addition, we have to add the flicker noise of an active device (1/*f* noise), as displayed in Figure B-15.

We now look at the noise model of the active device when pumped by an LO. The noise sources and equivalent circuit model parameters are modulated by the LO. This is indicated in Figure B-16.

The noise correlation matrix of the device is modulated by the LO. This means

$$R, P, C, g_m, C_{gs}, \ \ldots \ = f(V_{gs}, V_{ds}) \tag{B-16}$$

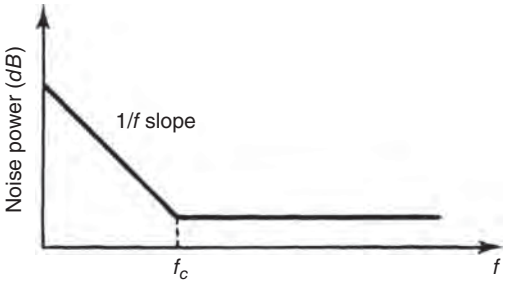

Figure B-15 The major parameter used to describe the flicker noise is f_c (corner frequency).

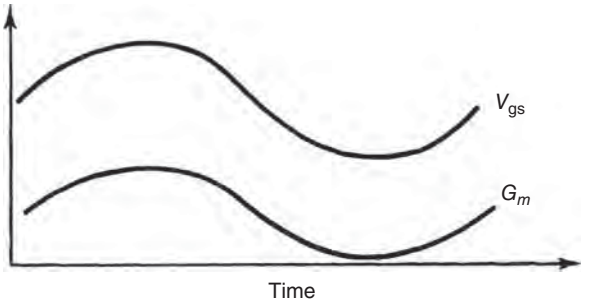

Figure B-16 The voltages and currents of devices are determined by harmonic-balance calculations.

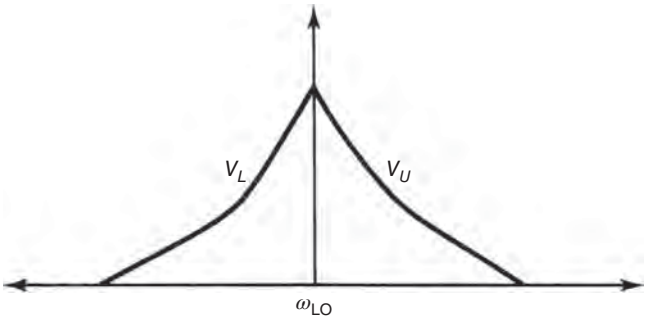

Figure B-17 LO signal with noise sidebands.

In addition, the flicker noise is modulated by the drain current using the following equation:

$$\left\langle |I_f|^2 \right\rangle = 2K_B T\delta\omega Q\frac{|I_D|^\beta}{f^\alpha} \tag{B-17}$$

If we consider an oscillator as a mixer driven by a noisy source, we have to consider the noise contribution of the external sources (LO). The source noise is given by the single sideband (SSB) RF spectrum, and the amplitude. Noise or frequency fluctuation is a set of frequency deviations from the carrier. This is frequently referred to as the *spectrodensity* of a signal, as shown in Figure B-17.

B-5 NOISE FIGURE OF MIXER CIRCUITS

In order to calculate the noise figure of a mixer circuit, we need to calculate the total internal noise of the circuit at the IF frequency.

Noise Analysis Step 1. Do the harmonic-balance analysis to determine the steady state of the mixer. Figure B-18 shows the arrangement. The harmonic-balance calculation determines the Fourier coefficients of voltages and currents of the circuit. Any receiver configuration (e.g., low-noise amplifiers (LNAs), IF amplifier, etc.) may be considered.

Noise Analysis Step 2. Calculate the transfer functions of the sideband signals to the IF band signal. The noise at each sideband frequency contributes to the noise at the IF through frequency conversion, as shown in Figure B-19. The block diagram, Figure B-20, is a summary of the IF noise contributions in a general nonlinear mixer circuit. Please note the large number of contributing elements that make up the total noise at the output.

The calculation of dN is performed by Eq. (B-20), where the intermediate steps are given in Ref. [8].

$$\langle|\delta\Phi|^2(f_d)\rangle = \frac{\langle|V_l(f_d)|^2\rangle + \langle|V_u(f_d)|^2\rangle - 2\mathrm{Re}\{\langle V_i^*(f_d)V_u^*(f_d)\rangle\exp(2j\Phi_0)\}}{|V_0|^2} \tag{B-18}$$

$$\langle|\delta A|^2(f_d)\rangle = 2\frac{\langle|V_l(f_d)|^2\rangle + \langle|V_u(f_d)|^2\rangle + 2\mathrm{Re}\{\langle V_i^*(f_d)V_u^*(f_d)\rangle\exp(2j\Phi_0)\}}{|V_0|^2} \tag{B-19}$$

$$\begin{aligned} dN(\omega_{\mathrm{IF}}) &= R_{\mathrm{IF}}\sum_p T_{0p}C_L(\omega_{\mathrm{IF}}+p\omega_0)T_{0p}^* \\ &= +R_{\mathrm{IF}}\sum_{p,q} T_{0p}\left[\sum_s H_{p-s}C_{\mathrm{dc}}(\omega_{\mathrm{IF}}+s\omega_0)H_{s-q}\right]T_{0q}^* \\ &= +R_{\mathrm{IF}}\sum_{p,q} Y_p^s\begin{bmatrix}\langle|V_u(\omega_{\mathrm{IF}})|^2\rangle & \langle V_u(\omega_{\mathrm{IF}})V_l^*(\omega_{\mathrm{IF}})\rangle \\ \langle V_u^*(\omega_{\mathrm{IF}})V_l(\omega_{\mathrm{IF}})\rangle & \langle|V_l(\omega_{\mathrm{IF}})|^2\rangle\end{bmatrix}Y_q^{s*} \end{aligned} \tag{B-20}$$

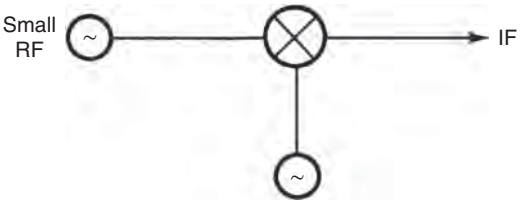

Figure B-18 Mixer arrangement.

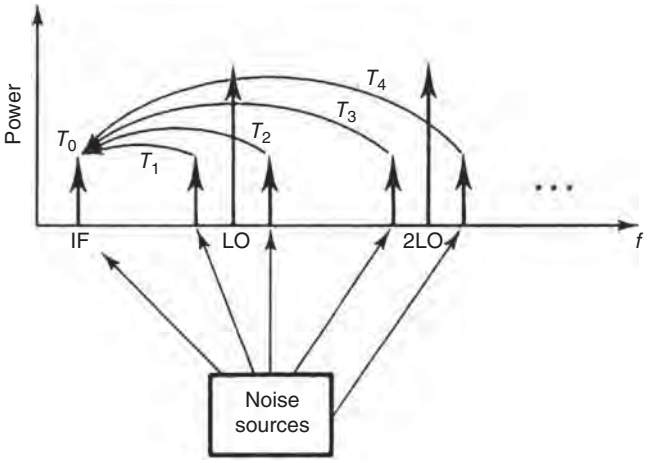

Figure B-19 Summary of noise sources mixed to the IF.

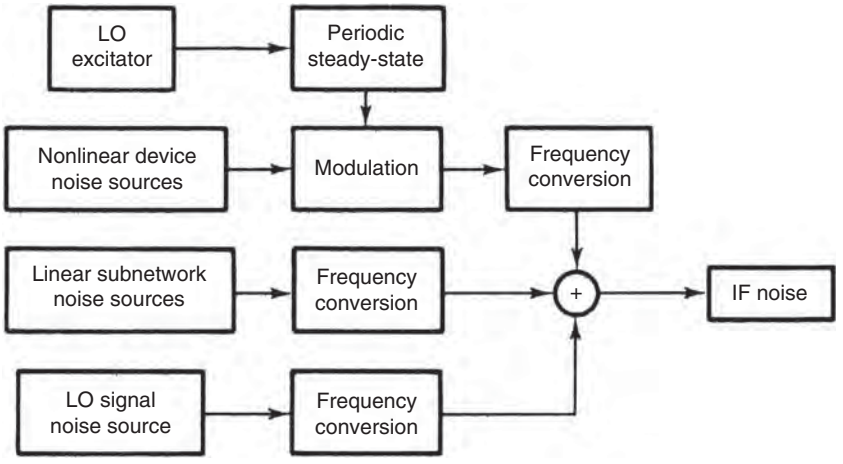

Figure B-20 Summary of IF noise contributions.

The noise sources at sideband and baseband frequencies contribute to near-carrier noise through frequency conversion. The noise contribution is significant at deviations far from the carrier, as shown in Figure B-22.

In Eq. (B-20), the T_{0x} terms are the sideband-to-IF conversion matrices; H_x terms are the spectral modulation components of the device; p, q, r, and s are sideband spectral indices; R_{IF} is the IF load; Y is a conversion admittance matrix between the LO noisy source and the IF load at the IF frequency; and ω_{IF} is a small frequency deviation in the neighborhood of the baseband frequency. The first term represents the noise contribution of the linear network, the second term is the noise contribution from the modulated nonlinear devices, and the third term is the noise contribution of the noisy LO.

B-6 OSCILLATOR NOISE ANALYSIS

The effect of the LO frequency (f_o) and its noise can be determined through perturbation analysis. The noise sources modulate the carrier frequency. Flicker noise is the predominant noise source. The arrangement in Figure B-21 looks similar to the mixer of Figure B-18. The near-carrier noise is proportional to the flicker, thermal, and device shot noise power and is inversely proportional to Q^2 of the oscillator. As shown in the block diagram, the noise contains the flicker components and the noise calculated via the correlation matrix.

The physical effects of random fluctuations taking place in the circuit are different depending on their spectral allocation with respect to the carrier:

- Noise components at low-frequency deviations
  - Frequency modulation of the carrier
  - Mean square frequency fluctuation proportional to the available noise power
- Noise components at high-frequency deviations
  - Phase modulation (PM) of the carrier
  - Mean square phase fluctuation proportional to the available noise power

The main purpose of this chapter is to show that the same results can be quantitatively derived from the nonlinear HB equations of the autonomous circuit and how the general nonlinear approach uses a nonlinear BIP or FET model for the noise calculation.

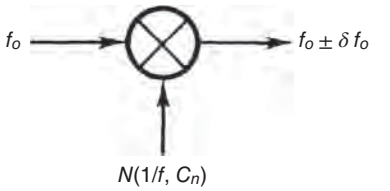

Figure B-21 Oscillator signal modulated by noise sources including flicker noise.

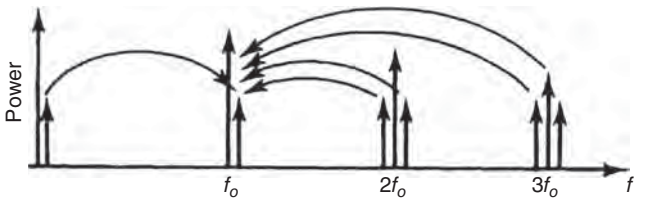

Figure B-22 Noise sources at different frequencies contribute to the near-carrier noise.

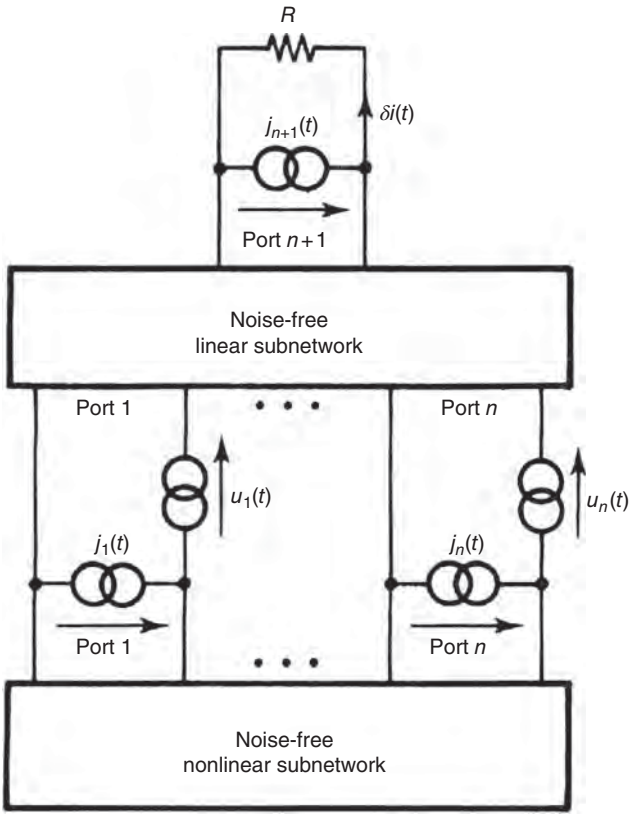

Figure B-23 Equivalent representation of a noisy nonlinear circuit.

A general noise nonlinear network can be described by the circuit in Figure B-23. The circuit shown is then divided into linear and nonlinear subnetworks, represented as noise-free multiports. The noise generation is accounted for by connecting a set of noise voltage and noise current sources at the ports of the linear subnetwork.

For the frequency-conversion noise analysis, we now make the following assumptions: The circuit supports a large-signal time-periodic steady state of fundamental frequency ω_0 (carrier). Noise signals are small perturbations superimposed on the steady state, represented by families of pseudo-sinusoids located at the sidebands of the carrier harmonics. Therefore, the noise performance of the circuit is determined by the exchange of power among the sidebands of the unperturbed steady state through frequency conversion in the nonlinear subnet-work. Due to the perturbative assumption, the nonlinear subnetwork can be replaced by a multifrequency linear multiport described by a conversion matrix. The flow of noise signals can be computed by means of conventional linear circuit techniques.

B-7 LIMITATIONS OF THE FREQUENCY-CONVERSION APPROACH

The frequency-conversion approach is not sufficient to predict the noise performance of an autonomous circuit. The spectral density of the output noise power and, consequently, the PM noise computed by conversion analysis are proportional to the available power of the noise sources.

In the presence of both thermal and flicker noise sources, PM noise increases as ω^{-1} for $\omega \to 0$ tends to a finite limit for $\omega \to \infty$. While the frequency-conversion analysis correctly predicts the far-from-carrier noise behavior of

an oscillator and, in particular, the oscillator noise floor, it does not provide results consistent with physical observations at low deviations from the carrier. The inconsistency is removed by the perturbation analysis of autonomous circuits.

B-7-1 Assumptions

The circuit supports a large-signal time-periodic autonomous regime. The circuit is perturbed by a set of small sources located at the carrier harmonics and at the sidebands at a deviation ω from carrier harmonics.

Now we can find the results of the perturbation of the HB equations. The perturbation of the circuit state $(\delta X_B, \delta X_H)$ is given by the uncoupled sets of equations:

$$\frac{\partial E_B}{\partial X_B}\delta X_B = J_B(\omega) \tag{B-21}$$

$$\frac{\partial E_H}{\partial X_H}\delta X_H = J_H(\omega) \tag{B-22}$$

where

E_B, E_H	=	Vectors of HB errors
X_B, X_H	=	Vectors of state-variable (SV) harmonics (since the circuit is autonomous, one of the entries of X_H is replaced by the fundamental frequency ω_0)
J_B, J_H	=	Vectors of forcing terms where the subscripts B and H denote sidebands and carrier harmonics, respectively

B-7-2 Conversion and Modulation Noise

For a spot noise analysis at a frequency deviation ω, the noise sources can be interpreted in either of two ways. For pseudo-sinusoids with random amplitude and phase located at the sidebands, noise generation is described by Eq. (B-21), which is essentially a frequency-conversion equation relating the sideband harmonics of the state variables and of the noise sources. This description is exactly equivalent to the one provided by the frequency-conversion approach. The mechanism is referred to as conversion noise. For sinusoids located at the carrier harmonics, randomly phase- and amplitude-modulated by pseudo-sinusoidal noise at frequency ω, noise generation is described by Eq. (B-22), which gives the noise-induced jitter of the circuit state, represented by the vector δX_H. The modulated perturbing signals are represented by replacing entries J_H with the complex modulation laws. This mechanism is referred to as modulation noise.

B-7-3 Properties of Modulation Noise

One of the entries in δX_H is $\delta\omega_0$. $\delta\omega_0(\omega)$ equals the phasor of the pseudo-sinusoidal components of the fundamental frequency fluctuations in a 1-Hz band at frequency ω. Equation (B-22) provides a frequency jitter with a mean square value proportional to the available noise power. In the presence of both thermal and flicker noise sources, PM noise increases as ω^{-3} for $\omega \to 0$ and tends to 0 for $\omega \to \infty$. Modulation-noise analysis correctly describes the noise behavior of an oscillator at low deviations from the carrier frequency but does not provide results consistent with physical observations at high deviations from the carrier frequency.

B-7-4 Noise Analysis of Autonomous Circuits

Conversion noise and modulation noise represent complementary descriptions of noise generation in autonomous circuits. The previous discussion has shown that very-near-carrier noise is essentially a modulation phenomenon, while very far-from-carrier noise is essentially a conversion phenomenon; also, Eqs. (B-21) and (B-22) necessarily yield the same evaluation of PM noise at some crossover frequency ωX. The computation of PM noise should be performed by modulation analysis below ω and by conversion analysis above ω_X.

This criterion is not artificial since Eqs. (B-21) and (B-22) provide virtually identical results in a wide neighborhood of ω_X (usually more than two decades). The same criterion can be applied to AM noise. (In many practical cases, modulation and conversion analyses yield almost identical AM noise at all frequency deviations.)

B-7-5 Conversion Noise Analysis Results

After performing all the necessary calculations, we obtain the following:

- kth harmonic PM noise

$$\langle \Phi_k(\omega)|^2 \rangle = \frac{N_k(\omega) + N_{-k}(\omega) - 2Re[C(\omega)]}{R|I_k^{SS}|^2} \tag{B-23}$$

- kth harmonic AM noise

$$\langle |\delta A_k(\omega)|^2 \rangle = 2\frac{N_k(\omega) + N_{-k}(\omega) + 2Re[C_k(\omega)]}{R|I_k^{SS}|^2} \tag{B-24}$$

- kth harmonic PM–AM correlation coefficient

$$\begin{aligned} C_k^{\text{PM–AM}}(\omega) &= \langle \delta\, \Phi_k(\omega)\delta A_k(\omega)^* \rangle \\ &= -\sqrt{2}\frac{2\,\text{Im}[C_k(\omega)] + j[N_k(\omega) - N_{-k}(\omega)]}{R|I_k^{SS}|^2} \end{aligned} \tag{B-25}$$

where

$N_k(\omega),\ N_{-k}(\omega)$	=	Noise power spectral densities at the upper and lower sidebands of the kth carrier harmonic
$C_k(\omega)$	=	Normalized correlation coefficient of the upper and lower sidebands of the kth carrier harmonic
R	=	Load resistance
I_k^{SS}	=	kth harmonic of the steady-state current through the load

B-7-6 Modulation Noise Analysis Results

Again, after performing all the necessary calculations, we obtain the following:

- kth harmonic PM noise

$$\langle |\delta\, \Phi_k(\omega)|^2 \rangle = \frac{k^2}{\omega^2} T_F \langle J_H(\omega) J_H^\dagger(\omega) \rangle T_F^\dagger \tag{B-26}$$

- kth harmonic AM noise

$$\langle |\delta A_k(\omega)|^2 \rangle = \frac{2}{|I_k^{SS}|^2} T_{\text{Ak}} \langle J_H(\omega) J_H^\dagger(\omega) \rangle T_{\text{Ak}}^\dagger \tag{B-27}$$

- kth harmonic PM–AM correlation coefficient

$$C_k^{\text{PM–AM}}(\omega) = \langle \delta\,\Phi_k(\omega)\delta A_k(\omega)^* \rangle$$
$$= \frac{k\sqrt{2}}{j\omega |I_k^{SS}|^2} T_F \langle J_H(\omega) J_H^{\dagger}(\omega) \rangle T_{\text{Ak}}^{\dagger} \tag{B-28}$$

where

$J_H(\omega)$	=	Vector of Norton equivalent of the noise sources
T_F	=	Frequency transfer matrix
T_{Ak}	=	Amplitude transfer matrix
R	=	Load resistance
I_k^{SS}	=	kth harmonic of steady-state current through the load

B-8 SUMMARY OF THE PHASE NOISE SPECTRUM OF THE OSCILLATOR

The numerical approach is important in understanding that the oscillator phase noise is composed of two parts:

(1) The near-carrier noise consists of contributions from the perturbation of the oscillating frequency caused by the noise sources at each sideband frequency. This part is the major noise source at the near-carrier frequencies.

(2) The far-carrier noise consists of contributions from each sideband noise source through sideband-to-sideband transfer functions. As can be seen in Figure B-24, this part is similar to the mixer noise calculation and is the major noise source at frequencies far away from the carrier.

B-9 VERIFICATION EXAMPLES FOR THE CALCULATION OF PHASE NOISE IN OSCILLATORS USING NONLINEAR TECHNIQUES

B-9-1 Example 1: High-*Q* Case Microstrip DRO

Figure B-25 shows the schematic topology of a Microstrip dielectric resonator oscillator (DRO). The specifications for this DRO are as follows:

• Oscillation frequency	4.6 GHz
• Output power	12.5 dBm
• Q of the dielectric resonator	1700

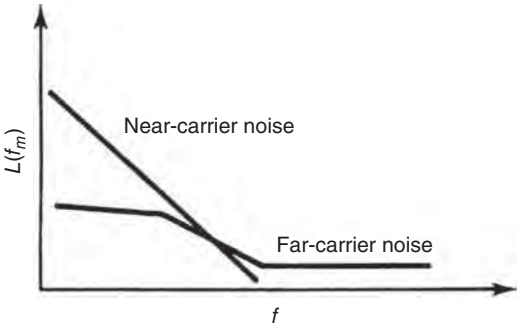

Figure B-24 Oscillator phase noise consisting of near- and far-carrier noise.

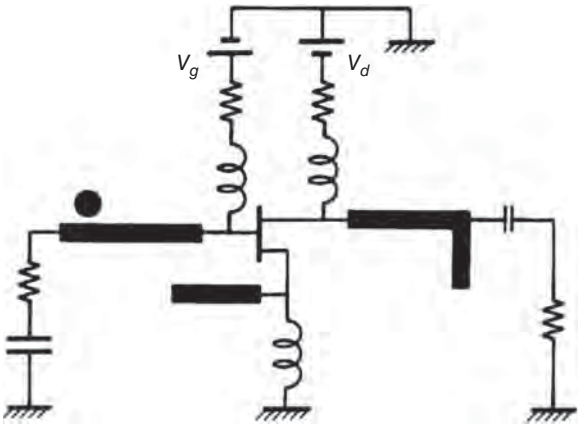

Figure B-25 Schematic topology of Microstrip DRO.

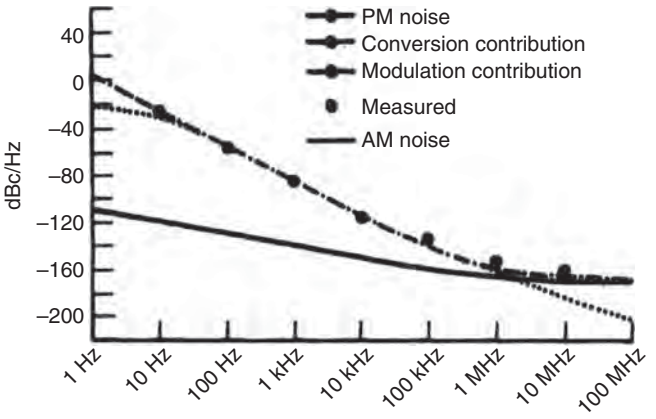

Figure B-26 Conversion contribution and modulation contribution have been calculated and plotted.

Noise sources considered in the analysis include channel noise and flicker noise. Flicker noise is modeled by a voltage source connected in series to the gate terminal. The dc spectral density of this source is $3.25 \times 10^{-9}\ \omega V^2/Hz$.

The various noise contributions such as AM noise, PM noise, conversion contribution, and modulation contribution have been calculated and plotted, as shown in Figure B-26.

B-9-2 Example 2: 10 MHz Crystal Oscillator

The equivalent of a DRO at low frequency is a crystal oscillator. In the HP3048 phase noise measurement system, Hewlett-Packard uses the HP10811A 1-MHz frequency standard. For many years, this frequency standard has been the state of the art for low phase noise performance and similar crystal oscillators are now built by a number of companies. Figure B-27a shows an abbreviated circuit of such a crystal oscillator, which uses an extremely high-Q crystal. Figure B-27b displays the simulated phase noise of this circuit.

Figure B-28 shows the phase noise measured and published by Hewlett-Packard and our findings using the Microwave Harmonica v.4.0 algorithm as previously outlined. The extremely good correlation between the two cases can be seen.

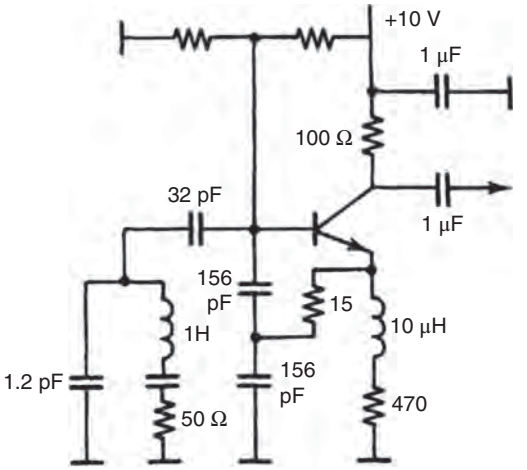

Figure B-27a Abbreviated circuit of a 10-MHz crystal oscillator, where $Q = 200{,}000$.

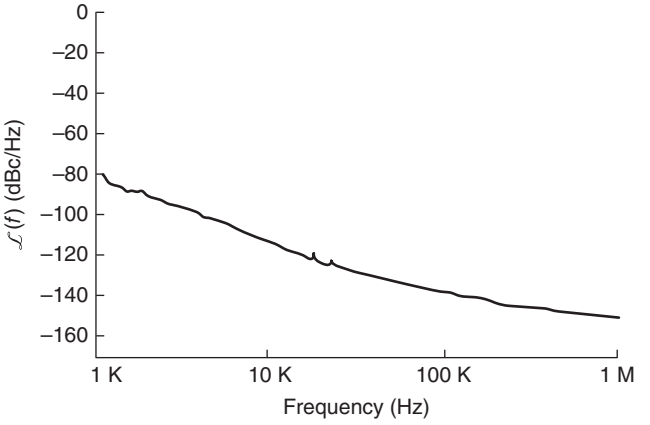

Figure B-27b Simulated phase noise of the oscillator shown in Figure B-24.

B-9-3 Example 3: The 1-GHz Ceramic Resonator VCO

A number of companies have introduced resonators built from ceramic materials with an e ranging from 20 to 80. The advantage of using this type of resonator is that they are a high-Q element that can be tuned by adding a varactor diode.

Figure B-29 shows a typical test circuit for use in a ceramic resonator. These resonators are available in the range of 500 MHz–2 GHz. For higher frequencies, dielectric resonators (DRs) are recommended. Figure B-30 shows the measured phase noise of the oscillator shown in Figure B-28. The noise pedestal above 100 kHz away from the carrier is due to the reference oscillator model HP8662.

Figure B-31 shows the predicted phase noise of the 1-GHz ceramic resonator voltage-controlled oscillator (VCO) without a tuning diode and Figure B-32 shows the predicted phase noise of the 1-GHz ceramic VCO with a tuning diode attached. Please note the good agreement between the measured and predicted phase noise.

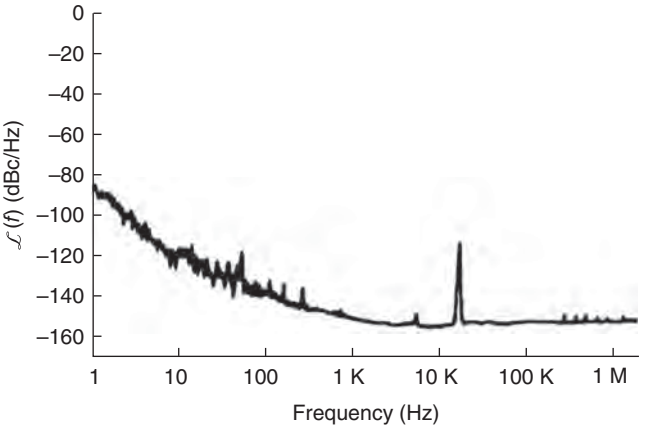

Figure B-28 Measured phase noise for this frequency standard by Hewlett-Packard.

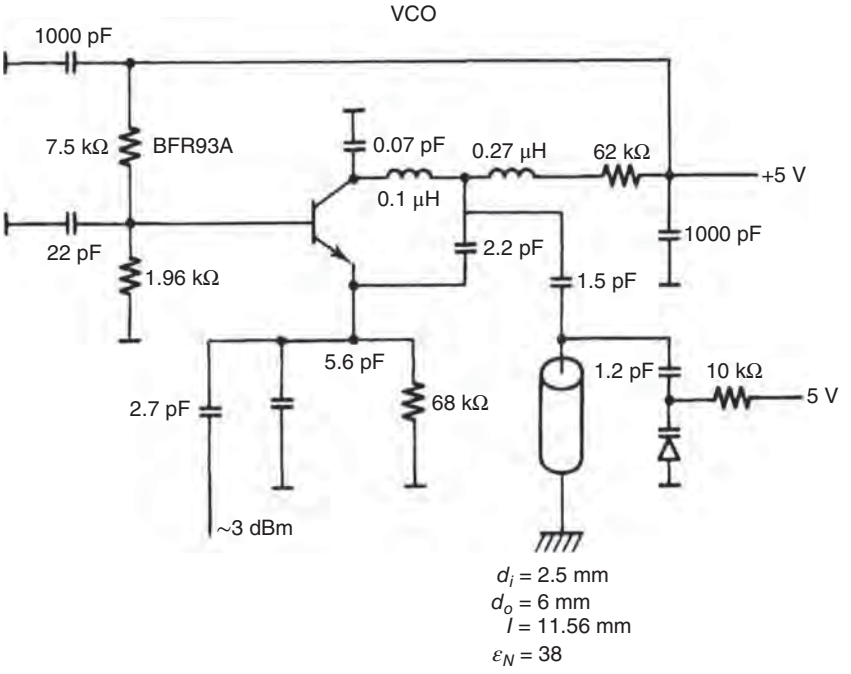

Figure B-29 Typical test circuit for use in a ceramic resonator.

The ceramic resonator has been modeled using the model "cable"; then the Spice type parameters of the BFR93A transistor data are shown at the beginning of the nonlinear program. The statement at the end of the last line "nois" = B noise indicates that the bias-dependent noise model of the bipolar transistor has been activated. In the data section, the bias-dependent flicker noise for the transistor (bnoise) and the bias-dependent noise of the tuning diode (dnoise) are defined. The center of the netlist shows the element values that are consistent

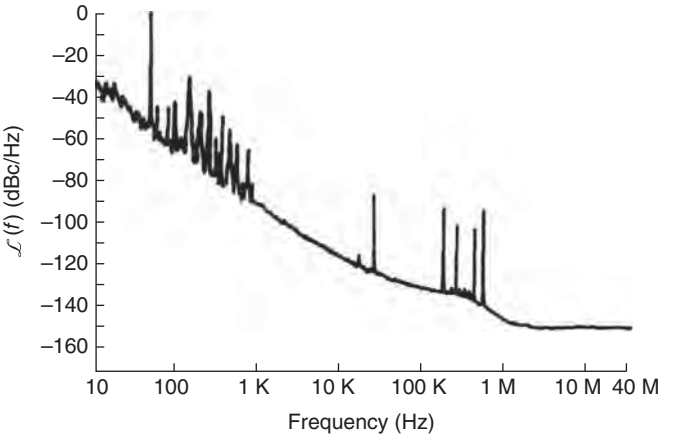

Figure B-30 Measured phase noise of the oscillator shown in Figure B-29.

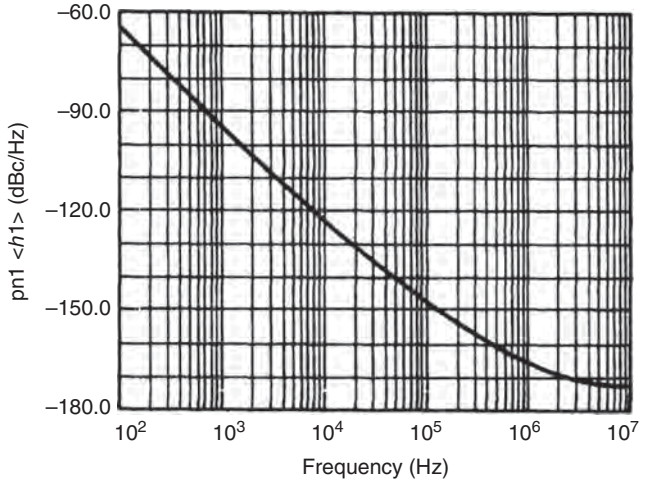

Figure B-31 Predicted phase noise of the 1-GHz ceramic resonator VCO without the tuning diode.

with the previous shown circuit diagram. This noise analysis approach is unique because it takes all factors into consideration and therefore is referred to as the "exact" solution.

B-9-4 Example 4: Low Phase Noise FET Oscillator

A number of authors recommend the use of a clipping diode to prevent the gate-source junction of an FET from becoming conductive and thereby lowering the phase noise. In reality, it turns out that this has been a misconception. A popular VCO circuit as described in the American Radio Relay League's (ARRL) manual and shown in Figure B-33 has been analyzed with and without the diode. Claims also have been made that the diode was necessary to obtain long-term stability.

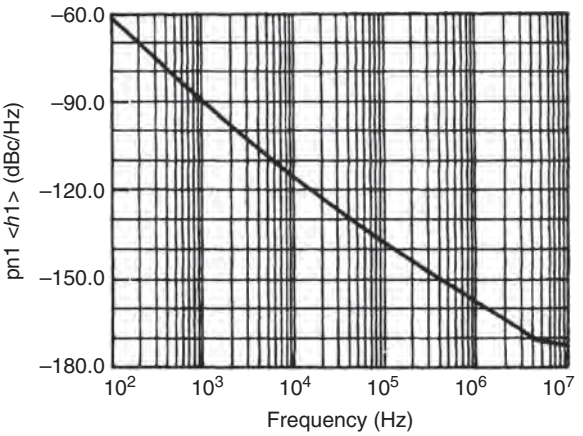

Figure B-32 Predicted phase noise of the 1-GHz ceramic resonator VCO with the tuning diode attached. Please note the good agreement between the measured and predicted phase noise.

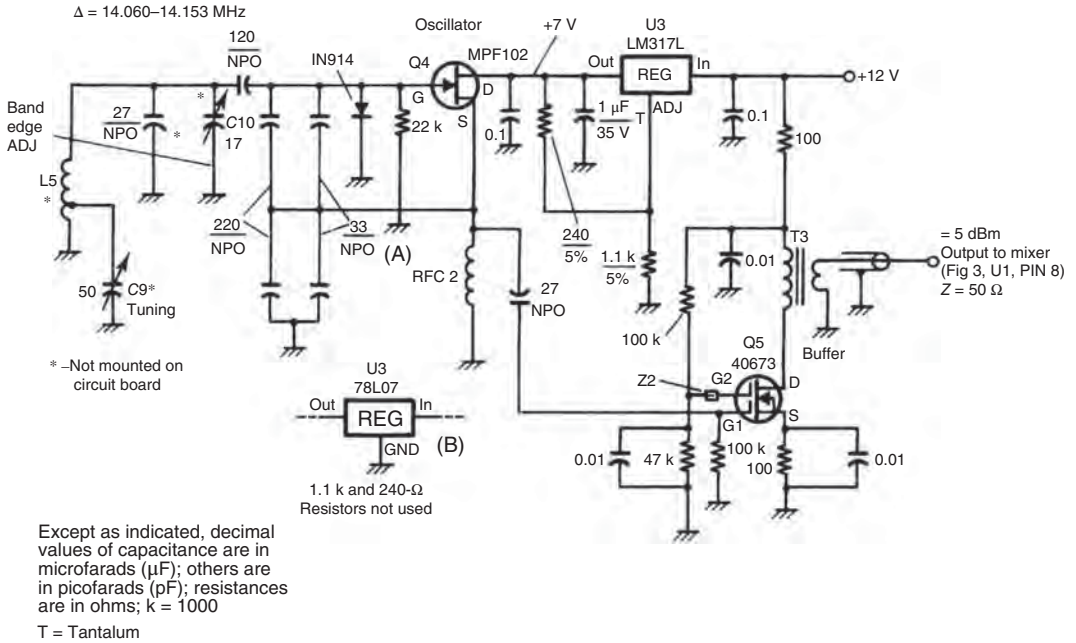

Figure B-33 A 20-m VFO circuit from the 1993 *ARRL Handbook*. VFO, variable frequency oscillator.

Figure B-34 shows the measured phase noise of an oscillator of this type and Figures B-35 and B-36 show the simulated phase noise of the type of oscillator shown in Figure B-33, with and without a clipping diode. Please note the degradation of the phase noise if the diode is used.

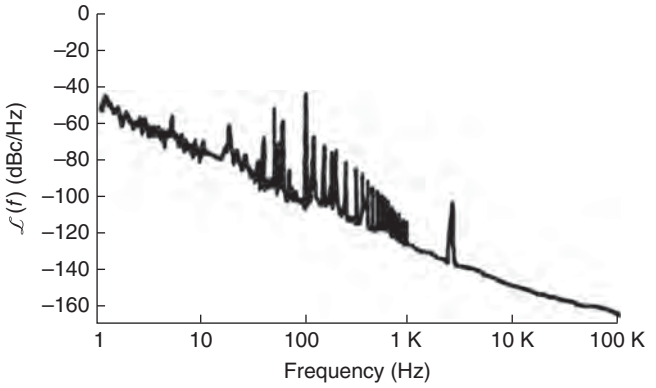

Figure B-34 Measured phase noise of a 10-MHz oscillator of the type shown in Figure B-33.

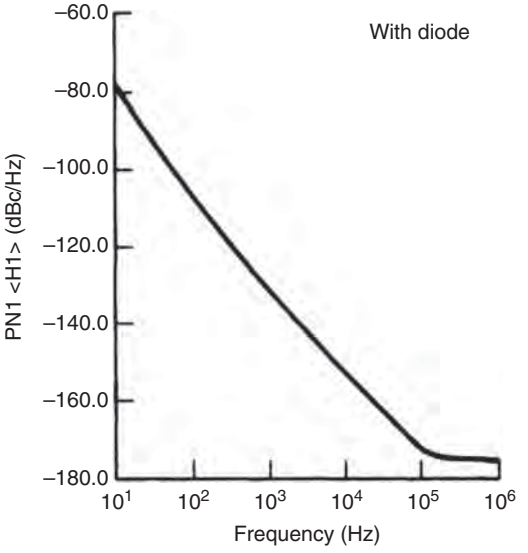

Figure B-35 Simulated phase noise of this type of oscillator with a clipping diode attached.

An experimenter found that by removing the diode it did not change or degrade the stability. Additionally, the clipping diode did degrade the phase noise close-in. We have developed a VCO, however, that clips the negative peaks, in the sense that it prevents the oscillator from shutting off. This VCO, as shown in Figure B-37, was incorporated in a scheme with a digital direct synthesizer.

The phase noise of the combined system was significantly improved. The phase noise of the oscillator shown in Figure B-38, which has only one VCO for the total range from 75 to 105 MHz, when compared with the phase noise of a very recent design like the synthesizer in the TS950, has a 10-dB better S/N ratio at 10 kHz (and further away). This is shown in Figure B-39.

Previous authors have tried to build similar wideband oscillators with varying degrees of success. The VCO shown in Figure B-40 violates several rules of designing a good VCO. First, resistor R2 of 68 kΩ, together with C2, provides a time constant that gets close to the audio frequency range. This may result in a super-regenerative receiver, which, of course, is counterproductive. Second, the diode from gate to ground working as a clipping diode also generates more noise. This was outlined earlier. Finally, the feedback selected between the two tuning diodes

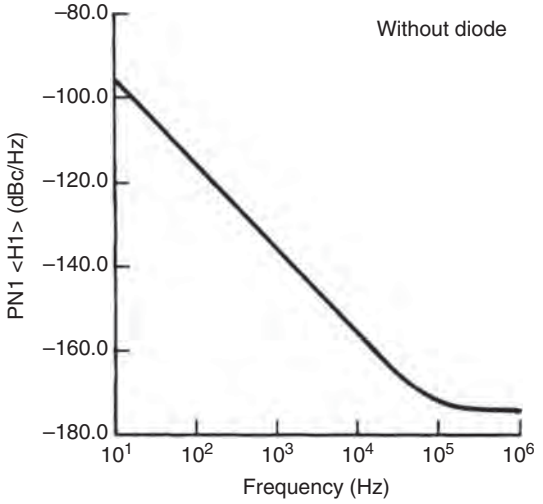

Figure B-36 Simulated phase noise of this type of oscillator without a clipping diode attached.

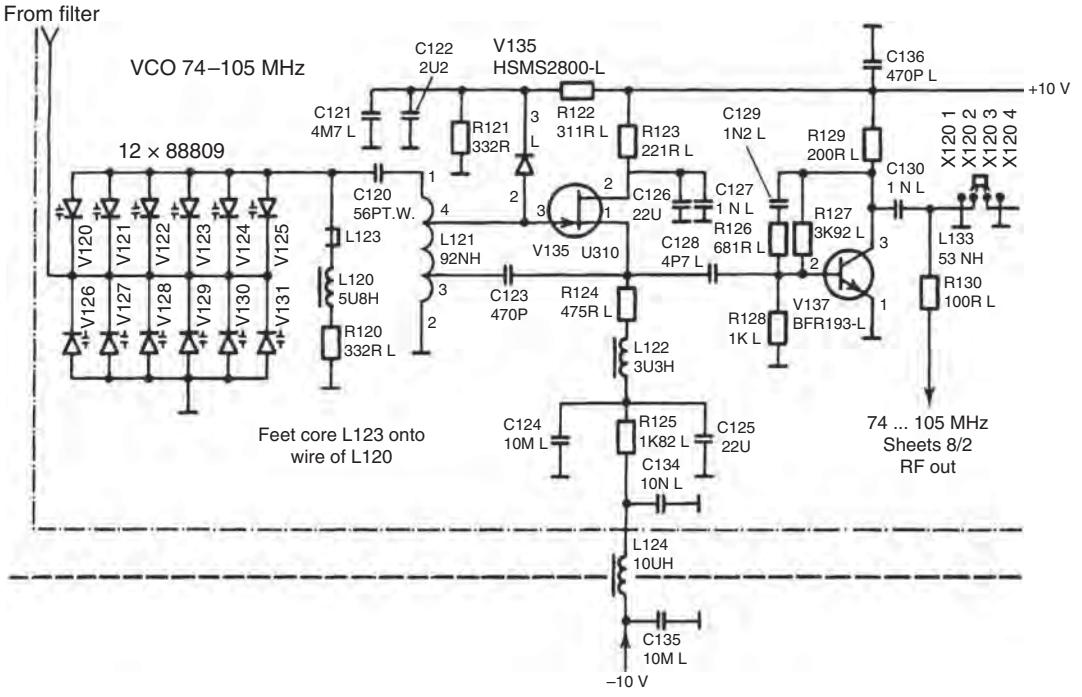

Figure B-37 Wideband VCO with a large number of tuning diodes to improve phase noise. Note that the diode is biased in reverse and does not follow the positive clipping as published by other authors.

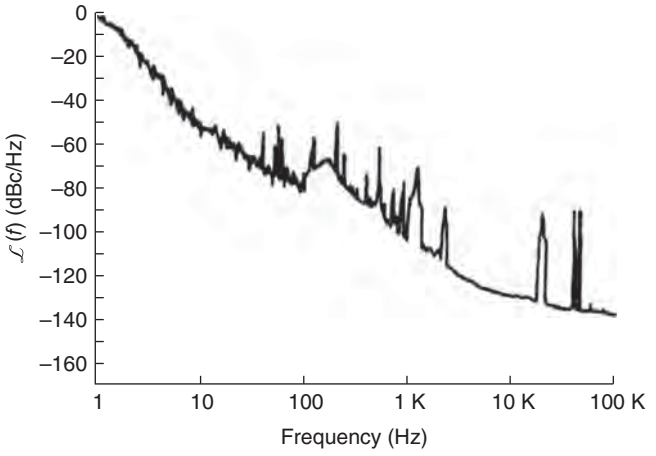

Figure B-38 Phase noise of the multidiode VCO in a phase-locked loop (PLL) system.

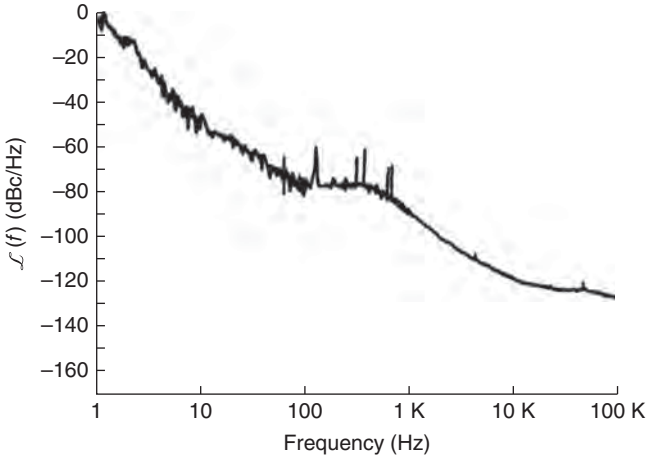

Figure B-39 Phase noise of the TS950, which is 10 dB worse than the multidiode system.

reduces the operating Q of the resonator to unreasonably small values. If this particular circuit is favored, then the tuning diode D2 should be made out of several (3–5) diodes in parallel. It is therefore not surprising that the measured phase noise shown in Figure B-41 is significantly below state of the art.

B-9-5 Example 5: Millimeter-Wave Applications

In millimeter-wave applications such as smart weapons, which use small radar units for the tracking of enemy targets, MMICs with VCOs are used. One of the most severe tests of software is the combination of millimeter-wave accuracy and nonlinear phase noise calculation. As a last test, we are showing the layout of such a VCO that operates at 39 GHz. While a detailed circuit description of this proprietary design is beyond the scope of this presentation, it should be noted that it is now possible to analyze such complex structures.

Figure B-42 shows the actual layout of the 39-GHz VCO. Figure B-43 shows its schematic presentation. Both transmission lines are used as a resonator and the varactors have fairly low Q values. The resulting phase noise therefore is significantly below that seen in other examples. Even if we take low-frequency oscillators and multiply

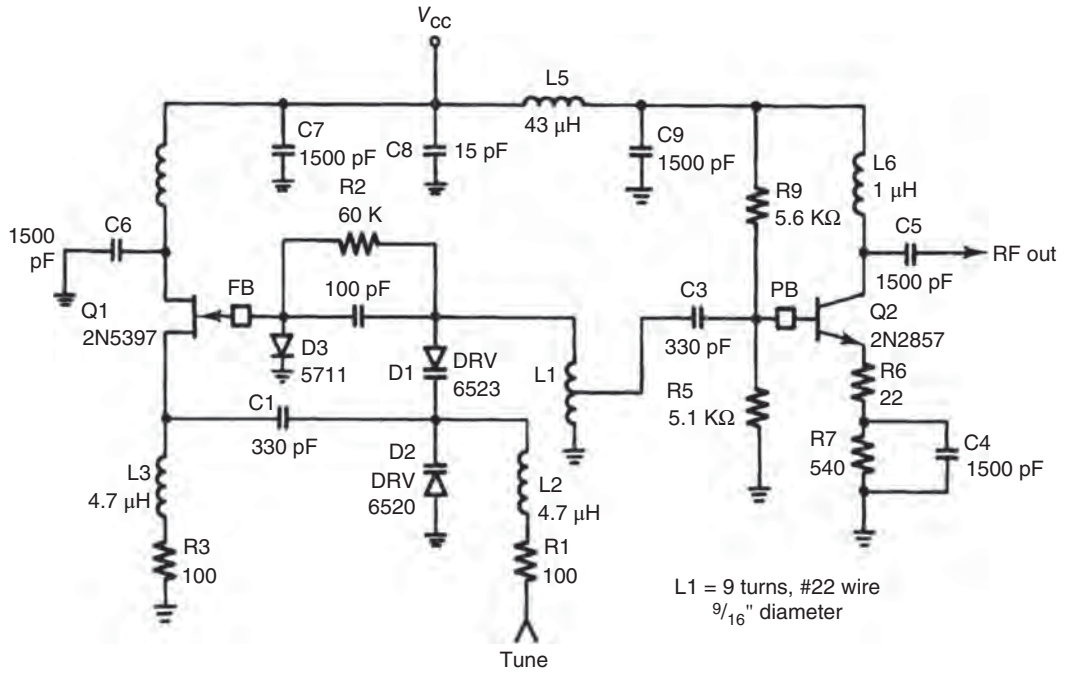

Figure B-40 41 MHz VCO that violates several rules of good design.

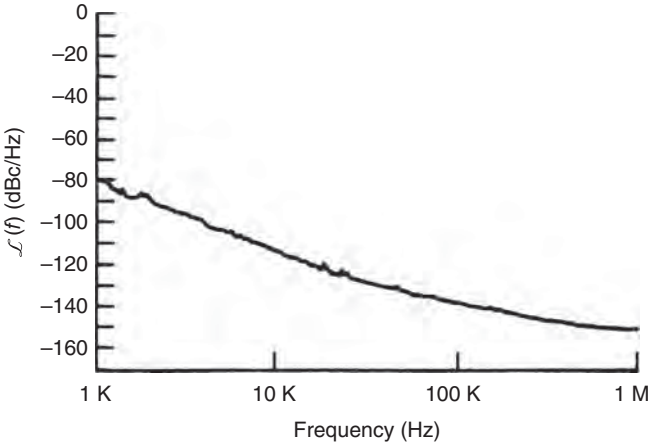

Figure B-41 Phase noise of a 41-MHz oscillator that is significantly below state of the art.

them up to 39 GHz, we would get better performance. VCOs like this are being used as part of PLL systems that "clean up" some of the noise.

Figure B-44 shows the "clean-up" from a PLL and at the same time shows the phase noise of the same oscillator in free-running mode. The operating conditions were 10-MHz reference and 100-kHz loop bandwidth. The "clean-up" is dramatic if one considers the multiplication factor up to 39 GHz. The crystal oscillator's reference is the best low noise crystal type 10811A made by Hewlett-Packard.

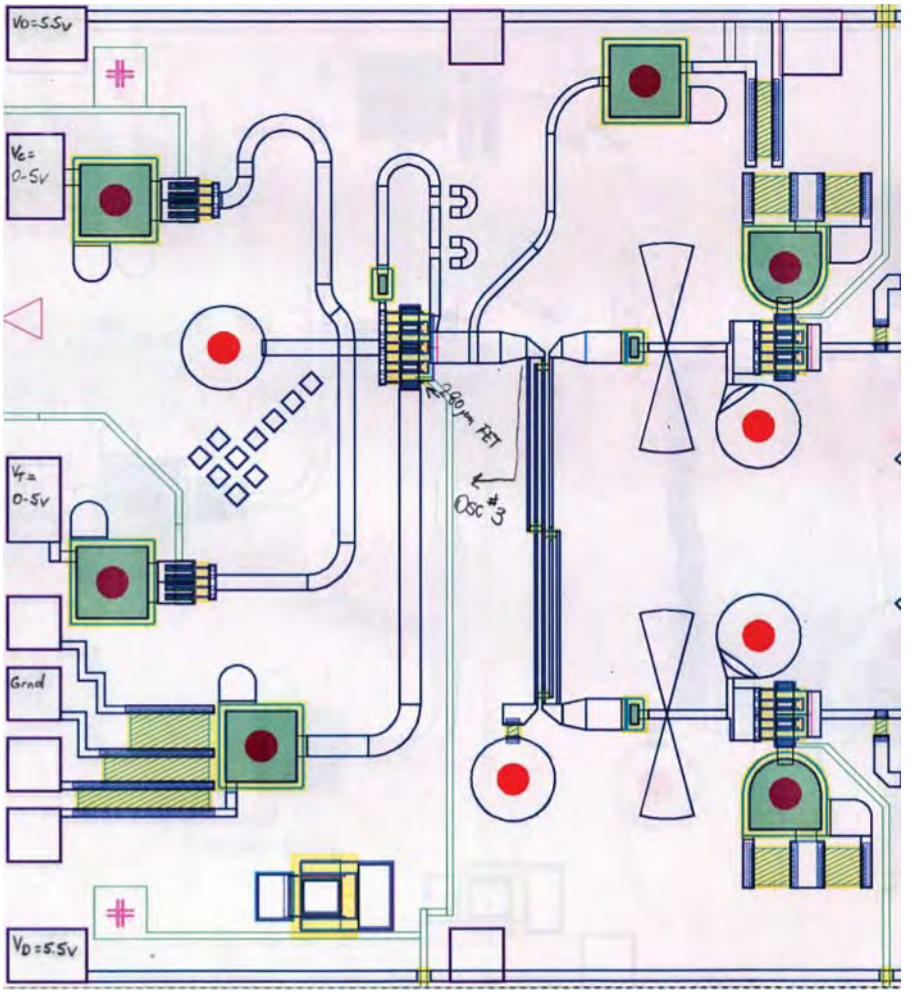

Figure B-42 Layout of a 39-GHz VCO.

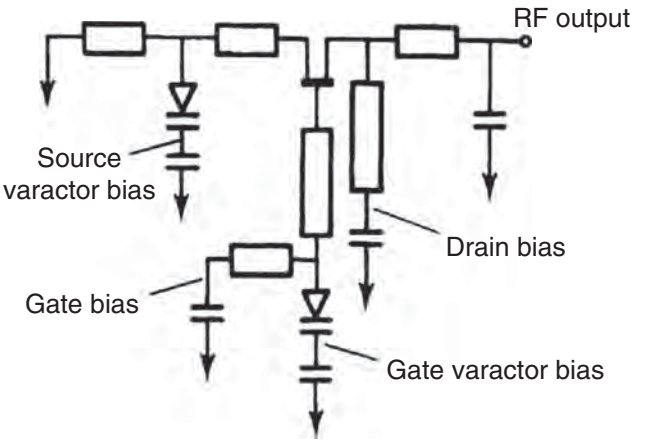

Figure B-43 Schematic presentation and topology of the millimeter-wave VCO.

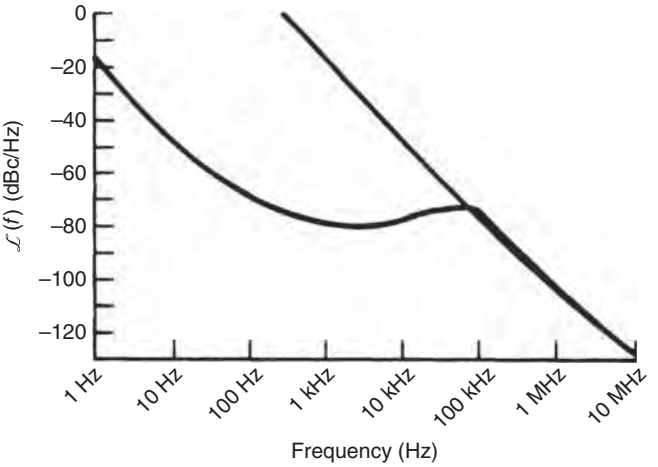

Figure B-44 "Clean-up" from a PLL, also showing the phase noise of the same oscillator in a free-running mode.

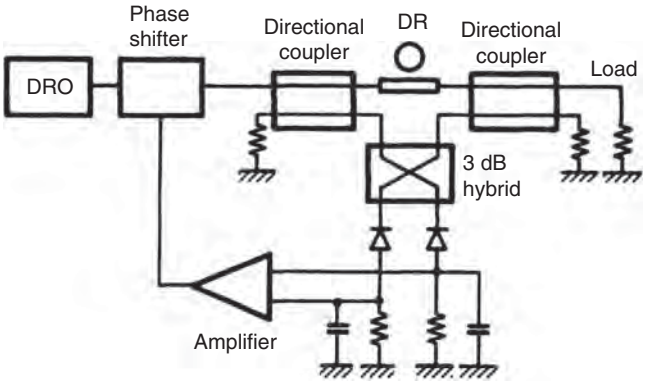

Figure B-45 Advanced system rather than an oscillator where a DRO is stabilized by a discriminator.

B-9-6 Example 6: Discriminator Stabilized DRO

Figure B-45 shows an advanced system rather than an oscillator where a DRO is stabilized by a discriminator. The oscillation frequency of the DRO is 6.161 GHz. The output signal is fed to a discriminator using a DR as the frequency selective element. The reflection and transmission coefficients of the DR are equal at the resonant frequency and change in opposite directions when frequency varies in the neighborhood of the resonance frequency. The reflected and transmitted waves are fed to a couple of detector diodes by two directional couplers and a 3-dB hybrid. The variation of the output voltage of the discriminator is roughly proportional to the frequency deviation of the oscillator from the resonance frequency of the DR.

The computed output voltage of the frequency discriminator is shown in Figure B-46. The phase fluctuations of the oscillator are compensated by feeding back the output signal of the discriminator to a phase shifter placed between the oscillator and the DR. After properly dimensioning the feedback loop, the DRO PM noise is virtually canceled, and the output noise is only determined by the noise contributions of the feedback amplifier and the detector diodes.

The noise analysis results are reported in Figure B-47.

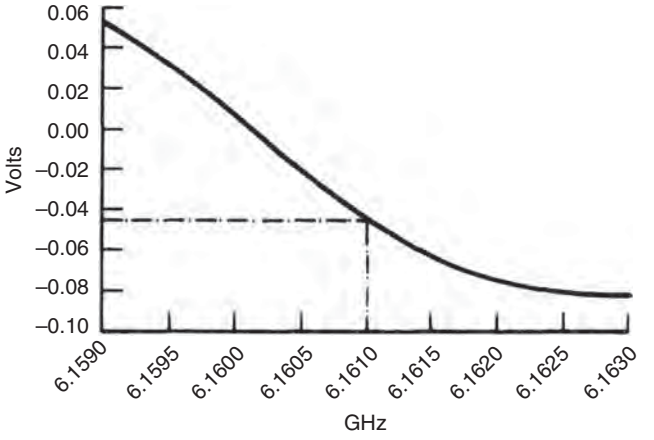

Figure B-46 Computed output voltage of the frequency discriminator shown in Figure B-45.

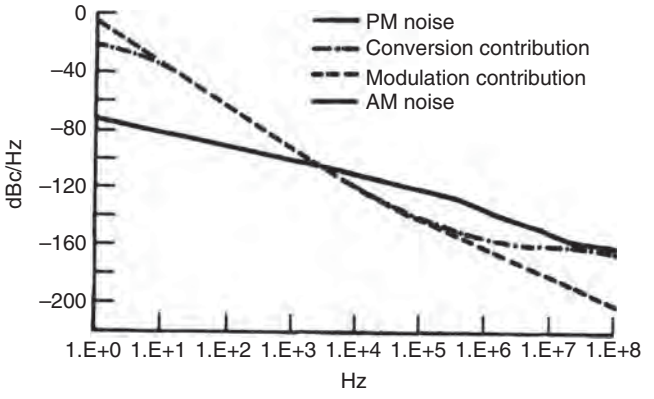

Figure B-47 Noise analysis results.

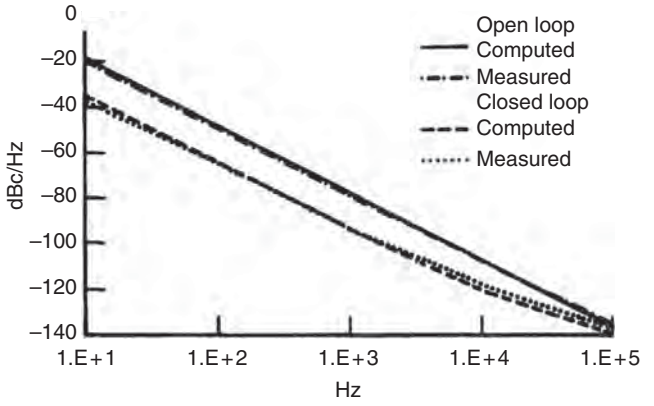

Figure B-48 Open-loop and closed-loop PM noise.

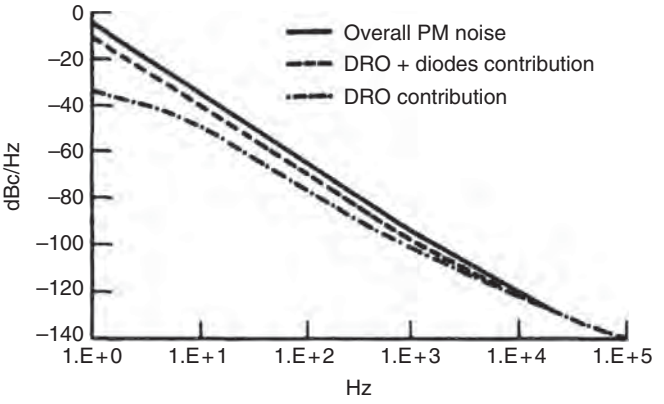

Figure B-49 Contributions to PM noise.

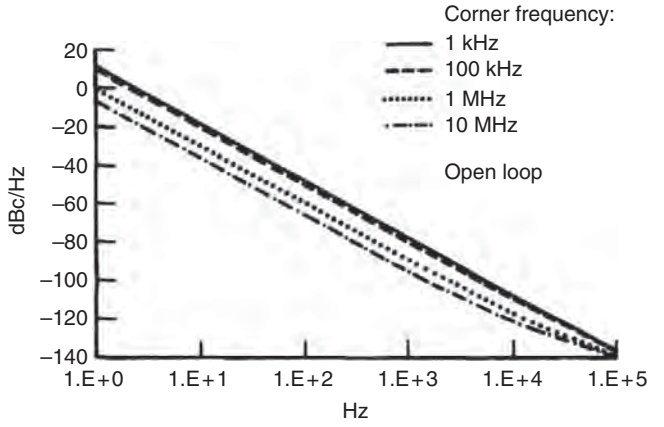

Figure B-50 PM noise versus diode corner frequency.

Figure B-48 provides a comparison between the open-loop and closed-loop PM noise. An improvement of about 15 dB is obtained up to frequency deviations of about 2 kHz. In the figure, measured data are also reported. Computed and experimental results are in very good agreement.

Figure B-49 shows the contribution of different noise sources to the output PM noise.

Finally, Figure B-50 shows the dependence of PM noise on the corner frequency of the detector diodes. (All previous results correspond to corner frequencies of 100 kHz for both the detector diodes and the feedback amplifier.)

B-10 SUMMARY

This combined mathematical and experimental discussion has shown that the new approach implemented in Compact Software's Microwave Harmonica and Scope workstation products provides a fast and accurate method for phase noise analysis. The results can be viewed on the workstation as shown in Figure B-51. This workstation approach is the result of a 2-year cooperative effort between Professor Vittorio and his group at the University of Bologna and the engineering staff of Compact Software, Inc. An additional benefit is that this approach also

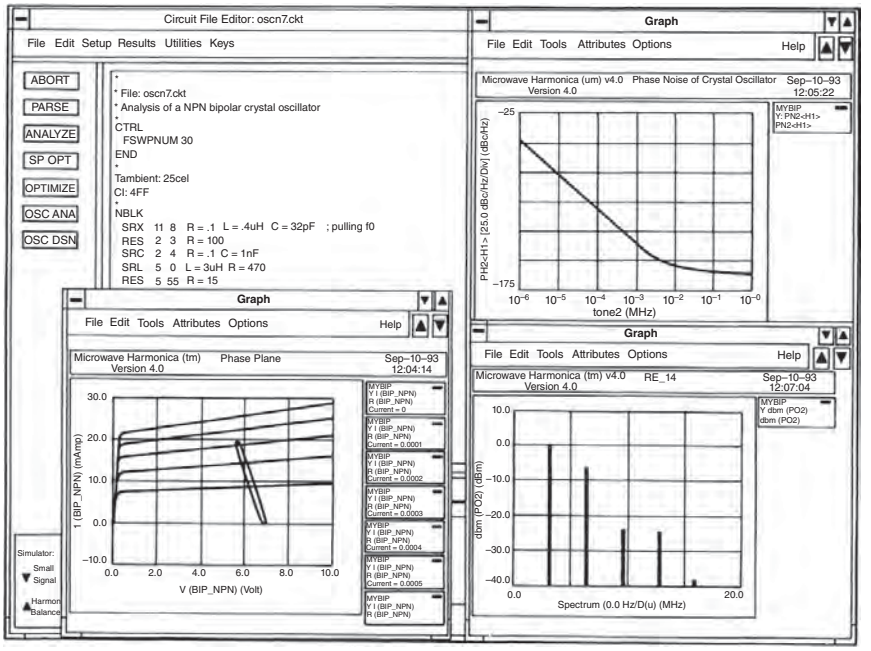

Figure B-51 Screen dump of Microwave Harmonica/Scope phase noise analysis.

handles mixer noise. A future enhancement will be the ability to optimize a circuit for output power and phase noise. References [8–13] refer to recent work done in this area.

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Microwave and Wireless Synthesizers: Theory and Design, Second Edition.
Ulrich L. Rohde, Enrico Rubiola, and Jerry C. Whitaker.
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APPENDIX C

EXAMPLE OF WIRELESS SYNTHESIZERS USING COMMERCIAL ICs

ANALOG DEVICES

3.5 GSPS Direct Digital Synthesizer with 12-Bit DAC

Data Sheet **AD9914**

FEATURES

- 3.5 GSPS internal clock speed
- Integrated 12-bit DAC
- Frequency tuning resolution to 190 pHz
- 16-bit phase tuning resolution
- 12-bit amplitude scaling
- Programmable modulus
- Automatic linear and nonlinear frequency sweeping capability
- 32-bit parallel datapath interface
- 8 frequency/phase offset profiles
- Phase noise: −128 dBc/Hz (1 kHz offset at 1396 MHz)
- Wideband SFDR < −50 dBc
- Serial or parallel input/output control
- 1.8 V/3.3 V power supplies
- Software and hardware controlled power-down
- 88-lead LFCSP package
- PLL REF CLK multiplier
- Phase modulation capability
- Amplitude modulation capability

APPLICATIONS

- Agile LO frequency synthesis
- Programmable clock generator
- FM chirp source for radar and scanning systems
- Test and measurement equipment
- Acousto-optic device drivers
- Polar modulator
- Fast frequency hopping

FUNCTIONAL BLOCK DIAGRAM

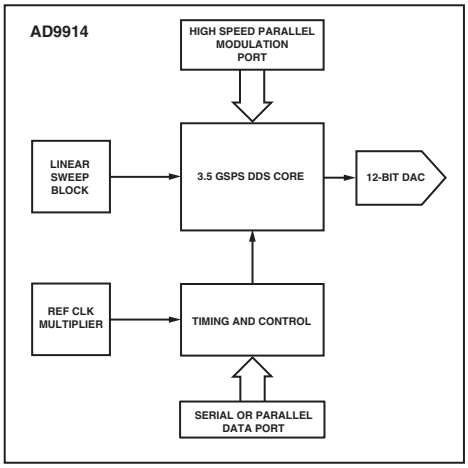

Figure 1.

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GENERAL DESCRIPTION

The AD9914 is a direct digital synthesizer (DDS) featuring a 12-bit DAC. The AD9914 uses advanced DDS technology, coupled with an internal high speed, high performance DAC to form a digitally programmable, complete high frequency synthesizer capable of generating a frequency-agile analog output sinusoidal waveform at up to 1.4 GHz. The AD9914 enables fast frequency hopping and fine tuning resolution (64-bit capable using programmable modulus mode). The AD9914 also offers fast phase and amplitude hopping capability. The frequency tuning and control words are loaded into the AD9914 via a serial or parallel input/output port. The AD9914 also supports a user defined linear sweep mode of operation for generating linear swept waveforms of frequency, phase, or amplitude. A high speed, 32-bit parallel data input port is included, enabling high data rates for polar modulation schemes and fast reprogramming of the phase, frequency, and amplitude tuning words.

The AD9914 is specified to operate over the extended industrial temperature range (see the Absolute Maximum Ratings section).

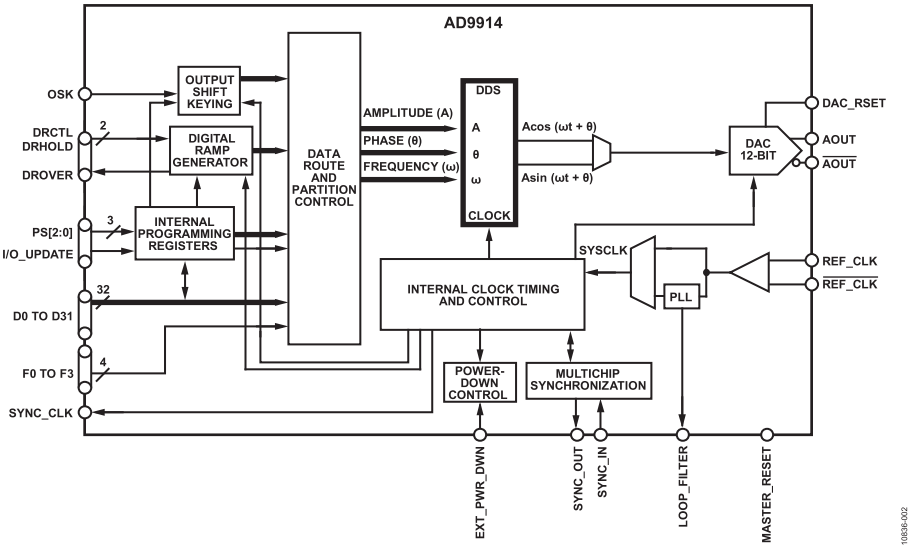

Figure 2. Detailed Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Nominal supply voltage; DAC R_{SET} = 3.3 kΩ, T_A = 25°C, unless otherwise noted.

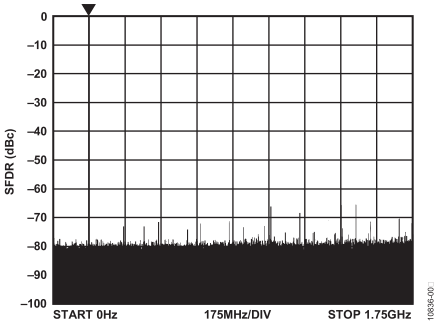

Figure 4. Wideband SFDR at 171.5 MHz SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

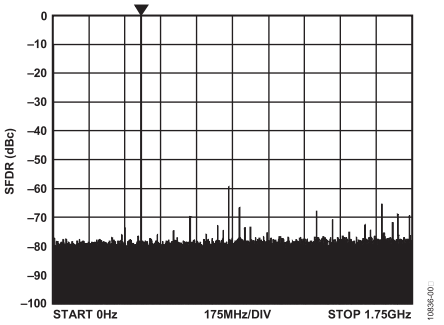

Figure 5. Wideband SFDR at 427.5 MHz SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

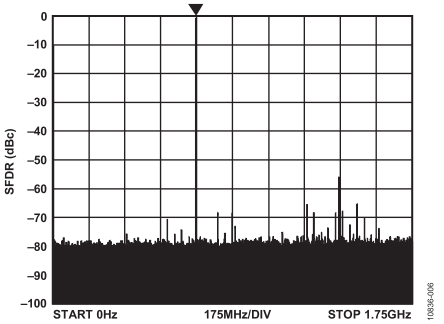

Figure 6. Wideband SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

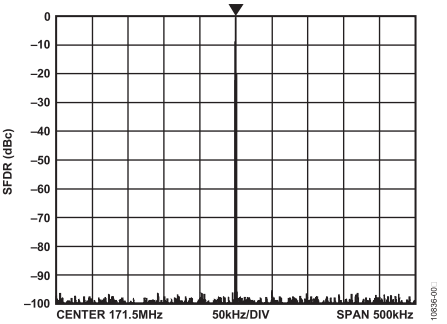

Figure 7. Narrow-Band SFDR at 171.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

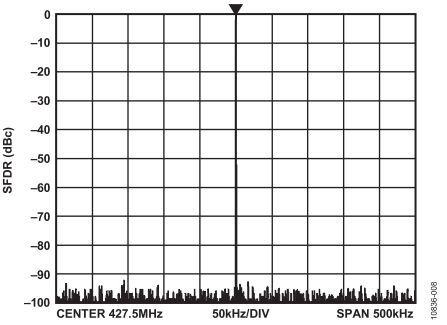

Figure 8. Narrow-Band SFDR at 427.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

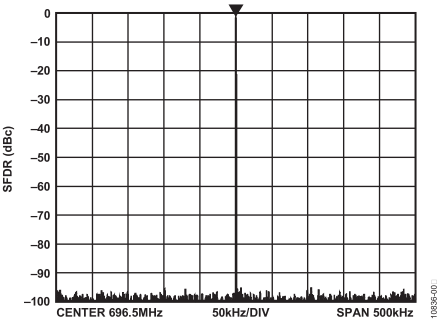

Figure 9. Narrow-Band SFDR at 696.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

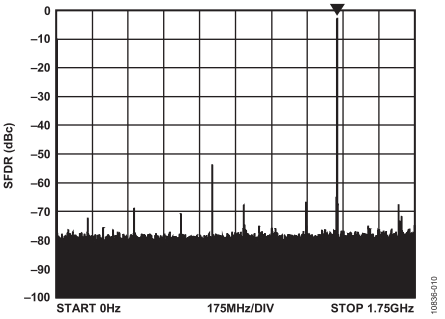

Figure 10. Wideband SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

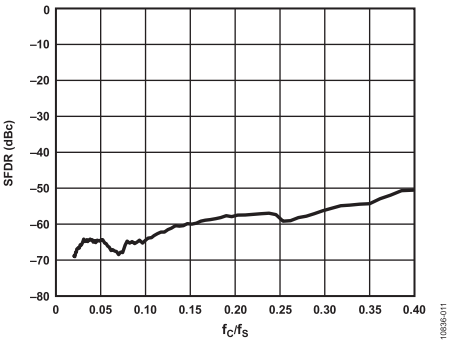

Figure 11. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 3.5 GHz

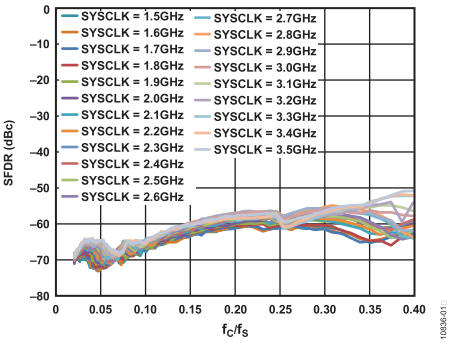

Figure 12. Wideband SFDR vs. Normalized f_{OUT}, SYSCLK = 2.5 GHz to 3.5 GHz

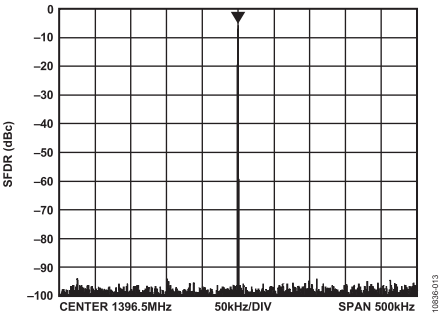

Figure 13. Narrow-Band SFDR at 1396.5 MHz, SYSCLK = 3.5 GHz (SYSCLK PLL Bypassed)

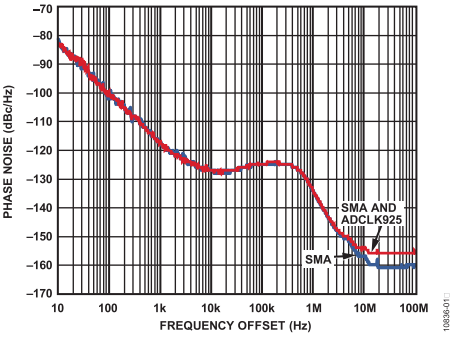

Figure 14. Absolute Phase Noise of REF CLK Source Driving AD9914 Rohde & Schwarz SMA100 Signal Generator at 3.5 GHz Buffered by Series ADCLK925

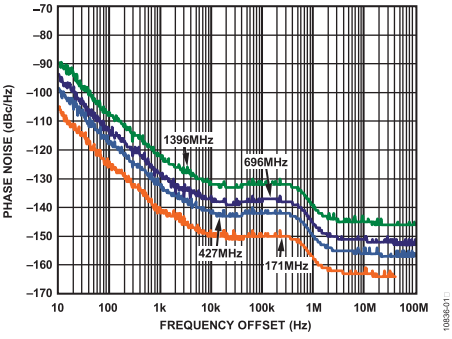

Figure 15. Absolute Phase Noise Curves of DDS Output at 3.5 GHz Operation

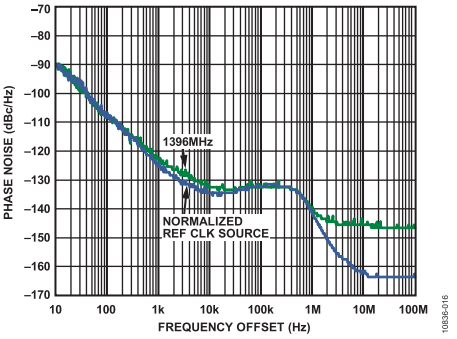

Figure 16. *Absolute Phase Noise Curves of Normalized REF CLK Source to DDS Output at 1396 MHz (SYSCLK = 3.5 GHz)*

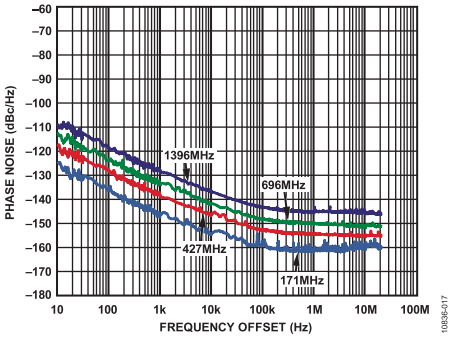

Figure 17. *Residual Phase Noise Curves*

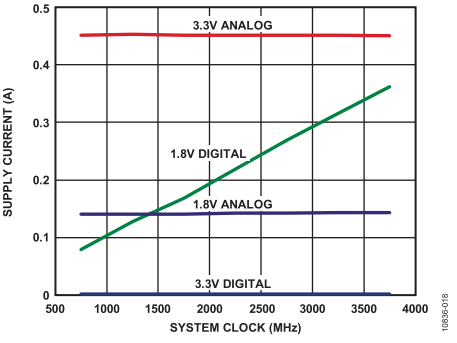

Figure 18. *Power Supply Current vs. SYSCLK*

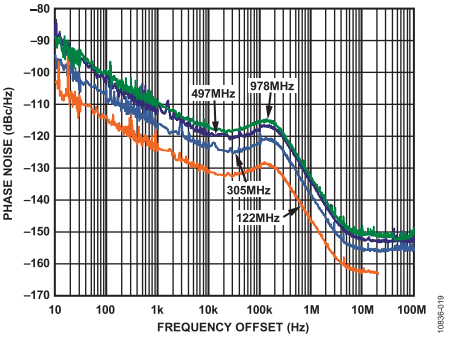

Figure 19. *Absolute Phase Noise Curves of DDS Output Using Internal PLL at 2.5 GHz Operation*

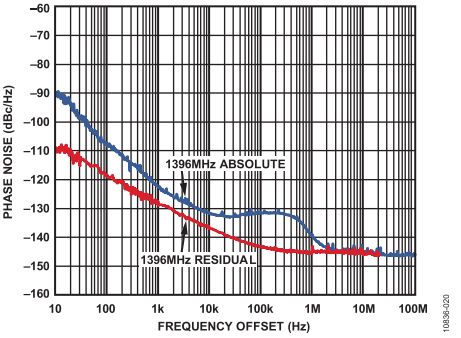

Figure 20. *Residual PN vs. Absolute PN Measurement Curves at 1396 MHz*

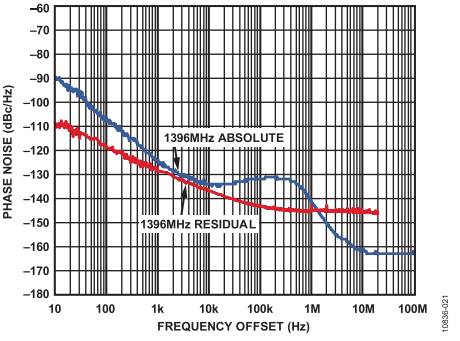

Figure 21. *Residual Phase Noise vs. Normalized Absolute REF CLK Source Phase Noise at 1396 MHz*

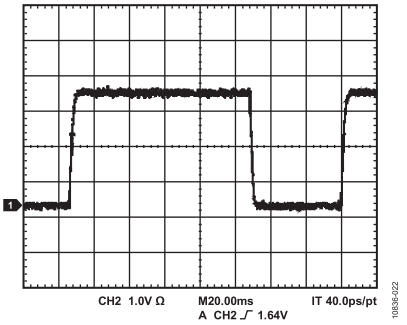

Figure 22. SYNC_OUT (f_{SYSCLK}/384)

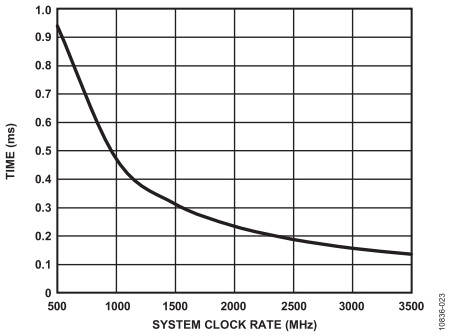

Figure 23. DAC Calibration Time vs. SYSCLK Rate. See the DAC Calibration Output Section for Formula.

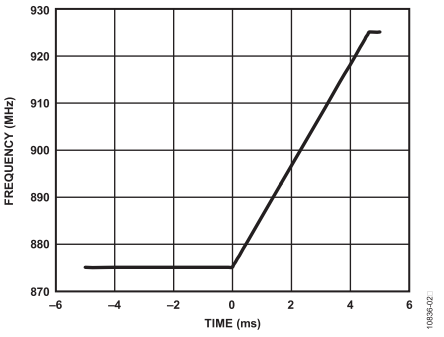

Figure 24. Measured Rising Linear Frequency Sweep

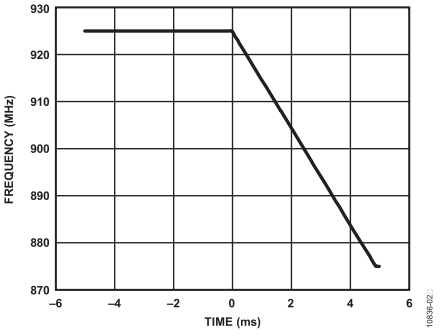

Figure 25. Measured Falling Linear Frequency Sweep

THEORY OF OPERATION

The AD9914 has five modes of operation.

- Single tone
- Profile modulation
- Digital ramp modulation (linear sweep)
- Parallel data port modulation
- Programmable modulus mode

The modes define the data source supplies the DDS with the signal control parameters: frequency, phase, or amplitude. The partitioning of the data into different combinations of frequency, phase, and amplitude is established based on the mode and/or specific control bits and function pins.

Although the various modes are described independently, they can be enabled simultaneously. This provides an unprecedented level of flexibility for generating complex modulation schemes. However, to avoid multiple data sources from driving the same DDS signal control parameter, the device has a built-in priority protocol.

In single tone mode, the DDS signal control parameters come directly from the profile programming registers. In digital ramp modulation mode, the DDS signal control parameters are delivered by a digital ramp generator. In parallel data port modulation mode, the DDS signal control parameters are driven directly into the parallel port.

The various modulation modes generally operate on only one of the DDS signal control parameters (two in the case of the polar modulation format via the parallel data port). The unmodulated DDS signal control parameters are stored in programming registers and automatically routed to the DDS based on the selected mode.

A separate output shift keying (OSK) function is also available. This function employs a separate digital linear ramp generator that affects only the amplitude parameter of the DDS. The OSK function has priority over the other data sources that can drive the DDS amplitude parameter. As such, no other data source can drive the DDS amplitude when the OSK function is enabled.

SINGLE TONE MODE

In single tone mode, the DDS signal control parameters are supplied directly from the profile programming registers. A profile is an independent register that contains the DDS signal control parameters. Eight profile registers are available. Note that the profile pins must select the desired register.

PROFILE MODULATION MODE

Each profile is independently accessible. For FSK, PSK, or ASK modulation, use the three external profile pins (PS[2:0]) to select the desired profile. A change in the state of the profile pins with the next rising edge on SYNC_CLK updates the DDS with the parameters specified by the selected profile. Therefore, the profile change must meet the setup and hold times to the SYNC_CLK rising edge. Note that amplitude control must also be enabled using the OSK enable bit in the CFR1 register (0x00[8]).

DIGITAL RAMP MODULATION MODE

In digital ramp modulation mode, the modulated DDS signal control parameter is supplied directly from the digital ramp generator (DRG). The ramp generation parameters are controlled through the serial or parallel input/output port.

The ramp generation parameters allow the user to control both the rising and falling slopes of the ramp. The upper and lower boundaries of the ramp,the step size and step rate of the rising portion of the ramp, and the step size and step rate of the falling portion of the ramp are all programmable.

The ramp is digitally generated with 32-bit output resolution. The 32-bit output of the DRG can be programmed to affect frequency, phase, or amplitude. When programmed for frequency, all 32 bits are used. However, when programmed for phase or amplitude, only the 16 MSBs or 12 MSBs, respectively, are used.

The ramp direction (rising or falling) is externally controlled by the DRCTL pin. An additional pin (DRHOLD) allows the user to suspend the ramp generator in the present state. Note that amplitude control must also be enabled using the OSK enable bit in Register CFR1.

PARALLEL DATA PORT MODULATION MODE

In parallel data port modulation mode, the modulated DDS signal control parameter(s) are supplied directly from the 32-bit parallel data port. The function pins define how the 32-bit data-word is applied to the DDS signal control parameters. Formatting of the 32-bit data-word is unsigned binary, regardless of the destination.

Parallel Data Clock (SYNC_CLK)

The AD9914 generates a clock signal on the SYNC_CLK pin that runs at 1/24 of the DAC sample rate (the sample rate of the parallel data port). SYNC_CLK serves as a data clock for the parallel port.

PROGRAMMABLE MODULUS MODE

In programmable modulus mode, the DRG is used as an auxiliary accumulator to alter the frequency equation of the DDS core, making it possible to implement fractions that are not restricted to a power of 2 in the denominator. A standard DDS is restricted to powers of 2 as a denominator because the phase accumulator is a set of bits as wide as the frequency tuning word (FTW).

When in programmable modulus mode, however, the frequency equation is:

$$f_0 = (f_S)(FTW + A/B)/2^{32}$$

Where $f_0/f_S < ½$, $0 \le FTW < 2^{31}$, $2 \le B \le 2^{32} - 1$, and $A < B$.

This equation implies a modulus of $B \times 2^{32}$ (rather than 2^{32}, in the case of a standard DDS). Furthermore, because B is programmable, the result is a DDS with a programmable modulus.

FUNCTIONAL BLOCK DETAIL

DDS CORE

The direct digital synthesizer (DDS) block generates a reference signal (sine or cosine based on Register 0x00, Bit 16, the enable sine output bit). The parameters of the reference signal (frequency, phase, and amplitude) are applied to the DDS at the frequency, phase offset, and amplitude control inputs, as shown in Figure 30.

The output frequency (f_{OUT}) of the AD9914 is controlled by the frequency tuning word (FTW) at the frequency control input to the DDS. The relationship among f_{OUT}, FTW, and f_{SYSCLK} is given by

$$f_{OUT} = \left(\frac{FTW}{2^{32}}\right) f_{SYSCLK} \quad (1)$$

where *FTW* is a 32-bit integer ranging in value from 0 to 2,147,483,647 ($2^{31} - 1$), which represents the lower half of the full 32-bit range. This range constitutes frequencies from dc to Nyquist (that is, ½ f_{SYSCLK}).

The FTW required to generate a desired value of f_{OUT} is found by solving Equation 1 for FTW, as given in Equation 2.

$$FTW = \text{round}\left(2^{32}\left(\frac{f_{OUT}}{f_{SYSCLK}}\right)\right) \quad (2)$$

where the round(*x*) function rounds the argument (the value of x) to the nearest integer. This is required because the FTW is constrained to be an integer value. For example, for f_{OUT} = 41 MHz and f_{SYSCLK} = 122.88 MHz, FTW = 1,433,053,867 (0x556AAAAB).

Programming an FTW greater than 2^{31} produces an aliased image that appears at a frequency given by

$$f_{OUT} = \left(1 - \frac{FTW}{2^{32}}\right) f_{SYSCLK}$$

for FTW ≥ 2^{31}

The relative phase of the DDS signal can be digitally controlled by means of a 16-bit phase offset word (POW). The phase offset is applied prior to the angle to amplitude conversion block internal to the DDS core. The relative phase offset ($\Delta\theta$) is given by

$$\Delta\theta = \begin{vmatrix} 2\pi\left(\frac{POW}{2^{16}}\right) \\ 360\left(\frac{POW}{2^{16}}\right) \end{vmatrix}$$

Where the upper quantity is for the phase offset expressed as radian units and the lower quantity as degrees.

To find the POW value necessary to develop an arbitrary $\Delta\theta$, solve the preceding equation for POW and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

The relative amplitude of the DDS signal can be digitally scaled (relative to full scale) by means of a 12-bit amplitude scale factor (ASF). The amplitude scale value is applied at the output of the angle to amplitude conversion block internal to the DDS core. The amplitude scale is given by

$$Amplitude\ Scale = \begin{vmatrix} \frac{ASF}{2^{12}} \\ 20\log\left(\frac{ASF}{2^{12}}\right) \end{vmatrix} \quad (3)$$

where the upper quantity is amplitude expressed as a fraction of full scale and the lower quantity is expressed in decibels relative to full scale.

To find the ASF value necessary for a particular scale factor, solve Equation 3 for ASF and round the result (in a manner similar to that described previously for finding an arbitrary FTW).

When the AD9914 is programmed to modulate any of the DDS signal control parameters, the maximum modulation sample rate is 1/24 f_{SYSCLK}. This means that the modulation signal exhibits images at multiples of 1/24 f_{SYSCLK}. The impact of these images must be considered when using the device as a modulator.

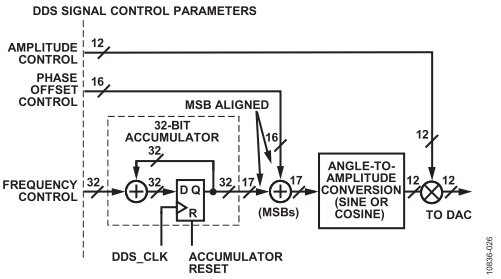

Figure 30. DDS Block Diagram

12-BIT DAC OUTPUT

The AD9914 incorporates an integrated 12-bit, current output DAC. The output current is delivered as a balanced signal using two outputs. The use of balanced outputs reduces the potential amount of common-mode noise present at the DAC output, offering the advantage of an increased signal-to-noise ratio. An external resistor (R_{SET}) connected between the DAC_RSET pin and AGND establishes the reference current. The recommended value of R_{SET} is 3.3 kΩ.

Attention must be paid to the load termination to keep the output voltage within the specified compliance range; voltages developed beyond this range cause excessive distortion and can damage the DAC output circuitry.

DAC CALIBRATION OUTPUT

The DAC CAL enable bit in the CFR4 control register (0x03[24]) must be manually set and then cleared after each power-up and every time the REF CLK or internal system clock is changed. This initiates an internal calibration routine to optimize the setup and hold times for internal DAC timing. Failure to calibrate may degrade performance and even result in loss of functionality. The length of time to calibrate the DAC clock is calculated from the following equation:

$$t_{CAL} = \frac{469{,}632}{f_S}$$

RECONSTRUCTION FILTER

The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth.

Because the DAC constitutes a sampled system, the output must be filtered so that the analog waveform accurately represents the digital samples supplied to the DAC input. The unfiltered DAC output contains the desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd numbered images (shown in Figure 31) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample-and-hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter must preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains significant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a third-, fifth-, or seventh-order elliptic low-pass filter is common.

Some applications operate from an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter. The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

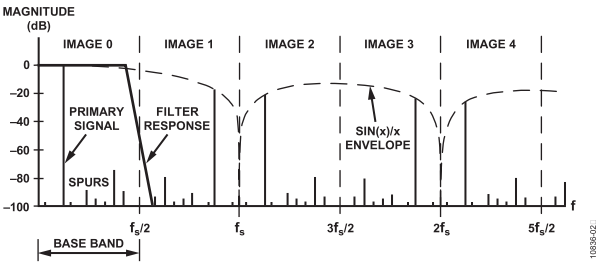

Figure 31. DAC Spectrum vs. Reconstruction Filter Response

ANALOG DEVICES

1 GSPS Direct Digital Synthesizer with 14-Bit DAC

AD9912

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz output directly)
- Integrated 1 GSPS 14-bit DAC
- 48-bit frequency tuning word with 4 μHz resolution
- Differential HSTL comparator
- Flexible system clock input accepts either crystal or external reference clock
- On-chip low noise PLL REFCLK multiplier
- 2 SpurKiller channels
- Low jitter clock doubler for frequencies up to 750 MHz
- Single-ended CMOS comparator; frequencies of <150 MHz
- Programmable output divider for CMOS output
- Serial I/O control
- Excellent dynamic performance
- Software controlled power-down
- Available in two 64-lead LFCSP packages
- Residual phase noise @ 250 MHz
  - 10 Hz offset: –113 dBc/Hz
  - 1 kHz offset: –133 dBc/Hz
  - 100 kHz offset: –153 dBc/Hz
  - 40 MHz offset: –161 dBc/Hz

APPLICATIONS

- Agile LO frequency synthesis
- Low jitter, fine tune clock generation
- Test and measurement equipment
- Wireless base stations and controllers
- Secure communications
- Fast frequency hopping

GENERAL DESCRIPTION

The AD9912 is a direct digital synthesizer (DDS) that features an integrated 14-bit digital-to-analog converter (DAC). The AD9912 features a 48-bit frequency tuning word (FTW) that can synthesize frequencies in step sizes no larger than 4 μHz. Absolute frequency accuracy can be achieved by adjusting the DAC system clock.

The AD9912 also features an integrated system clock phase-locked loop (PLL) that allows for system clock inputs as low as 25 MHz.

The AD9912 operates over an industrial temperature range, spanning –40°C to + 85°C.

BASIC BLOCK DIAGRAM

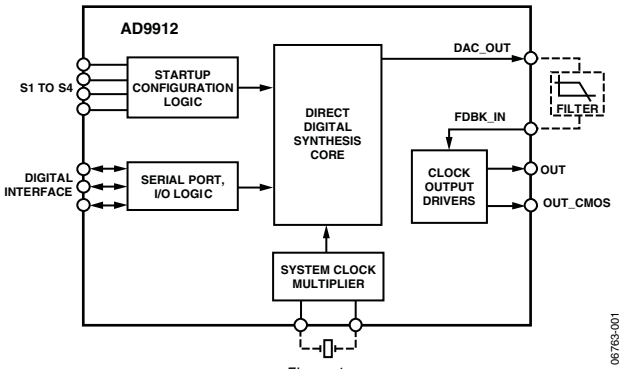

Figure 1.

Rev. F

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TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, AVDD3, and DVDD at nominal supply voltage; DAC R_{SET} = 10 kΩ, unless otherwise noted. See Figure 26 for 1 GHz reference phase noise used for generating these plots.

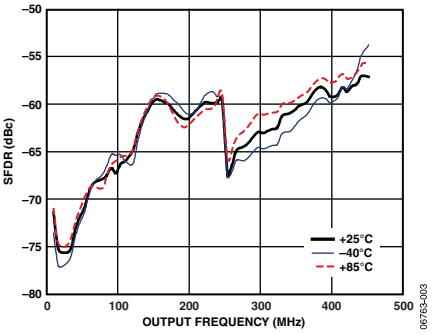

Figure 3. Wideband SFDR vs. Output Frequency at –40°C, +25°C, and +85°C, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

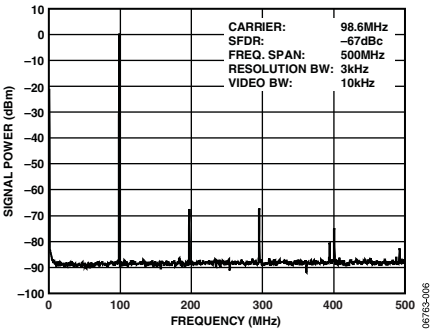

Figure 6. Wideband SFDR at 98.6 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

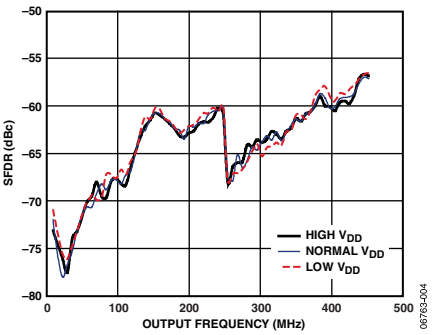

Figure 4. Variation of Wideband SFDR vs. Frequency over DAC Power Supply Voltage, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

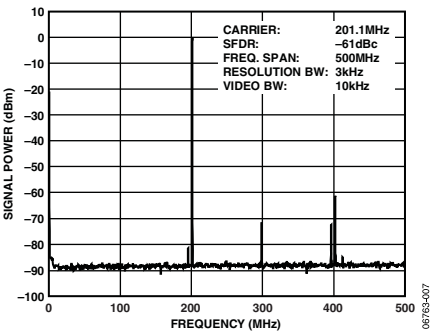

Figure 7. Wideband SFDR at 201.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

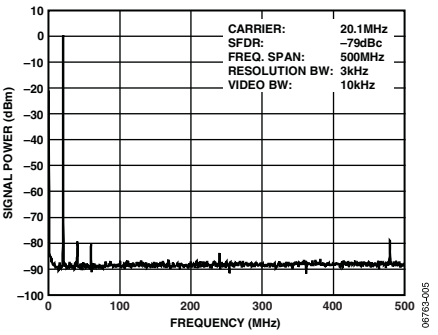

Figure 5. Wideband SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

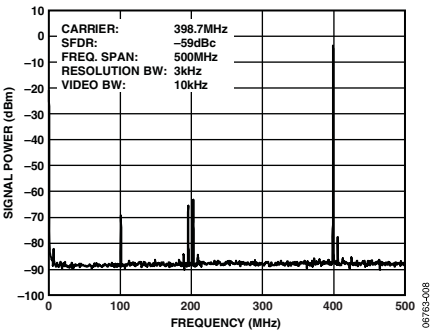

Figure 8. Wideband SFDR at 398.7 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

AD9912

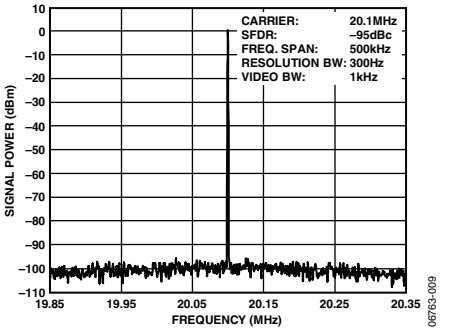

Figure 9. Narrow-Band SFDR at 20.1 MHz, SYSCLK = 1 GHz (SYSCLK PLL Bypassed)

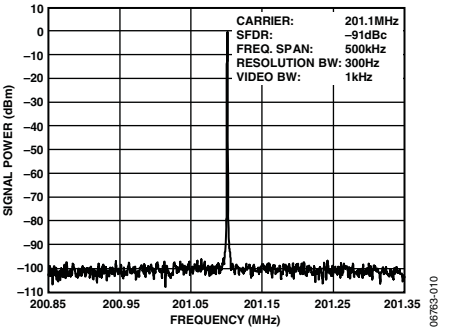

Figure 10. Narrow-Band SFDR at 201.1 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

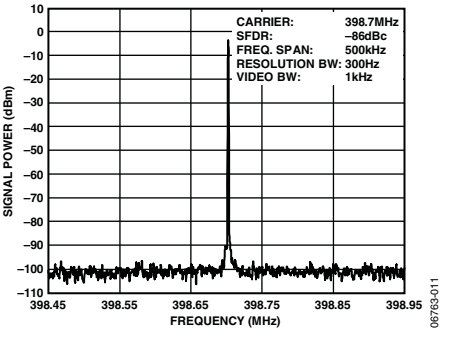

Figure 11. Narrow-Band SFDR at 398.7 MHz, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

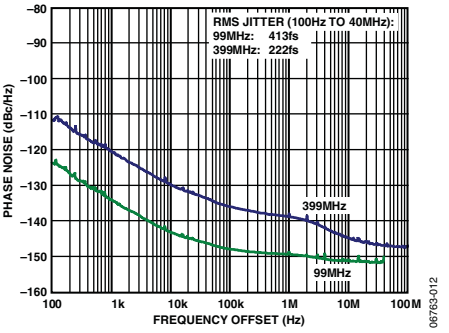

Figure 12. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)

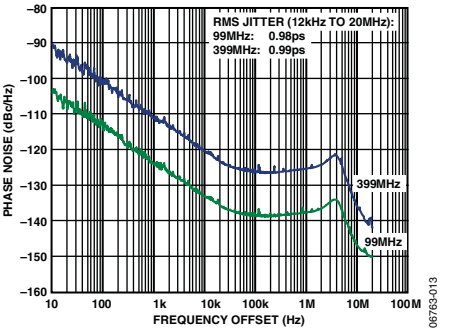

Figure 13. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 83.33 MHz)

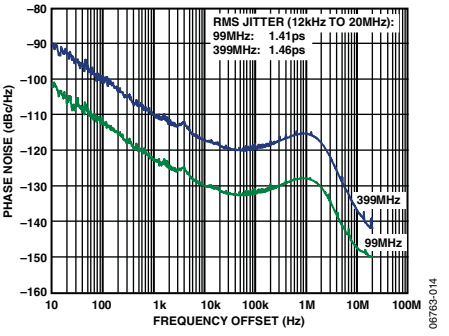

Figure 14. Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz (SYSCLK PLL Driven by Rohde & Schwarz SMA100 Signal Generator at 25 MHz)

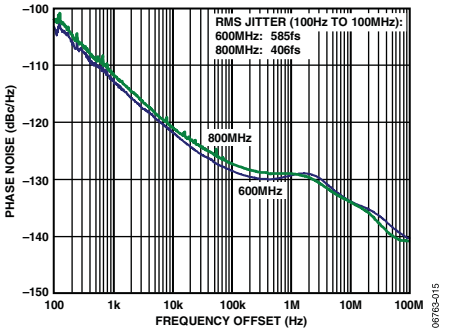

Figure 15. *Absolute Phase Noise Using HSTL Driver, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed), HSTL Output Doubler Enabled*

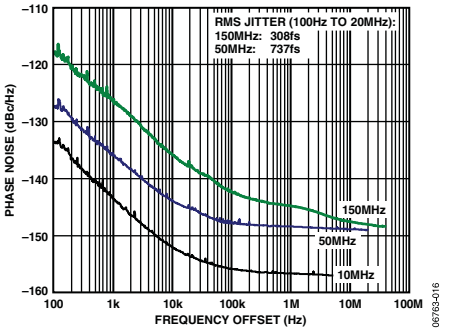

Figure 16. *Absolute Phase Noise Using CMOS Driver at 3.3 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed) DDS Run at 200 MSPS for 10 MHz Plot*

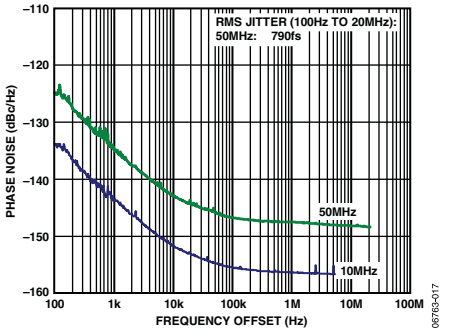

Figure 17. *Absolute Phase Noise Using CMOS Driver at 1.8 V, SYSCLK = 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

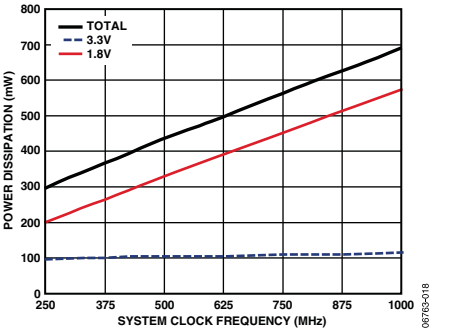

Figure 18. *Power Dissipation vs. System Clock Frequency (SYSCLK PLL Bypassed), $f_{OUT} = f_{SYSCLK}/5$, HSTL Driver On, CMOS Driver On, SpurKiller Off*

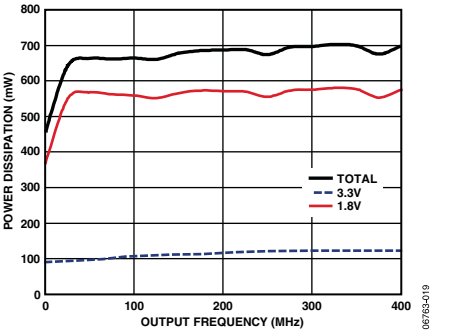

Figure 19. *Power Dissipation vs. Output Frequency SYSCLK = 1 GHz (SYSCLK PLL Bypassed), HSTL Driver On, CMOS Driver On, SpurKiller Off*

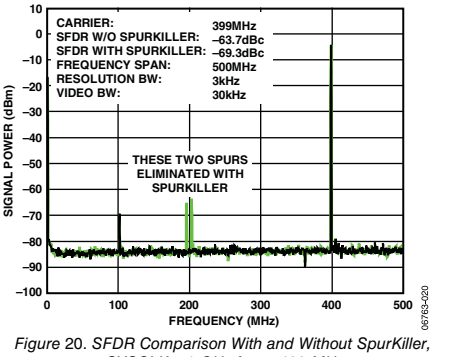

Figure 20. *SFDR Comparison With and Without SpurKiller, SYSCLK = 1 GHz, f_{OUT} = 400 MHz*

AD9912

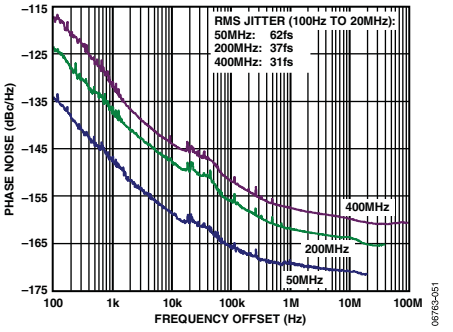

Figure 21. *Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 50 MHz, 200 MHz, and 400 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

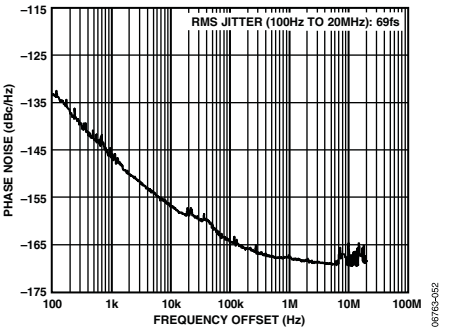

Figure 22. *Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 63 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

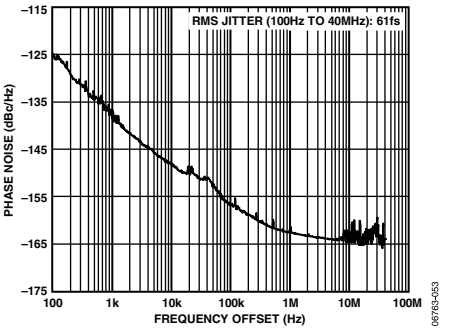

Figure 23. *Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 171 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

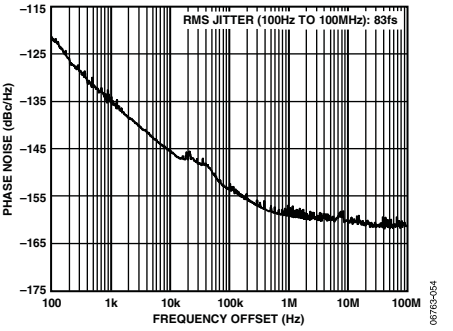

Figure 24. *Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 258.3 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

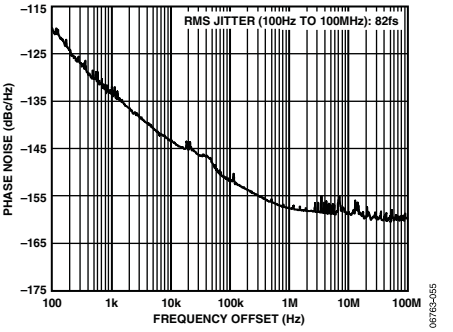

Figure 25. *Absolute Phase Noise of Unfiltered DAC Output, f_{OUT} = 311.6 MHz, SYSCLK Driven by a 1 GHz Wenzel Oscillator (SYSCLK PLL Bypassed)*

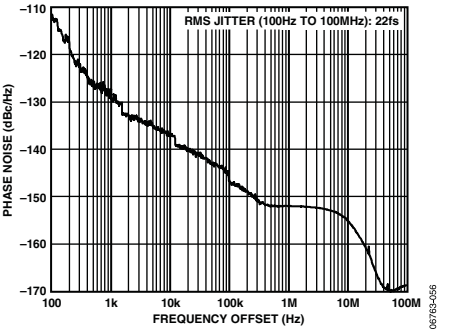

Figure 26. *Absolute Phase Noise of 1 GHz Reference Used for Performance Plots; Wenzel Components Used: 100 MHz Oscillator, LNBA-13-24 Amp, LNOM 100-5 Multiplier, LNDD 500-14 Diode Doubler*

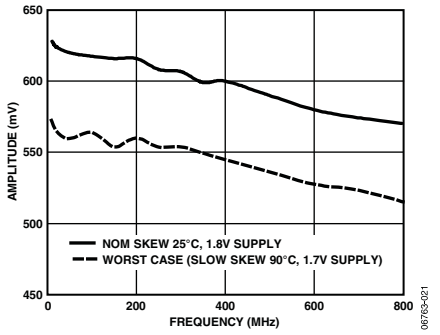

Figure 27. *HSTL Output Driver Single-Ended Peak-to-Peak Amplitude vs. Toggle Rate* (100 Ω *Across Differential Pair*)

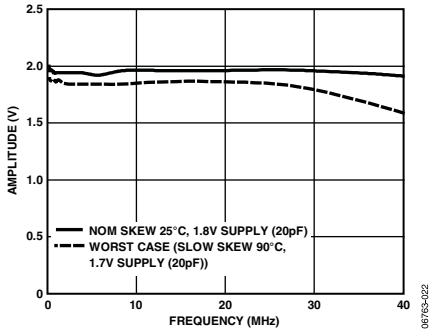

Figure 28. *CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate* (*AVDD*3 = 1.8 *V*) *with* 20 *pF Load*

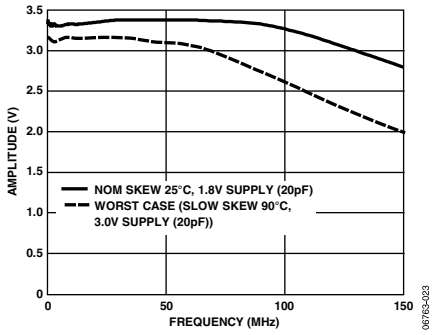

Figure 29. *CMOS Output Driver Peak-to-Peak Amplitude vs. Toggle Rate* (*AVDD*3 = 3.3 *V*) *with* 20 *pF Load*

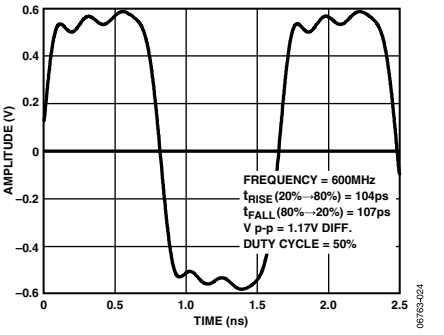

Figure 30. *Typical HSTL Output Waveform, Nominal Conditions, DC-Coupled, Differential Probe Across* 100 Ω *load*

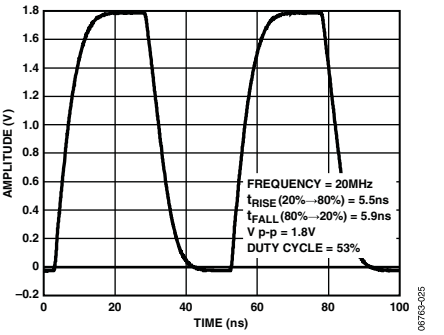

Figure 31. *Typical CMOS Output Driver Waveform* (@ 1.8 *V*), *Nominal Conditions, Estimated Capacitance* = 5 *pF*

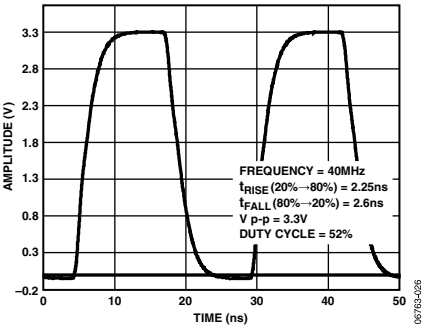

Figure 32. *CMOS Output Driver Waveform* (@ 3.3 *V*), *Nominal Conditions, Estimated Capacitance* = 5 *pF*

THEORY OF OPERATION

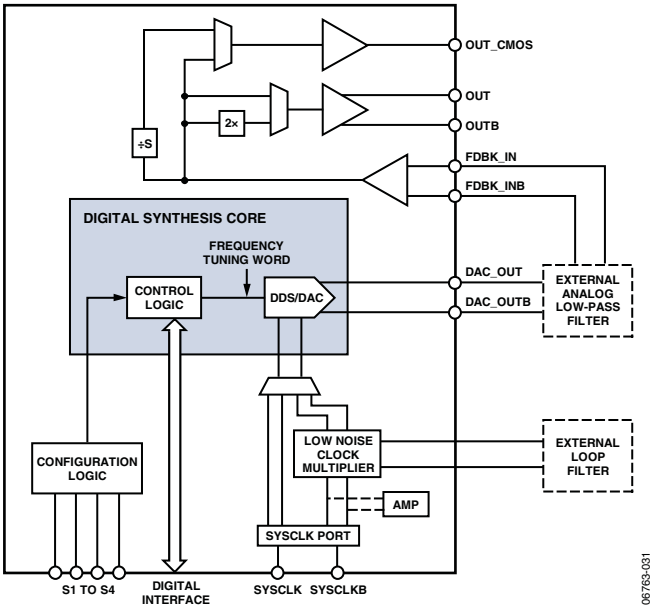

Figure 39. Detailed Block Diagram

OVERVIEW

The AD9912 is a high performance, low noise, 14-bit DDS clock synthesizer with integrated comparators for applications desiring an agile, finely tuned square or sinusoidal output signal. A digitally controlled oscillator (DCO) is implemented using a direct digital synthesizer (DDS) with an integrated output DAC, clocked by the system clock.

A bypassable PLL-based frequency multiplier is present, enabling use of an inexpensive, low frequency source for the system clock. For best jitter performance, the system clock PLL should be bypassed, and a low noise, high frequency system clock should be provided directly. Sampling theory sets an upper bound for the DDS output frequency at 50% of f_S (where f_S is the DAC sample rate), but a practical limitation of 40% of f_S is generally recommended to allow for the selectivity of the required off-chip reconstruction filter.

The output signal from the reconstruction filter can be fed back to the AD9912 to be processed through the output circuitry.

The output circuitry includes HSTL and CMOS output buffers, as well as a frequency doubler for applications that need frequencies above the Nyquist level of the DDS.

The AD9912 also offers preprogrammed frequency profiles that allow the user to generate frequencies without programming the part. The individual functional blocks are described in the following sections.

DIRECT DIGITAL SYNTHESIZER (DDS)

The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{48} counter with a programmable step size that is determined by the frequency tuning word (FTW). A block diagram of the DDS is shown in Figure 40.

AD9912

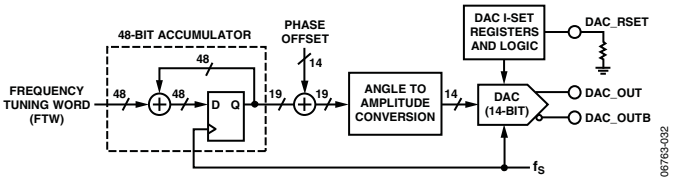

Figure 40. DDS Block Diagram

The input to the DDS is a 48-bit FTW that provides the accumulator with a seed value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total of its output. For example, given an FTW = 5, the accumulator increments the count by 5 sec on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case) and then rolls over, retaining the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The following equation defines the average rollover rate of the accumulator and establishes the output frequency (f_{DDS}) of the DDS:

$$f_{DDS} = \left(\frac{FTW}{2^{48}}\right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48}\left(\frac{f_{DDS}}{f_S}\right)\right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 19.44 MHz, then FTW = 5,471,873,547,255 (0x04FA05143BF7).

The relative phase of the sinusoid can be controlled numerically, as well. This is accomplished using the phase offset function of the DDS (a programmable 14-bit value (Δphase); see the I/O Register Map section). The resulting phase offset, ΔΦ (radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{14}}\right)$$

DIGITAL-TO-ANALOG (DAC) OUTPUT

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. This series is translated to an analog signal by means of a digital-to-analog converter (DAC).

The DAC outputs its signal to two pins driven by a balanced current source architecture (see the DAC output diagram in Figure 41). The peak output current derives from a combination of two factors. The first is a reference current (I_{DAC_REF}) that is established at the DAC_RSET pin, and the second is a scale factor that is programmed into the I/O register map.

The value of I_{DAC_REF} is set by connecting a resistor (R_{DAC_REF}) between the DAC_RSET pin and ground. The DAC_RSET pin is internally connected to a virtual voltage reference of 1.2 V nominal, so the reference current can be calculated by

$$I_{DAC_REF} = \frac{1.2}{R_{DAC_REF}}$$

Note that the recommended value of I_{DAC_REF} is 120 μA, which leads to a recommended value for R_{DAC_REF} of 10 kΩ.

The scale factor consists of a 10-bit binary number (FSC) programmed into the DAC full-scale current register in the I/O register map. The full-scale DAC output current (I_{DAC_FS}) is given by

$$I_{DAC_FS} = I_{DAC_REF}\left(72 + \frac{192FSC}{1024}\right)$$

sing the recommended value of R_{DAC_REF}, the full-scale DAC output current can be set with 10-bit granularity over a range of approximately 8.6 mA to 31.7 mA. 20 mA is the default value.

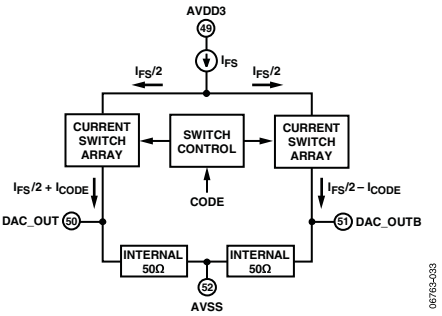

Figure 41. DAC Output

RECONSTRUCTION FILTER

The origin of the output clock signal produced by the AD9912 is the combined DDS and DAC. The DAC output signal appears as a sinusoid sampled at f_S. The frequency of the sinusoid is determined by the frequency tuning word (FTW) that appears at the input to the DDS. The DAC output is typically passed through an external reconstruction filter that serves to remove the artifacts of the sampling process and other spurs outside the filter bandwidth. If desired, the signal can then be brought back on-chip to be converted to a square wave that is routed internally to the output clock driver or the 2× DLL multiplier.

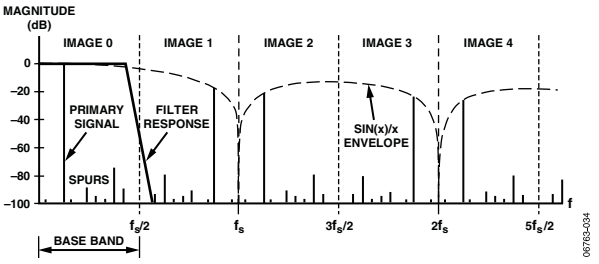

Figure 42. DAC Spectrum vs. Reconstruction Filter Response

Because the DAC constitutes a sampled system, its output must be filtered so that the analog waveform accurately represents the tdigital samples supplied to the DAC input. The unfiltered DAC output contains the (typically) desired baseband signal, which extends from dc to the Nyquist frequency ($f_S/2$). It also contains images of the baseband signal that theoretically extend to infinity. Notice that the odd images (shown in Figure 42) are mirror images of the baseband signal. Furthermore, the entire DAC output spectrum is affected by a sin(x)/x response, which is caused by the sample-and-hold nature of the DAC output signal.

For applications using the fundamental frequency of the DAC output, the response of the reconstruction filter should preserve the baseband signal (Image 0), while completely rejecting all other images. However, a practical filter implementation typically exhibits a relatively flat pass band that covers the desired output frequency plus 20%, rolls off as steeply as possible, and then maintains signi cant (though not complete) rejection of the remaining images. Depending on how close unwanted spurs are to the desired signal, a third-, fifth-, or seventh-order elliptic low-pass filter is common.

Some applications operate off an image above the Nyquist frequency, and those applications use a band-pass filter instead of a low-pass filter.

The design of the reconstruction filter has a significant impact on the overall signal performance. Therefore, good filter design and implementation techniques are important for obtaining the best possible jitter results.

FDBK_IN INPUTS

The FDBK_IN pins serve as the input to the comparators and output drivers of the AD9912. Typically, these pins are used to receive the signal generated by the DDS after it has been band-limited by the external reconstruction filter.

A diagram of the FDBK_IN input pins is provided in Figure 43, which includes some of the internal components used to bias the input circuitry. Note that the FDBK_IN input pins are internally biased to a dc level of ~1 V. Care should be taken to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance.

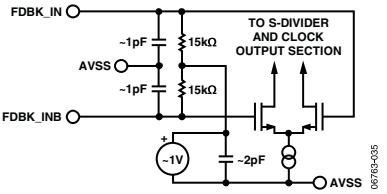

Figure 43. Differential FDBK_IN Inputs

Although the worst spurs tend to be harmonic in origin, the fact that the DAC is part of a sampled system results in the possibility of spurs appearing in the output spectrum that are not harmonically related to the fundamental. For example, if the DAC is sampled at 1 GHz and generates an output sinusoid of 170 MHz, the fifth harmonic would normally be at 850 MHz. However, because of the sampling process, this spur appears at 150 MHz, only 20 MHz away from the fundamental. Therefore, when attempting to reduce DAC spurs it is important to know the actual location of the harmonic spur in the DAC output spectrum based on the DAC sample rate so that its harmonic number can be reduced.

The mechanics of performing harmonic spur reduction is shown in Figure 48. It essentially consists of two additional DDS cores operating in parallel with the original DDS. This enables the user to reduce two different harmonic spurs from the second to the 15th with nine bits of phase offset control (±π) and eight bits of amplitude control.

The dynamic range of the cancellation signal is further augmented by a gain bit associated with each channel. When this bit is set, the magnitude of the cancellation signal is doubled by employing a 1-bit left-shift of the data. However, the shift operation reduces the granularity of the cancellation signal magnitude. The full-scale amplitude of a cancellation spur is approximately –60 dBc when the gain bit is a Logic 0 and approximately –54 dBc when the gain bit is a Logic 1.

The procedure for tuning the spur reduction is as follows:

1. Determine which offending harmonic spur to reduce and its amplitude. Enter that harmonic number into Bit 0 to Bit 3 of Register 0x0500/Register 0x0505.
2. Turn off the fundamental by setting Bit 7 of Register 0x0013 and enable the SpurKiller channel by setting Bit 7 of Register 0x0500/Register 0x0505.
3. Adjust the amplitude of the SpurKiller channel so that it matches the amplitude of the offending spur.
4. Turn the fundamental on by clearing Bit 7 of Register 0x0013.
5. Adjust the phase of the SpurKiller channel so that maximum interference is achieved.

Note that the SpurKiller setting is sensitive to the loading of the DAC output pins, and that a DDS reset is required if a SpurKiller channel is turned off. The DDS can be reset by setting Bit 0 of Register 0x0012, and resetting the part is not necessary.

The performance improvement offered by this technique varies widely and depends on the conditions used. Given this extreme variability, it is impossible to dene a meaningful specification to guarantee SpurKiller performance. Current data indicate that a 6 dB to 8 dB improvement is possible for a given output frequency using a common setting over process, temperature, and voltage. There are frequencies, however, where a common setting can result in much greater improvement. Manually adjusting the SpurKiller settings on individual parts can result in more than 30 dB of spurious performance improvement.

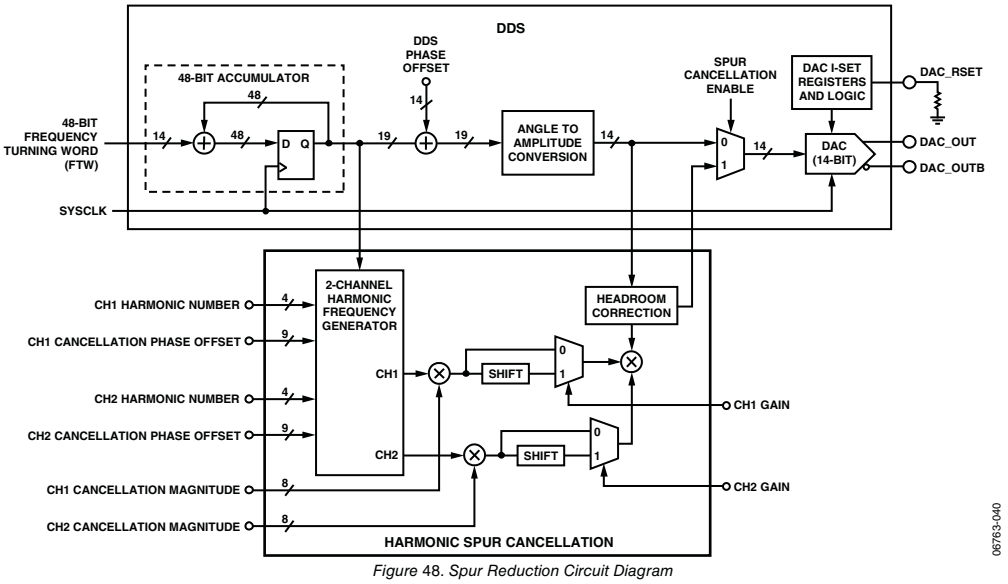

Figure 48. Spur Reduction Circuit Diagram

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APPENDIX D

MMIC-BASED SYNTHESIZERS

D-1 INTRODUCTION

The design of monolithic microwave integrated circuit (MMIC)-based synthesizers is limited to companies equipped with GaAs foundries, but the synthesizers are interesting in the sense of seeing where the frequency limitations lie. As previously outlined, the millimeter-wave oscillators generally have a low Q and therefore are fairly noisy. This means they either have to be cleaned up by a wide loop bandwidth or special precautions must be taken to make them high performance.

Figure D-1 shows the component diagram of such a voltage-controlled oscillator (VCO). This particular VCO has been selected on the basis of common source, common gate, and common drain as outlined in Figure D-2.

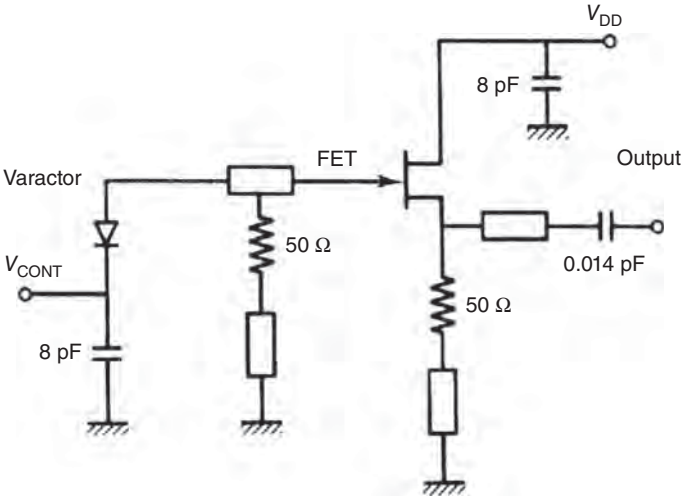


Figure D-1 VCO circuit diagram.

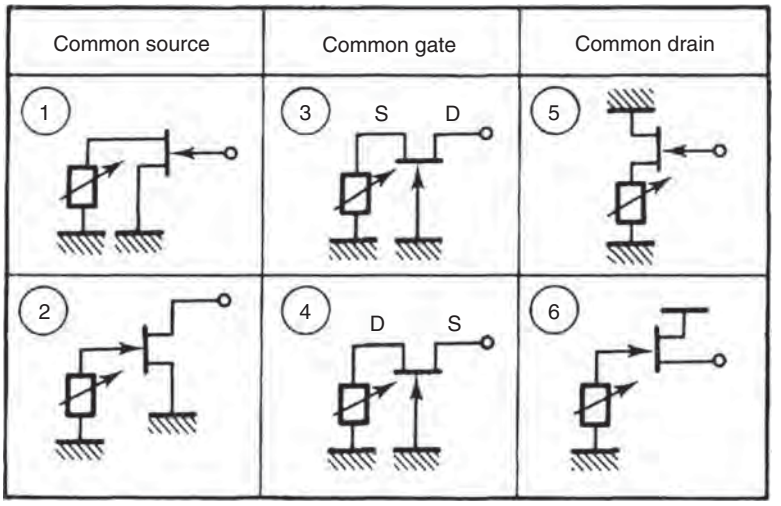


Figure D-2 VCO circuit configurations.

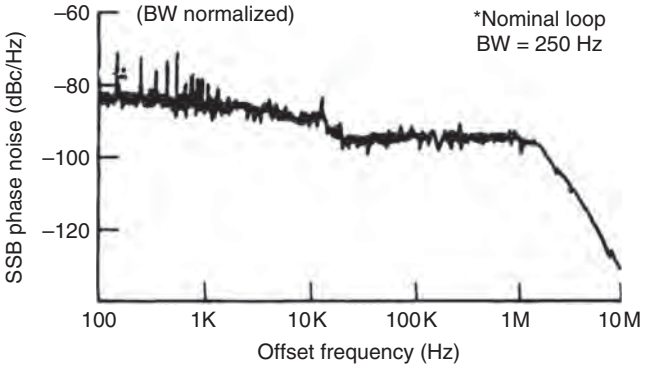


Figure D-3 VCO output single-sideband (SSB) phase noise (f_{osc} = 15.0 GHz).

Figure D-3 shows the measured phase noise of such a VCO at 18 GHz using a characteristic MMIC chip. In order to obtain the appropriate frequency division, a parametric type of frequency divider must be used, as shown in Figure D-4. The dividers can be characterized as either regenerative, dynamic, or static devices. The dynamic frequency divider refers to a "flip-flop" type of frequency divider using a delay line between the input and output and is built on a heterojunction bipolar approach. These types of divider have been built up to 26 GHz. The regenerative frequency dividers are built on the popular principle shown in Figure D-5. A modification of this principle using a double-balanced mixer can also be used as a frequency doubler. This Ku band frequency synthesizer is contained in two GaAs monolithic chips, as shown in Figure D-6.

Some of these integrated circuits can be obtained as discrete components. Figure D-7 shows a high-gain stage model MGF7201 GaAs monolithic microwave IC. At 14 GHz it exhibits 20-dB gain and approximately 20-dBm output power.

Figure D-8 shows a photograph of the MMIC synthesizer.

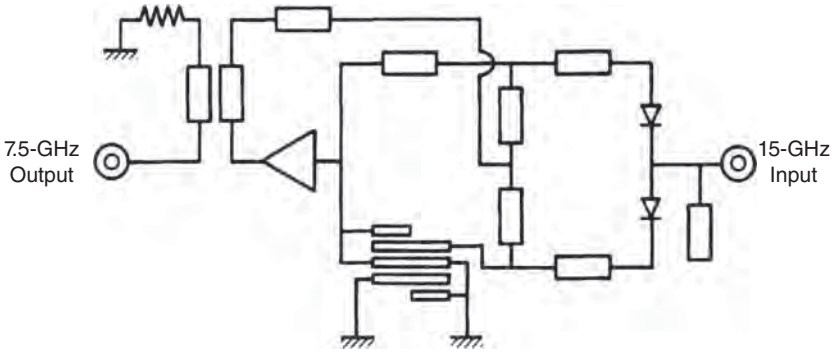


Figure D-4 MMIC frequency divider.

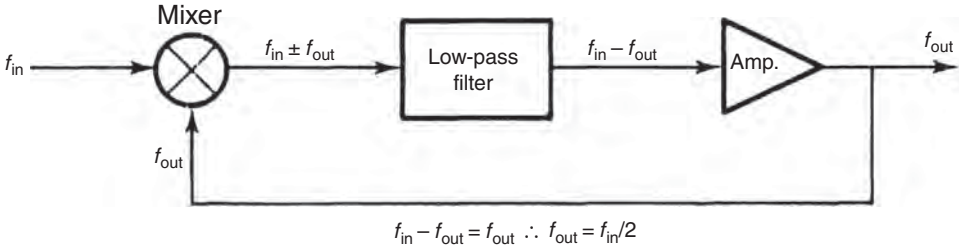


Figure D-5 Principle of the regenerative frequency divider.

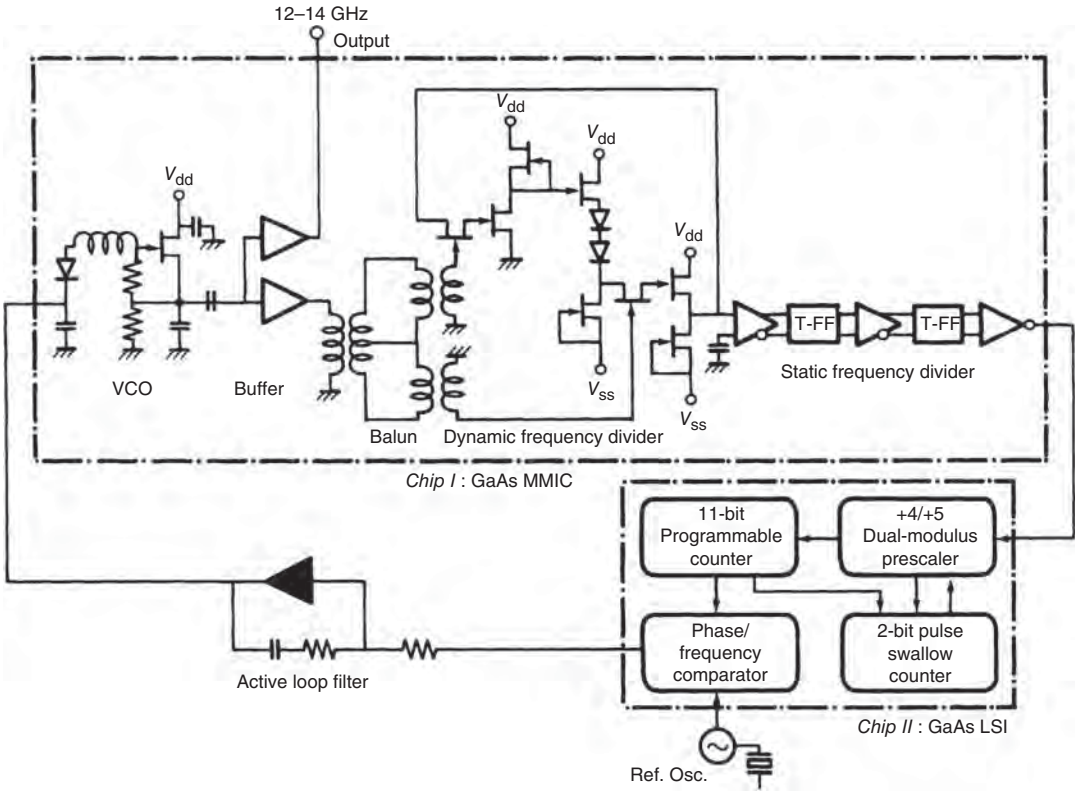
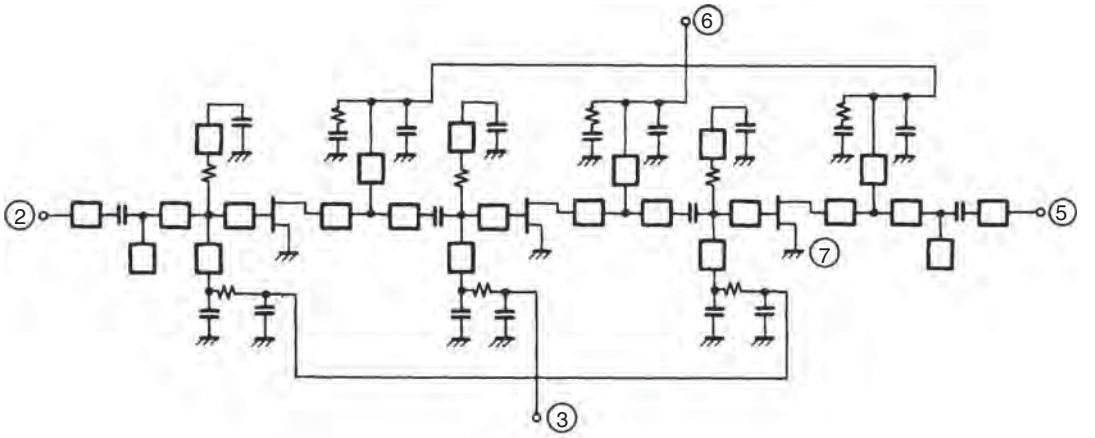


Figure D-6 Ku-band frequency synthesizer integrated in two GaAs monolithic chips.



Precaution
It is recommended to connect dc block capacitors to input and output terminal (2 and 5) in order to prevent failure to surge

Figure D-7 Equivalent circuit of the IC.

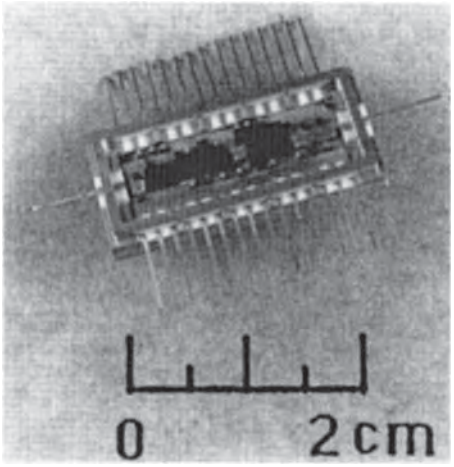


Figure D-8 Photograph of synthesizer.

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APPENDIX E

ARTICLES ON DESIGN OF DIELECTRIC RESONATOR OSCILLATORS

E-1 THE DESIGN OF AN ULTRA-LOW PHASE NOISE DRO[1]

E-1-1 Basic Considerations and Component Selection

A dielectric resonator is basically a cylindrical puck made of material with high permittivity and a low dissipation factor. This does imply that at the boundary, any field distribution does have a large tangential component ratio of the electrical displacement inside the puck compared with its outside, because the tangential electrical field is steady on the boundary. Any resonator arrangement within a closed conductive surface does exhibit Eigenmodes, the real parts of which are determined mainly by the physical dimensions of the puck and the imaginary part, mainly by dielectrical volume loss inside the dielectric resonator (DR) and to surface conductor loss outside.

The environment the puck is surrounded with does have a minor influence on the real part as well. As we will see later depending on the volume of the conductive containment and its surface conductivity, the unloaded quality factor Q_u of a DR may drop from, for example, 4500 (1/tg(δ) of the material) to about 3000 at 10 GHz. In order to allow interaction with an active device (gain element), an appropriate waveguide arrangement needs to be created that allows for electromagnetic (EM) energy being transferred from and to the resonator. Depending on the dielectric resonator oscillator (DRO) topology, power may leak to even more ports. The externally consumed power does lead to a more or less reduced loaded figure of merit Q_L according to the well-known equation

$$\frac{1}{Q_L} = \frac{1}{Q_u} + \frac{1}{Q_{\text{ext}}} = \frac{1}{Q_u} \cdot (1 + k) \tag{E-2}$$

where $k = Q_u/Q_{\text{ext}} = P_{\text{ext}}/P_{\text{res}}$ is the coupling coefficient.

A rough estimation of phase noise for a given loaded figure of merit Q_L can be obtained by Leeson's equation as explained thoroughly in [1].

For a DRO operating at $f_0 = 10$ GHz with $P_0 = -1.65$ dBm input to the oscillator core (gain element) having an effective noise figure of 3 dB ($F = 2$), a flicker corner of $f_c = 20$ kHz, and a loaded Q of 1 k, we would expect a phase noise value of -137 dBc/Hz at 100 kHz offset, which must be considered as fairly good for a 10 GHz source. However, in terms of the definitions in [1], this oscillator must still be viewed as a low-Q device since $f_c < F_L = f_0/(2Q_L) = 5$ MHz. The values for P_0 and Q_L are taken from the simulation results presented below, while those for f_c and F are reasonable assumptions (see Figure E-1).

[1]Thomas Hüllen (Part 1); Ulrich L. Rohde and Ajay K. Poddar (Part 2).

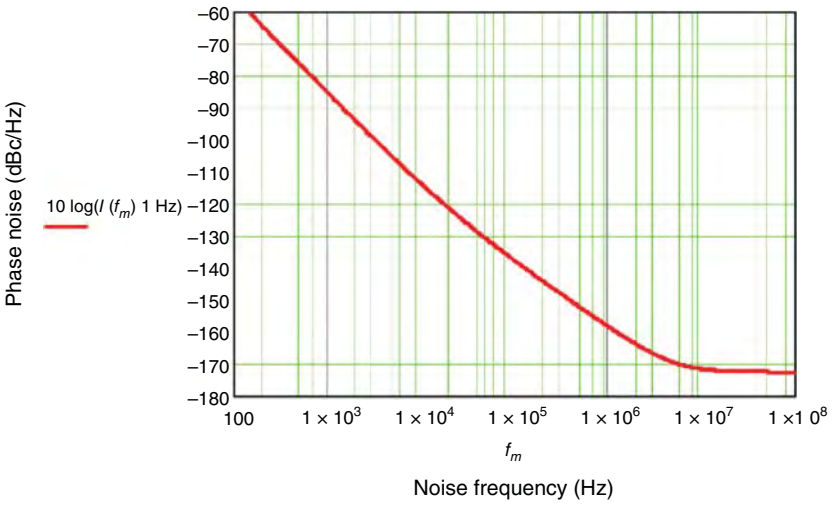


Figure E-1 Phase noise-versus-offset from carrier [1].

As we will see later, a Q_L of 1 k at 10 GHz is not easily achieved, even with a DR arrangement offering Q_u values of 4 k and above.

Nonlinear noise effects like the increase of noise figure with increasing input power are not included in this simple estimation and tend to deteriorate the phase noise further.

E-1-2 Component Selection

For the oscillator core and the necessary buffer amplifier, an active device among those with the lowest available noise figure at the frequency of interest should be chosen. For the 10 GHz DRO we chose the BFP740 SiGe transistor from Infineon, which has a minimum small signal noise figure of about 1.7 dB at 10 GHz and a transition frequency of >35 GHz for the target bias point of $V_{ce} = 3.5$ V and $I_c = 15$ mA. For a SiGe device, we expect a flicker corner somewhere between 10 and 100 kHz.

Infineon does provide both *S*-parameter data and a Gummel–Poon model for the transistor, ready to be used within Agilent/EEsof ADS2009 or AWR MWO. However, a simple comparison of the small signal *S*-parameters against the simulated data does raise some skepticism about the trustworthiness of either one of them or both (see Figure E-2).

The results of the other *S*-parameters diverge in a similar way for frequencies above 5 GHz. The situation for the noise parameters is even worse.

We decide to trust the measured *S*-parameter data for AC and assume that the model does properly reflect the real device behavior at DC.

The model is now optimized in such a way that its DC properties remain unchanged while all parameters with AC relevance (only including housing parasitics) are being altered to fit the measured data as good as possible (see Figure E-3).

Agreement between the model and tabulated noise data could not be established. This remains an open issue. However, since the final phase noise results do agree quite well with the prediction, the simulated transistor noise is likely to match the real behavior sufficiently well.

Lumped Passive Components

At microwave frequencies the use of lumped passives should be avoided wherever possible. For the remaining items we use ATC600L (0402 size) chip capacitors, Coilcraft 0402CS inductors, KOA0402 resistors, and the corresponding substrate and pad scalable models from Modelithics for simulation purposes. These include the effects

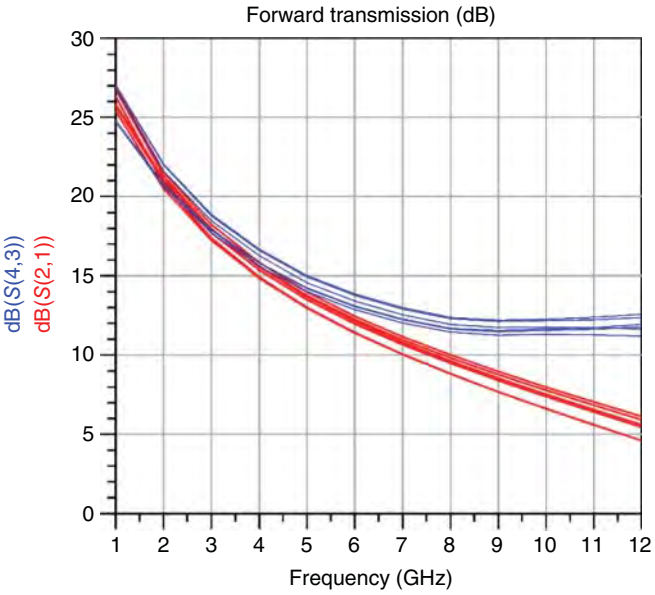


Figure E-2 S_{21} magnitude simulated (upper group of traces) and measured (lower group of traces) versus frequency for different bias conditions [1].

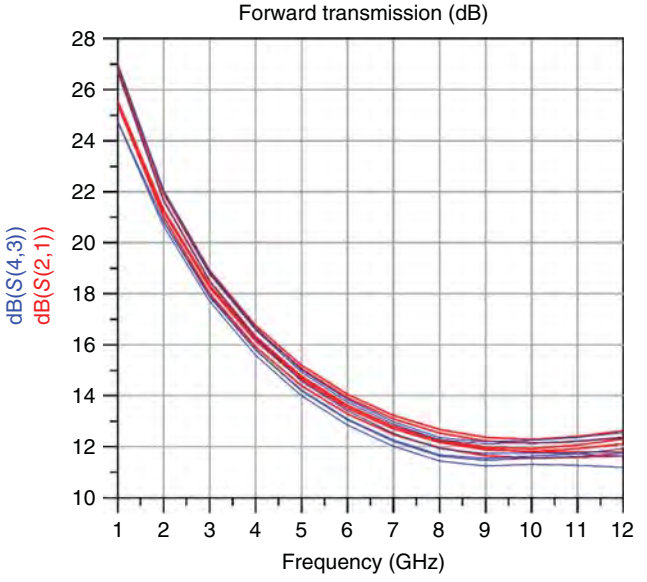


Figure E-3 S_{21} magnitude of the improved model simulated (upper group of traces) versus measured (lower group of traces) [1].

of the pads and in conjunction with the recently introduced SMD-ports in ADS2011/Momentum should guarantee a high accuracy for EM co-simulation at least at the fundamental of a quasi-stationary (harmonic balance—HB) simulation below and around 10 GHz.

However, since the validity of most of these lumped component models does not exceed 18 GHz, the accuracy of the simulation might suffer since the harmonics of an oscillator operating at frequencies above 6 GHz might not be predicted very well. Therefore, care should be taken to avoid excessive harmonic content at places where lumped passives are used, if possible.

Another potential problem in conjunction with the SMD-ports used in harmonic-balance simulations may arise if the attached two ports are not strictly symmetrical, which seems to be the case for some of the Modelithics models. This problem has been communicated to Modelithics, strongly supported by Agilent, but up to release 9.6 has not been resolved completely. In such cases the use of internal calibrated single ports is recommended.

Substrate Considerations

Low-loss high frequency circuit material with low thermal expansion coefficients (lateral and z-axis), such as RO4350B, is recommended. However, since the reported permittivity values differ depending on measurement method and substrate height, we rely on the most recent measurement-based data from Modelithics who have gained high reputation in accurate device modeling. For 10 mil RO4350, they report a mean relative permittivity of 4.0 instead of the Rogers recommendation of 3.66.

Dielectrical Resonator Selection and Characterization

DR pucks, as well as complete assemblies, including standoffs, are available from a variety of vendors such as Trans-Tech (now part of Skyworks Solutions) or Temex (France). These companies offer application notes that describe types, EM basics, and assembly details of the DR, as well as helping to select the right material for a specific application (including ordering details).

Vendors sometimes provide tables assigning specific diameters for a given material to frequency ranges, leaving the resonator length to determine the exact resonance frequency. An approximate for the most commonly used $TE_{01\delta}$ mode is given by the formula in [2], where D denotes the DR diameter and L its length (both in mm),

$$f_{\text{res}}\,(\text{GHz}) = \frac{68}{D\sqrt{\varepsilon_r}}\left(\frac{D}{2L} + 3.45\right)$$

$$0.5 < \frac{D}{2L} < 2 \quad \wedge \quad 30 < \varepsilon_r < 50$$

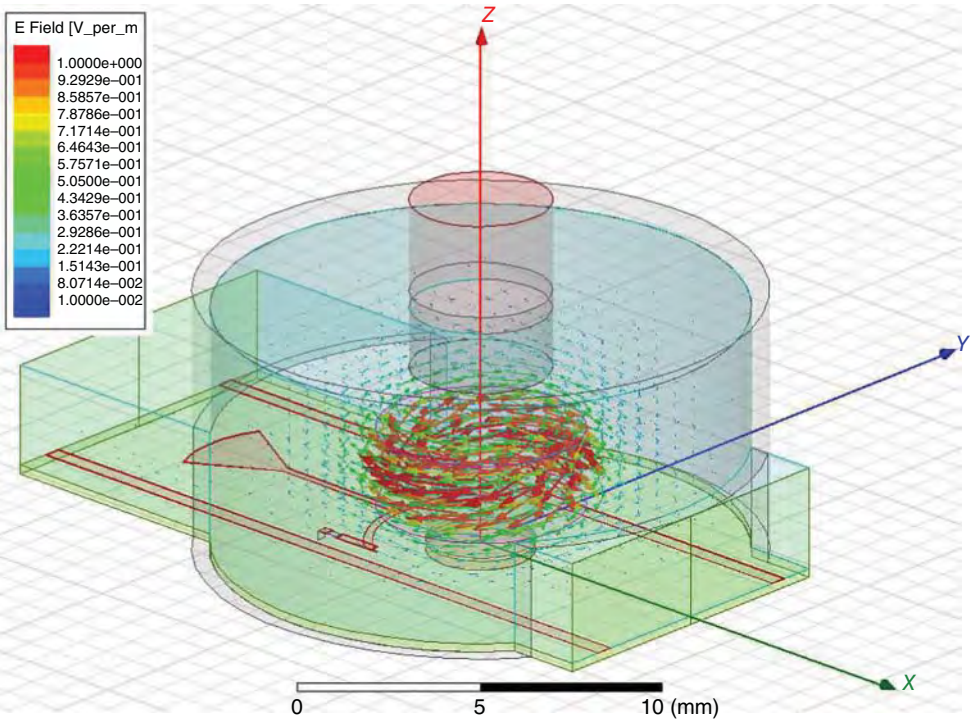
with about 2% accuracy within the ranges indicated.

A closed conductive containment for the DR assembly leaving openings for the ports only is mandatory because otherwise the Q_u would be diminished by radiation loss. Since the proximity of the surrounding matter does alter the boundary conditions to some degree, the resonant frequency is shifted upwards in case of metal (conductive) proximity and downwards in case of dielectric proximity for the $TE_{01\delta}$ mode. Since most arrangements constitute a combination of both, either measurement or EM simulation of the specific situation can predict the exact resonant frequency.

Determination of the Eigenmodes of the complete resonator arrangement (DR and cavity) allows for verification and adjustment of the geometrical parameters of the DR and/or tuning elements for a specific target resonant frequency while at the same time giving an estimation for Q_u. This is most conveniently done with the help of a 3D-EM tool like HFSS. Any additional unwanted modes in the vicinity of the desired one may be identified as well. It is recommended to solve for two Eigenmodes within a 20% bandwidth centered at the target frequency.

The Eigenmode report consists of a listing of complex Eigenfrequencies as well as the ratio of magnitude versus 2× imaginary part; that is, the quality factor Q of the Eigenmode.

In a second step, a modal solution including all four ports of the arrangement shown in Figures E-4a–E-4c is generated yielding the S-parameter versus frequency data to be used in conjunction with the circuit-simulator later on.



(a)

Figure E-4a HFSS $TE_{01\delta}$ E-field vector-plot (normalized), generated from an Eigenmode solution of a DR assembly within a conductive cavity [1].

Eigenmode	Frequency [GHz]	*Q*
Mode 1	9.60868 + *j* 0.00206755	2323.69
Mode 2	10.0043 + *j* 0.00162318	3081.70

(b)

Figure E-4b HFSS Eigenmode report, mode 1 is of TM-type [1].

E-1-3 DRO Topologies

Series Feedback (Reflection) Type DRO

Series feedback (reflection) is the most common type of DRO mainly because it is easier to handle than the feedback type discussed later, once the oscillator core properly exhibits the required reflection gain around the frequency of interest (and ideally only there). The oscillator core consists of an active device, the input port of which presents a reflection coefficient of magnitude >1 to the connected resonator arrangement. The latter is simply formed by the DR placed in close proximity to a microstrip line terminated with its characteristic impedance (reaction type resonator) (see Figure E-5).

Oscillation build up is established if $\mathrm{Re}\{r_{\mathrm{line}} \cdot r_{\mathrm{oc}}\} > 1$ and $\mathrm{Im}\{r_{\mathrm{line}} \cdot r_{\mathrm{oc}}\} = 0$, with r_{line} and r_{oc} denoting the input reflection coefficients of the resonator line and the oscillator core, respectively. Adjustment of phase is done by moving the DR along the line at a constant distance and adjustment of the reflection magnitude; thus, the level of oscillation can be controlled by varying the distance between the line and DR. Additionally, as with the parallel

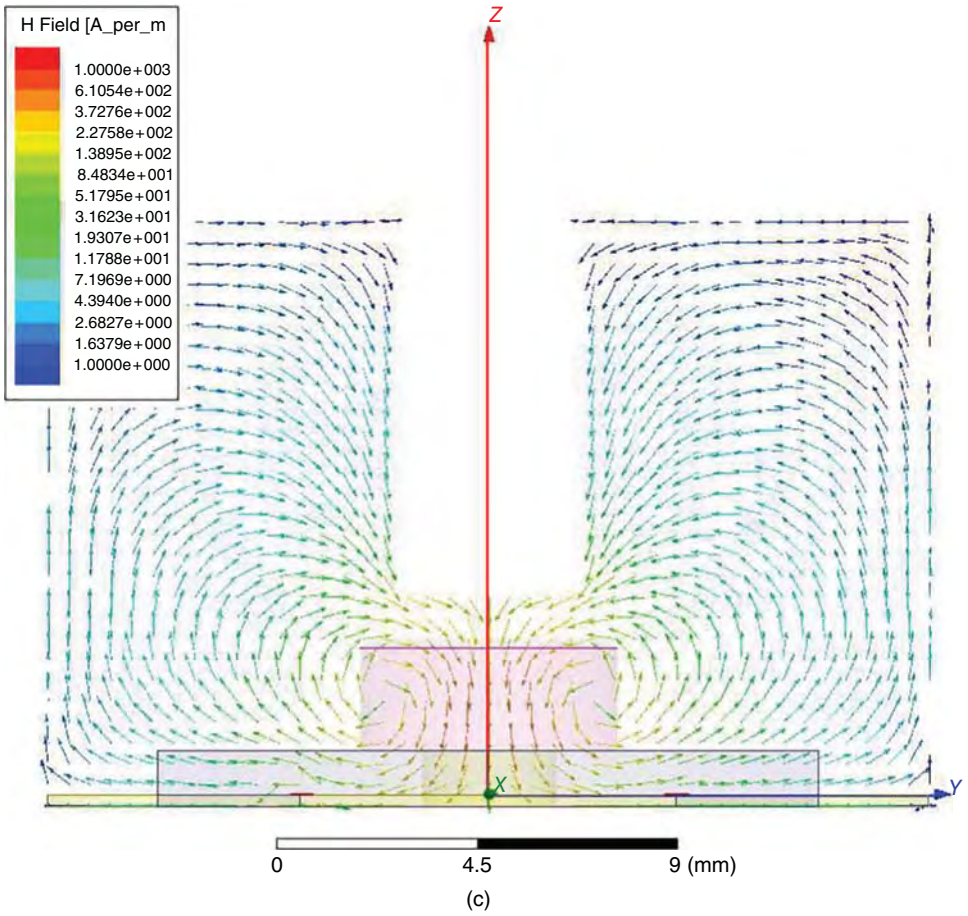


Figure E-4c H field vector plot of the $TE_{01\delta}$ resonant mode in *Y–Z* plane (logarithmic scaling) [1].

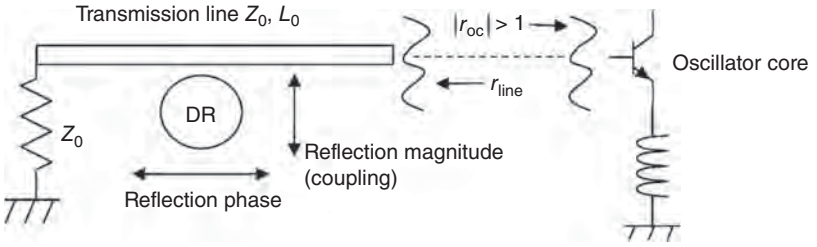


Figure E-5 Reflection type DRO [5].

feedback variant discussed below, matching between the resonator and core may be applied. Since we did not pursue this topology in depth yet, this paper will focus on the following approach, which seemed to be more promising in terms of low phase noise after a few trials with the less complex reflection type.

Parallel Feedback Type DRO

The parallel feedback type uses a stable gain element as the oscillator core. The feedback is established by a set of two microstrip lines mutually coupled thru the interaction with a DR placed between them (transmission type

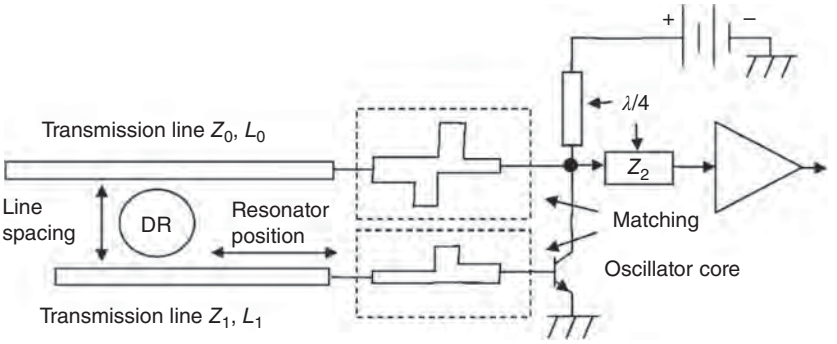


Figure E-6 Feedback type DRO with transmission type DR [1].

resonator). The two lines do not require a resistive termination. In order to achieve a high Q_L, it is rather preferable to use reactive terminations instead; that is, open stubs the lengths of which constitute two additional degrees of freedom. In addition to that matching structures, interfacing the oscillator core input and output is required to maximize the loaded Q and at the same time establish the necessary round trip phase shift of $2\pi{\cdot}n$ (integer n) at the target frequency (see Figure E-6).

The topology shown earlier includes at least 6 degrees of freedom plus the additional parameters of the matching networks not defined yet. For simplicity, in order to preserve the symmetry of the resonator layout (as in Figures E-4a and E-4b), the characteristic impedances of the resonator lines are chosen to be equal (e.g., $Z_0 = Z_1 = 50\,\Omega$). An appropriate quarter-wave transformer between the oscillator-core and post-amplifier may be required in order to achieve optimum performance.

Since the available layout area is limited in most cases, it is desirable to have fixed positions for the resonator as well as for the core terminals. Therefore, a combination of stub matching-elements and meander lines is used to realize arbitrary matching and phase shift while maintaining the mechanical length of the structures.

E-1-4 Small Signal Design Approach for the Parallel Feedback Type DRO

A design strategy using the Agilent/EEsoft ADS is as follows:

(1) The upper matching section between resonator and gain element is split to create a fixed (e.g., $50\,\Omega$) impedance level between them to allow for arbitrary phase shift to be inserted (meandered if necessary) without changing the outer impedances. Additionally, this allows access to an open-loop S-parameter simulation and optimization. In order to simplify the process further, the matching process is treated separately and variable reference impedances are used instead at the oscillator-core input and the resonator-element output, respectively.

(2) The lower section is a cascade of a stub matching element and a 180° meander line allowing for adjustment of the mechanical length while maintaining the reflection coefficient of the oscillator core's output.

(3) In ADS, a layout component is created with ports interfacing the resonator and the gain element. In order to speed up the optimization process, microstrip library elements are used and a synchronized schematic (i.e., analytical) model created. This allows for a coarse optimization to be conducted using the analytical representation and a subsequent fine optimization using EM co-simulation. This may save significant computational effort provided that the differences between the two representations are rather small, which unfortunately is not granted depending on the actual situation and frequency (see Figure E-7).

(4) The resonator S-parameters are taken from the results of a 4-port modal 3D-EM simulation. The reference positions of the four ports need to exactly match the corresponding positions in the layout component. The effect of the two tuning varactors has been modeled by voltage dependent lumped boundary conditions at their respective places the tuning voltage being an additional parameter of the HFSS-model (see Figures E-8a and E-8b).

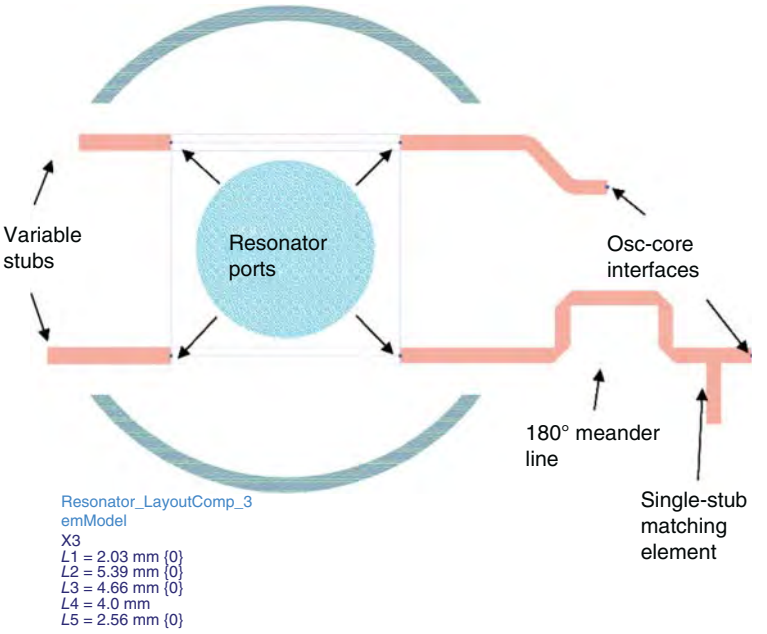


Figure E-7 Layout component with resonator interface and matching structures [1].

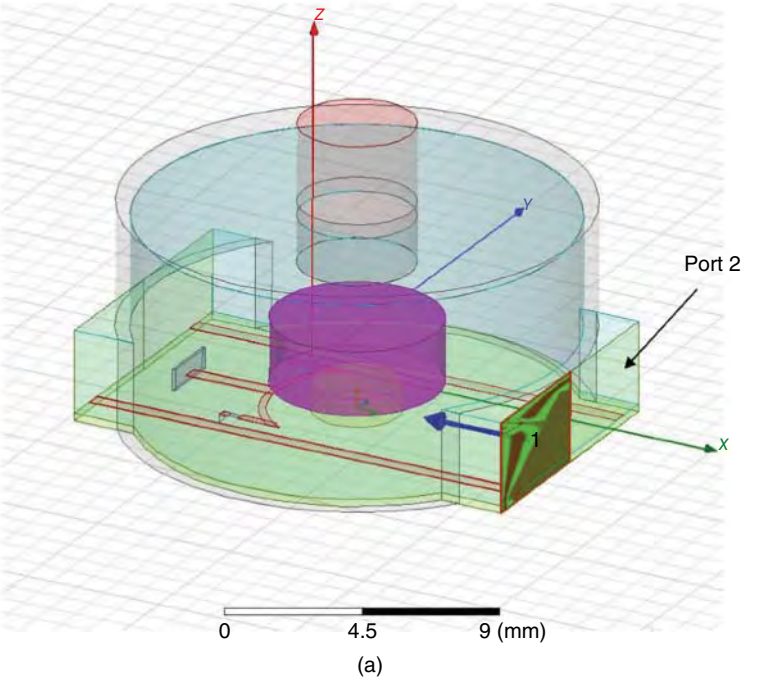
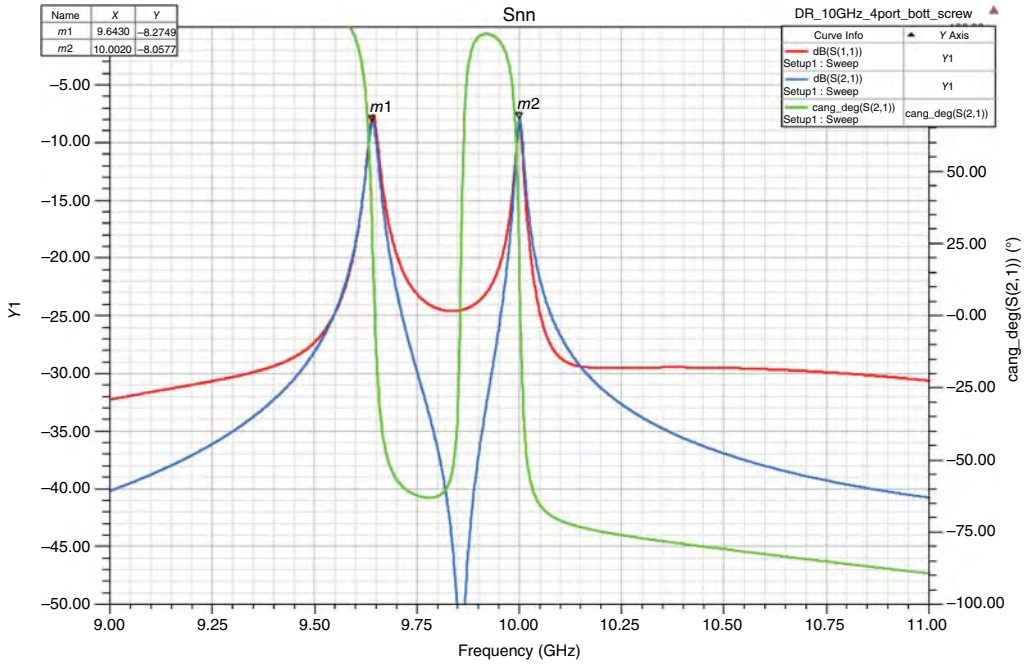


Figure E-8a Four-port 3D resonator model with port references (shown for port 1) deembedded to the actual interface positions [1].



(b)

Figure E-8b S_{11} magnitude, S_{21} magnitude, and phase of the 4-port model above for a tuning voltage of 7 V [1].

(5) The oscillator core consists of a BFP740 transistor in common-emitter configuration and a bias-stabilization circuitry. Again, planar EM co-simulation is utilized in conjunction with substrate and pad scalable lumped component models from Modelithics as well as calibrated internal ports for them (see Figure E-9).

(6) A broadband *S*-parameter analysis of the oscillator core is recommended in order to identify potential instability issues and available and associated gain properties around 10 GHz (see Figures E-10a and E-10b).

Since the regions of instability are rather small and very close to unity magnitude, it is unlikely to encounter instability since lossy matching and phase shifting elements are likely to force the terminations inside the stable region anyway. Therefore, we decide to continue without additional stabilization measures (see Figures E-11a and E-11b).

(7) The complete setup allows for an open-loop 2-port *S*-parameter simulation the reference impedances of which being additional variables of the problem. Since the *S*-parameter data for the resonator does not reflect DC properties, ideal DC-blocks must be added if necessary while in reality an open circuit is present at 0 Hz.

(8) For the coarse optimization the random or hybrid optimizer is utilized. There is a set of four main goals: $|S_{11}| < R$, $|S_{22}| < R$, $|S_{21}| > G_{\min}$ and $Q_L \geq 1$ k at or closely around the target frequency F_0. Appropriate values for the limits are $20 \times \log(R) = -20$ dB and $20 \times \log(G_{\min}) = 6$ dB. Q_L is derived from the frequency of maximum gain and the corresponding 3 dB-bandwidth DF according to $Q_L = F_0/\Delta_F$. Since the target value for the open-loop gain is associated with the coupling coefficient of the resonator, a higher gain may increase its value, which is still below unity; that is, subcritical. In practice it was not possible to increase it much further without diminishing the other goals. On the other hand, a higher gain would increase the overdrive level of the oscillator with a severe impact on large signal noise figure and input reflection of the gain element.

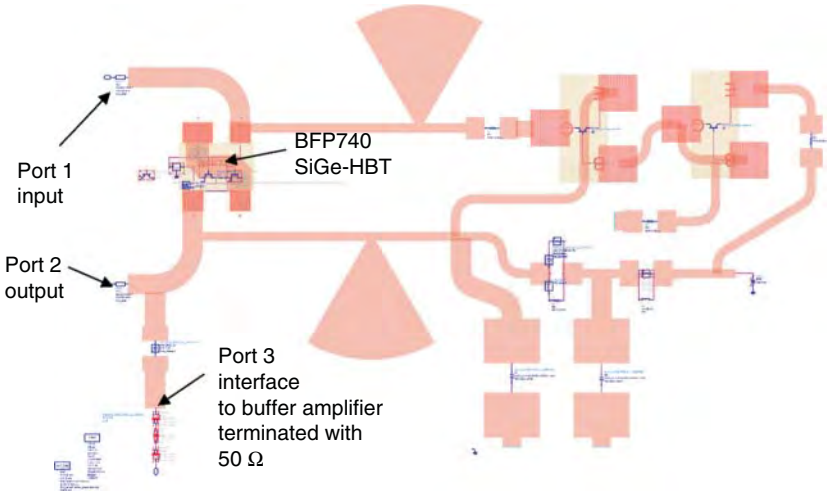


Figure E-9 Oscillator core model including bias stabilization circuitry consisting of the layout component for EM co-simulation and models for the gain element, the bias-stabilization transistors, and additional lumped components [1].

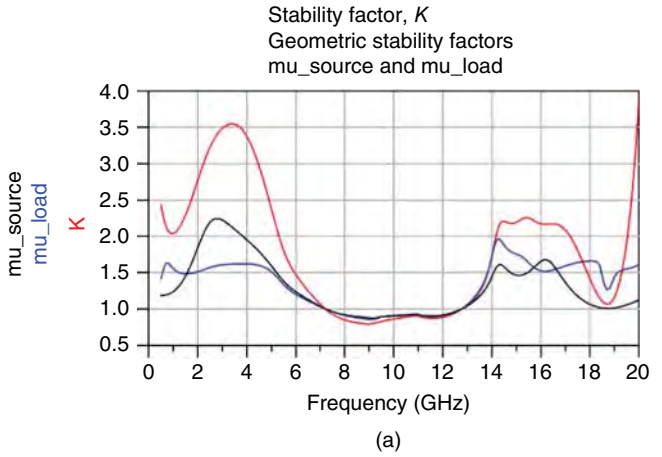
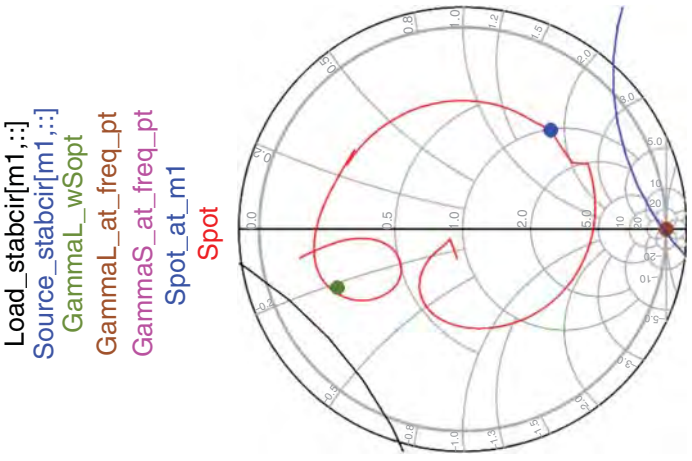


Figure E-10a Unconditional stability is not completely satisfied, as illustrated here. (If either mu_source or mu_load is >1, the circuit is unconditionally stable.) [1]

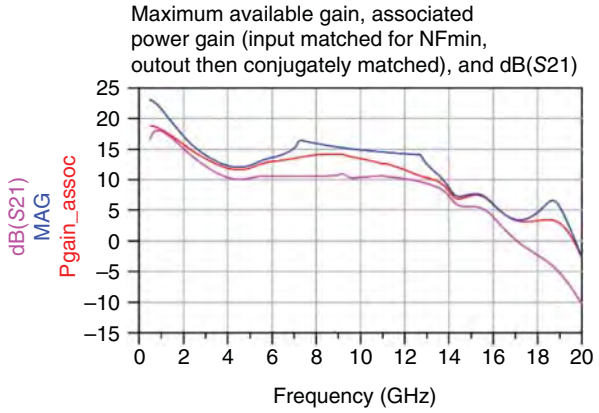
A phase goal is expendable since arbitrary phase shift may be inserted afterwards. As we will see later, the small signal phase shift is decreased significantly at higher drive levels. A large signal S-parameter simulation will yield an estimation for the additional phase shift necessary in order to arrive at 0° unwrapped phase for 0 dB large signal gain at F_0. Fine adjustment of the phase noise versus phase shift will be done at a later stage. Direct optimization versus phase noise is not recommended at this stage because potential HB convergence problems during the process for certain sets of parameters may cause the optimizer to fail.

(9) For the fine optimization, the gradient optimizer is engaged using the same set of goals but this time invoking the EM view (-model) for the matching layout component instead of the analytical models (see Figures E-12a–E-12c).



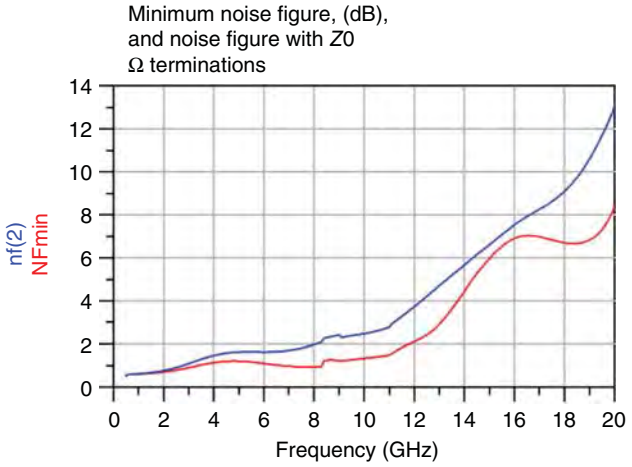
(b)

Figure E-10b Source and load stability circles at the most critical frequency (9 GHz) [1].



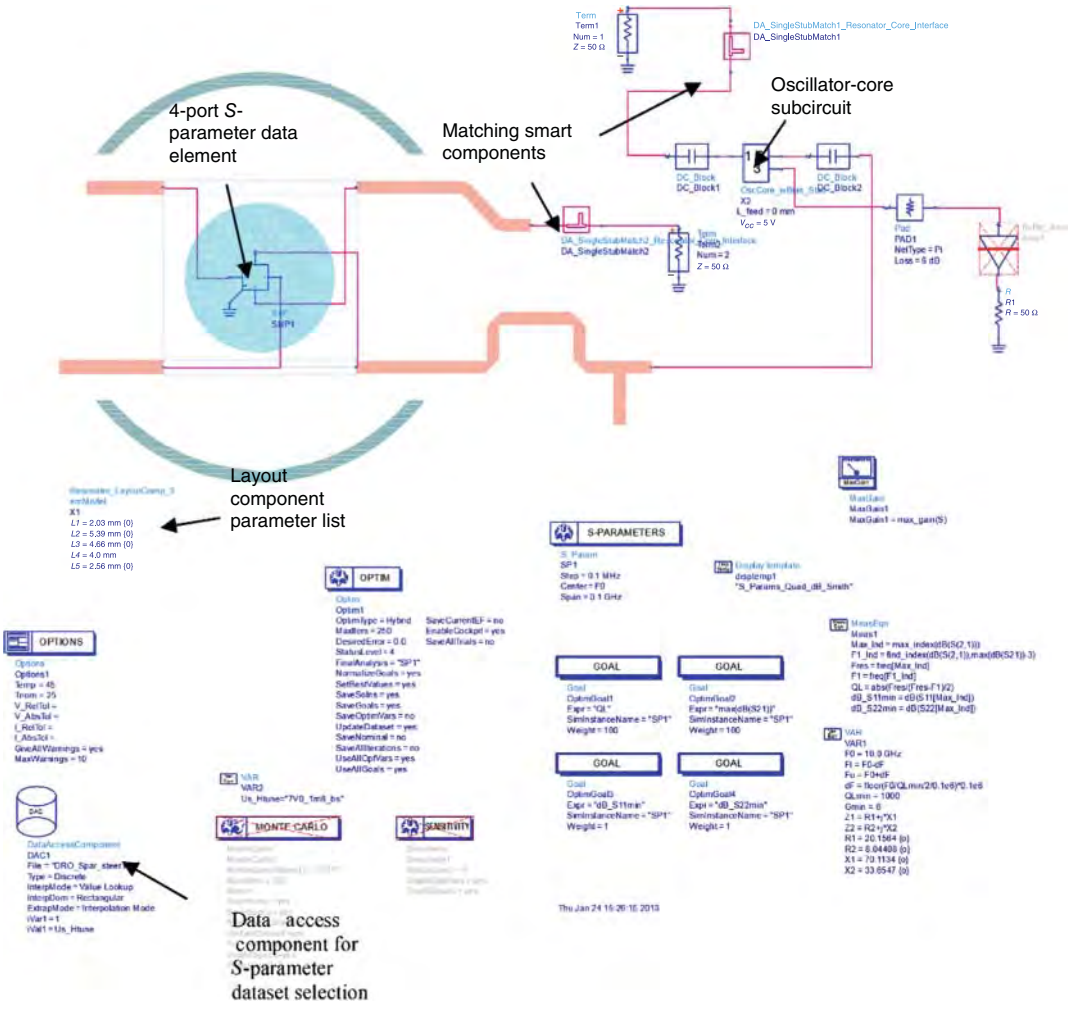
(a)

Figure E-11a Gain characteristics of the oscillator core. Note that the maximum available gain is invalid within the region of potential instability between 7 and 13 GHz [1].



(b)

Figure E-11b Noise figure and minimum noise figure versus frequency [1].

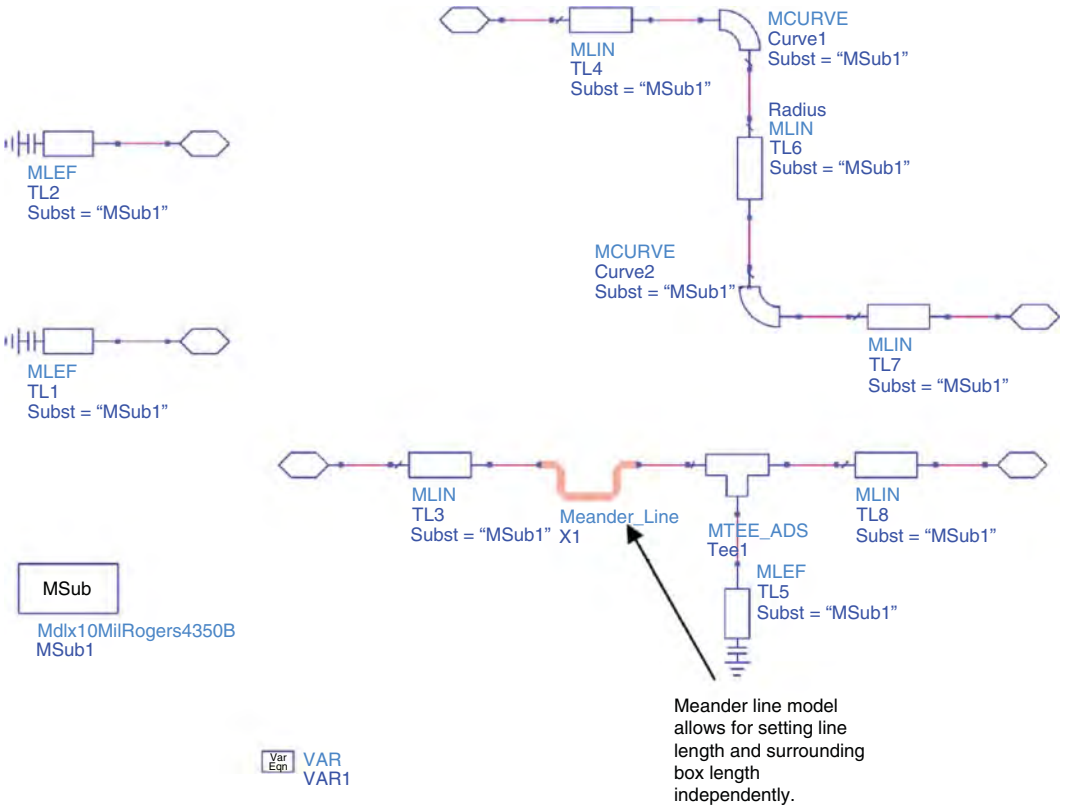


(a)

Figure E-12a ADS open-loop (small signal) *S*-parameter simulation and optimization setup [1].

(10) When the optimization process is accomplished, the resulting reference impedances then need to be matched to a common (e.g., 50 Ω) real impedance. This is accomplished in two steps: First, two Single-Stub smart components are inserted to quickly design an electrical (ideal) transmission-line model for each matching element using the ADS-Filter/Matching Design-Guide and then a physical equivalent is created using the ADS-LineCalc or similar tools. The physical model potentially needs some refinement in order to work properly (see Figures E-13a and E-13b).

(11) Now that the small signal open-loop response and matching are well at their target values, we need to estimate the necessary additional phase shift at large signal excitation and near unity gain at the frequency of maximum gain in the small signal scenario (see Figures E-14a and E-14b).



(b)

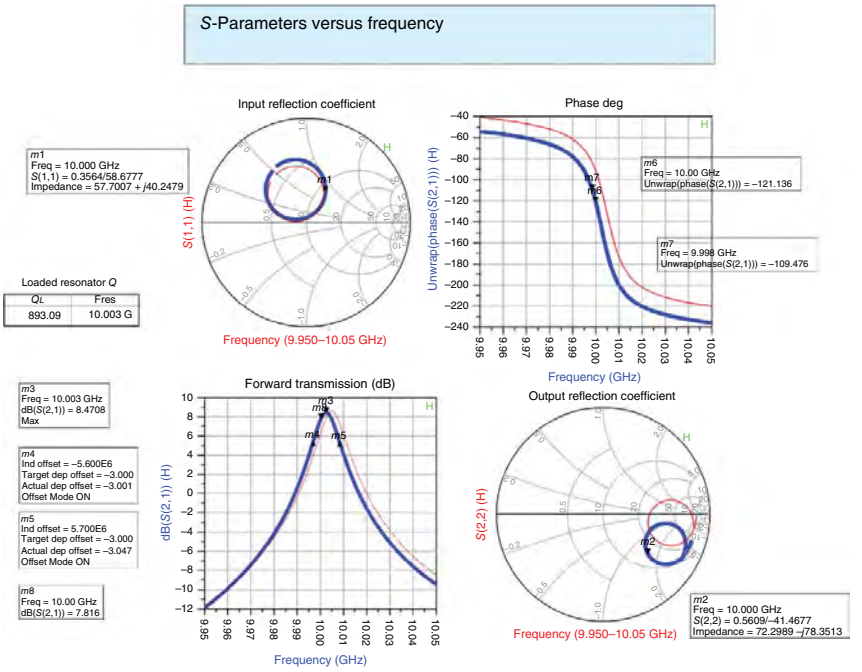
Figure E-12b Schematic view of the resonator layout component [1].

(12) The result obtained earlier indicates an additional phase shift of −116°, in this case to be inserted between the two ports to arrive at the required phase shift of 0°. In order to save board space, we use an additional meander line of equivalent electrical length to establish the required phase shift. The surrounding box length of the meander should be set such as to meet the fixed layout positions of the oscillator-core, if relevant (see Figure E-15).

(13) As the reflection coefficients and the source impedance for minimum large signal noise figure of the active device do more or less vary with increasing drive level, some correction mainly to the matching element at the oscillator core's input may be required in order to establish optimal conditions with respect to minimum phase noise (see Figures E-16a and E-16b).

E-1-5 Simulated Versus Measured Results

The predicted phase noise does match the measured values for a set of real devices quite well as can be seen in Figure E-17.



(c)

Figure E-12c Open-loop *S*-parameters following coarse optimization using schematic and EM-view [1].

SingleStub_Mtch_phys
emModel
X3
W = 0.5 mm
*L*1 = 1 mm {–0}
*L*2 = 4.26 mm {0}
*L*3 = 3.29 mm {0}
(a)

Figure E-13a Physical replacement for the smart matching components in Figure E-12a [1].

From the plots we can derive a Leeson-frequency f_L of about 4 MHz corresponding to $Q_L = 1250$—slightly higher than the simulated value—and a flicker corner of $fc = 35$ kHz, slightly higher (worse) than the original assumption. Only the phase noise data for device #78 does not match the theory close to the carrier for some unknown reason.

As the results of the harmonic balance solution allow access to every individual node voltage and branch current, we are able to estimate some additional quantities of the oscillator:

- Power into the resonator at the port location (see Figure E-7) $P_{\text{res_in}} = 7.1$ mW
- Power out of the resonator at the port location $P_{\text{res_out}} = 2.3$ mW
- Power dissipated in resonator including cavity, tuning etc. $P_{\text{res}} = 4.8$ mW
- Coupling coefficient at the interface plane $k = 0.48$ (subcritical coupling)
- Electromagnetic energy stored in resonator (with Q_u taken from HFSS result) $W_{\text{em}} = 235$ pWs
- Reactive power inside the resonator $Q_{\text{em}} = 14.8$ VA
- Power dissipated in matching and phase shift circuitry $P_{\text{ext}} = 3.2$ mW
- Power into gain element $P_{\text{in}} = 0.66$ mW (=−1.8 dBm)
- Power into buffer amplifier $P_{\text{ba}} = 3.3$ mW (=5.2 dBm)
- Total power out of the oscillator core $P_{\text{tot}} = 12.0$ mW (=10.8 dBm)

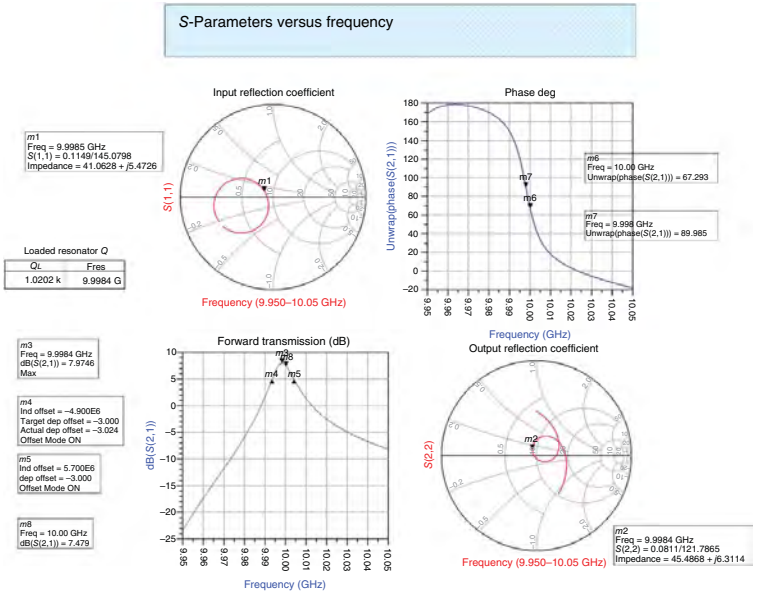
E-1-6 Physical Embodiment

The design procedure presented here was actually carried out twice with slightly different starting conditions (e.g., board relative permittivity $\varepsilon_r = 3.66$ for the original (realized) design and $\varepsilon_r = 4.0$ for the one demonstrated in this paper). Therefore, the original layout differs slightly from the one presented here as does the biasing circuitry using the BCR400W instead of two separate PNP BJTs. However, the results are practically the same with a little bit of tuning of the bottom screw introduced by Mr. Hinneck (on top of which the DR-standoff is glued) as well as of some of the stubs required in order to arrive at the predicted phase noise values. Segmented stubs are used in order to easily vary their length.

The design data for the printed circuit board (PCB) and the resonator cavity was imported to a separate CAD tool and supplemented with additional housing details including the necessary connectors. Based on this data the housing was externally machined and surface finished (see Figures E-18a–E-18d).

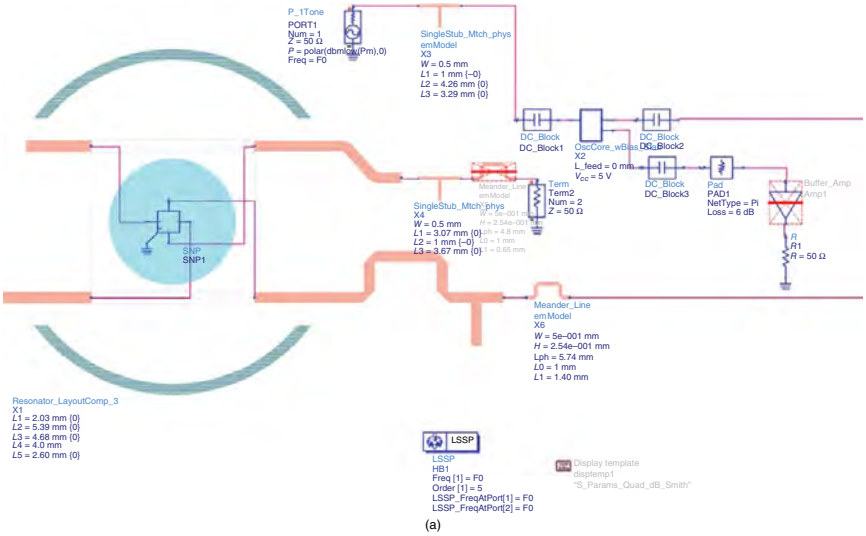
E-1-7 Acknowledgments

The authors would like to thank Mr. Guido Naruhn for his accurate work on preparation of the housing details as well as assembly of the prototypes, and Mr. Uwe Hinneck on setting-up operation and tuning of the prototypes as well as doing the environmental tests.



(b)

Figure E-13b Final optimization result with EM-models for the Single-Stub matching elements replacing the smart matching components. Note that another 180° meander line has already been added to the lower section to compensate for the physical lengths of the matching elements [1].



(a)

Figure E-14a Setup for large-signal open-loop *S*-parameter simulation [1].

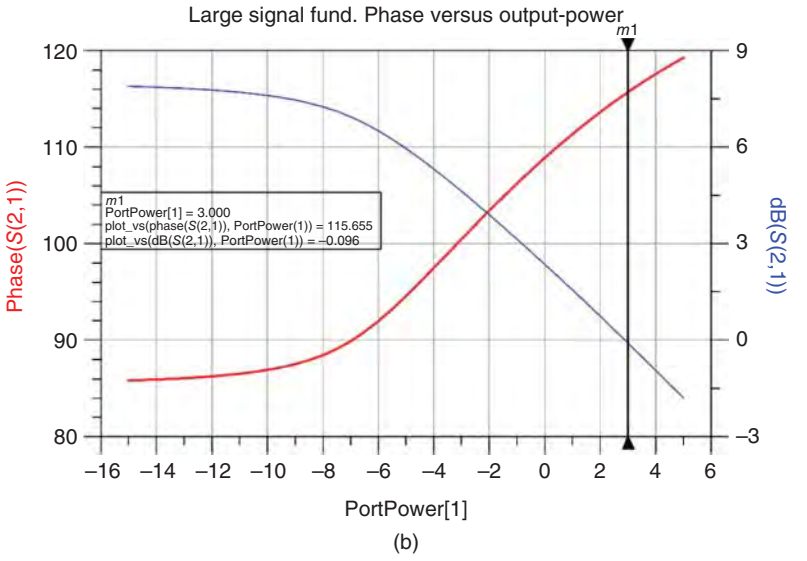


Figure E-14b Large signal forward transmission at resonance frequency versus input-power. The marker is set to near unity-gain. The corresponding phase shift is about 116° [1].

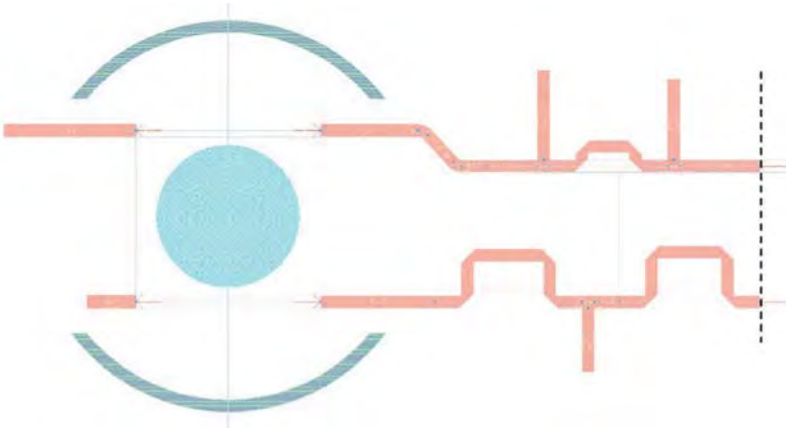


Figure E-15 Resonator matching section with delay line added and meander lines adjusted to achieve equal lateral reference positions for the interface ports to the oscillator core [1].

E-1-8 Final Remarks

The small signal approach presented in this paper maybe doubtful since oscillators is always subject to large signal conditions. The most severe impact is expected in terms of large signal shift of S_{11} of the transistor. However, although a large signal design approach has not been fully exercised yet, both the final simulation results and associated sensibility analysis and the practical embodiment indicate that significant improvement beyond the results obtained here is hardly possible.

The achieved phase noise results for the 10 GHz DRO (−112 dBc/Hz @ 10 kHz, −137 dBc/Hz @ 100 kHz and < -170 dBc/Hz @ >10 MHz) are to our knowledge the lowest currently available in the industry.

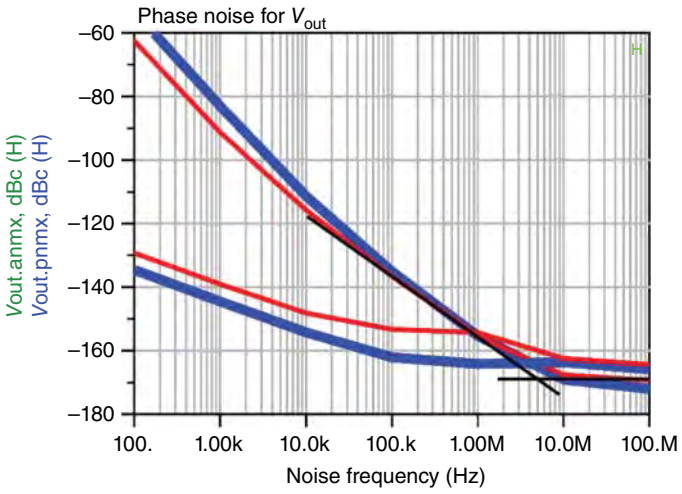


Figure E-16a Amplitude and phase noise before and after minor optimization of the input matching component. From the intersection of the 20 and 0 dB/decade tangent, a Q_L of approximately 1 k can be derived, assuming that the Leeson formula does adequately reflect the situation [1].

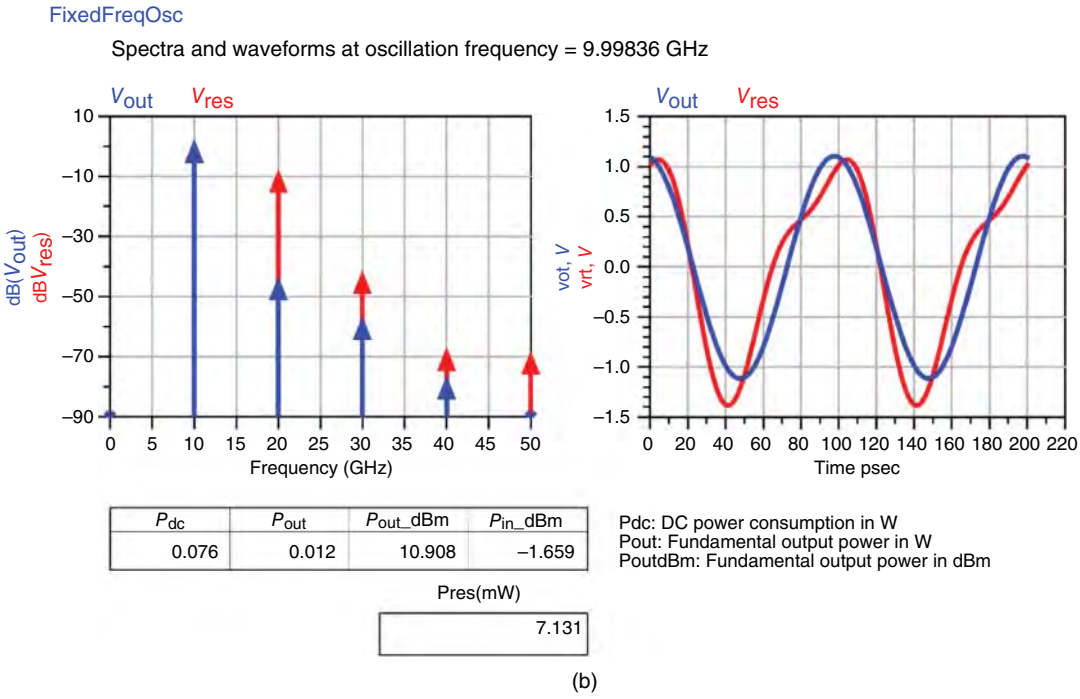


Figure E-16b Corresponding spectra and time-domain waveforms of the voltages at the output of the buffer amplifier and at the oscillator core output [1].

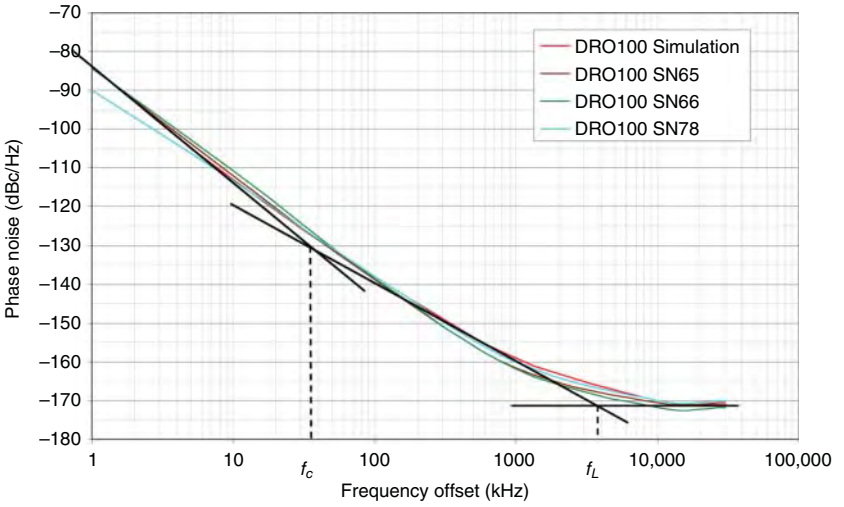
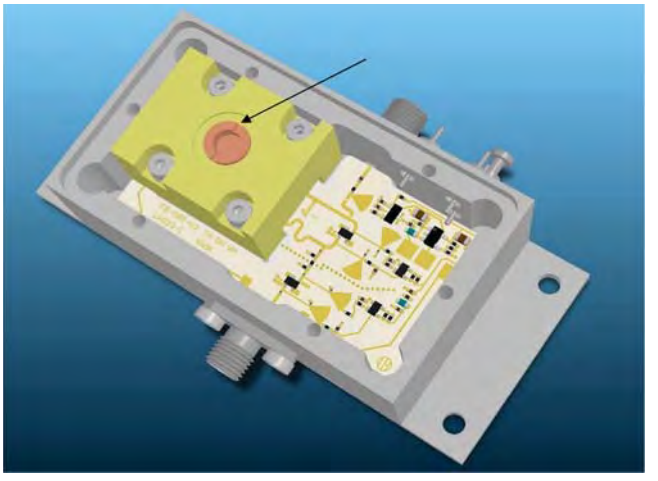
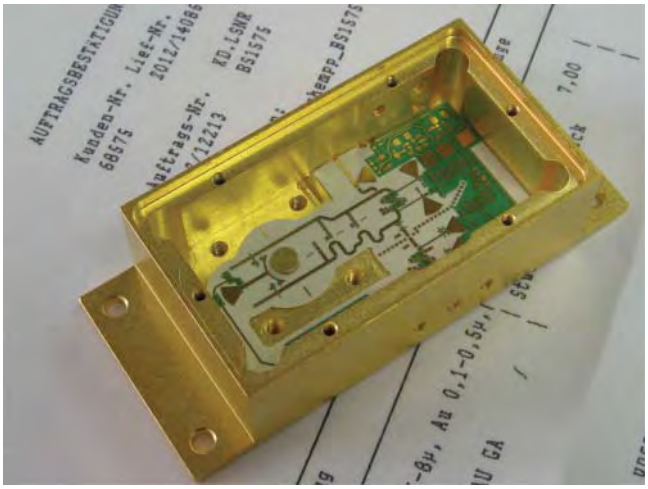


Figure E-17 Phase noise results, measured and simulated [1].



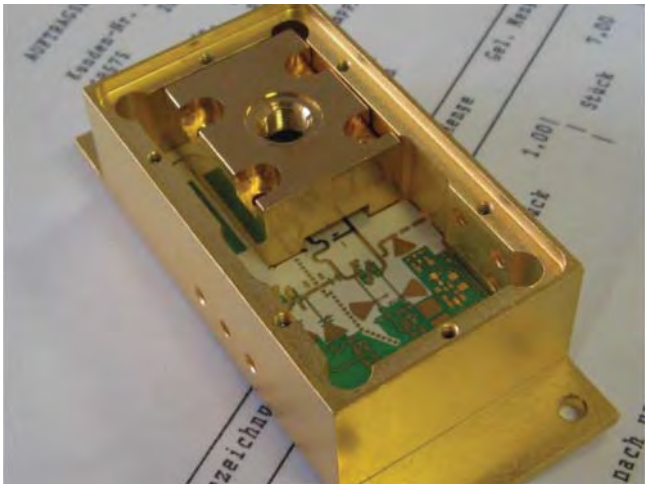
(a)

Figure E-18a CAD internal view of the complete DRO [1].



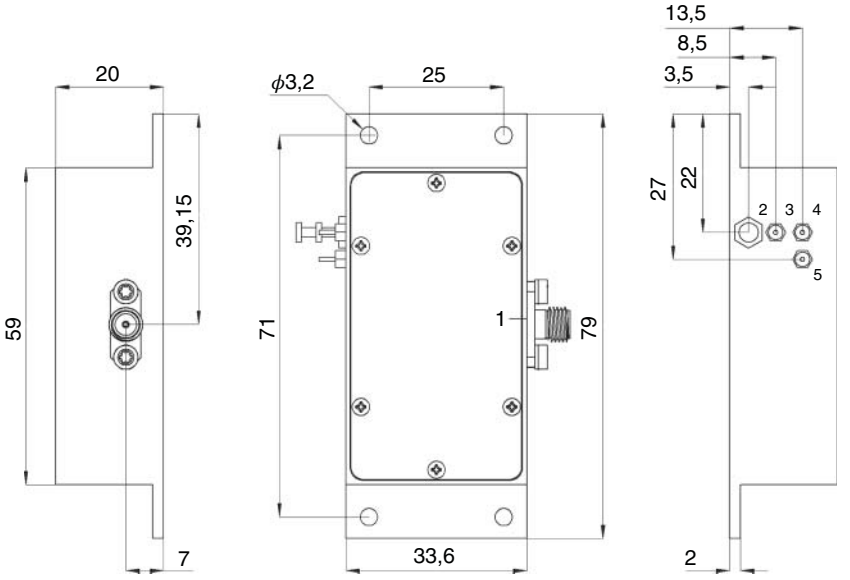
(b)

Figure E-18b Internal view of the DRO without the resonator cavity and DR. The DR bottom tuning screw is slightly elevated [1].



(c)

Figure E-18c Resonator cavity and DR (not visible) added [1].



(d)

Figure E-18d Mechanical drawing of the 10 GHz DRO [1].

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Subramanian, A. (2008). A low phase noise K-band oscillator utilizing an embedded dielectric resonator on multilayer high frequency laminates. Master thesis. University of Central Florida. (Author's note: Similar to Bischoff and Schwoch but this time in English, including a good summary of achievements in the field of DROs and related topics.)

Bernard, O. and Croston, R. (2000). Simulate and build a Ku-band DRO. *Microwaves & RF*. (Author's note: Another design example with inferior results.).

E-2 A NOVEL OSCILLATOR DESIGN WITH METAMATERIAL-MÖBIUS COUPLING TO A DIELECTRIC RESONATOR

E-2-1 Abstract

With the aid of a Metamaterial-Möbius coupling mechanism, these fundamental-frequency DROs operate through X-band with low phase noise and superior figure of merit (FOM). Manipulating and tailoring the EM wave coupling properties, several interesting properties of Metamaterial-Möbius Strips (MMS) envisage, such as reduction in the size for a given operating frequency and suppression of spurious resonance modes, thereby improving the FOM of tunable oscillator. FOM can be a limiting factor in modern communications systems, especially those that rely on power efficient low phase noise signal source. Phase noise can increase the bit error rate (BER) of

a telecommunications link, degrade the stability of beams in particle accelerators, and degrade the sensitivity of radar systems. Phase noise is an oscillator parameter that grows in importance with the complexity of modern communications modulation formats. Fortunately, work on Metamaterial-Möbius coupling inspired DROs by us has resulted in a line of compact surface-mount DROs with extremely low phase-noise levels at fundamental-frequency outputs through 8 GHz and higher, suitable for use in commercial, industrial, and military applications.

E-2-2 Introduction

These new DROs rely on planar resonators based on MMS, which are simple examples of anholonomy. Therefore, it was possible to maintain the phase noise in a much smaller package compared with the previous example. The geometrical phenomenon of anholonomy depends on the failure of a quantity to recover its original value, when the parameters on which it depends are varied around a closed circuit [3–5]. Metamaterials are engineered periodic composites that have negative refractive-index characteristics not available in natural materials [6–9]. Such composite materials, in typical topological arrangements can achieve values of negative permeability ($-\mu$) and negative permittivity ($-\varepsilon$) [10]. In general, the refractive index of a medium can be characterized by four possible sign combinations for the permeability–permittivity pair ($\mu\epsilon$) and can be described [8, 11–18] by means of Eqs. (E-2–E-5).

$$n = \sqrt{(+\varepsilon)(+\mu)} = +\sqrt{\mu\varepsilon} \rightarrow (\text{DPS} : \text{double} + \text{ve material}) \tag{E-3}$$

$$n = \sqrt{(-\varepsilon)(+\mu)} = j\sqrt{\mu\varepsilon} \rightarrow (\text{ENG} : \text{epsilon} - \text{ve material}) \tag{E-4}$$

$$n = \sqrt{(-\varepsilon)(-\mu)} = -\sqrt{\mu\varepsilon} \rightarrow (\text{DNG} : \text{double} - \text{ve material}) \tag{E-5}$$

$$n = \sqrt{(+\varepsilon)(-\mu)} = j\sqrt{\mu\varepsilon} \rightarrow (\text{MNG} : \text{mu} - \text{ve material}) \tag{E-6}$$

where $\varepsilon_o = 8.85 \times 10^{-12}$ and $\mu_0 = 4\pi \times 10^{-7}$, and n = the refractive index of the medium.

Equation (E-2) is valid for double positive substrate (DPS) materials, with permittivity and permeability both positive; Eq. (E-3) is valid for epsilon negative (ENG) substrate materials, with negative permittivity and positive permeability; Eq. (E-4) is for double negative (DNG) substrate materials, with permittivity and permeability both having negative values; and Eq. (E-5) is for mu negative (MNG) substrate materials, where the permeability is negative but the permittivity has positive values.

The DNG materials described in Eq. (E-4) are typically defined as artificial materials and commonly referred to as "metamaterials" in the technical literature. In addition, they are called left-handed materials (LHMs), negative index materials (NIMs), and backward-wave materials (BWMs) [19]. The unusual characteristics of metamaterials, such as backward-wave propagation, exhibit group velocity characteristics in a direction opposite to that of its phase velocity, causing strong localization and enhancement of fields. This can result in significant enhancement of a resonator's quality factor (Q), if losses can be minimized [20].

The realization of true DNG material (metamaterial) is questionable. In general, it is difficult to build a material or medium simultaneous with negative permittivity and negative permeability for broad operating frequency ranges from a set of arbitrary passive structure unit cells arranged in predetermined order. This may lead to a violation of energy conservation principle at the intersecting plane between a right-handed material (RHM) and LHM media because of the generation of energy.

An attempt to build the DNG material or medium—based on the fact that for a specific orientation and arrangement of the passive structure, the values of permittivity and permeability diminish as the frequency increases—has been applied to demonstrate virtual negative permittivity and permeability at specific frequencies, but it lacks validity for broadband operation. In reality, it is easier to demonstrate independently negative permeability or negative permittivity, but achieving both negative characteristics in a DNG material can be difficult.

Printed multi-coupled slow-wave resonators exhibit improved Q-factor characteristics and are commonly employed in low phase noise oscillator applications [21]. For example, improvement in the Q-factor of a slow-wave resonator ($\lambda/4$ coplanar strip line) can be realized by forming an open-circuit load where the incident and reflected EM waves move entirely in-phase with each other. In reality, such open-circuit conditions are difficult to maintain over a desired frequency band.

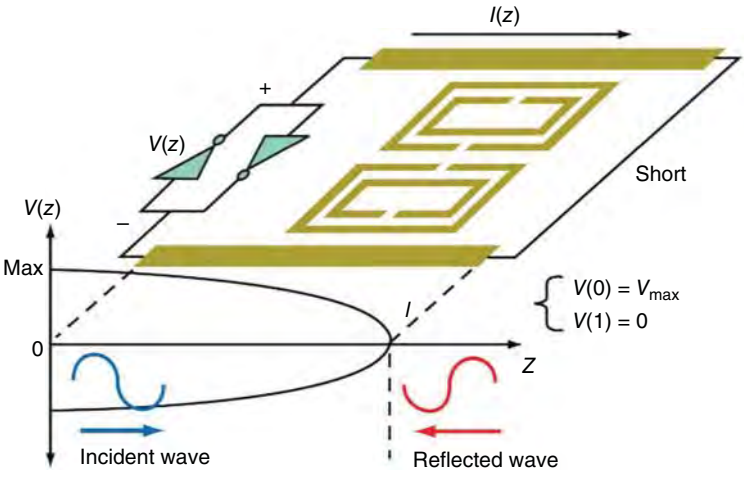

Figure E-19 A typical simplified representation of differential transmission line based SR [20].

In addition, the implementation of a $\lambda/4$ coplanar strip-line circuit on a substrate can increase the overall size of the circuit. Insertion of additional floating metal shields may help alleviate some of the problems with slow-wave circuit designs [21–25].But negative-permeability-based planar split-ring-resonator (SRR) structures and complementary split-ring-resonator (CSRR) structures can enable compact on-chip implementations of these circuits, with promising and cost-effective solutions for metamaterial oscillator and filter applications [9, 26–28].

In the proper arrangement, planar SRR and CSRR structures can achieve independently negative permeability and negative permittivity at the resonance needed to create optimum coupling for a disc resonator in a high-performance DRO. These structures can be characterized as magnetic and electric dipoles excited by the magnetic (H) and electric (E) fields along the ring axis [9].

Interestingly, a single-negative property (ε or μ) supported by an SRR or CSRR structure can yield a sharp stopband in the vicinity of the resonant frequency, enabling storage of EM energy into an SRR or CSRR structure through an evanescent-mode coupling mechanism, resulting in high Q. It should be noted that the Q multiplier effect does not violate the law of conservation of energy since the evanescent mode in SRR stores energy but does not transport energy [21].

Figure E-19 shows a typical differential transmission-line-loaded, SRR-based metamaterial resonator oscillator. For a differential (push-pull) oscillator, the incident wave energy injected by the cross-coupled inverters propagates in forward waves along the transmission line toward the circuit's short point; the energy is reflected at the SRR load, and the reverse wave has a superposition of the incident wave and leads to a resonance when in phase. Stronger wave reflection means less loss and higher resonator Q [20].

When working with artificial composite materials, the negative permeability response can be manipulated by including electrically small resonant shapes, such as split rings. Figure E-20 depicts a typical SRR structure for the realization of tunable μ ($\mu < 0$) and ε ($\varepsilon < 0$) characteristics for applications in tunable oscillator circuits [17, 18].

Möbius strips offer unique characteristics, including self-phase-injection properties along the mutually coupled surface of the strips, enabling enhanced Q for a given size of printed transmission-line resonator. The oscillator's loaded Q_L is described by Eqs. (E-6) and (E-7).

$$Q_L = \frac{\omega_0}{2}\left|\frac{d\varphi(\omega)}{d\omega}\right|_{\omega=\omega_0} = \frac{\omega_0}{2}\tau_d; \quad \tau_d = \left|\frac{d\varphi(\omega)}{d\omega}\right|_{\omega=\omega_0} \tag{E-7}$$

$$\tau_d = \frac{d\varphi(\omega)}{d\omega}\bigg|_{\omega=\omega_0} = \frac{\varphi(\omega_0+\Delta\omega)-\varphi(\omega_0-\Delta\omega)}{2\Delta\omega} \tag{E-8}$$

where $\varphi(\omega)$ is the phase of the oscillator's open-loop transfer function at a steady state and τ_d is the group delay of the metamaterial Möbius strips resonator [2].

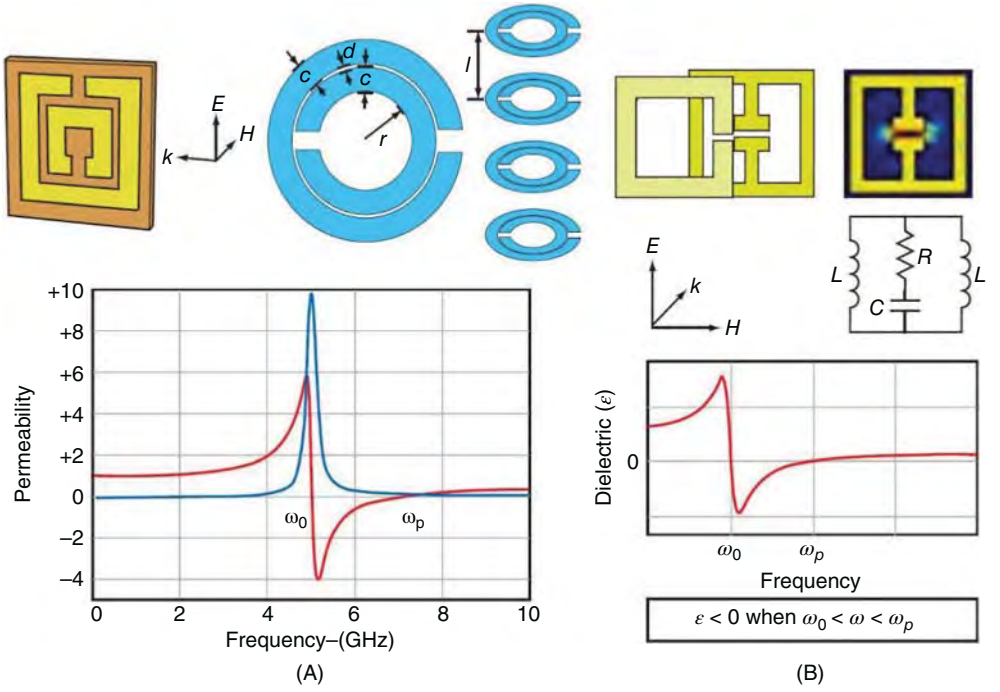

Figure E-20 A typical SRR structure exhibits the tunable characteristics for permeability (A) for μ ($\mu < 0$) near resonance condition and (B) for permittivity ε ($\varepsilon < 0$) near resonance condition [17, 18].

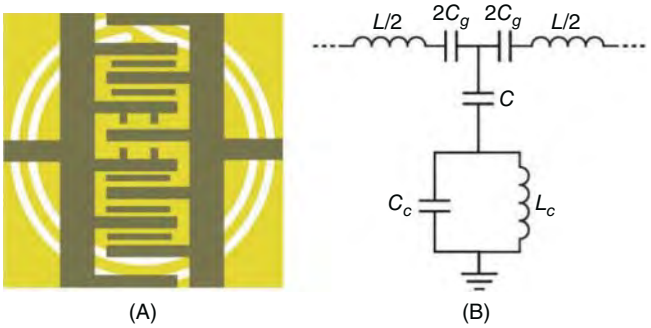

Figure E-21 A typical Metamaterial based Möbius strips resonator: (A) layout and (B) electrical equivalent lumped-element model circuit [11].

Figure E-21 shows a typical metamaterial-based Möbius-strip resonator and its equivalent lumped-element model circuits. From Eqs. (E-6) and (E-7), by introducing mode injection into metamaterial Möbius strips, phase-dispersion, loss, and group delay can be optimized.

Figure E-22 shows the typical arrangement of varactor-tuned metamaterial resonator utilizing SRR. Utilizing varactor diodes can improve the tuning range but maintaining the effective negative index properties of the resonator network is a challenging task. As shown in the figure, coupled SRR is being realized for improving the effective negative index characteristics without degrading the quality factor. Figure E-23 shows the coupled SRRs for the realization of Möbius coupling for enhancing evanescent mode energy based on energy harvesting techniques (transformation of unwanted modes and dissipated energy into Metamaterial-Mobius Resonator (MMR) cavity.

Figure E-24 shows the typical DRO for the understanding of the DR placement on the PCB. It can be noticed that typically the DR is in a disk configuration, attached through spacer made of low dielectric material. As shown

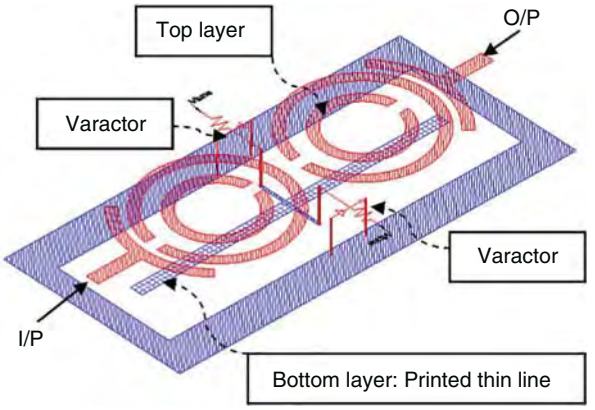

Figure E-22 A typical varactor-tuned metamaterial resonator comprised of coupled split-rings resonator (SRR) network [1, 12].

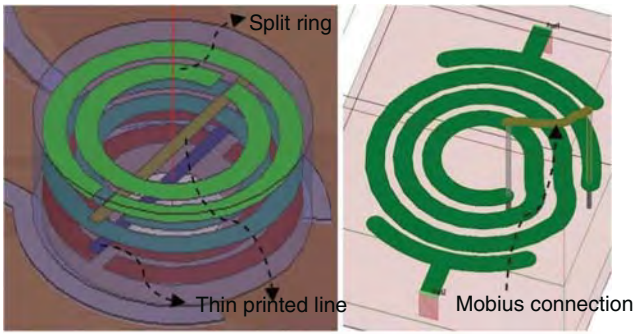

Figure E-23 A typical printed coupled line structure: (A) transverse coupled metamaterial resonator using SRR and thin printed line, and (B) Möbius Strips [1, 11, 12, 13].

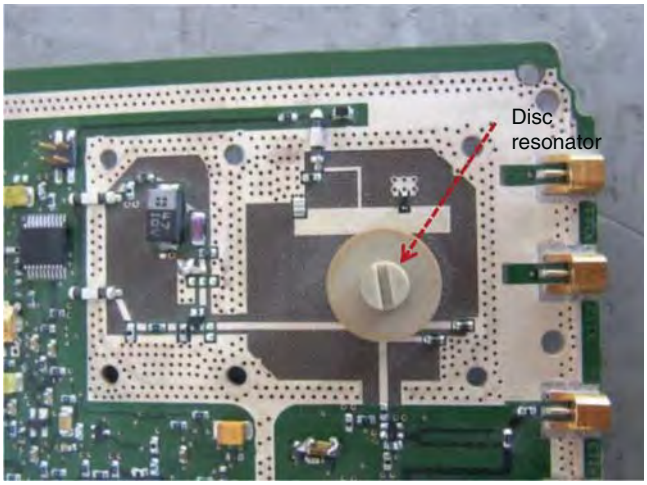

Figure E-24 DRO circuit using a dielectric resonator in a disk configuration [1].

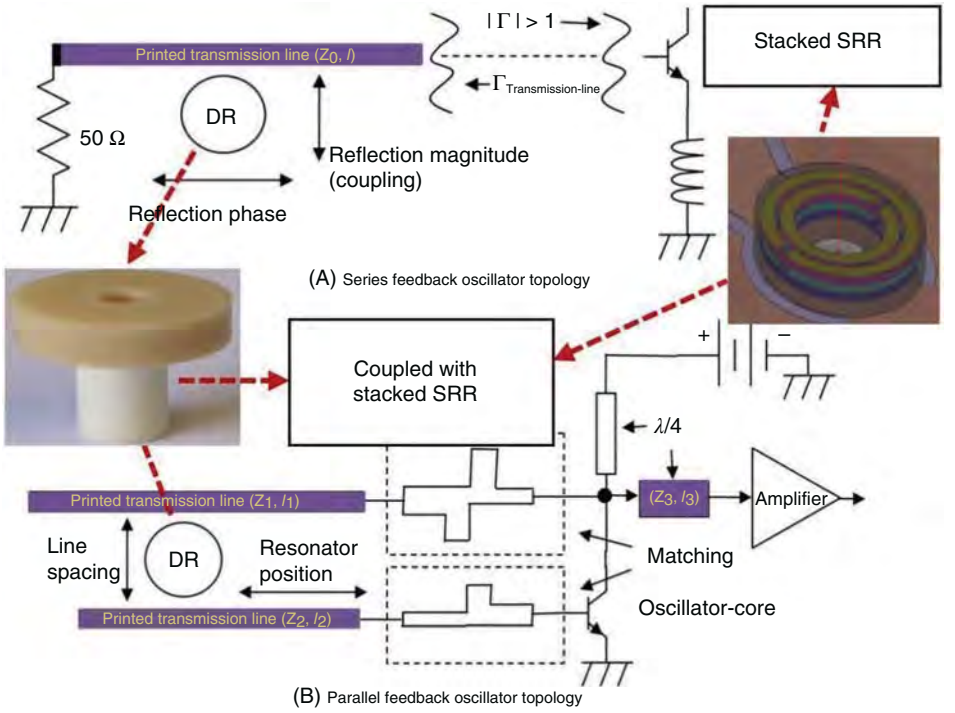

Figure E-25 A typical DRO circuit: (A) series feedback (reflection type), and (B) parallel feedback (transmission type) [12].

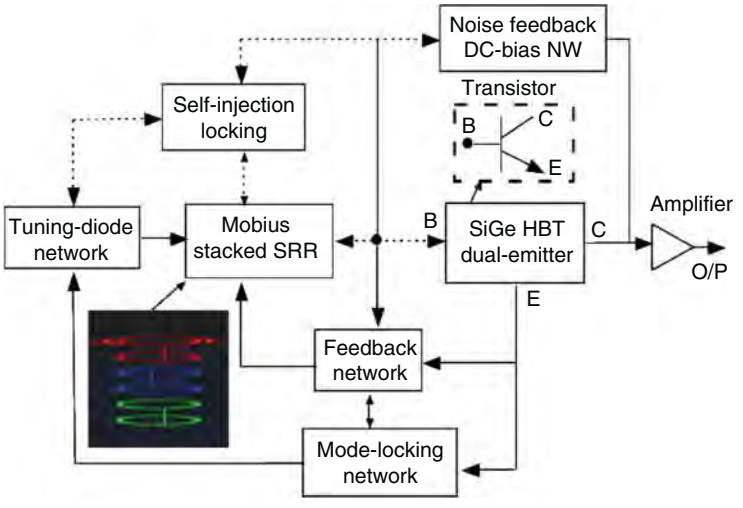

Figure E-26 Block diagram of the Mobius stacked SRR K-band oscillator [1, 12].

Specifications

Frequency	8 GHz
Tuning voltage	1 – 10 VDC
Bias voltage	+8 VDC 25 mA (Max.)
Output power	+1 dBm (Min.)
Tuning sensitivity	1.5 MHz/V (Typ.)
Thermal drift	2 ppm/°C (Typ.)
Output impedance	50 Ohms (Nom.)
Harmonic suppression	34 dBc (Typ.)
Frequency pulling	500 kHz (Typ. @ 1.75:1 VSWR)
Frequency pushing	400 kHz/V (Typ.)
Tuning port capacitance	10 pF (Typ.)
Modulation bandwidth	> 20 MHz
Phase noise	

Offset	dBc/Hz (GYP.)
10 kHz	–114
100 kHz	–140
1 MHz	–160
10 MHz	–170

Phase noise

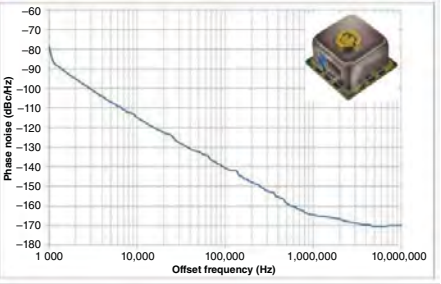

Figure E-27 Specification and phase noise plot for the model SDR0800-8 oscillator [12].

in the figure, with the help of a screw mounted on the DR, the frequency can be tuned for narrow band applications. However, DR placement using spacer/puck for optimum coupling and mechanical screw for tuning is sensitive to frequency drift under vibration. For applications where g-sensitivity is a critical issue, the DRO inherently exhibits poor phase noise performance in presence of vibration and acceleration. Figure E-25 shows the typical schematic of DRO using disc in conjunction with stacked SRR for the realization of Metamaterial-Möbius inspired SRR for frequency shaping resonant module, yielding stable oscillator circuits for applications as local oscillators (LO) [21].

For applications requiring compact size DROs, Metamaterial-Mobius DROs have been developed in SMD housings measuring just 0.75×0.75 in square packages. These oscillators can be extended to any number of fixed frequencies, typically from 3 to 18 GHz, without long lead times required to produce the sources. Figure E-26 shows a block diagram of a K-band oscillator.

Figure E-27 depicts the specification and phase noise plot for a model SDR0800-8, operating at 8 GHz in SMD housings measuring just 0.75×0.75 in square packages. These oscillators should be powered by a clean DC bias voltage; otherwise an external regulator should be employed to minimize variations in supply voltage. A DRO factory set for an output frequency of 10 GHz, for example, can be mechanically adjusted by about ± 50 MHz. An electrical tuning port provides an adjustment range of ± 1 MHz with tuning voltages of $+1$ to $+15$ VDC to compensate for frequency drift in phase-locked systems. The supply-current is typically 30 mA and the temperature range is specified from -25 to $+70\,^{\circ}$C.

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APPENDIX F

OPTO-ELECTRONICALLY STABILIZED RF OSCILLATORS

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F-1 INTRODUCTION

F-1-1 Oscillator Basics

Stable local oscillators are one of the basic building blocks of many microwave systems employed in communications, surveillance, imaging, remote sensing, and radar applications. Figure F-1 depicts the conceptual diagram of a feedback based oscillator, where ubiquitous noise is amplified using an active gain element and fed back in phase through a narrow bandpass filter or a resonator. The resulting power spectra suffer from close-in to carrier phase noise. A high quality factor for this resonant circuit has a great selectivity to filter out the broadband amplified noise spectra. Leeson's simplified model [1] predicts that the power spectral density of noise decreases as the inverse square of the loaded quality factor, Q_c, as follows:

$$S_\phi(f) = \left(1 + \frac{1}{f^2}\left(\frac{f_{\text{osc}}}{2 \cdot Q_C}\right)^2\right) S_\Phi(f) \tag{F-1}$$

where the noise sideband is expressed as $S_\Phi(f) = |\Delta\Phi|^2 = \frac{P_n}{P_{\text{signal}}}$. Note in this expression the effect of flicker phase is neglected and P_n corresponds to noise power in a 1 Hz bandwidth and P_{signal} is the oscillator output power. It is quite common for convenience to use the logarithmic value of single sideband residual phase noise in dBc/Hz as:

$$\mathcal{L}(f) = 10 \log_{10}(S_\Phi(f)) - 3 \text{ dB}$$

F-1-2 Resonator Technologies

Narrowband resonant circuits can be realized using acoustic, electromagnetic, or optical techniques. The technologies based on acoustic and electromagnetic techniques are quite popular and mature. Acoustic based resonators exhibit small size and they are extremely attractive at MHz range using Quartz crystals (both AT and SC cut),

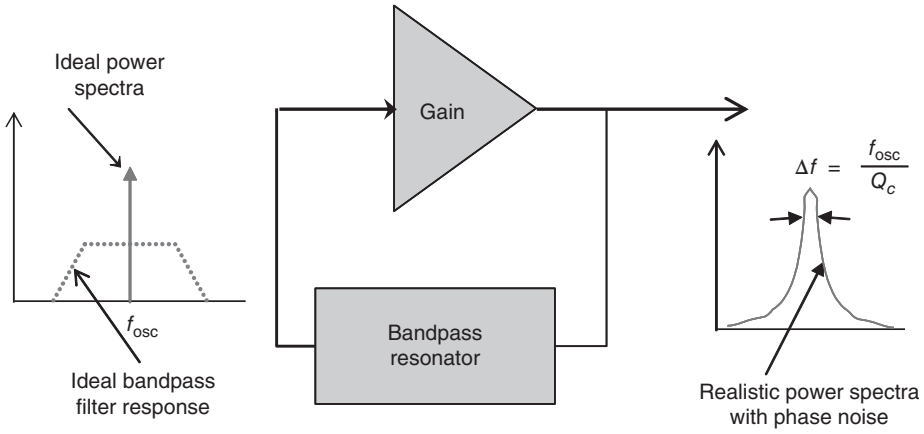


Figure F-1 Block diagram of feedback oscillator using the gain element and bandpass resonator. The power spectrum is controlled by the selectivity of the bandpass resonator [83].

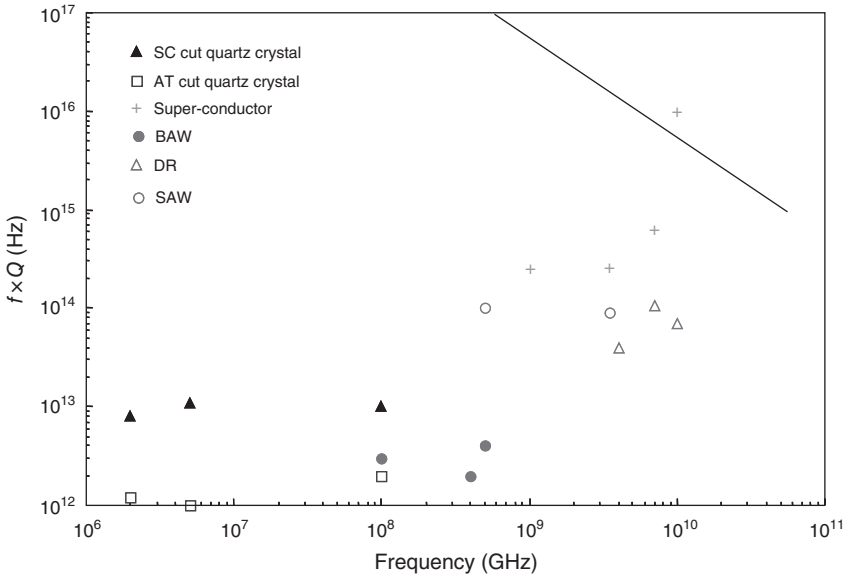


Figure F-2 Comparison of *Q* factors for acoustic and electromagnetic based resonators. Acoustic resonators are based on Quartz crystal, SAW (surface acoustic wave), and BAW (bulk acoustic wave). Electromagnetic resonators are based on DR (dielectric resonator) and super-conductors [2].

but bulk acoustic wave (BAW) and surface acoustic wave (SAW) resonators have demonstrated lossy behavior at microwave frequency. Electromagnetic resonators could be realized based on metallic structures, which are inherently large and lossy. To overcome these limitations, dielectric resonators (DRs) realized using high relative dielectric constant are small in size and super-conductor-based resonators exhibit a higher Q factor due to significant reduction in the Ohmic loss.

Figure F-2 that is adopted from Ref. [2] compares the performance of electromagnetic and acoustic resonators in terms of $f \times Q$ figure of merit (i.e. f, resonant frequency of the resonator times the resonator quality factor, Q) as a function of frequency. A line is also depicted in the figure that represents roll-off rate of 10 dB/decade versus

Table F-1 Comparison of phase noise and thermal stability of microwave oscillators realized using different resonator technologies in terms of loaded quality factor, Q_c and oscillator frequency, f_{osc}.

Resonator technology		f_{osc}	Q_C	Phase noise (dBc/Hz)	Stability (ppm/°C)
Quartz	BAW[126]	<200 MHz	10^5	100 MHz: −140 @ 100 Hz <−170 @ 10 kHz	0.1
	SAW[127]	<GHz	10^5	1 GHz: <−130 @ 1 kHz	<2
Coaxial cable		300 MHz–3 GHz	10^2–10^3	1 GHz: −70 @ 1 kHz −110 @ 10 kHz	100
Metallic cavity		L-C band	$\sim 10^3$–10^4	≈4 GHz: −110 @ 10 kHz	100
DRO	Ceramic [128]	L to Ku band	$\sim 10^4$	∼1 GHz: −159 @ 10 kHz ∼4 GHz: −133 @ 10 kHz ∼10 GHz: −118 @ 10 kHz	0.1–10
	Sapphire [129]	L to X band	$>10^5$	4.85 GHz: −138 @ 1 kHz −170 @ 10 kHz	NA

frequency for $f \times Q$ figure of merit (i.e. 20 dB/decade drop in Q versus frequency), which provides insight on how Q factor of resonators technologically change at higher frequencies. The highest figure of merit at microwave and millimeter wave frequencies is attained in super-conductor based resonators; however, cryogenic coolers are required. On the other hand, resonators based on fiber optic delay line are potentially *small size and low loss*, when the fiber optic transducer losses are maintained at a low level [3].

Table F-1 compares the performance of various microwave oscillators realized using acoustic and electromagnetic resonators in terms of close-in to carrier phase noise in dBc/Hz. Naturally resonators based on metallic structures are more sensitive to temperature variation as compared with dielectric based structures. In fact, dielectric resonators based on ceramics [4] have demonstrated passive compensation of physical and dielectric change with temperature, which results in high temperature stability. However, dielectric loss at higher microwave frequencies limits achieving high unloaded quality factor Q_u, while micro-phonics makes these resonators undesirable at high-g vibration.

The long-term frequency stability of the oscillator is primarily dictated by temperature sensitivity of the resonant circuit. Table F-1 also compares temperature sensitivity of microwave oscillators in terms of temperature stability measure in ppm/°C. The temperature stability of an oscillator is directly related to changes in physical dimension and dielectric constant of the high quality factor resonator as the temperature changes.

The electronic oscillators generate low phase noise signal up to a few GHz, but suffers phase noise degradation at higher frequencies, which is principally due to low quality factor (Q) resonator. The conventional approach for high frequency signal generation is based on frequency multiplier technique, but this technique suffers from higher phase noise due to AM-PM noise conversion [2]. There are different types of resonators used in electronic oscillator circuits such as printed coupled transmission line (TL) resonators using SAW resonators, DR, ceramic coaxial resonators, yttrium iron garnet (YIG) resonators, and sapphire-loaded cavity resonators (SLC). These resonators have their unique characteristics and limitations, operate typically from 500 MHz to 20 GHz; however their quality factor degrade as operating frequency increases and at best limited to $f \ Q < 10^{14}$. SLC based oscillator offers low phase noise signal generation, but has limited tuning and requires precise low temperature cooling system, which makes them expansive. The recent emerging technologies focus on metamaterial resonator based oscillator for microwave and millimeter wave applications.

The novel approach for generating low phase noise synthesized signal source trades phase noise with tuning, therefore not suited for wideband applications. The optoelectronic oscillator (OEO) has advantages of high quality factor due to long storage delay using low loss optical fiber, potential for high frequency operation due to inherently broadband of electro-optic (EO) and opto-electronic transducers, and great immunity to electromagnetic interferences.

F-1-3 Motivation for OEO

Optical techniques have found applications in a variety of microwave systems [5]. For example, optical analog to digital conversion (ADC) is one of the applications of microwave photonics in which a stable clock signal is required. Performance comparisons of various techniques to generate a stable clock signal are rendered in Table F-2. Comparison is made in terms of close-in to carrier phase noise measured at different microwave and millimeter wave frequencies. The results are, to the authors' knowledge, the best ever reported in each category. As shown in this table, the best result is achieved using OEO topology [6] at 10 GHz. The motivation for realization of microwave oscillators for frequency of f_{osc} using optical techniques is due to the potential for having a high quality factor using low loss optical delay lines, where the unloaded quality factor, Q_u, is directly proportional to the delay time, τ by $Q_u = -27.3\, f_{\text{osc}}\tau/S_{21}$ (dB), where S_{21}(dB) is insertion gain of delay line. Therefore, OEO realized using optical techniques are potentially suitable to generate microwave signals with extremely low phase noise by taking advantage of long low loss optical delay lines to maximize Q_c^2, as represented by Leeson's equation [cf. (F-1)].

F-1-4 Operation Principle of the OEO

The OEO is a special class of oscillator [7–10] that is based on converting continuous light energy from a pump laser into RF signals. The OEO is fundamentally similar to the Van der Pol oscillator [11]. Figure F-3 depicts the basic principle of realizing the OEO, where the high Q bandpass resonator is replaced by a fiber optic delay combined with an RF bandpass filter. In this figure an externally modulated fiber optic link is realized using a high power optical source, electro-optic modulator, and high optical power handling photodiode, where procedures to achieve excellent performance have already been exhibited [3, 5].

The superior performance of the OEO is due to long delay lines with low optical loss (e.g. fiber loss using Corning SMF-28 is less than 0.5 dB/km at 1550 nm). For example, a fiber delay length of 4 km will lead to an unloaded $Q_u \approx 10^5$ at 10 GHz for a fiber optic link loss of about 27 dB. Moreover, now photonic components generally exhibit greater maturity, resulting in high efficiency and low dispersion at millimeter wave frequencies as high as 110 GHz [12–14]. The OEO may also be considered a hybrid oscillator in so far as its operation involves both optical energy and microwave signals. Nevertheless, as a hybrid oscillator, the OEO is unique in that its output may be obtained both directly as a microwave signal, and as intensity modulation of an optical carrier [15]. This property of the OEO makes it naturally suited as a stable clock for all optical analog-to-digital converters (OADCs).

The OEO consists of a ring configuration consisting in turn of an electro-optic modulator that is fed back with a signal from the detected light at its output. As shown in Figure F-3, when the electrical signal is fed back in phase after a long delay time τ, a highly stable oscillation could be attained when the Barkhausen oscillation criterion is satisfied. Note that the oscillation frequency is directly related to the fiber delay time τ as $f_m = m(2\pi\tau)^{-1}$, where m is an integer number. This delay is related to fiber length (L) and fiber index of refraction (n) for the operating

Table F-2 Performance comparison of various optical techniques to generate a stable microwave signal.

Parameter		f_{osc} (GHz)	Phase noise (dBc/Hz)
Two independent sources	Lasers DFB [130]	64	−73 @ 10 kHz −90 @ 100 kHz
	Solid-state laser	1	−100 @ 10 kHz
	Er:Yb [131]	30	−90 @ 10 kHz
Master/slave lasers [133]	Nd:YAG [132]	50	−100 @ 100 kHz
Dual-mode laser [134]		57	−77 @ 10 kHz
Laser (nonlinear) [86]		37	−75 @ 5 kHz
Photo-HBT oscillator [135]		10	−108 @ 10 kHz
Opto-electronic oscillator [6]		10	−143 @ 10 kHz

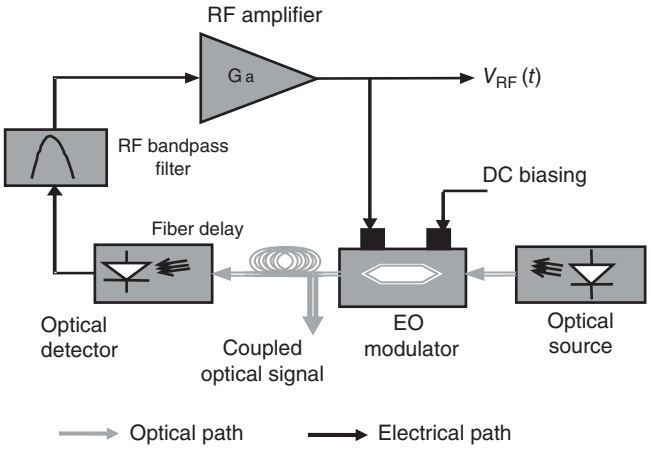


Figure F-3 Block diagram of opto-electronic oscillator used as the basis of stable microwave source. Note the frequency tuning is achieved in this architecture by adjusting the center frequency, f_{osc}, of the narrow bandpass filter [83].

source wavelength of λ as $\tau = nL/c$, where c is speed of light in free space (i.e. $c \approx 300\,\text{km kHz}$). Therefore, the shortest length causing the start of oscillation at 10 GHz is about a 1-cm-long fiber. In practice, fiber lengths are selected to be very large integer multiples of this minimum length of 1 cm long in order to meet high stability requirements.

However as result of this long fiber length, the oscillation frequency could be satisfied in a large number of frequencies that are clustered around a peak oscillation at f_{osc} with mode separation frequency of $\Delta f_m = 1/\tau$. Note that a narrow band microwave filter with bandwidth better than 100 kHz is required at 10 GHz to select one of these side-modes when mode competition is taking place. Various dual loop systems have been reported in literature [16–19] to limit the number of possible modes. Nonetheless, a narrowband microwave filter at frequency of f_{osc} could limit the number of side-modes around the oscillation frequency. In particular, a better frequency selectivity of this OEO is achieved when a narrower microwave filter at f_{osc} is selected. An optical filtering approach could also be employed for achieving narrow-band microwave filtering [20].

The phase noise of an OEO with 4 km fiber delay is shown in Figure F-4. At 6 kHz offset, the achieved phase noise is −163 dBc/Hz; however, the offset frequency span does not include beyond 10 kHz, where a large number of side-mode oscillations at approximately every 50 kHz will also exists. These side-modes of $f_m = m(2\pi\tau)^{-1}$contribute to aperture jitter degradation and only forced oscillation techniques suppress these side-modes. Nonetheless, the superior performance results from an extremely low-loss energy storage system when realized using a long optical fiber combined with efficient electrical–optical–optical conversion in fiber optic delay line, its corresponding low-noise figure delay line, and low amplitude modulation–phase modulation (AM–PM) noise conversion of RF amplifiers. The optical fiber by itself is also virtually free of any RF frequency-dependent losses, resulting in the same long storage time and high spectral purity signals for both low and high radio-frequency oscillation.

F-2 EXPERIMENTAL EVALUATION AND THERMAL STABILITY OF OEO

F-2-1 Experimental Setup

An experimental setup, shown in Figure F-5, is realized similarly to the system block diagram of Figure F-3. The high optical power source is realized using a distributed feedback laser (DFB) laser diode at 1550 nm (Philips CQF939) that is amplified by an Erbium-doped fiber amplifier (EDFA) from highwave. The high optical power of about 150 mW is injected into a Mach–Zehnder electro-optic modulator (Pirelli) with bandwidth of 10 GHz

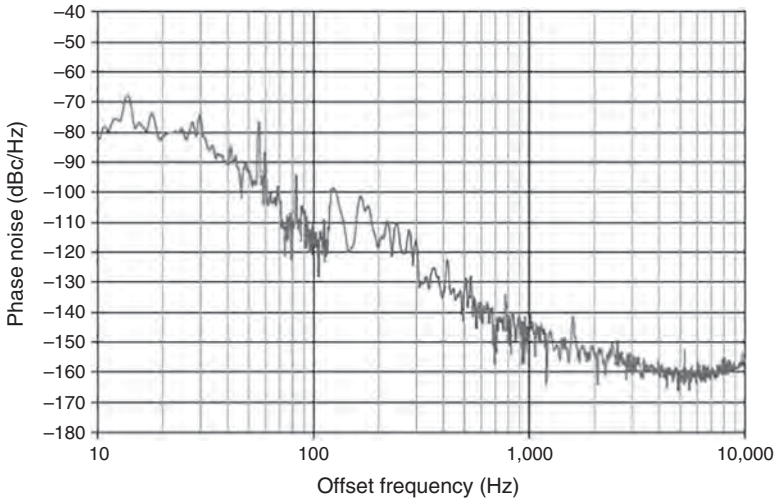


Figure F-4 Experimental result of and OEO with 4 km loop reported by D. Eliyahu et al. in [125]. Even though an excellent clean close-in to carrier is attained for a 4 km long OEO, but a number of side-modes are generated that contribute to timing jitter of this RF source [83].

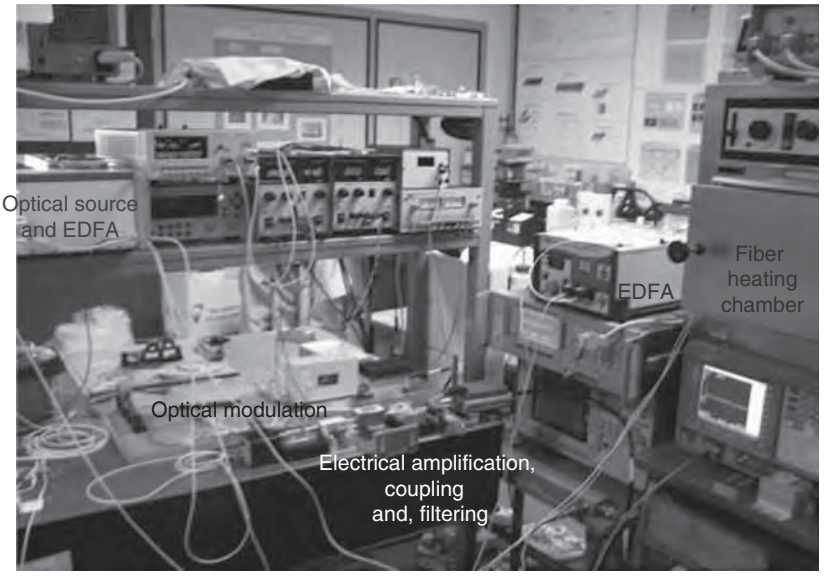


Figure F-5 Photograph of experimental setup employed for characterization of OEO using a topology shown in Figure F-3 [83].

and $V_{\pi} \approx 4$ V. The output of the EO modulator is delayed using a fiber optic (FO) delay line and then detected by a high power photodetector (DSC 50S). Two versions of optical fibers—standard single mode optical fiber (Corning SMF-28) and solid-core photonic crystal fiber (PCF) that are fabricated at Laboratoire de Physique des Lasers, Atomes et Molécules, UMR 8523, Université des Sciences et Technologies de Lille (UST-Lille)—were considered in the OEO experiments. The detected electrical signal is filtered by a 10 GHz narrow-band microwave

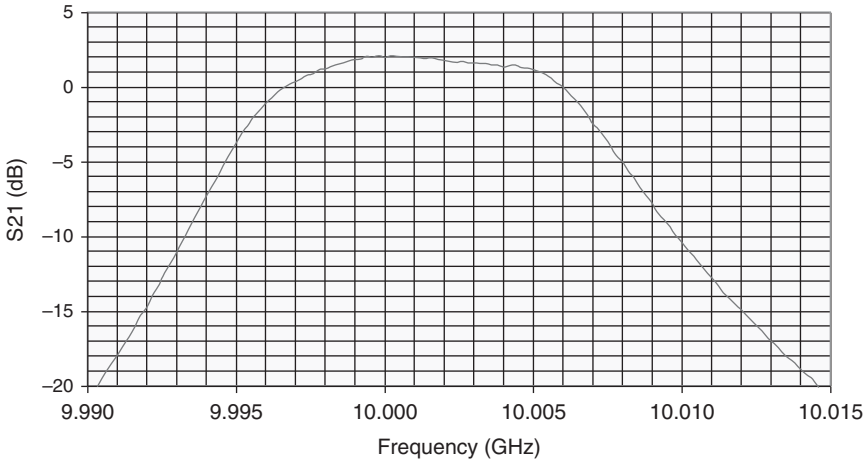


Figure F-6 Measured open loop insertion gain of the opto-electronic oscillator used in the experimental setup shown in Figures F-3 and F-5 that indicates the filter bandwidth of 10 GHz filter [83, 84, 122].

filter (Filtek: BP26/10000-10-4), and amplified by an electrical power amplifier (CIAO: 1011-541). The open loop gain of the fiber optic delay link as a narrow bandpass filter is measured using an automatic network analyzer and is depicted in Figure F-5, where a linear gain of at least 2 dB is observed at about 10 GHz. A 3 dB bandwidth is about 1 MHz (Figure F-6).

When the amplified signal is fed back to the RF driving port of the electro-optic modulator, while meeting the Barkhausen oscillation criterion, the OEO oscillates at a frequency close to the center frequency of the narrow-band microwave filter. The high selectivity of our bandpass RF filter allows for selecting only one oscillation mode, among the many supported by the loop, and therefore generates a high spectral purity microwave signal at 10 GHz. Figure F-7 depicts the measured averaged optical power as a function of the DC bias applied to the EO modulator. Note the highest power at the sidebands of double sideband (DSB) modulation format does not occur at quadrature operation points of 0.6 and 4.6 V, but rather at the pinch-off point of 6.5 V. This phenomenon is explained by the

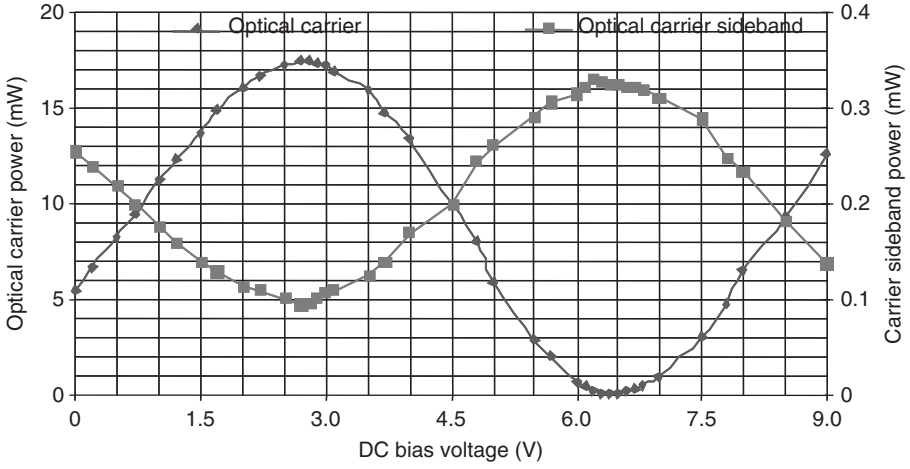


Figure F-7 Measured optical output power of the OEO at the optical carrier and sideband frequencies versus DC bias applied to the EO modulator [123, 124].

fact that the optical carrier is the dominant term in DSB modulation, which causes saturation of the photodiode. As the optical power of carrier signal is reduced, a higher optical power is obtained for the sidebands, leading to DSB-SC (suppressed-carrier) operation mode. RF power level of 25 dBm is predicted using a theoretical model in [21], which matches quite well with our measurement results. This level is limited by the saturation power level of the RF power amplifier.

Both short and long term frequency stability are employed as measures of the spectral purity and frequency drift of oscillators. In the following sections experimental evaluation of this OEO are evaluated in terms of frequency stability. The short term stability is presented in terms of residual phase noise, whereas the long-term stability is evaluated in terms of the temperature sensitivity of the oscillator.

F-2-2 Phase Noise Measurements

Residual phase noise measurements describe the oscillator stability over a short time scale. Close-in to carrier phase noise of the OEO in terms of various optical delay lengths is measured using an Agilent E550 system. Phase noise as low as −125 dBc/Hz is measured at an offset frequency of 10 kHz using a 1-km long SMF-28 fiber. The experimental results match the analytical prediction using models presented in [21]. A comparison of the achieved phase noise results is depicted in Figure F-8 for a 1 km long fiber with either FC/PC or FC/APC optical connectors. The measured phase noise is at least 5 dB better for FC/APC as opposed to FC/PC for offset frequencies of above 10 kHz. This degradation in phase noise is associated with higher optical reflection experienced in the FC/PC than FC/APC connectors. Additional experiments are also conducted using ≈57 m long solid-core photonic crystal fiber (SC-PCF) and the results are being presented for the first time. This special fiber is based on an ordered nano-structured material [22] whose interesting characteristics are an adjustable dispersion coefficient and an expected low thermal sensitivity. The physical structure of SC-PCF fiber is depicted in Figure F-8. We observed an increase in the optical delay line loss primarily due to the mode mismatch between the standard and SC-PCF fibers and non-negligible propagation loss in the PCF fiber due to less confinement in the core region. As a consequence of this additional loss of 20 dB, we inserted a supplementary optical amplifier (OSICS—maximum output power at 17 dBm) just before the optical detection and a second electrical amplifier (ALC/dc to 12 GHz—AWB0512-34-08) to maintain oscillation conditions.

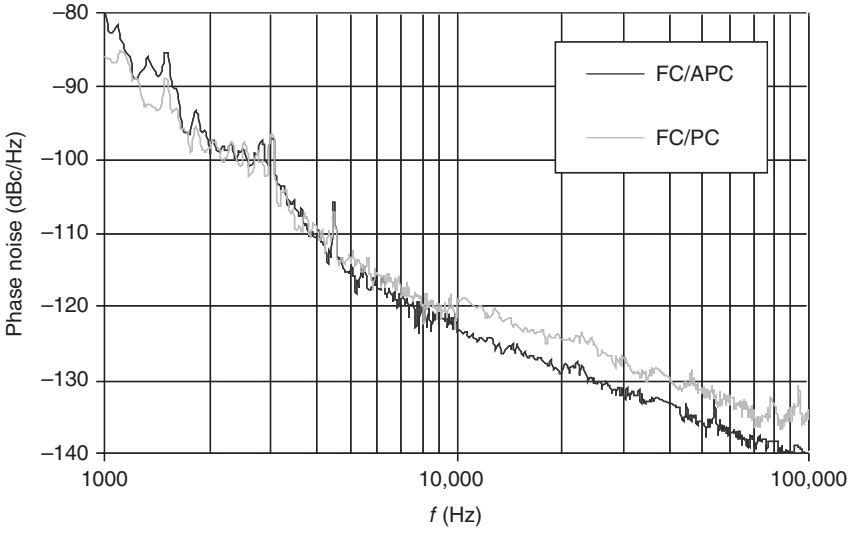


Figure F-8 Comparison of measured close-in to carrier phase noise attained for 10 GHz OEO using 1 km of SMF-28 fiber with FC/PC and FC/APC optical connectors [83, 84, 122].

Obviously as the insertion loss increases the Q_u decreases, and the close-in to carrier phase noise is degraded from −125 to −90 dBc/Hz at 10 kHz offset carrier. This result may appear to be discouraging, but the primary advantage of SC-PCF is its higher temperature stability over standard fibers as will be demonstrated in Section F-2-3. Moreover, this relatively poor residual phase noise could be significantly improved as technology matures and a lower loss PCF fiber becomes available. In fact, we anticipate that the loaded Q of delay line using SC-PCF will increase to the same levels as experienced by standard optical fibers (such as Corning SMF-28) as the optical attenuation decreases in our PCFs.

F-2-3 Thermal Sensitivity Analysis of Standard Fibers

Allan variance is an important parameter for the measurements of the frequency stability over (relatively) long time scales as opposed to close-in to carrier phase noise that is a measure of short term stability [1]. Aging in oscillators has been utilized as a systematic method measuring variation of frequency with time when all environmental parameters are held constant. Though there have not been any studies on aging of OEOs, Filler and Vig [23] reported results on the aging of crystal oscillators with expedited time periods as long as 1–10 years. The high Q elements of the OEO are the optical fiber and the RF filter. The thermal sensitivity of the oscillator's frequency will depend mostly on the sensitivity of both of those elements to the ambient temperature. When the temperature sensitivity of the fiber delay line is primarily considered, the frequency sensitivity can be expressed as:

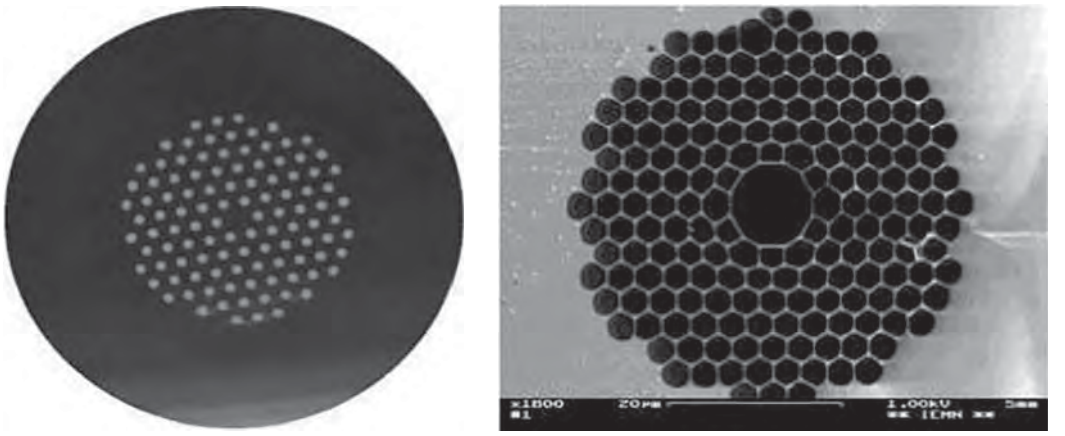
$$\delta f/f\delta t = -\delta L/L\delta T - \delta n/n\delta T \tag{F-2}$$

where L is representative of physical dimension and n corresponds to index of refraction (i.e. $n = \sqrt{\varepsilon_r}$). In practice, the variation of physical length is about two orders of magnitude smaller than index variation [24]; therefore to the first order, the first term in (F-2) could be neglected. Eliyahu et al. [6] showed that by thermally stabilizing the OEO, its frequency stability was improved from −8.3 to −0.1 ppm/°C with short term frequency stability of 0.02 ppm. Also, the mode hopping effect, resulting from center frequency drift of the non-stabilized RF filter, was eliminated. Locking the OEO to an external 100 MHz oscillator through a phase lock loop (PLL) circuit and frequency control device in the OEO loop improved the long-term frequency stability to that of the reference oscillator and at the same time maintained its low phase noise. As the wavelength of the optical source is adjusted while other parameters are kept fixed, a frequency shift occurs, expressed as:

$$|\Delta f_{\text{osc}}/(f_{\text{osc}})| = D_C \cdot L_{\text{SMF}} \cdot \Delta\lambda/\tau_{\text{LOOP}} \tag{F-3}$$

which is because of fiber dispersion ($D_C = 16.6$ ps/nm km in Corning SMF-28) experienced in a fiber length of L_{SMF} due to wavelength tuning of $\Delta\lambda$ in a loop delay of τ_{LOOP}. The measured normalized frequency shift is ≈3.05 ppm/nm with a predicted range of 3.25 ppm/nm. This feature could be exploited to build a tunable OEO with applications to frequency synthesizers. However, it is attractive to develop low thermal sensitivity optical delay lines by using combinations of air and glass fibers, such as photonic bandgap engineered fibers depicted in Figure F-9. This special fiber is based on an ordered nano-structured material [23] whose interesting characteristics are an adjustable dispersion coefficient. The PCF is made using the stack-and-draw fabrication technique, in which silica tubes are drawn down to form meter-length capillaries, which are then stacked by hand to form the required close-packed array.

Solid-core PCF (SC-PCF) is obtained by adding a rod in the center of the stack. In hollow-core PCF (HC-PCF), seven capillaries were omitted from the center of the stack to form the core in the final fiber, and the entire stack was jacketed before being drawn down to fiber. The core diameter d and the pitch Λ of the SC-PCF are about 3.2 and 6.7 μm respectively as shown in Figure F-9a. The resulting core diameter is about 9.7 μm that proves to exhibit a good coupling efficiency with standard telecommunication fibers. For the HC-PCF fiber, the spacing between the holes in the cladding (Λ) is 3.2 μm and the hole diameter is about 2.9 μm, as shown in Figure F-9b. These parameters have been chosen in order to have a transmission windows centered at 1550 nm. The expected attenuation of SC-PCF is as low as 20 dB/km, whereas the HC-PCF is of order of 50 dB/km. Even though the current optical attenuation suffers from significant optical attenuations due to optical mode mismatch and poor quality of ordered structure, but these challenges are expected to be resolved over time. The advantages of the OEO systems using such fiber delay lines are explored next.



(a) (b)

Figure F-9 Structure of a solid-core photonic crystal fibers used in the OEO experiment with cladding diameter of 125 μm. (a) SC-PCF with core diameter ≈9.7 μm, hole diameter ≈3.2 μm, and holes center to center separation ≈6.7 μm; (b) close-up view of HC-PCF with hollow-core diameter ≈9.7 μm, hole diameter ≈2.9 μm, and holes center to center separation ≈3.2 μm [83, 84, 122].

F-2-4 Temperature Sensitivity Measurements

We have also conducted temperature sensitivity measurements on the OEO to compare frequency drift performance utilizing standard fiber (e.g. SMF28) against PCF (e.g. SC-PCF), as a passive technique to reduce the temperature sensitivity of the OEO. The primary question is whether PCF exhibits a reduced thermal sensitivity! Characterization of this figure is tabulated for SC-PCF. As part of this experimental study, we have measured the frequency shift of the 10 GHz OEO by thermally-induced delay in the fiber optic delay line. Figure F-10 depicts the heating

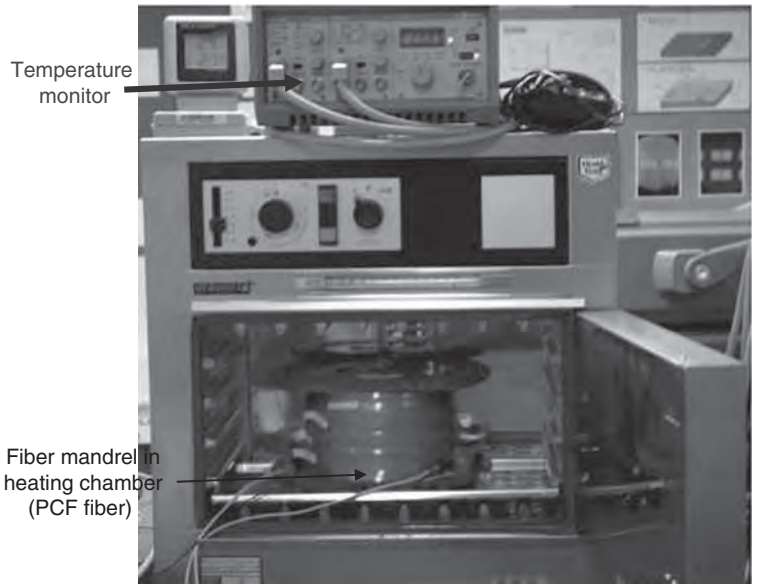


Figure F-10 Experimental set up for thermal sensitivity evaluation of the SC-PCF based OEO [83, 84, 122].

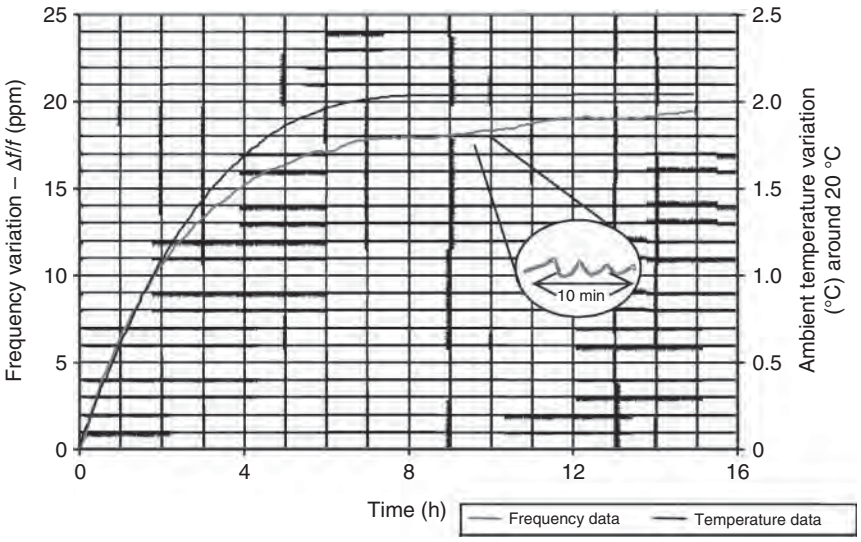


Figure F-11 Measured temperature stability (lower trace) of 10 GHz OEO using SMF-28 fiber, as temperature (upper trace) is varied [83, 84, 122].

chamber employed for OEO thermal sensitivity measurements and performance comparison of the SMF-28 against the SC-PCF. Temperature of the fiber under test (FUT) can be modified from ambient (25 °C) to 220 °C in a heating chamber (MEMMERT with ventilation option – DIN 12-880-KI).

Long-term temperature sensitivity of the OEO is measured and the results are depicted in Figure F-11, where the highest variation during the first range of 6h is $|\Delta f_{osc}/(f_{osc} \cdot \Delta T)| \approx 10\,\text{ppm}^\circ\,\text{C}$. Note that short-term stability for 10 min during the thermally stabilized range of time is $|\Delta f_{osc}/f_{osc}| = 0.0511$ ppm as depicted in the inset of Figure F-11. As reported in [24], the temperature sensitivity of the index refraction is much higher than the temperature sensitivity of the fiber length. A correction coefficient had to be calculated before extracting the index variation ($\Delta n/n \cdot \Delta T$) of each fiber by accounting for the extra propagation delay due the other optical and electrical components (τ_{FIX}) and the propagation delay of the FUT (τ_{FUT}) in the oscillation loop. The revised (F-2) is:

$$\Delta f/f \cdot \Delta T = -k(\Delta n/n \cdot \Delta T + \Delta L/L \cdot \Delta T) \tag{F-4}$$

where

$$k = (1 + \tau_{FIX}/\tau_{FUT})^{-1} \tag{F-5}$$

We first employed a 12.55-m length of SMF-28 and measured the temperature sensitivity of this fiber as a baseline measurement. Although the loss of SMF-28 is negligible compared to SC-PCF, to keep the same operation condition and equivalent global time delay the additional optical and electrical amplifiers are kept in the loop, since those are required for oscillation condition for OEO experiments at 10 GHz utilizing SC-PCF. Comparison of the measured thermal sensitivity of oscillation frequency for the 10 GHz OEO and the calculated index of refraction for SMF-28 and SC-PCF is tabulated in Table F-3, where a factor of three reduction in temperature sensitivity of index of refraction is observed for SC-PCF fibers. Therefore, to achieve the required thermal stability of the OEO, the temperature control requirement is markedly less stringent when SC-PCF is employed in place of the standard fiber.

Even though the SC-PCF provides about a factor of three reductions in temperature sensitivity, but it is not still sufficient. Eliyahu et al. [6] showed active thermal stabilization of the OEO, where its frequency stability was improved from −8.3 to −0.1ppm/°C with short term frequency stability of 0.02 ppm. Also, the mode hopping effect, resulting from center frequency drift of the non-stabilized RF filter, was eliminated. Locking the OEO to

Table F-3 Calculations of k and the effective index change versus temperature for both standard and photonic crystal fibers in OEO, as fiber under test (FUT).

FUT	SMF-2812.5 m	SC-PCF56.5 m
$\Delta f/(f\,\Delta T)$ (ppm/°C)	−2.58	−2.70
τ_{FUT} (ns)	60.8	274.9
k	4.425	1.754
$\Delta n/(n\,\Delta T)$ (ppm/°C)	11.37	4.73

an external 100 MHz oscillator through a PLL circuit and frequency control device in the OEO loop improved the long-term frequency stability to that of the reference oscillator and at the same time maintained its low phase noise.

F-2-5 Temperature Sensitivity Improvement with HC-PCF

The complexity of active temperature compensation begs passive compensation techniques. Focus of our current work—reported for the first time here—is to combine standard and HC-PCF to reduce temperature sensitivity, which is expressed as:

$$\Delta f/f\Delta T = -(1 + n_s L_s/n_p L_p)\Delta n_p/n_p \Delta T - (1 + n_p L_p/n_s L_s) \times \Delta n_s/n_s \Delta T \tag{F-6}$$

where subscript "s" stands for standard fiber and "p" for PCF. Note since the slope of index of refraction variation in standard fiber is negative with respect to temperature, a passive compensation is achieved for a positive slope for effective index of refraction of HC-PCF. The estimated optical power distribution in the HC-PCF is predicted to be at least 98% using our analytical modeling [25] (i.e. fill factor inside silica fiber is expressed as $K = 0.02$). From the published literature, the reported negative slope for index of refraction of air is $\Delta n_{air}/n_{air}\Delta T \approx -0.89$ ppm/°C [26] as compared to a positive change in silica of order $\Delta n_{silica}/n_{silica}\Delta T \approx 9.7$ ppm/° C [27]. The estimated effective index of refraction of HC-PBG is $n_{eff} \approx K n_{silica} + (1 - K) n_{air} = 1.00915$. The expected change in index of refraction of HC-PCF fiber due to temperature then can then be approximated as:

$$\Delta n_{eff}/\Delta T = K\Delta n_{silica}/\Delta T + (1 - K)\Delta n_{air}/\Delta T = -0.587 n_{eff} = -0.592 \text{ ppm/°C} \tag{F-7}$$

This anticipated negative change in index of refraction of HC-PCF fibers could be used for passive temperature compensation as represented in Eq. (F-6). More specifically in the OEO realized using the standard silica based fibers, the oscillation frequency shifts to a lower frequency due to temperature increase at the rate of 9.7 ppm/°C. However for an HC-PCF fiber based OEO, the oscillation frequency shifts to a higher frequency due to rate of −0.592 ppm/°C.

F-2-6 Improve Thermal Stability Versus Phase Noise Degradation

Although this reduced temperature compensation technique was useful for the OEO in achieving thermal stability, it comes at the cost of degradation in the close-in to carrier phase noise of the 10 GHz OEO, as depicted in Table F-4. The predicted and measurement results of the reported OEO are shown in Figure F-12. A 65 dB degradation is measured in the phase noise of the OEO. The phase noise degradation was attributed to additional electrical and optical amplifiers required to compensate for the excessive optical losses, but this paper identifies it as primarily due to excessive losses (2 dB/m) of PCFs that results in reduction of an effective Q of resonant structure.

Table F-4 Phase noise comparison of standard and temperature compensated OEO using HC-PCF.

OEO	Standard fiber 1 km 0.2 dB/km	HC-PCF 30 m (2 dB/m)
Experiment [28]	−123 dBc/Hz @ 10 kHz	−58 dBc/Hz @ 10 kHz
Simulation	−125 dBc/Hz @ 10 kHz	−60 dBc/Hz @ 10 kHz

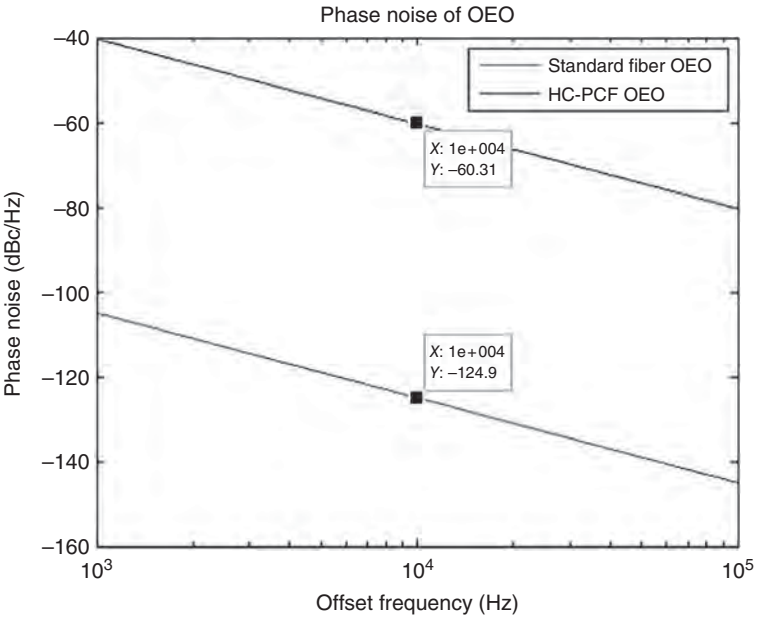


Figure F-12 Measured (single data point) is fitted to Leeson's close-in to carrier phase noise model of OEO using equal lengths of standard fiber and using composite fiber using HC-PCF [83, 84, 122].

F-2-7 Passive Temperature Compensation

A combination of standard and HC-PCF is considered as a composite fiber that could be used as a delay line. The total delay time in a composite fiber is expressed as:

$$\tau = \frac{n_s L_s}{c} + \frac{n_p L_p}{c} = \frac{1}{f} \tag{F-8}$$

when used in Eq. (F-8) can be reduced to the frequency variation due to temperature in a composite fiber structure as a function of the refractive index of each type of fiber that is given in [28] as

$$\frac{\Delta f}{f \Delta T} = -\frac{n_s L_s}{n_s L_s + n_p L_p}\left(\frac{\Delta n_s}{n_s \Delta T}\right) - \frac{n_p L_p}{n_s L_s + n_p L_p}\left(\frac{\Delta n_p}{n_p \Delta T}\right) \tag{F-9}$$

Length variations being almost three orders of magnitude smaller than the refractive index variation [29] are neglected in the Eq. (F-9) and n_s, n_p, and L_s, L_p stand for the refractive index and lengths of the silica based and photonic crystal based fibers respectively. The measured temperature sensitivity of different fibers is as summarized in the Table F-5. The positive refractive index variation slope of silica based fiber and the negative refractive index

Table F-5 Temperature sensitivity of different fibers.

	Silica	SC-PCF	HC-PCF (HC–1550–04)
$\frac{\Delta n}{(n\Delta T)}$ (ppm/°C)	9.7	4.73	−0.361

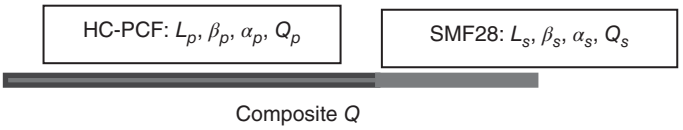


Figure F-13 Representation of composite fiber with individual characteristics in terms of Q for each section of the structure [83, 84, 122].

variation slope of HC-PCFs together help in passive temperature compensation as described earlier. The required length ratio is then found from Eq. (F-10) is to be:

$$\frac{L_p}{L_s} = -\frac{An_s}{Bn_p} \tag{F-10}$$

where $A = \frac{\Delta n_s}{n_s \Delta T}$ and $B = \frac{\Delta n_p}{n_p \Delta T}$. Using the specifications of the commercially available PCF fiber HC–1550–04 from NKT photonics, the aforementioned length ratio has been determined to be approximately around 38:1. This length ratio of the composite structure would ensure greater temperature stability, but would degrade the phase noise performance in comparison to a single standard fiber as presented in the analysis in the following text.

The basic definition of quality factor "Q" is given as:

$$Q = \omega_0 \frac{\text{Energy Stored}}{\text{Power Loss}} \tag{F-11}$$

When the optical fiber is recognized to be similar to a transmission delay line, its Q could be expressed as [30]:

$$Q = \frac{\beta}{2\alpha} \tag{F-12}$$

where β is the phase propagation constant and α is the attenuation in the fiber. The composite fiber structure is depicted in Figure F-13. The Q associated with a combination of fibers as shown in Figure F-13 can be expressed as:

$$Q_{\text{total}} = \left(\frac{\beta_s L_s + \beta_p L_p}{2\alpha_s L_s + 2\alpha_p L_p} \right) \tag{F-13}$$

From earlier, it is evident that the high attenuation level of HC-PCFs is the limiting factor in the improvement of Q and hence it contributes to the significant degradation of phase noise of the OEO reported in Table F-5.

F-2-8 Improving Effective *Q* with Raman Amplification

To mitigate the effect of degradation of phase noise due to increased attenuation of composite fiber delay line, in this paper we propose for the first time Raman amplified composite fiber delay line. More specifically, by taking advantage of nonlinear stimulated Raman scattering (SRS) in the silica portion of the HC-PCF the effective fiber attenuation is reduced and hence resulting in increase in the quality factor of the composite structure while still passive temperature compensation is being maintained in the composite fiber.

With respect to the other nonlinear optical fiber amplification processes (e.g. the stimulated Brillouin amplifier, erbium doped fiber amplifier), the Raman amplification (RA) is the most attractive technique due to its benefits like flat gain over broad bandwidths, improved noise performance and reduced nonlinear penalty allowing for longer fiber lengths, and closer channel spacing. Raman amplification results from the nonlinear scattering process in optical fibers wherein a part of the pump optical energy at a higher optical frequency is transferred to the signal operating at a lower frequency signal. The optical gain spectrum is peaked, when optical signal is spectrally coinciding with the Stokes lines of 13.2 THz lower than the pump frequency.

In our approach, Raman amplifier gain is designed to compensate for losses associated with the PCF in the composite fiber such that the signal output power remains very close to the input optical power. Therefore, the overall loss/gain of the fiber would be approaching 0 dB as expressed as:

$$\alpha_{\text{Effective}} = \frac{P_s(L) - P_s(0)}{L}$$

where $P_s(L)$ and $P_s(0)$ are the signal power levels at length of L and 0 km respectively. The pump laser source is judiciously selected with the optical signal source wavelength and it can be either forward (along the direction of signal) or reverse direction (opposite to the direction of the signal) propagating, but reverse pumping is preferred over forward pumping because the Pin Photodiode based optical receivers would not suffer from a higher shot noise and nonlinear limitations of the forward propagating systems. The location of the pump source would be at the beginning of the PCF fiber in forward pumping so that the signal and pump wavelengths enter the fiber at the same point and travel in the same direction and at the end of the fiber for reverse pumping so that the signal and pump wavelengths enter the fiber at its two ends and travel in the opposite directions.

To achieve effective loss/gain of 0 dB over a fiber length in a practical OEO, pump power levels have to be appropriately selected for the fiber length of choice. For example for an extremely long length of fiber delay lines of 80 km length in a standard optical fibers with 0.33 dB/km attenuation (e.g. Corning SMF-28 fiber), a pump power of 20 dBm (22 dBm) is required for 5 dBm (10 dBm) input signal power. Table F-6 depicts the comparison of the quality factor of standard SMF-28 fiber with the composite fiber before and after Raman amplification in the composite fiber. On the other hand, the required laser pump power is around 35 dBm for a 1 km length of commercial HC-PCF fiber with 15 dB/km attenuation (e.g. NKT Photonics HC-1550-04) for signal power level of 5 dBm. As technology of HC-PCF has advanced and now commercial products are readily available (though at a very high cost) with attenuation levels of 15 dB/km compared to 2 dB/m of circa 2005, we anticipate that attenuation levels could be reduced from 15 dB/km gradually to 1 dB/km in the next few years. Therefore, for two practical signal powers of 5 and 10 dBm prediction of the required pump power and associated maximum length are depicted in Figure F-14, as an effective optical attenuation 0.33 dB/km is attained in the composite fiber while the optical attenuation of HC-PCF fiber is reduced from 10 dB/km in gradual steps to values of 5, 3, and eventually to 1 dB/km.

In Table F-6 performance comparison of OEO in terms of effective Q and close-in to carrier phase noise at 10 kHz offset are made for cases of with (shaded column) and without (unshaded columns) RA. Note passive temperature compensation is attained with HC-PCF fiber length of 38:1 to SMF-28; moreover, the achieved maximum length of composite fiber increases from 1.23 to 3 km as attenuation of the HC-PCF fibers are reduced from 15 to 10 dB/km for the same pump power of 35 dBm. Moreover, the optimum length can be increased to 10 km for a pump power of only 30 dBm. The calculated effective optical attenuation of the composite fiber with RA are about 0.1 for the 3 dB/km, 0.16 for 10 dB/km, and even approaching 0.14 dB/km for commercially available HC-PCF (NKT Photonics HC-1550-04) with loss of 15 dB/km. Values of the effective Q are calculated using Eq. (F-13) for composite fibers and compared relative to Q of standard fiber, Q_s. Note that with RA there is a Q enhancement for the composite fiber, while without RA a loss dominated by HC-PCF causes a significant reduction the effective Q. The resulting achieved close-in to carrier phase noise at two offset frequencies of 1 and 10 kHz from 10 GHz carrier are also rendered in Table F-6. A significant reduction in phase noise in composite fibers with RA with an effective loss of 0.1 dB/km and 10 kHz/C drift is estimated due to the enhancement of about 7 dB compared to OEO with SMF-28 fiber.

Table F-6 Effective Q and phase noise comparison between SMF-28 and composite fibers before and after Raman amplifier.

	Fiber delay length (km)/ Pump power (dBm)	Effective attenuation of HC-PCF without RA (α_p in dB/Km)	Effective attenuation of composite fiber with RA (α_p in dB/Km, $\alpha_s = 0.33$ dB/k)	Relative Q without RA	Relative Q with RA	Phase noise degradation without RA	Phase noise degradation with RA	Phase noise (dBc/Hz) @ 1 kHz without RA	Phase noise (dBc/Hz) @ 1 kHz with RA	Phase noise (dBc/Hz) @ 10 kHz without RA	Phase noise (dBc/Hz) @ 10 kHz with RA
SMF-28	10/NA	—	—	Q_s	—	—	—	−123	—	−143	—
Composite fibers with passive temperature compensation of $Lp{:}Ls = 38{:}1$	10/30	3	0.10	$\frac{Q_s}{12.6}$	$2.2Q_s$	22	−7	−101	−130	−121	−150
	3/35	10	0.16	$\frac{Q_s}{41.8}$	$1.5Q_s$	32	−3	−91	−126	−111	−146
	1.23/35	15	0.14	$\frac{Q_s}{62.6}$	$1.6Q_s$	36	−4	−87	−127	−107	−147

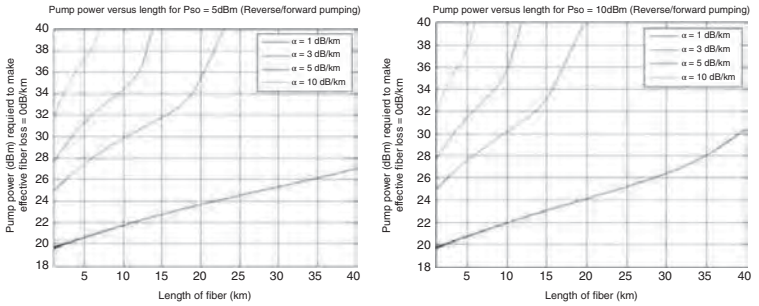


Figure F-14 Minimum optical pump power versus optical fiber lengths to overcome excessive loss in the composite fiber using HC-PCF with optical attenuation of 1, 3, 5, and 10 dB/km for signal power levels of 5 and 10 dBm [83, 84, 122].

F-3 FORCED OSCILLATION TECHNIQUES OF OEO

Short and long term stability of high frequency oscillators are important for high-speed data transmission. Forced oscillation has been a technique where oscillation frequency could be stabilized using concept of injection locking (IL) [31, 32] and PLL [33–35], as the concept of PLL has been the focus of this book. Distribution of a highly stable with low phase noise external frequency reference is employed to force oscillators to lock to clean phase noise characteristics of the frequency reference. Among them first the indirect optical injection locking [36, 37] has been applied to distribute microwave [38] and millimeter wave oscillators [39–44] for optical control of large phased array antennas for radar and communications [44–48]. The analytical modeling of injection-locked oscillators have been developed based on parametric oscillation [49–53] to achieve low phase noise from various frequency references. The combination of both injection locking and phase lock loop functions are proposed as an injection-locked phase locked loop (ILPLL) based forced stabilization process and its superior performance is experimentally demonstrated [54]. A number of different oscillator topologies [55–57] are used for efficient front-end operations for low phase noise/frequency stability [57], low free-running phase noise oscillator that is combined with mixing conversion gain with high dynamic range, while prime power and space saving is also achieved [55, 56]. In fact, it is feasible to combine operation of mixing combined with oscillation and phase shifting [47] as a very elegant solution for electronically scanned phased array antennas for communication and remote sensing applications.

A new category of oscillators is based on long optical delay lines to provide high frequency stability [58] and is known as OEO [59]. This structure has been widely employed for implementing high frequency RF oscillators because of their high spectral purity [60] and it has been extended to operation of 50 GHz [8]. One of the challenges encountered with OEO is temperature sensitivity of the long fiber optic delay lines [61], which can be improved on by employing passive temperature compensation using special hollow-core PCFs (HC-PhC) [62] that results in both short term and long term frequency stability [28]. The broadband behavior of fiber optic delay lines provides frequency tuning of OEO with a large number of potential oscillation frequencies. Narrow-band filters are the core part of an OEO operation, which it determines the oscillation frequency by employing extremely narrow band fixed frequency filters [61]. To achieve broadband frequency tuned OEO, YIG filter structures [29] are integrated in the optical delay line based OEO [63], as also reported earlier with field effect transistor (FET) based tunable oscillators [29]. Even though the OEO could exhibit higher quality factor with longer fiber delay lines, but the multiple side-modes exists around the oscillation frequency, as 5 km of fiber corresponds to side-mode oscillations of every 40 kHz, which is not feasible to be removed even using narrowband electronic filters. A coarse tuning of wideband YIG [29] filter combined with a fine tuning narrowband wavelength-tuned optical transversal filter [64–67] using short delay lines or chirped fiber Bragg grating (CFBG) [68] provides high resolution frequency selectivity, but nonetheless a number of side-modes still persists. However, forced oscillation techniques could help to reduce the oscillation side-modes [68].

Benefits of ILPLL [54] in electronic systems are enumerated in [69] due to improvement in close-in to carrier phase noise, reduction in pull-in time, and enhanced locking range and tracking range over the standard IL or PLL and reduced prime power and space saving over a multiplier chain. These benefits could be equally achieved in oscillators without using an external frequency reference using a concept of self-IL [2, 70–72] or self-PLL [73–75] for improvement in phase noise at both close-in and far-away from carrier, while oscillation side-modes are also suppressed using multiple loops with non-harmonic delays. In addition, the concept of self-injection locked (SIL) and self phase locked loop (SPLL) are combined as self-forced oscillation techniques are employed for further improvement in close-in to carrier phase noise, while maintaining a low thermal sensitivity of OEO using composite fibers. The forced oscillation are really extension of standard oscillator stabilizations that are known as injection locking, phase locking, and combination of injection- and phase-locked loop techniques. The phase noise modeling of each technique is covered in the following sections.

F-3-1 Analysis of Standard Injection-Locked (IL) Oscillators

In this section, a system level modeling is used as a unified model for phase noise modeling of oscillators with injection scheme. Since the phase dynamics of injection locking process is equivalent to that of first-order type I PLL [76], it is intuitive for us to derive the phase noise expression of injection locked oscillator (ILO) using PLL model. This approach is preferred as there is opportunity to extend modeling to PLL and implement a unified

modeling of ILPLL oscillators [48, 51, 52]. As part of the modeling, let y_i and y_o be the injecting signal and the output signal of the oscillator in the free-running case, respectively:

$$y_i = \cos(\omega t + \theta_i(t)) \tag{F-14}$$

$$y_o = \cos(\omega t + \theta_o(t)) \tag{F-15}$$

Defining $\phi_i(t) = \omega t + \theta_i(t)$, $\phi_o(t) = \omega t + \theta_o(t)$, and using Eqs. (F-14) and (F-15) with the famous Adler's equation [31], then phase dynamics of IL can be written as

$$d\theta_o(t)/dt = \rho\omega_{3\text{dB}} \sin(\theta_i(t) - \theta_o(t)) \tag{F-16}$$

where $\rho = \sqrt{(P_i/P_o)}$ is the injection strength, and $\omega_{3\text{dB}} = \omega_r/2Q$ is half the 3 dB bandwidth of the oscillator resonator. When the frequency difference between the injecting signal and the free-running oscillator is small, the phase difference between them is also small. Thus we can linearize Eq. (F-16) to have

$$d\theta_o(t)/dt = B(\theta_i(t) - \theta_o(t)) \tag{F-17}$$

where $B = \rho\omega_{3\text{dB}}$. Eq. (F-17) is of the same form of the phase dynamics for the first-order type I PLL. Performing the Laplace transform of the aforementioned time domain variable, Eq. (F-17) can be expressed in s-domain as

$$s\theta_o(s) = B(\theta_i(s) - \theta_o(s)) \tag{F-18}$$

The transfer function of phase of IL can be found as

$$H_\theta(s) = \theta_o(s)/\theta_i(s) = (B/s)/(1 + B/s) \tag{F-19}$$

The block diagram representing Eq. (F-19) is depicted in Figure F-15a. We can see that IL resembles a negative feedback control loop that contains an integrator. The integrator is usually a voltage controlled oscillator (VCO), which is suitable for integration of PLL function. The loop behavior in the presence of noise sources is systematically presented in Figure F-15b, where the major noise contributors in IL are $n_1(s)$ at the injection point that contains injecting signal noise and residual noise of the system, and $n_2(s)$, which is the oscillator phase noise.

Assuming the noises are a small perturbation to the steady oscillation, thus linearity still holds in the IL system. Then we can find the oscillator output due to noise using superposition principle. We first use standard loop analysis to find out the output θ_{o1} due to input noise n_1 only as

$$\theta_{o1} = -(B/s)\theta_{o1} + (B/s)n_1 \tag{F-20}$$

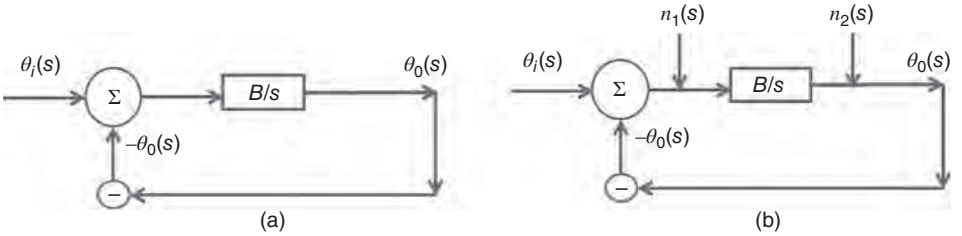


Figure F-15 Conceptual block diagram representation of IL using control theory representation; (a) without noise sources present; (b) with noise sources of n_1(s) and n_2(s) added in the loop [83, 84, 122].

After rearranging Eq. (F-20) in terms of θ_{o1}, results in

$$\theta_{o1} = (B/s)/(1 + B/s)n_1 = H_\theta(s)n_1 \tag{F-21}$$

Similarly, the output θ_{o2} due to oscillator phase noise n_2 only is expressed as

$$\theta_{o2} = 1/(1 + B/s)n_2 = (1 - H_\theta(s))n_2 \tag{F-22}$$

Hence the output θ_o due to contributions of both noises is

$$\theta_o = H_\theta(s)n_1 + (1 - H_\theta(s))n_2 \tag{F-23}$$

The power spectral density of the output phase θ_o of offset angular frequency ω becomes

$$S_{\theta o}(\omega) = |H_\theta(j\omega)|^2 S_{n1}(\omega) + |1 - H_\theta(j\omega)|^2 S_{n2}(\omega) \tag{F-24}$$

where $S_{n1}(\omega)$ and $S_{n2}(\omega)$ are the power spectral densities of n_1 and n_2 respectively.

F-3-2 Analysis of Self-Injection Locked (SIL) Oscillators

In this section, the conceptual block diagram of SIL using control theory representation is shown in Figure F-16. A portion of the oscillator output signal is delayed by a long delay (τ_d) and is fed back to the oscillator with coupling factor of ρ. The phase of the delayed signal is then compared against that of current signal to generate an error signal for self-injection to the oscillator similar to the one shown in Figure F-15b.

The phase noise of the SIL can be found by using the same procedure as presented in Section F-3-1 for external IL. The only difference is that n_1 in this case does not contain the injecting signal noise but only the residual noise of the system. We can first find the output θ_{o1} due to n_1 as

$$\theta_{o1} = -(B/s)\theta_{o1} + \exp(-s\tau_d)(B/s)\theta_{o1} + (B/s)n_1$$

and hence after regrouping

$$\theta_{o1} = \frac{B}{s + B(1 - e^{s\tau}d)}n_1 \tag{F-25}$$

Output θ_{o2} due to oscillator phase noise n_2 is:

$$\theta_{o2} = -(B/s)\theta_{o2} + \exp(-s\tau_d)(B/s)\theta_{o2} + n_2$$

and hence after regrouping

$$\theta_{o2} = \frac{s}{s + B(1 - e^{s\tau}d)}n_2 \tag{F-26}$$

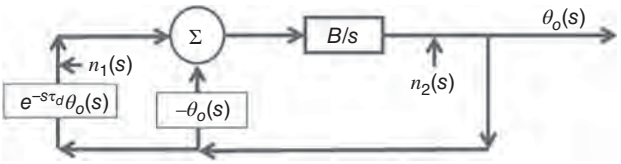


Figure F-16 Conceptual block diagram of SIL using control theory representation with a self-feedback after a delay of τ_d with coupling factor of ρ integrated to system [83, 84, 122].

Overall output θ_o is found as

$$\theta_o = \theta_{o1} + \theta_{o2} = \frac{B}{s + B(1 - e^{s\tau}d)} n_1 + \frac{s}{s + B(1 - e^{s\tau_d})} n_2 \tag{F-27}$$

Then the power spectral density of θ_o becomes

$$S_{\text{sil}}(\omega) = |H_a(j\omega)|^2 S_{n1}(\omega) + |H_b(j\omega)|^2 S_{n2}(\omega) \tag{F-28}$$

where $H_a(s) = \frac{B}{s+B(1-e^{s\tau_d})}$ and $H_b(s) = \frac{s}{s+B(1-e^{s\tau_d})}$

Note that the transfer functions $H(s)$ has resonant peaks that are related to the harmonic of frequencies $s = j\omega$, where $e^{-js\tau_d} = 1$. $S_{n1}(\omega)$ is the residual noise at offset frequency of f:

$$S_{n1}(f) = \frac{kTBF}{2P_s}\left(\frac{f_c}{f} + 1\right) \tag{F-29}$$

while $S_{n2}(\omega)$ is expressed using Leeson's equation [1] at offset frequency of f_m

$$S_{n2}(f) = \frac{kTBF}{2P_s}\left[\frac{1}{f^3}\left(\frac{f_o^2 f_c}{4Q_L^2}\right) + \frac{1}{f^2}\left(\frac{f_o^2}{4Q_L^2}\right) + \frac{f_c}{f} + 1\right] \tag{F-30}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant; $T = 290\,^{\circ}$K is the room temperature in Kelvin; $B = 1$ Hz is the noise bandwidth being considered; F is the system noise figure; P_s is the carrier power level; f_o is the oscillation frequency; $f_c = 1$ MHz is the flicker noise corner frequency; Q_L is the loaded Q of the oscillator resonator. For oscillator phase noise $S_{n2}(\omega)$, a roll-off rate of 30 dB/decade is expected when $f_m < f_c$ and 20 dB/decade for $f_m > f_c$. A higher Q_L provides lower single side band (SSB) phase noise in the region where $f_m > f_c$. Advantage of opto-electronic oscillators is that Q_L could be enhanced by increasing the fiber delay length.

An opto-electronic oscillator with fiber delay line of 1 km is considered for achieving high loaded quality factor. Phase noise of OEO with SIL is simulated and depicted in Figure F-17, where the phase noise of a standard OEO and SIL OEO are depicted with various feedback delays for $\rho = 0.0316$. The phase noise of this standard OEO is shown in black dashed curve; other colored curves show the phase noise of SIL OEO with different optical delays in the feedback loop. The simulated phase noise is the lowest in the case of 8 km delay. Phase noise performance for OEO with 8 km SIL delay remains the same under injection strengths of 0.00316, 0.01, and 0.0316. The spikes that appear in Figure F-17 are the poles associated with the transfer functions of different delays, and they may not represent the actual location and level of the spurious signals.

F-3-3 Experimental Verification of Self-Injection Locked (SIL) Oscillators

The block diagram for standard OEO configuration is depicted in the dashed black box of Figure F-18, where the metallic resonant cavity is employed as a narrowband bandpass filter. Two low-noise amplifiers (LNA) and two power amplifiers (Amp) are used to compensate for the RF signal loss in the MZM link. The power amplifiers employed here have very high 1 dB compression points to achieve higher oscillator output power while in the current form of the OEO a 1 dB compression is experienced in MZM at a lower power level than the power amplifiers. Hence the saturation is due to the MZM but not the amplifiers. The fiber optic delay line of 1 km long is selected for the OEO and the RF filtering is performed using the metallic cylindrical resonant cavity with unloaded Q of 2500. The measured oscillation is at 10 GHz and output power of this standard OEO is 16 dBm. Phase noise performance for this standard OEO is shown in the black curve in Figure F-18. The measured phase noise is −83 and −109 dBc/Hz at 1 and 10 kHz offset, respectively. The black diamond shows the actual location of the first spurious signal at 197 kHz offset and the level is −40 dBc.

The block diagram of SIL OEO is also depicted in Figure F-18. The output of the MZM is split into two parts; one passes through a 1 km delay and another passes through a longer delay and a 10 dB optical attenuator. The

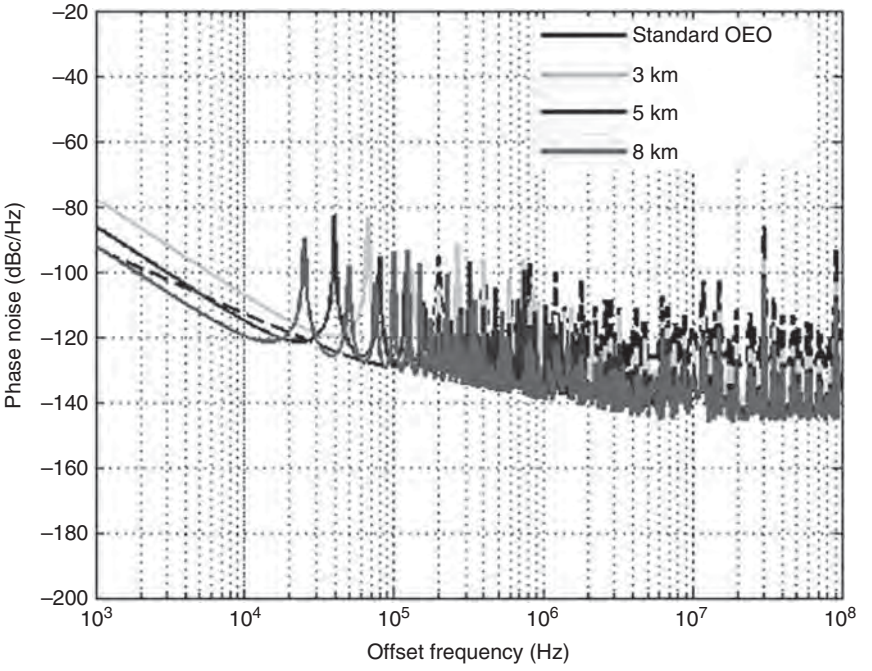


Figure F-17 Simulated phase noise of a standard OEO realized using a 1 km long fiber delay without (Black: standard OEO) and with SIL (Light gray: standard OEO with 3 km SIL; Dark gray: standard OEO with 5 km SIL; Gray: standard OEO with 8 km SIL). The SIL is accomplished for injection ratio of $\rho = 0.0316$ for different fiber delay lengths. ($P_S = 16$ dBm, fiber optic link NF = 60 dB, $P_N = -114$ dBm) [83, 84, 122].

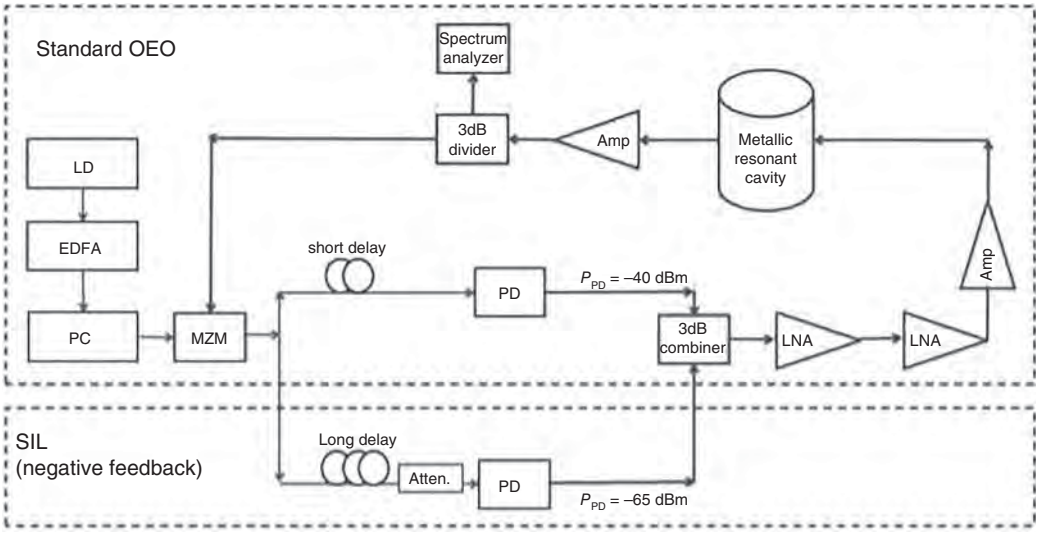


Figure F-18 System block diagram of 1 km long standard OEO with SIL using various fiber delay lengths. Optical attenuation provided by block of "Atten." assures a negative feedback using the longer delay and the 10 dB optical attenuation results in $\rho \approx 0.06$ [83, 84, 122].

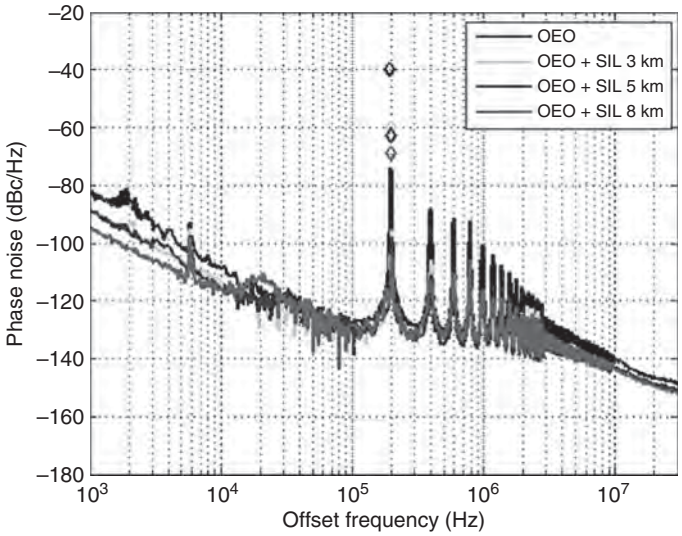


Figure F-19 Experimental measurement results of SSB phase noise of a standard OEO (Black: standard 1 km OEO) with various SIL lengths (Light gray: 3 km; Dark gray: 5 km; Gray: 8 km) and spurious signal levels (Black diamond: 196,627 Hz, −40 dBc; Light gray diamond: 199,645 Hz, −60 dBc; Dark gray: Diamond: 200,485 Hz, −63 dBc; Gray diamond: 201,002 Hz, −69 dBc). The OEO electrical characteristics are $P_S = 16$ dBm, $P_N = -114$ dBm, and NF = 60 dB [83, 84, 122].

RF gain is sufficient to compensate for the loss in the 1 km loop, but not the second delay; hence optoelectronic oscillation will take place in the 1 km loop and not at the longer delay. Because of the optical attenuator, the longer delay will not get enough gain to oscillate thus it forms a SIL to the OEO. Phase noise for SIL OEO is shown in Figure F-19 for various long delays. Delays of 3, 5 and 8 km are selected, and the lowest phase noise is achieved using an 8 km delay as predicted at levels of −96 dBc/Hz at 1 kHz offset (13 dB lower than standard OEO) and −118 dBc/Hz at 10 kHz offset (9 dB lower than standard OEO). The spurious level of −69 dBc for 8 km delay is also the lowest that is 29 dB lower than standard OEO.

F-3-4 Analysis of Standard Phase Locked Loop (PLL) Oscillators

In this section analysis of phase locked loop is to be presented. Let us express the input signal y_i and the output signal y_o as

$$y_i(t) = \cos(\omega t + \phi_i(t)) \tag{F-31}$$

$$y_o(t) = \cos(\omega t + \phi_o(t)) \tag{F-32}$$

The phase detector output is

$$u_1 = K_d \cos(\phi_i(t) - \phi_o(t)) \tag{F-33}$$

After the filter,

$$u_2 = f(t) * K_d \cos(\phi_i(t) - \phi_o(t)) \tag{F-34}$$

Then the relationship between the VCO output frequency and u_2 becomes

$$\frac{d(\omega t + \phi_o(t))}{dt} = \omega + K_o u_2 \tag{F-35}$$

$$\frac{d\phi_o(t)}{dt} = K_o u_2 = K_o K_d f(t) * \cos(\phi_i(t) - \phi_o(t)) \tag{F-36}$$

Now perform Laplace transform on both sides

$$s\phi_o(s) = K_o K_d F(s)(\phi_i(s) - \phi_o(s)) \tag{F-37}$$

Then we can find the transfer function of the PLL as

$$H(s) = \frac{\phi_o(s)}{\phi_i(t)} = \frac{G}{1+G} \tag{F-38}$$

where $G = \frac{K_o K_d F(s)}{s}$

From the system transfer function, we can represent the PLL system in frequency domain as shown in Figure F-20. Assuming the noise is a small perturbation to the steady state solution, thus the linearity still holds, then we can derive the overall output noise using superposition principle. Let's first find out the output noise ϕ_{n1} due to the input noise n_1. Using basic loop analysis, we have

$$\phi_{n1}(s) = -G\phi_{n1}(s) + Gn_1(s) \tag{F-39}$$

$$\phi_{n1}(s) = \frac{G}{1+G} n_1(s) = H(s)n_1(s) \tag{F-40}$$

Then the noise spectrum can be found as

$$S_{\phi_{n1}}(\omega_m) = |H(s)|^2 S_{n_1}(\omega_m) \tag{F-41}$$

Similarly, we can find the output noise ϕ_{n2} due to the VCO noise n_2 as follows

$$\phi_{n2}(s) = -G\phi_{n2}(s) + n_2(s) \tag{F-42}$$

$$\phi_{n2}(s) = \frac{1}{1+G} n_2(s) = (1 - H(s))n_2(s) \tag{F-43}$$

The noise spectrum is

$$S_{\phi_{n2}}(\omega_m) = |1 - H(s)|^2 S_{n_2}(\omega_m) \tag{F-44}$$

The overall output noise spectrum becomes

$$S_{\text{pll}}(\omega_m) = |H(s)|^2 S_{n_1}(\omega_m) + |1 - H(s)|^2 S_{n_2}(\omega_m) \tag{F-45}$$

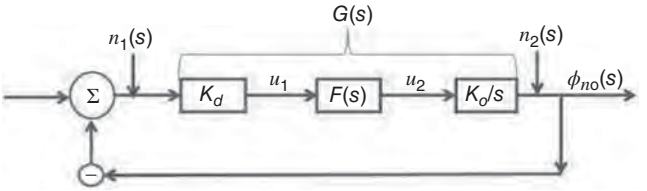


Figure F-20 Control theory representation of conventional PLL [83, 84, 122].

F-3-5 Analysis of Self Phase Locked Loop (SPLL) Oscillators

The control theory representation is shown in Figure F-21 for SPLL. A portion of the VCO output is being delayed and the phase of the delayed signal is compared against the phase of the current signal. Again, we can use superposition principle to find out the overall noise of the SPLL system. We first find out the output noise ϕ_{n1} due to the input noise n_1. Using standard loop analysis, the transfer function of output phase ϕ_{n1} is given as

$$\phi_{n1}(s) = -G\phi_{n1}(s) + e^{-s\tau_d}G\phi_{n1}(s) + Gn_1(s) \tag{F-46}$$

Rearrange Eq. (F-46) to become

$$\phi_{n1}(s) = \frac{G}{1 + G(1 - e^{-s\tau_d})}n_1(s) \tag{F-47}$$

Output noise ϕ_{n2} due to VCO noise n_2 can be found in a similar fashion as

$$\phi_{n2}(s) = \frac{1}{1 + G(1 - e^{-s\tau_d})}n_2(s) \tag{F-48}$$

Then the overall noise ϕ_{no} is given by

$$\phi_{no}(s) = \phi_{n1}(s) + \phi_{n2}(s) = \frac{G}{1 + G(1 - e^{-s\tau_d})}n_1(s) + \frac{1}{1 + G(1 - e^{-s\tau_d})}n_2(s) \tag{F-49}$$

Then the noise spectrum become

$$S_{\text{spll}}(\omega_m) = |H_a(s)|^2 S_{n_1}(\omega_m) + |H_b(s)|^2 S_{n_2}(\omega_m) \tag{F-50}$$

where

$$|H_a(s)|^2 = \frac{G}{1 + G(1 - e^{-s\tau_d})}$$
$$|H_b(s)|^2 = \frac{1}{1 + G(1 - e^{-s\tau_d})}$$

Simulation results of SPLL OEO using Eq. (F-50) is shown in Figure F-22. The black dashed curve is measured phase noise of an OEO with 100 m delay in the free-running case. Colored curves represent phase noise of OEO with SPLL for different delays. From the simulation results, phase noise decreases as the delay in SPLL increases. Simulation is also performed to investigate the impact of different filter components. In the simulation, SPLL delay is fixed at 5 km while different "Mixer Filter" boards are used. We can see from Figure F-23 that board #3 provides best phase noise reduction due to its large filter bandwidth. It should also be noted that when constructing SPLL, loop stability is of practical concern. A combination of large filter bandwidth and a long fiber delay may result in an unstable loop as the long fiber delay will introduce additional poles (side-modes) in the system (Figure F-24).

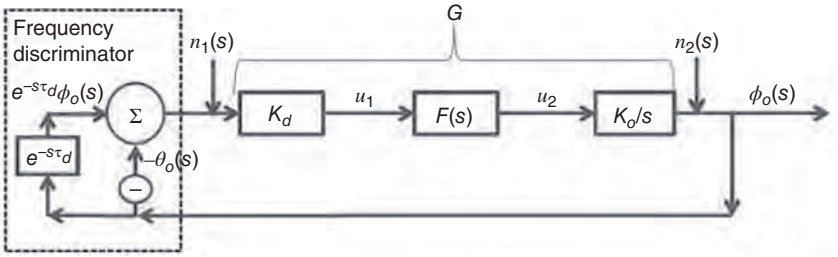


Figure F-21 Control theory representation of SPLL [83, 84, 122].

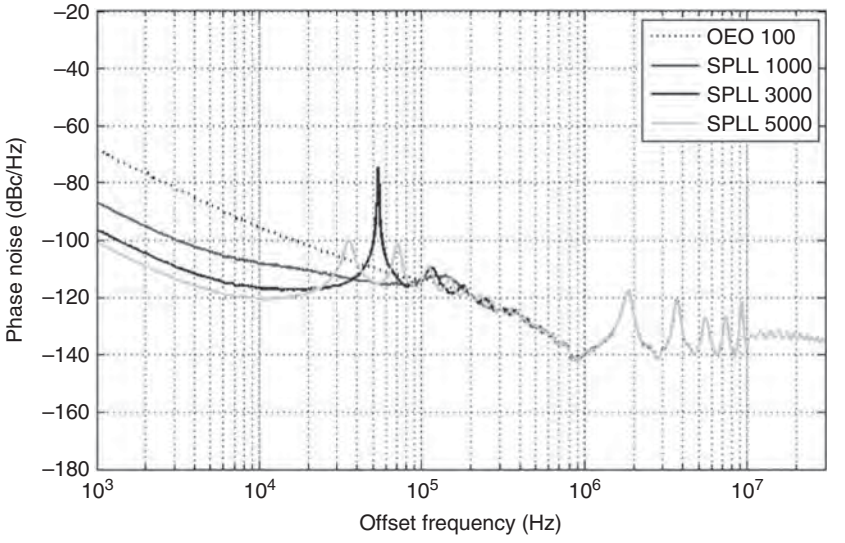


Figure F-22 Simulated phase noise of SPLL with Circuit 1 (medium loop BW) for different delays using RoF Link 2. $K_d = 0.01$ V/rad and $K_o = 2\pi \times 200$ kHz/V [83, 84, 122].

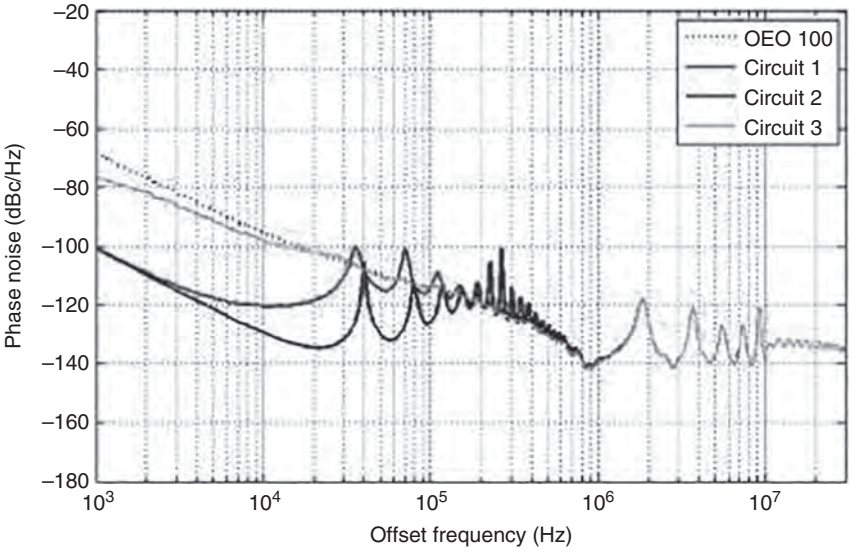


Figure F-23 Simulated phase noise of SPLL with 5 km delay for different "Mixer+LPFA" boards using RoF Link 2. $K_d = 0.01$ V/rad and $K_o = 2\pi \times 200$ kHz/V [83, 84, 122].

F-3-6 Experimental Verification of Self-Phase Locked Loop (SPLL) Oscillators

The block diagram for standard OEO configuration is depicted in the dashed black box of Figure F-25. Power amplifiers with 30 dB gain between 8.5 and 9.6 GHz from Avantek (AMT 9634) are used in blocks of "Amp1," "Amp2," and "Amp3." Moreover, the phase error signal is applied to the MZM bias port to achieve the frequency control of the OEO. The measured oscillation is at 9.6 GHz with output power of 6 dBm. Phase noise performance

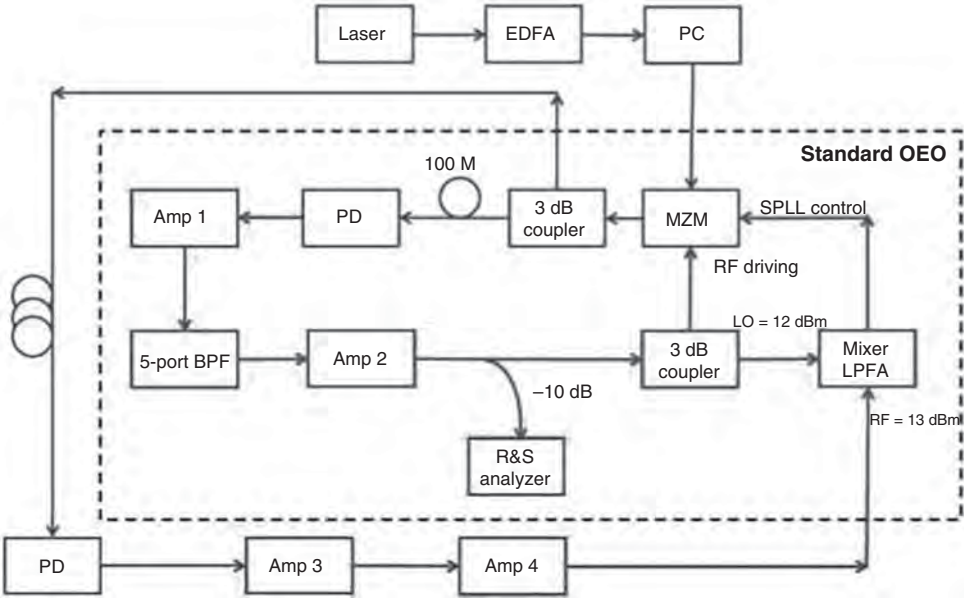


Figure F-24 Experiment setup of SPLL OEO based on MZM [83, 84, 122].

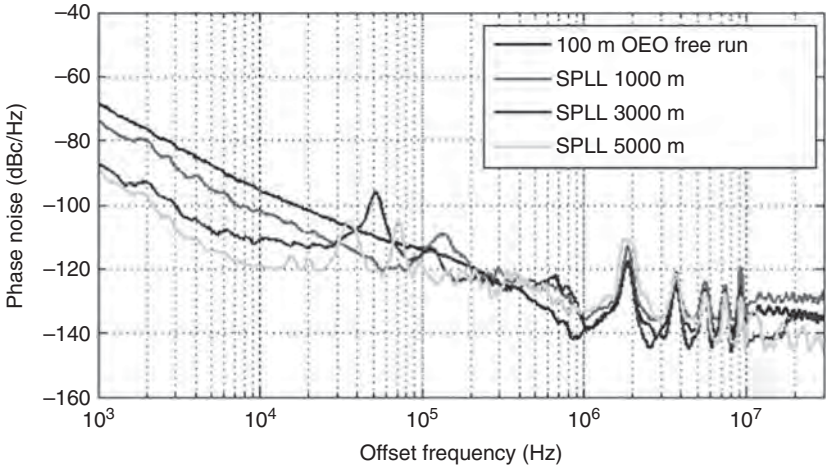


Figure F-25 Measured phase noise of SPLL with Circuit 1 (medium loop BW) for different delays using RoF Link 2. The loop parameters are $K_d = 0.01$ V/rad and $K_o = 2\pi \times 200$ kHz/V. Black curve: phase noise of free-running 100 m OEO; Gray curve: phase noise of SPLL with 1000 m delay; Dark gray curve: phase noise of SPLL with 3000 m delay; Light gray curve: phase noise of SPLL with 5000 m delay [83, 84, 122].

for this standard OEO is shown in the black curve in Figure F-25. The measured phase noise is −69 and −96 dBc/Hz at 1 and 10 kHz offset, respectively.

Experimental phase noise of SPLL OEO with MZM control is shown in Figure F-25. The phase noise reduces with the delay in SPLL increases as expected from the analytical modeling. Best result is obtained using a 5 km delay in SPLL, and the noise level is reduced by 20 dB reaching −89 dBc/Hz at 1 kHz offset and by 23 dB reaching

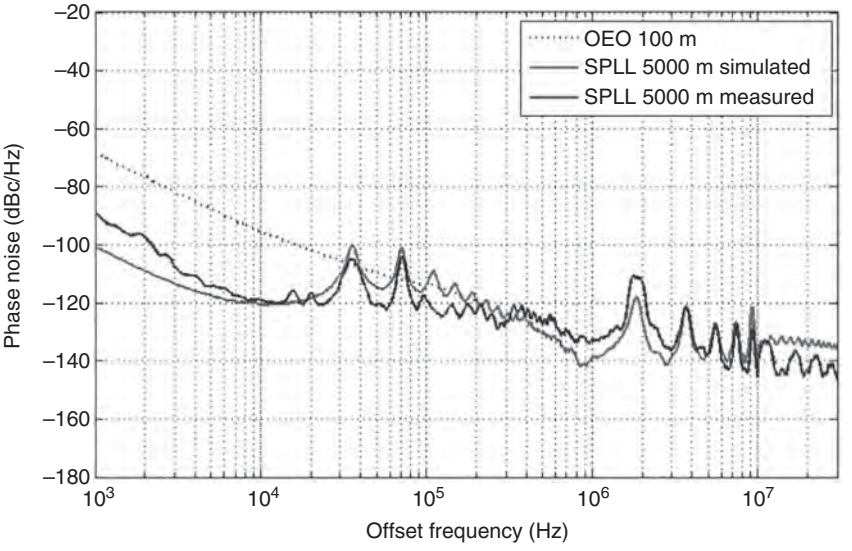


Figure F-26 Comparison of SPLL phase noise between measured and simulated. RoF Link 2 is used and the loop parameters are $K_d = 0.01$ V/rad and $K_o = 2\pi \times 200$ kHz/V [83, 84, 122].

−119 dBc/Hz at 10 kHz offset. Figure F-26 shows the excellent agreement between simulation (gray curve) and measured (dark gray curve) results of SPLL OEO using MZM control for 5 km delay.

F-3-7 Analysis of Self-Injection Locked Phase Locked Loop (SILPLL) Oscillators

Phase dynamics of IL and PLL are as follows based on Eqs. (F-17) and (F-36) respectively:

$$\frac{d\phi_o(t)}{dt} = B[\phi_i(t) - \phi_o(t)]$$
$$\frac{d\phi_o(t)}{dt} = G[\phi_i(t) - \phi_o(t)]$$

where $B = \rho\omega_{3dB}$ and $G = K_d K_v f(t)$, and K_d is the phase detector sensitivity in V/rad; K_v is the VCO tuning sensitivity in rad/V; $f(t)$ is the impulse response of the loop filter. Assume linearity still holds when the system is in locked state, the ILPLL phase dynamics can be obtained by adding IL and PLL phase dynamics as

$$\frac{d\phi_o(t)}{dt} = B[\phi_i(t) - \phi_o(t)] + G[\phi_i(t) - \phi_o(t)] \tag{F-51}$$

We can find the phase dynamics of ILPLL in the presence of noise in a similar fashion as we did in cases of IL and PLL:

$$\frac{d[\phi_o(t) + n_0(t)]}{dt} = B[\phi_i(t) + n_i(t) - \phi_o(t)] + G[\phi_i(t) + n_i(t) - \phi_o(t)] \tag{F-52}$$

Convert the Eq. (F-52) to Laplace domain, then the output phase of SILPLL due to noise can be found as

$$\phi_o = \frac{B + G}{s + B(1 - e^{-s\tau_{d_i}}) + G(1 - e^{-s\tau_{d_p}})} n_i - \frac{s}{s + B(1 - e^{-s\tau_{d_i}}) + G(1 - e^{-s\tau_{d_p}})} n_o \tag{F-53}$$

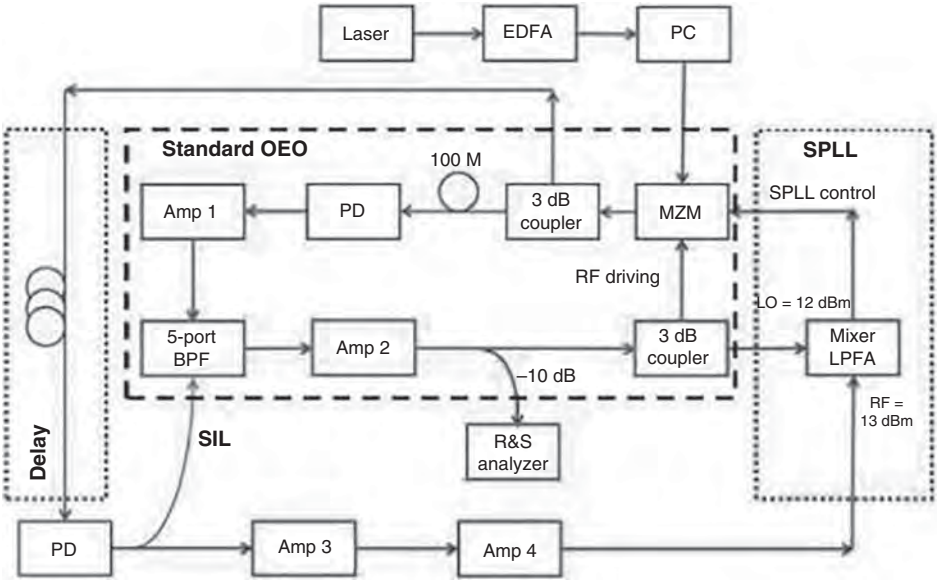


Figure F-27 Block diagram for SILPLL OEO [83, 84, 122].

Relation of $\phi_i(t) = e^{-s\tau_d}\phi_o(t)$ is used to find the Eq. (F-53). Then the power spectrum for phase of SILPLL becomes

$$S_{\phi_o} = \left|\frac{B+G}{s+B(1-e^{-s\tau_{d_i}})+G(1-e^{-s\tau_{d_p}})}\right|^2 S_{n_i} - \left|\frac{s}{s+B(1-e^{-s\tau_{d_i}})+G(1-e^{-s\tau_{d_p}})}\right|^2 S_{n_o} \tag{F-54}$$

The technique of SILPLL is applied to a standard OEO for phase noise reduction, and the experimental results are presented. The block diagram of SILPLL OEO is shown in Figure F-27, where a standard OEO with 100 m fiber delay is shown within the black dashed box. A portion of the optical signal of the OEO is coupled out and is being delay by a longer fiber of 5 km.

The delayed optical signal is converted to electrical signal by a photodetector, half of the photodetector output is sent back to the standard OEO directly to form an SIL path (shown in a light gray curve); another half is amplified and is sent to the "Mixer+LPFA" board for comparison against the non-delayed signal to generate an error signal for frequency adjustment of the OEO by changing the MZM bias voltage. The SPLL portion is shown in dark gray in Figure F-27. The measured SILPLL phase noise with 5 km delay is shown in dark gray curve of Figure F-28. The achieved phase noise is −96 dBc/Hz at 1 kHz offset and is −120 dBc/Hz at 10 kHz offset, which demonstrates a reduction of 27 and 24 dB at 1 and 10 kHz offset, respectively. Simulated phase noise of SILPLL using Eq. (F-54) is also provided as gray curve in Figure F-28, which agrees well with the measurement.

Phase noise of OEO with different frequency stabilization techniques are plotted in Figure F-29, the spot noise at 1 and 10 kHz are also tabulated in Table F-7. From the measured results, the distinction between different technologies are insignificant even though SILPLL is expected to achieve lower phase noise than SIL in the close-in to carrier offset region while maintaining same noise level of SIL in the far-out offsets. A reason for the limitation is due to the high noise level of the system and related to the PLL operation. The input power at the mixer RF port is limited, which results in a low sensitivity (estimated to be 0.01 V/rad) of the phase detector function. Also, the tuning sensitivity of OEO using MZM control is limited to 200 kHz/V at 5 V. These parameters result in a PLL loop BW of about 80 kHz, which is not sufficient to provide significant phase noise reduction.

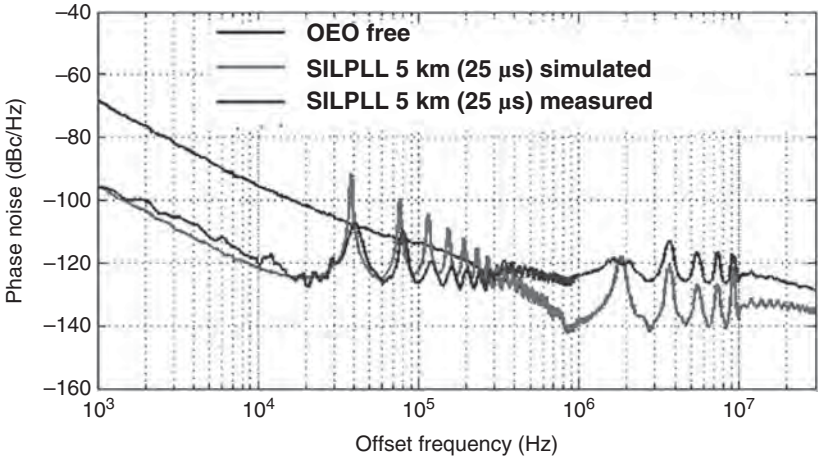


Figure F-28 SILPLL OEO phase noise for 5 km delay. Parameters for SPLL portion: $K_d = 0.01$ V/rad, $K_o = 2\pi \times 200$ kHz/V and Board #1 is used. Gray curve is simulated; dark gray is measured [83, 84, 122].

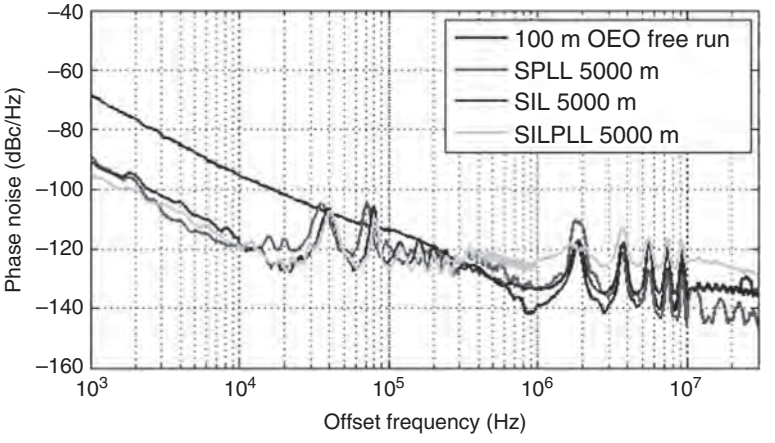


Figure F-29 Comparison for OEO with different frequency stabilization techniques [83, 84, 122].

Table F-7 Comparison of SSB phase noise for free-running OEO and SPLL OEO with band pass filter (BPF) Control.

	PN at 1 kHz (dBc/Hz)	PN at 10 kHz (dBc/Hz)
OEO free-run	−69	−96
SPLL 5 km	−89	−119
SIL 5 km	−91	−119
SILPLL 5 km	−96	−120

F-4 SILPLL BASED *X*- AND *K*-BAND FREQUENCY SYNTHESIZERS

The self-injection locking phase locking of OEO as a SILDPLL is depicted in Figure F-30, where a wavelength tunable fiber laser (TWL-C-HP-M) is used to provide wavelength control of light propagating in the OEO. The signal transmits through optical fiber to create the long fiber optic delay line. A narrow band filter is the core of reducing the number of supported modes in OEO. The classic OEO design employs a fixed frequency narrowband microwave filter (e.g. high Q aluminum cavity filter (HP X532B) [74], whispering gallery mode resonator [77], and micro-disk resonator [78]) and suffer from mechanical and thermal stability. Moreover, its fixed resonance frequency makes the design not suitable for frequency synthesis. A combination of electrically coarse tuned YIG filter (Tektronix 183-60) and optical fine-tuned optical transversal filter [66, 67] are introduced in this section to replace the role of fixed frequency high Q aluminum cavity filter [79]. A very high frequency selectivity in a small size is demonstrated using CFBG [80] in place of long fiber delay based narrowband optical transversal filter.

In addition to the highly tuned and narrowband RF filtering using optical wavelength control of the fiber laser source, SILPLL [81] is employed to provide reduction of phase noise in both close-in and far away to the carrier frequency, while enhancing the oscillation side mode suppression [82]. The block diagram of Figure F-30 simultaneously depicts both SIL and DSPLL [83, 84]; there are two paths for modulated signal after Mach-Zehnder modulator (MZM): one transmits the main loop of OEO and the other loop is split into two using as 3 and 8 km dual phase locking signal. The combined phase locking signal is then inputted to a custom designed "Mixer+LPFA" board [85]. A double-balanced mixer is integrated on this board with a low-pass filter amplifier (using Op-Amp circuits) to work as phase detector and low-pass portion of the PLL. The phase error of the OEO main loop is compared with the delayed version of oscillation signal from a dual non-harmonically related fiber delay lines as a self-phase locking loop and the phase error signal is fed back to the bias port of MZM for phase correction of oscillation signal. Self-injection locking signal takes the advantage of phase lock loop path and share the same 3 km fiber of the SPLL path to force oscillation frequency and improve the phase locked tracking and pull-in time. The high resolution and wavelength sensitive tuning is due to fine tuning of an optical transversal filter using a CFBG as dispersive component for narrowband filtering. A 19″ rack mountable frequency synthesizer at *X*-and *K*-band are fabricated, which demonstrates potential for self-contained portable box for long term reliability testing. *X*-Band operation is achieved by distinct operation at the quadrature bias point ($V_\pi/2$) of MZM, while changing bias to and

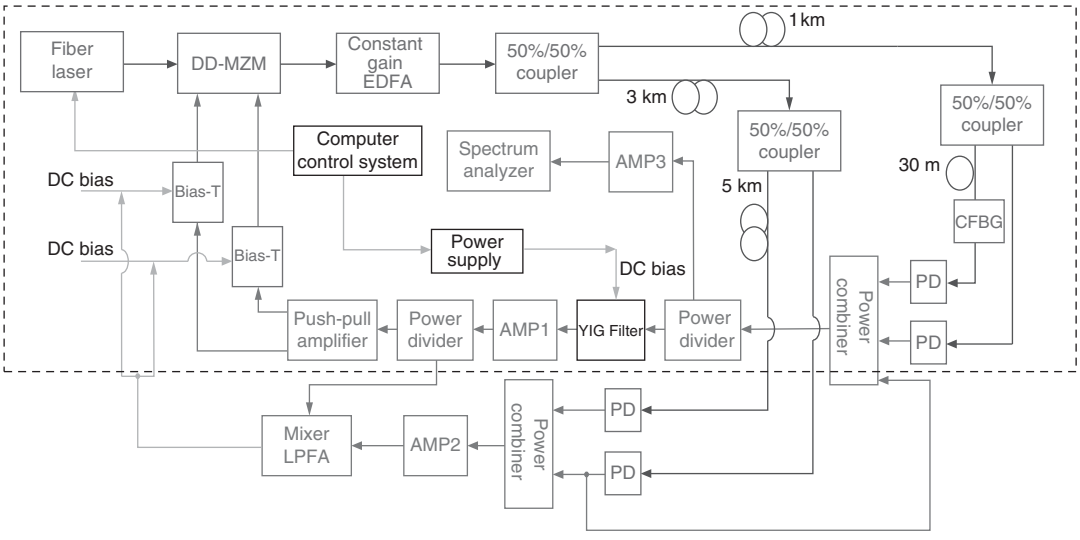


Figure F-30 Block diagram of experimentally demonstrated SILDPLL OEO system as a frequency synthesizer by employing electrically coarse tuned YIG and optically fine-tuned transversal filter using 30 m of SMF-28 or a CFBG [83, 84, 122].

highly nonlinear V_π results in second harmonic generation at *K*-band. The performance of frequency synthesizers covering 8–12 GHz (*X*-band) and 16–24 GHz (*K*-band) are discussed next.

F-4-1 *X*-Band Frequency Synthesizer

A tunable fiber laser source over *C*-band optical wavelength with low relative intensity noise (RIN) of −157 dB/Hz (TWL-C-HP-M) from Optilab. Different fiber optic delay lengths (e.g. 100, 500, and 1000 m) are employed to make comparison in terms of phase noise and side-modes, as shown in Figure F-31. This performance is a baseline performance for performance comparison to forced oscillation. Using short fiber delay line 100 m, the achieved close-in to carrier phase noise is −72 dBc/Hz at offset 1 kHz with first side-mode peak at 2000 kHz at level of −60.3 dBc; for fiber length of 500 m a close-in to carrier phase noise of −85 dBc/Hz at 1 kHz offset carrier is measured with the first side mode of 400 kHz at level of −57.5 dBc; for fiber length of 1000 m a close-in to carrier phase noise of −90 dBc/Hz at 1 kHz offset carrier is measured with the first side mode of 200 kHz at level of −55.5 dBc. The achieved results follow a 20 dB/decade roll off for fiber delay lengths before reaching offset frequency 60 kHz and there is significant phase noise reduction when longer delay line is applied. However, with increasing fiber length in the main loop, the OEO frequency will result in a larger number of side-modes inside the passband of the aluminum cavity filter and exhibit more temperature sensitivity leading to dramatic increase in the timing jitters. Therefore, an optimum length of delay is to be selected.

The forced technique of SILPLL utilize the characteristic of delayed signal to improve the phase noise performance of classic OEO that reduces the need for further increase of the fiber length of the OEO main loop, while reduces the side-mode levels. As depicted in Figure F-30, forced SILPLL technique is then applied to the 1 km OEO system in the region outside the dashed box. Using the structure depicted in Figure F-30, 3 km SIL and dual SPLL (DSPLL) of 3 and 8 km are incorporated to the OEO. In order to check the overall performance covering the whole *X*-band, the pass band of aluminum cavity filter is mechanically adjusted to 8, 10, and 12 GHz separately. The performances are similar over these frequency, as depicted in Figure F-32. The *X*-band OEO phase noise is approximately −102 dBc/Hz at 1 kHz offset and −135 dBc/Hz at 10 kHz. Moreover, the side-mode level is reduced to −120 dBc. Nonetheless, this mechanically tuned OEO is not suitable for computer control system employed in frequency synthesizers. Therefore, electronic tuning based on broadband YIG filter combined with narrowband, but periodic, optical transversal filter are explored as a viable solution.

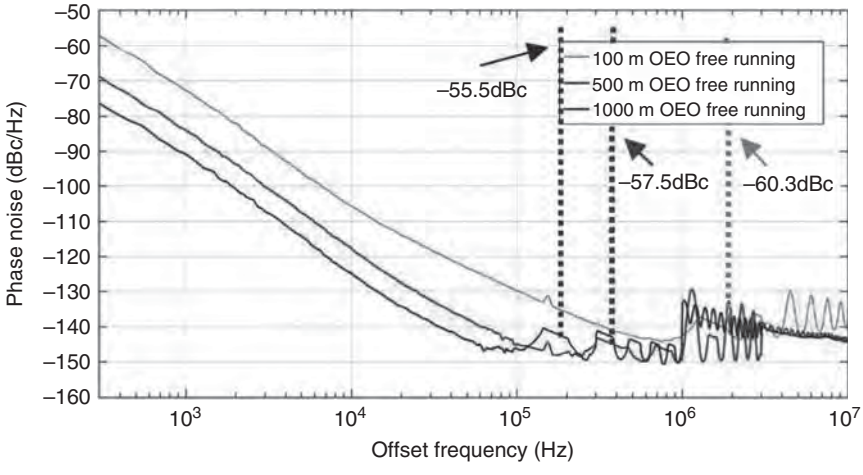


Figure F-31 Comparison of free-running 10 GHz OEO SSB phase noise performance using different delay lengths 100, 500, and 1000 m. A large number of side modes are seen in close-in to carrier for a longer fiber lengths. The closest side-mode levels in reference to carrier are indicated in the figure [83, 84, 122].

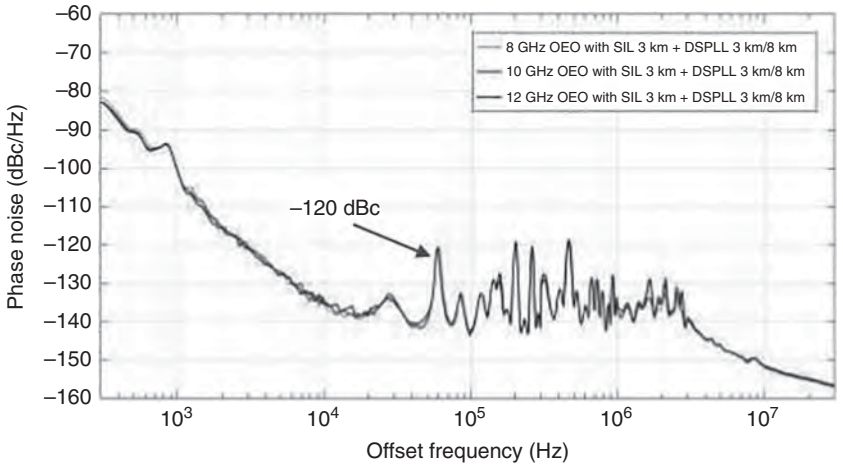


Figure F-32 Comparison of measured SSB phase noise of the forced SILPLL (3 km SIL and DSPLL of 3 and 8 km) 1000 m OEO at *X*-band [83, 84, 122].

Coarse Tunability Using YIG Filter

A YIG filter (Tektronix 183-60) is current controlled device that provides broadband tuning of 2–18 GHz, when the bias current is adjusted from 100 to 730 mA. The highest current control resolution from Agilent E3631A power supply is 1 mA working at constant current mode of about 410 mA. The coarse tuning of 25 MHz/mA [86] is measured at 10 GHz synthesizer by bias current control of YIG filter, as depicted in Figure F-33.

Fine Tunability Using Optical Transversal Filter

An optical transversal filter, as reported in [67] could provide a periodic transfer function of narrowband filtering of microwave signals. For the first-order transversal filter depicted in Figure F-34, one path is using short SMF-28 fiber as the reference path, while the other is delayed using dispersive CFBG.

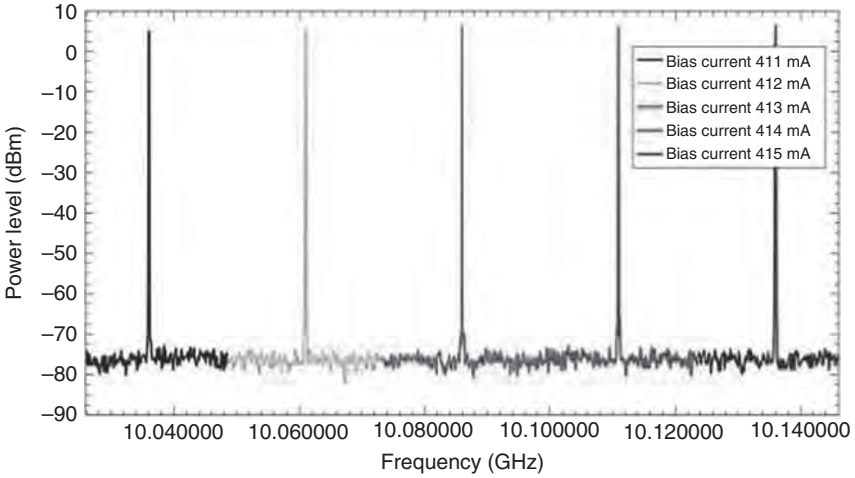


Figure F-33 Synthesizer output frequency versus YIG filter current tuning [83, 84, 122].

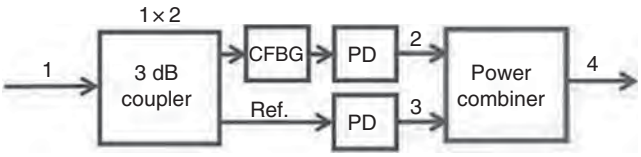


Figure F-34 First order optical transversal filter using 3 dB couplers and CFBG [83, 84, 122].

Transfer function of this filter at RF frequency is:

$$H(\omega) = 1 + \cos[\omega(\tau_d + \tau_D)]/2 \tag{F-55}$$

where τ_d is the delay difference at fiber laser wavelength. It's related to delay of the CFBG at wavelength λo. Parameter τ_D is due to wavelength dispersion characteristics of the CFBG and is expressed as:

$$\tau_D = (\Delta\lambda) \tag{F-56}$$

In Eq. (F-56), D is the dispersion parameter of CFBG in unit of ps/nm, while $\Delta\lambda$ is difference between the optical source wavelength and the original wavelength λo. The tuning performance of transversal optical filter cascaded with a commercially available YIG filter (Tektronix 183-60) is depicted in Figure F-35. Two possible dispersive CFBG structures were explored, as depicted in Figure F-36. First shown in a anodized black box is a commercial fiber Bragg grating module (Motorola DCM-20A/SCA) with the dispersion D is −150 ps/nm and delay τ_d of about 20 ns. This delay creates 40 MHz null to null pass band, which is too wide compared with high Q transversal filter needed; therefore, a 30 m of SMF-28 fiber was added to reduce passband filter and achieve a null to null bandwidth to around 4.5 MHz. Meanwhile, because of power imbalance introduced by CFBG, RF attenuator, and amplifier is required to balance output signal level in the two photodetected arms. A fine tuning sensitivity of 10 kHz/pm [70] is measured using pico-meter resolution of the fiber laser (TWL-C-HP-M). The wavelength tuning range is 40 nm, which results in an overall tuning range reaches up to 400 MHz. This fine-tuning range is much larger than 30 m SMF-28 transversal filter tuning range (1 MHz maximum) as reported in [80]; moreover, this optical transversal filter easily covers the tuning gap that exist due to the coarse tuning of 25 MHz/mA using YIG filter.

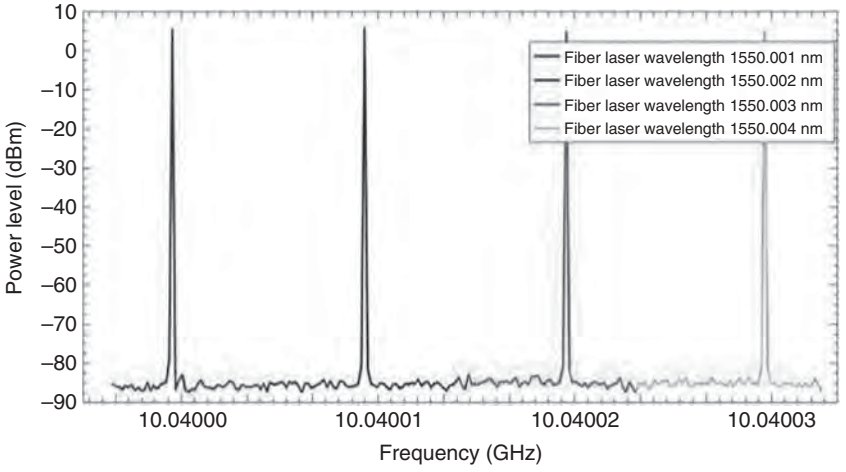


Figure F-35 The frequency synthesizer output frequency versus optical wavelength tuning using a commercial CFBG (Motorola DCM-20A/SCA) module [83, 84, 122].

Figure F-36 Physical size comparison of the Motorola CFBG as dispersion compensation module (anodized black box) with dispersive delay time of −150 ps/nm, while a custom-designed chirped fiber Bragg grating with delay of 40 ps/nm that is placed on top of this anodized box [83, 84, 122].

In order to further reduce the size for CFBG part that can fits space requirement for use in a 19″ rack-mountable SILPLL OEO box, a small size (cf. Figure F-36) custom fabricated CFBG (courtesy of Professor Jianping Yao from University of Ottawa) is employed to replace the large size commercial CFBG module. The CFBG is designed with 40 ps/nm dispersion coefficient and 10 nm effective reflection bandwidth at about 1550 nm. CFBG is still connected with 30 m SMF-28 fiber to ensure enough delay for approximately 4.5 MHz null to null bandwidth. This new optical transversal filter achieves a tuning sensitivity of 2.6 kHz/pm (cf. Figure F-37) using pico-meter wavelength tuning of the fiber laser, which is four times higher sensitivity than the Motorola module. Meantime, with designed 10 nm effective tuning range, the total tuning frequency will be 26 MHz, which is also enough to cover the YIG filter coarse tuning gap of 25 MHz. In this way, the new CFBG system takes fully advantage of the tuning ability and its tuning performance is depicted in Figure F-37.

The phase noise performance is an important measurement to quantify spectral power density of OEO based synthesizer system. However, the timing jitters is a more relevant measure to quantify clock performance. Both parameters are related and calculated from the measured close-in to carrier phase noise from Rohde and Schwarz

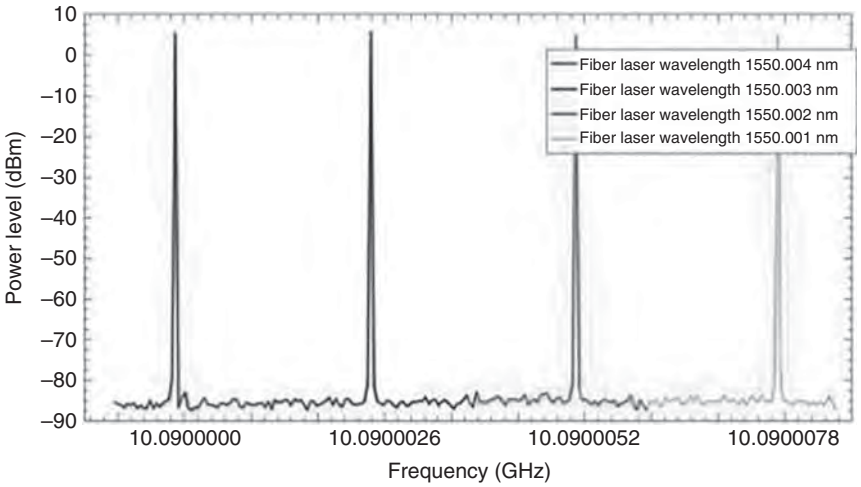


Figure F-37 The frequency synthesizer output frequency versus optical wavelength tuning using a custom designed CFBG from University of Ottawa [83, 84, 122].

(FSWP-26) RF phase noise analyzer measurement system. In the commercial CFBG module from Motorola that is used for dispersion compensation, both close in to the carrier and far to the carrier phase noise get reduction is obtained with the forced SILDPLL technique. The measured phase noise is −115 dBc/Hz at offset frequency 1 kHz and −137 dBc/Hz at offset frequency 10 kHz, as depicted in Figure. F-38. The side mode peak is also successfully suppressed using narrow band filtering of dual loop phase locked and injection-locked system for this OEO. When the custom designed CFBG is employed, the phase noise performance is somewhat similar to the Motorola module, while space saving is achieved. The measured phase noise is −115 dBc/Hz at offset frequency 1 kHz and −138 dBc/Hz at 10 kHz with a similar side mode levels, as depicted in Figure F-39.

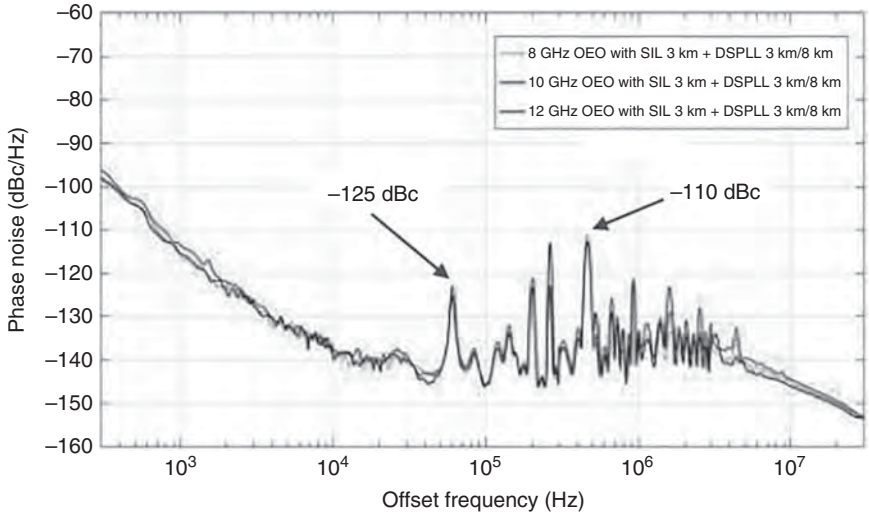


Figure F-38 *X*-Band synthesizer phase noise performance based on the Motorola CFBG module at different frequencies of 8, 10, 12 GHz. Note side-mode levels of −125 dBc at 60 kHz and −110 dBc at 450 kHz [83, 84, 122].

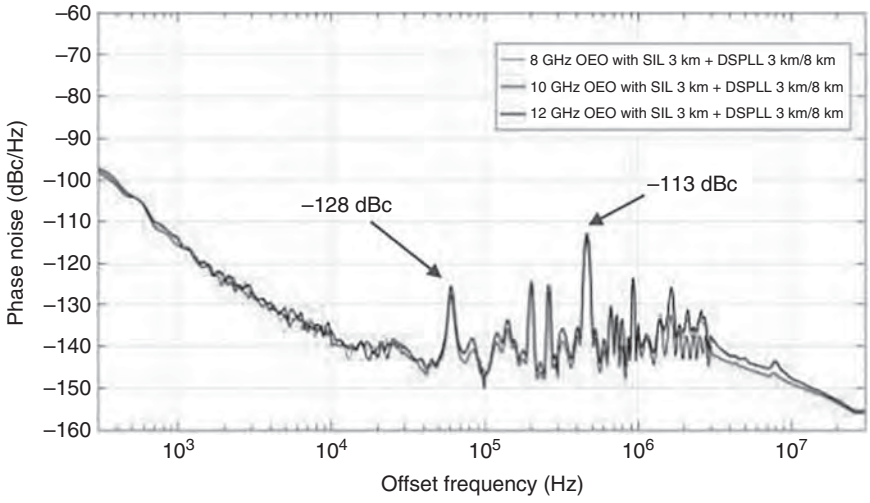


Figure F-39 *X*-Band synthesizer phase noise performance based on the custom designed CFBG at different frequencies of 8, 10, 12 GHz. Note side-mode levels of −128 dBc at 60 kHz and −113 dBc at 450 kHz [83, 84, 122].

Table F-8 Calculated timing jitter results (integrating from 300 Hz to 10 MHz) for different forced OEO configuration.

Baseline OEO	Timing jitter (fs)	SILDPLL OEO	Timing jitter (fs)
100 m/10 GHz	400.013	1000 m/8 GHz	21.041
500 m/10 GHz	100.024	1000 m/10 GHz	19.062
1000 m/10 GHz	41.685	1000 m/12 GHz	17.023
Forced OEO with Motorola module	**Timing jitter (fs)**	**Forced OEO with custom CFBG**	**Timing jitter (fs)**
1000 m/8 GHz	7.864	1000 m/8 GHz	7.755
1000 m/10 GHz	6.122	1000 m/10 GHz	6.115
1000 m/12 GHz	5.170	1000 m/12 GHz	5.170

The close-in to carrier phase noise and associated timing jitters (integrating from 300 Hz to 10 MHz) for different operation of OEO are calculated and summarized in Table F-8. Forced OEO system using 1000 m fiber delay line shows significant decrease in both phase noise and timing jitters compared with baseline OEO condition and the best condition using the custom CFBG provides 5.170 fs timing jitters at 12 GHz output.

F-4-2 19″ Rack-Mountable *K*-Band Frequency Synthesizer

The assembling detail is shown in a number of images, where step by step assembly of the whole system is performed following the block diagram of Figure F-30. Figure F-40 is the first floor level of the realized synthesizer box, where there are three fiber mandrills and a DC power supply are placed on this level. With necessary cover over the level of fiber mandrills and DC power supply, laser driver, laser, and YIG filter are secured on the top side of the cover. Their assembling is depicted in Figure F-41 using commercially available products from Optilab and Teledyne. The next level is realized by placement of the rest of the RF and fiber optic components on the sheet metal cover used on top of the second level to construct the third level assembly. The detail of various component names and positions are rendered in Figure F-42. All the RF and optical components are also properly connected using coaxial cable or optical fibers. The OEO box will then be closed using coverage metal for its front side, top side and back side that contain vent hole for power supply heat dissipation. There are also DB9 and RS232 input ports for laser source and DC power supply, which will be used for remote computer control. The front view after

Figure F-40 The placement of custom fiber mandrills and commercially available computer controlled DC power supply (Agilent E3631A) and fiber mandrills [83, 84, 122].

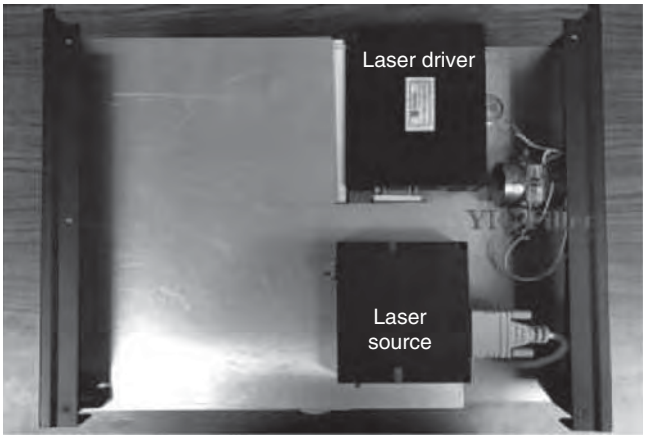


Figure F-41 The placement of fiber laser source and its driver from Optilab limited liability capability (LLC) (TWL-C-HP-M) and a commercial YIG filter (Teledyne) [83, 84, 122].

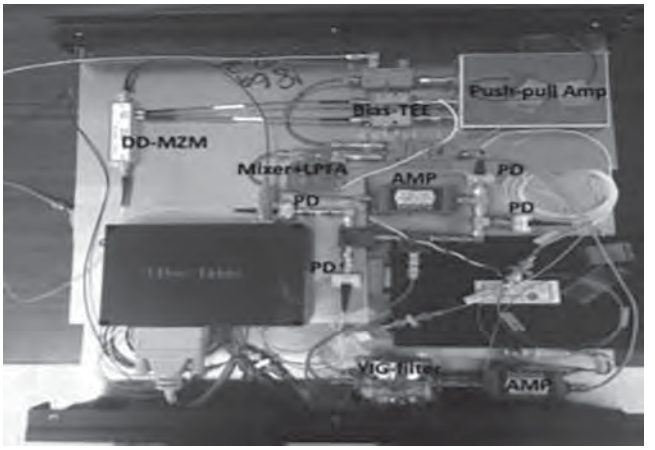


Figure F-42 The placement of RF and fiber optic components on the third level of frequency synthesizer box [83, 84, 122].

finishing RF/optical components placement is shown on Figure F-43. The overall height of the circuits is limited within the range of the box size. The last step is to secure the commercially available EDFA outside the OEO box after completing the OEO box assembly. Its final realization is shown on Figure F-44. The EDFA shares the screws with top coverage of OEO box for stabilization, so there will be very good connection between itself and OEO.

The computer control program is then developed using LabVIEW 2018. Figure F-45 is the front panel of the computer control program. The program controls the wavelength output of fiber laser and current bias of the YIG filter to realize narrowband frequency selection. For a desired operation frequency of the synthesizer, users only need to type their needs in the position of gray circle. Then, the program will iteratively change the current bias of the YIG filter and wavelength of the fiber laser using a pre-loaded look-up table, corresponding to coarse and fine tuning respectively, to rapidly reach (<15 s) to the desired frequency. A portion of time dedicated for frequency acquisition is related to iterative process till a proper YIG filter bias current and fiber laser wavelength is attained for extremely narrowband bandpass characteristics of the cascaded YIG filter and optical transversal filter. This settling time can be further reduced using custom power supply and controllers.

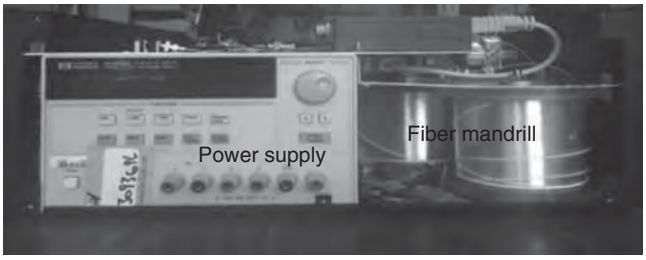


Figure F-43 Front view of different levels of OEO synthesizer box depicting commercially available power supply (Agilent E3631A) and custom fiber mandrills of 5 and 1 km long along with laser driver and modular components [83, 84, 122].

Figure F-44 Overview of the completed SILPLL OEO based source as a highly stable *K*-band frequency synthesizer [83, 84, 122].

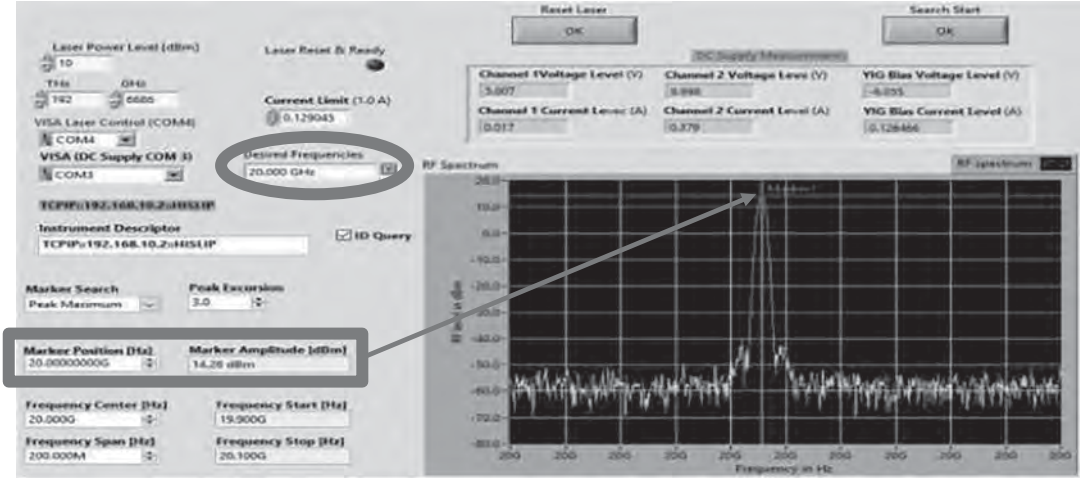


Figure F-45 Front panel of the *K*-band synthesizer LabVIEW control [83, 84, 122].

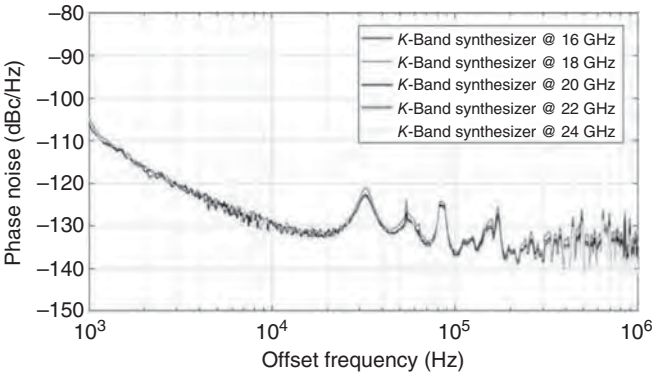


Figure F-46 Measured phase noise of *K*-band OEO in a 19″ rack-mountable box [83, 84, 122].

The measured phase noise of the OEO system is depicted in Figure F-46, where the synthesizer outputs are measured at a frequency step of 2 GHz-starting from 16 to 24 GHz for whole *K*-band operation. The measured phase noise level is −105 dBc/Hz at offset frequency of 1 kHz and −130 dBc/Hz at offset frequency of 10 kHz. The long-term stability condition of the 19″ rack-mountable box is also evaluated, where a 4.5 kHz synthesized frequency shift is recorded over one hour. The estimated rms timing jitters of this synthesizer is under 10 fs, which can be even further reduced using self-injection locked triple phase-lock loop (SILTPLL) [87, 88]. Part of this phase noise is due to 1/*f* noise characteristics of amplifier used. This performance could be improved using Si-Ge based hetrojunction bipolar transistor (HBT) amplifiers in place of GaAs based p-HEMT [89, 90] and proper selection of operation condition of transistor amplifiers [91].

Computer control of this *K*-band frequency synthesizer is also demonstrated by generating appropriate frequencies for a number of practical applications. In Figure F-47 a linear frequency modulation is produced for practical FM-CW radar applications using LabVIEW. The program is designed to have frequency starting from 17 GHz with six linear steps of frequency increase to 19 GHz and then dropping at the same rate back to 17 GHz. In Figure F-48, a pseudo-random frequency hopped pattern is generated to depict broadband frequency shift for frequency hopped communication systems. The pattern selected to demonstrate complete frequency hopped results is designed to

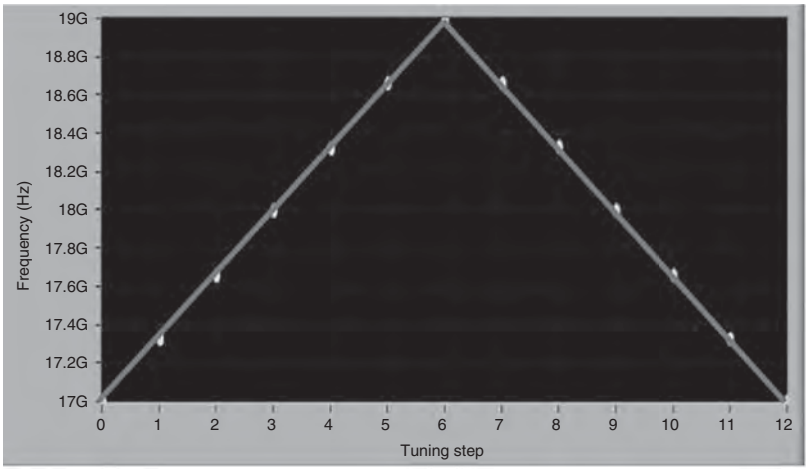


Figure F-47 Linear frequency sweep output using LabVIEW based computer control program. White dots are selected frequencies and gray lines shows the generated pattern linearly modulated frequencies of FM-CW pattern [83, 84, 122].

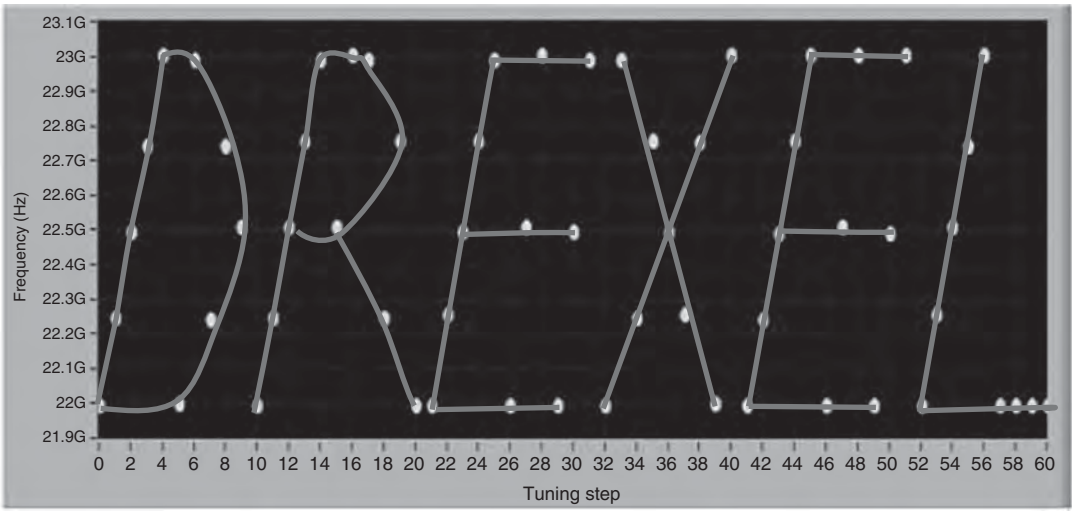


Figure F-48 Complete frequency hopped results showing "DREXEL" using 60 running steps. White dots are hopped frequencies and gray lines shows the generated pattern for a more clarified code [83, 84, 122].

Table F-9 Performance of *X*-band and *K*-band frequency synthesizers using novel concept of SILPLL OEO.

Frequency tuning range	8–12 GHz	16–24 GHz
Accuracy (computer control)	<10 kHz	<20 kHz
Accuracy (manual control)	<35 Hz	<70 Hz
RF output power	>14 dBm	>10 dBm
SSB phase noise	−109.97 dBc/Hz @ 1 kHz −136.45 dBc/Hz @ 10 kHz −141.91 dBc/Hz @ 100 kHz −143.66 dBc/Hz @ 10 MHz	−102.30 dBc/Hz @ 1 kHz −127.37 dBc/Hz @ 10 kHz −133.16 dBc/Hz @ 100 kHz −140.67 dBc/Hz @ 10 MHz
Timing jitter (300 Hz–10 MHz)	8.5 *fs*	11 *fs*
Side-mode levels (300 Hz–10 MHz)	<−100 dBc	<−100 dBc
Short-term stability	±0.15 ppm (60 min)	±0.15 ppm (60 min)
Prime power consumption	20 W	20 W
Package size	19″ × 14″ × 9″	19″ × 14″ × 9″
Package weight	<30 lb	<30 lb
Output connector	SMA (F)	SMA (F)

show the wording for "DREXEL" after 61 running steps. This final output demonstrates frequency synthesizer tuning while maintaining the demonstrated low close-in to carrier phase noise with a computer controlled output frequency selection. The summary of results for the *X*- and *K*-band OEO frequency synthesizers is listed in Table F-9.

A modular performance is attractive due to individual component optimization, however, this solution is not cost effective. Even though the new revised solution provides significantly size reduction; however, because of the limits of optical fiber mandrills and complex electrical circuits, there is no further reduction is to reach unless an integrated solution is pursued. Meantime, the frequency limits of RF modular components also affect performance above 60 GHz frequency. An ideal realization of high frequency synthesizer beyond 24 GHz will rely on realization of opto-electronics on Si-photonics as an integrated design.

F-5 INTEGRATED OEO REALIZATION USING SI-PHOTONICS

First approach integrated OEO is based on design implementation using hybrid integrated SILPLL system [91] using EO-polymer based optical modulators. To avoid the bias dependent characteristics of MZM, an optical phase modulation (PM) based design [92] is considered using Si-photonics technique, which is compatible with Si-Ge Bi-CMOS high-speed integrated electronics processes. The detail structure of the proposed phase modulator with 1 cm interaction length design topology is shown in Figure F-49. CPO-1/PMMI guest–host system (20 wt%) is used as the optical core material, and it has a refractive index of $n_o = 1.63$ and a conservative EO coefficient of $r_{e0} = 70$ pm/V at 1550 nm. Norland Optical Adhesive 65 (NOA65) is selected as cladding material with a refractive index of $n = 1.51$, a loss tangent of tan $\delta = 2.2 \times 10^{-2}$. The geometrical dimensions are calculated by high frequency structure simulator (HFSS) and optical beam propagation methods (Opti BPM) to achieve 50 Ω characteristic impedance for the in-plane common mode sense (CMS) electrodes [92]. Design requirements are for bandwidth of at least 20 GHz.

To enhance the modulation efficiency, a slowlight 1D PhC structure with lattice constant of 470 nm consisting of a base material of PMMI with a substrate width 47 nm of air gaps is placed close to the optical core as a superstrate shown in Figure F-49. The dispersive characteristic of the propagating light inside the optical core is affected by the slowlight effect, as depicted in Figure F-50. Such effect is maximized when the PhC layer touches the optical core, but the optical loss is significant as a side-effect. Moreover, the dispersive effect gets stronger as the PhC layer thickens at the cost of increased optical loss.

A combination of h_{buffer} of 0.6 μm and h_{PhC} of 0.2 μm thus represents a compromise between thickness of the buffer layer and height of the PhC layer, and the modulator figure of merit $V_\pi \times L$ and optical loss are then simulated in an optical commercial simulator, OptiBPM by approximately 3 dB/cm and 3 V cm, respectively. Compare to a $V_\pi \times L$ of 7.2 V cm for a PM without PhC layer, the half-voltage magnitude is over 100% improved. The detail structure of the proposed phase modulator with 1 cm interaction length design topology uses CPO-1/PMMI guest-host system (20 wt%) is used as the optical core material, and it has a refractive index of $n_o = 1.63$ and a conservative EO coefficient of $r_{e0} = 70$ pm/V at 1550 nm. Norland Optical Adhesive 65 (NOA65) is selected as cladding material with a refractive index of $n = 1.51$, a loss tangent of tan $\delta = 2.2 \times 10^{-2}$ [23]. The geometrical dimensions are calculated to achieve 50 Ω characteristic impedance for the in-plane CMS electrodes [92].

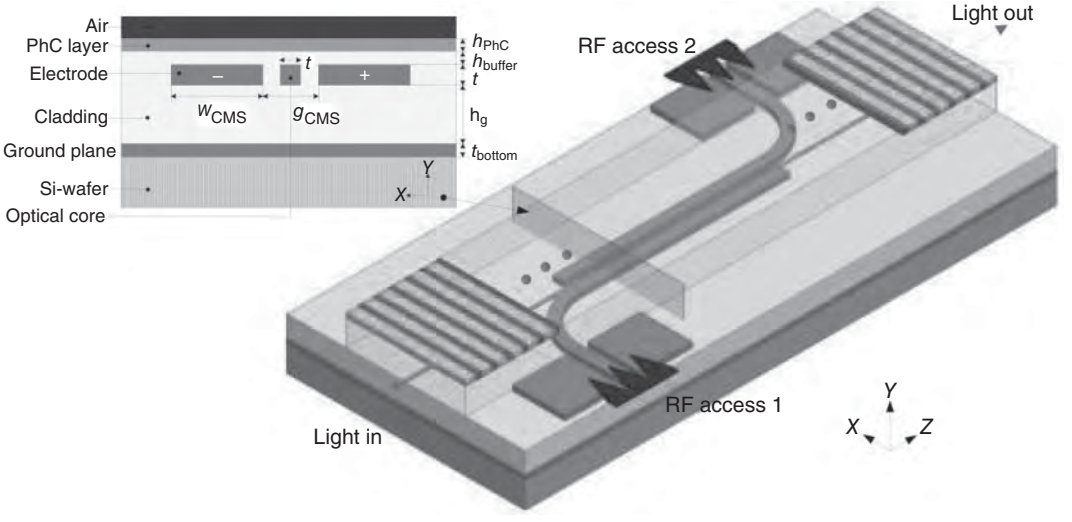


Figure F-49 Conceptual overview of electro-optic PM with integrated 1D PhC that is driven by in-plane CMS electrodes. The parameters shown are $t = 1.6$ μm, $W_{CMS} = 94$ μm, $g_{CMS} = 10$ μm, $h_g = 40$ μm, $t_{bottom} = 0.2$ μm, $h_{PhC} = 0.6$ μm, and $h_{buffer} = 0.2$ μm [83, 84, 122].

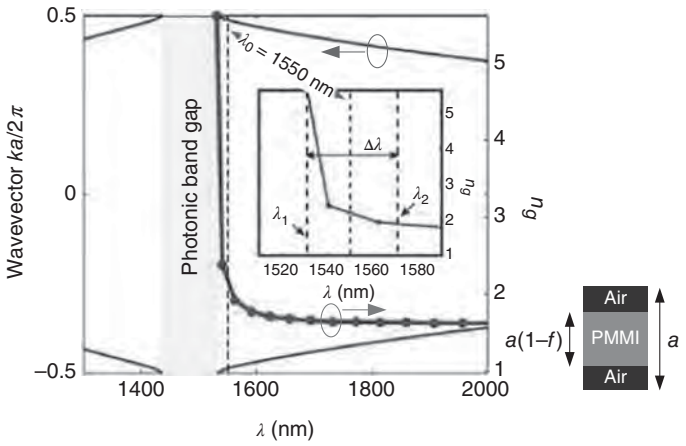


Figure F-50 Photonic band structure and group index versus wavelength for lattice constant $a = 470$ nm and filling fraction $f = 0.1$. The other parameters are $\lambda_1 = 1530$ nm, $\lambda_2 = 1570$ nm and $\Delta\lambda = 40$ nm [83, 84, 122].

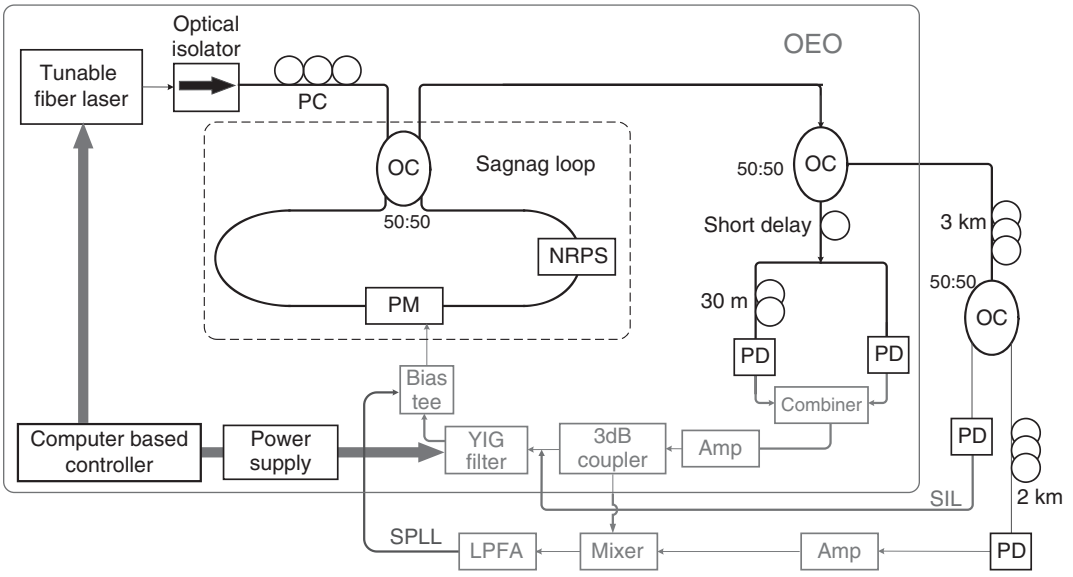


Figure F-51 Block diagram of PM based SILPLL K-band OEO synthesizers in light gray dashed box with Sagnac loop in black dashed box and optical/RF paths in dark gray/gray, SPLL/SIL in dark gray/light gray [83, 84, 122].

The realization of SILPLL based OEO is based on a Sagnac loop, as shown in Figure F-51, where the input light coming from the tunable laser source is fed into an optical coupler (OC) and equally divided into clockwise (CW) and coherent continuous wave (CCW) paths around the loop. Both CW and CCW signals propagate through the PM and then travel around the other half of the loop, where only CCW propagating signal is phase shifted by non-reciprocal phase shifter (NRPS) because of the polarization controller (PC). Our simulated phase noise performance is better than −148 dBc/Hz at 10 kHz offset using SILPLL technique, as depicted in Table F-10.

Table F-10 SSB phase noise of Sagnac loop based SILPLL OEO at 20 GHz for various PM with different values of $V\pi$ and IL.

Phase noise (dBc/Hz)	$V_\pi = 1.38$ V IL = 5 dB	$V_\pi = 5$ V IL = 3 dB	$V_\pi = 3$ V IL = 3 dB
1 kHz offset	−120.7	−120.2	−120.5
10 kHz offset	−148.2	−145.0	−147.0

F-6 COMPACT OEO USING InP MULTI-MODE SEMICONDUCTOR LASER

Further direction of developing a compact size OEO at RF oscillator relies on chip level integration of dual mode lasers [93, 94], using lasers with external cavity [95, 96], and Si-photonics based integrated semiconductor laser [97]. There are two major methods for semiconductor laser based structures of using beatnotes of two symmetric lasers output [98, 99] while another utilize inter-modal operation of multi-mode lasers [100–103]. The former method usually targets at hundreds of GHz range benefiting from high optical frequency [98]. Meantime, its linewidth is very poor, which is around tens of megahertz [98, 99]. On the other hand, second method using inter-modal output of multi-mode semiconductor laser usually targets efficiently at tens of GHz frequency range. Its performance using different locking methods are reported in [100–108] with maximum output frequency less than 40 GHz. However, in these publications, the performance of semiconductor laser inter-modal RF oscillation all depends on the purity of the external RF reference, as the RF free-running inter-modal oscillation signal has poor frequency stability.

F-6-1 Structure of Multi-mode InP Laser

A distributed Bragg reflector (DBR) based multi-mode multi-section semiconductor laser is considered for RF output generation without utilizing any external reference; its design diagram is shown in Figure F-52, using different optical components from shared InP wafer run of SmartPhotonics foundry service (https://smartphotonics.nl/). There are four major sections of gain medium (SOA), PM, filtering DBR, and electro-absorption modulator (EAM) sections [109]. The SOA is fabricated by multi quantum well InGaAs/InP structure for operation at 1550 nm. The front and back DBR is functioned as reflection mirror filter [110] to form laser cavity, which its bandwidth affects the effective number of output modes in the multi-mode laser. For frequency tuning of RF signal output, material index variation of PM section [111] is employed using electro-optic property of InP by static bias condition variations. Meantime, its dynamic modulation plays an important role in phase locking process of RF signal over 50 MHz of bandwidth. Last, the EAM section outside the laser cavity controls laser modes by shifting edge of wavelength dependent absorption rate. The output of the laser is monitored in an optical spectrum analyzer and its intermodal oscillations are detected using an external high-speed photodetector (Discovery Semiconductor DSC50S) and displayed on RF phase noise analyzer. Besides the compact multi-mode laser chip design, novel forced technique of self-injection locking [74] and self-phase locking [112] are also employed in this paper for further reduction of the output phase noise and improving inter-modal oscillation frequency stability. Moreover, optimized delay line using SILTPLL [88] is achieved with reported best phase noise performance without any external reference.

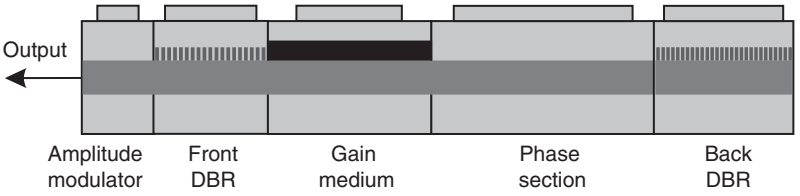


Figure F-52 Block diagram of inter-modal laser based RF synthesizer on a microchip structure [83, 84, 122].

F-6-2 Multi-mode Laser and Inter-Modal RF Oscillation

The design detail of multi-mode semiconductor DBR laser is shown in Figure F-53. The length of DBR back mirror and DBR front mirror is 600 and 200 μm separately. Phase section length is designed with 1250 μm while SOA is 800 μm. Different section is connected by shallow etched waveguide to form the complete laser cavity. The total cavity length (including connecting waveguide) of approximately about 4000 μm corresponds to an intermodal oscillation frequency of about 11.5 GHz for multi-modes that are supported under 80 GHz gain spectra of SOA. The external EAM has a length of 200 μm and is used for optical amplitude control and suppression of various modes. The electrical wiring connections are also placed on the chip to provide DC biasing for SOA, PM, and EAM. A ground (GND) pad is connected with via hole for ground access on the chip surface.

The microchip placement on a temperature controlled environment is depicted in Figure F-54 for static and dynamic optical characterization, where mechanical probe-stations support electrical microprobe to provide necessary electrical (DC/RF) input and optical lensed fiber holder to collect optical output. A copper sheet is placed under the custom designed microchip and mounted on a Peltier cooler for maintaining 20 °C temperature throughout test environment using a thermistor and temperature controller (Thorlabs TED8040) with temperature fluctuation of ±0.2 °C. The optical output of this laser under test is monitored on optical spectrum analyzer (Agilent MS9710C) through lensed fiber, optical coupler, and then photodiode to monitor RF characteristics. The PM bias and EAM bias is kept initially at 0.0 V for initial performance measurement and static characterization. The measured test results of the integrated laser are shown in Table F-11, where there are five dominant modes existing in multi-mode

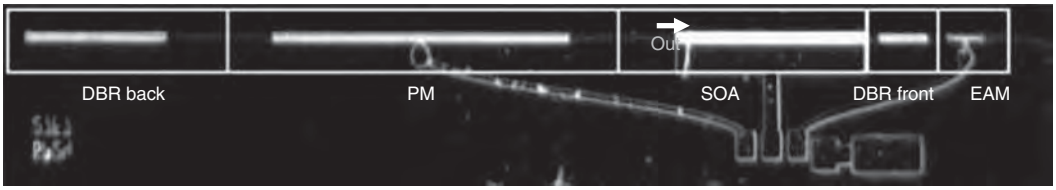


Figure F-53 Fabricated DBR based multi-mode multi-section semiconductor laser on InP chip using SmartPhotonics foundry (https://smartphotonics.nl) [83, 84, 122].

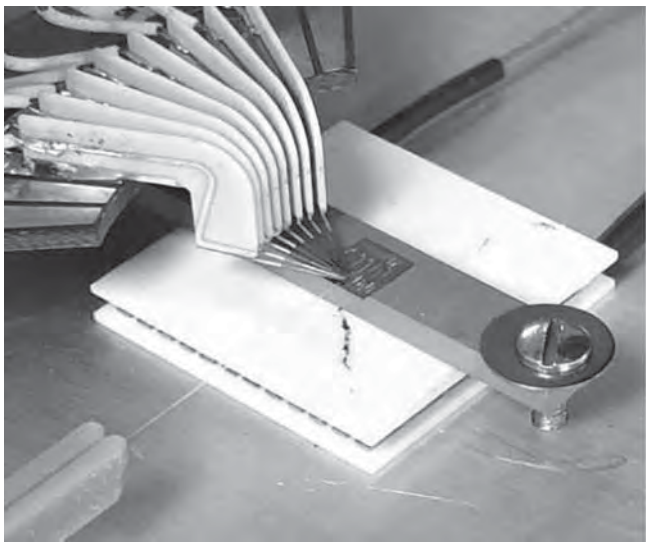


Figure F-54 Testing environment of the DBR based multi-mode multi-section semiconductor laser [83, 84, 122].

Table F-11 Multi-mode laser output wavelength and related power level.

Output modes	Wavelength (nm)	Power level (dBm)
1	1550.648	−30.1
2	1550.747	−21.3
3	1550.847	−12.3
4	1550.950	−19.5
5	1551.050	−36.2

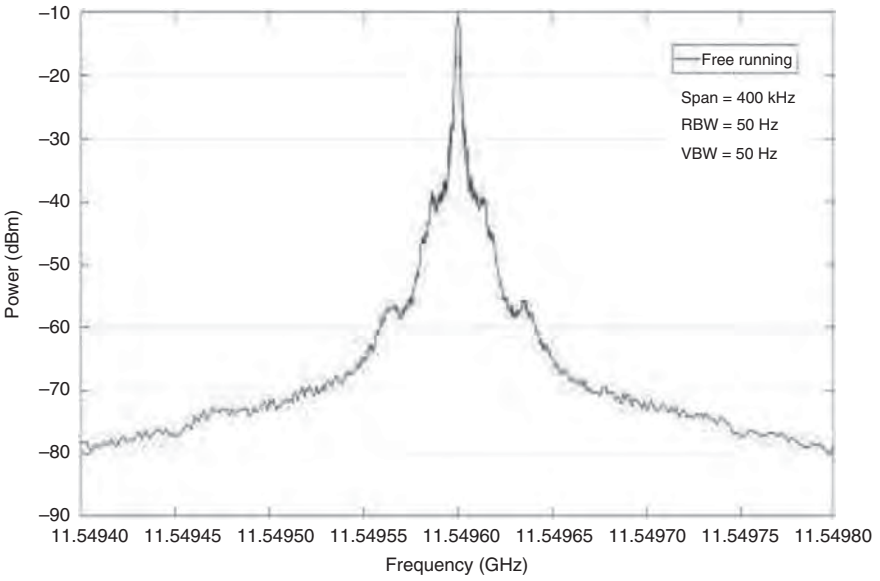


Figure F-55 Free-running performance of inter-modal RF output: center frequency of 11.5496 GHz with output power of −10.59 dBm, frequency span of 400 kHz, resolution bandwidth (RBW) of 50 Hz and video bandwidth (VBW) of 50 Hz [83, 84, 122].

laser operation. The measured optical output power for the fundamental mode is around −12 dBm at 1550.85 nm, when SOA injection current is 80 mA. The mode gap between each mode is around 11.5 GHz, which matches well with estimated effective cavity length of 13.065 mm. Free-running measurement of inter-modal output around 11.5 GHz is depicted in Figure F-55. The detected RF output power is about −10.59 dBm at 11.5496 GHz for SOA bias current of 80 mA and 0.0 V bias voltages applied to PM and EAM sections. The spectral purity of intermodal oscillation is studied here and key performance is close-in to carrier phase noise and its related timing jitters. Measured close-in to carrier phase noise is depicted in Figure F-56, where a poor phase noise of −5 dBc/Hz at offset 1 kHz and −30 dBc/Hz at 10 kHz offset is recorded for the free-running inter-modal oscillation frequency. The max hold operation for 10 min on this signal shows up to 30 MHz center frequency shift. The estimated timing jitter of this oscillator is 266.1 ps for 1 kHz–1 MHz offset carrier frequencies.

The inter-modal RF frequency is tuned, when different DC injection voltage is applied to the PM section (cf. Figure F-53). The applied bias of −5.0 to +1.0 V to the PM section changes the index of refraction in the optical waveguide portion, causes a phase shift of 20–17.5°/mm respectively, and changes the effective laser cavity length of the multi-section laser. The achieved phase shift and eventual change in the cavity length causes shift in the inert-modal oscillation frequency (i.e. adjusting mode gap) within multi-mode laser operation. Besides the static

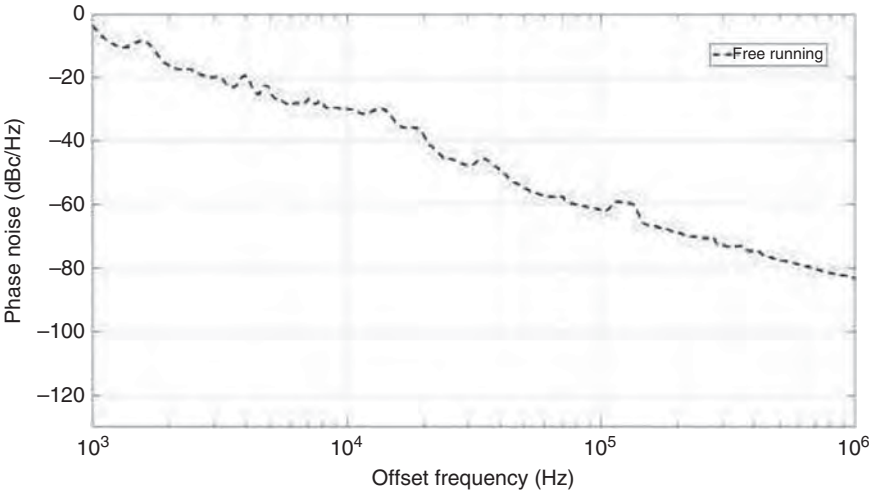


Figure F-56 Close-in to carrier phase noise over 1 kHz–1 MHz offset carrier frequency. A time averaging of 10 is used [83, 84, 122].

Table F-12 PM tuning sensitivity and RF output frequency versus DC bias of DBR laser PM section.

DC bias of PM (V)	Output frequency (GHz)	PM sensitivity (MHz/V)
−5.0	12.2725	189.5
−4.5	12.1827	179.5
−4.0	12.0975	170.3
−3.5	12.0159	163.2
−3.0	11.9382	155.3
−2.5	11.8647	147.0
−2.0	11.7949	139.5
−1.5	11.7288	132.1
−1.0	11.6659	125.8
−0.5	11.6062	119.4
0.0	11.5496	113.2
+0.5	11.4964	106.4
+1.0	11.4462	100.3

optical performance measurements, phase section tuning sensitivity is then measured for various PM biasing conditions. Table F-12 summarizes the precise inter-modal results related to PM bias, which is over 800 MHz at *X*-band with an average frequency tuning sensitivity of around 150 MHz/V. This achieved tuning range and sensitivity is among the best reported compared to other techniques and is significantly larger than conventional RF VCO tuning sensitivity [113].

F-6-3 Self-Forced Frequency Stabilizations

The test setup diagram of self-injection locking is depicted in Figure F-57, where the instantaneous laser output is amplified using a constant gain EDFA, delayed (25 μs using 5 km fiber), and fed back to laser through an optical circulator. A tunable optical attenuator is placed before an optical circulator port for evaluating dynamic performance by adjusting optical injection power levels that are verified using optical power meter (EXFO FPM-600). There is

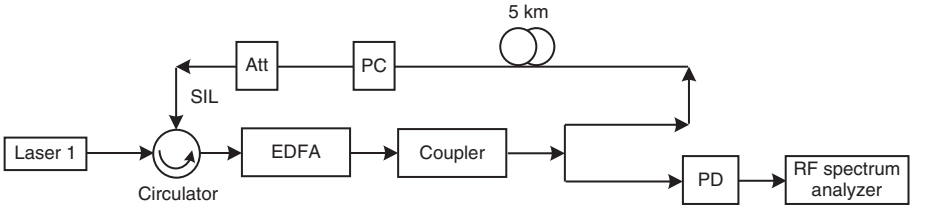


Figure F-57 Block diagram of self-injection locking system [83, 84, 122].

a PC after optical delay line in order to provide high efficiency optical injection signal to the optical waveguide. The inter-modal RF oscillation is measured using RF phase noise analyzer (Rohde-Schwarz FSWP-26).

Phase noise performance comparison of free-running intermodal oscillation with SIL under various injected optical levels are presented in Figure F-58a, where significant reduction in phase noise is observed with $P_{\text{inj}}/P_o = 0.3$ ratio (i.e. SIL power of −10 dBm after optical attenuator, the coupling loss of lensed fiber to waveguide is 6 dB). It provides the best phase noise performance among other situations with level of −40 dBc/Hz (i.e. 35 dB reduction with free running) at 1 kHz offset and −80 dBc/Hz (50 dB reductions with free running) at 10 kHz. On the other hand, phase noise performances of forced SIL are also compared in Figure F-58b in order to quantify the best optical delay length. Nonetheless, 5 km delay lines provides the best phase noise performance using optimized power injection power ratio among several different delay lines. Meantime, the best achieved timing jitter is 5.17 ps which is 50 times better than free-running case for offset frequencies of 1 kHz–1 MHz. From Figure F-58a, side-modes at harmonics of 40 kHz are distinctly visible, which are due to 25 μs delay time of injection loop, which contributes to timing jitters of RF reference. A similar side-mode peaks are also seen in Figure F-58b, which is related to round trip time delay of various fiber delay lengths of 1–7 km. These side-modes introduce degradation in timing jitters and are to be reduced using either dual feedback loop of dual self-injection locking (DSIL) [74] or combination of SILPLL [107]. Moreover, single or multiple delayed self-phase lock loop of SPLL technique [112] reduce the phase noise further and at the same time reduce the side mode peak observed in SIL case.

The core component of PLL function is an integrated low-pass filter and mixer board for phase error detection between instantaneous signal and a reference (either external or a delayed version of instantaneous signal). The design concept and related description is reported in [112]. The phase detector is realized using an *X*-band mixer combined with a low-pass filter amplifier (i.e. Mixer+LPFA board of Figure F-59). A 50 MHz loop bandwidth PLL board is redesigned accordingly in this paper because the nature variation of the inter-modal output is between 30 and 35 MHz at fixed temperature of 20 °C. Therefore, the loop bandwidth of operational amplifier on PLL board needs to cover whole potential frequency variation in order to maintain phase locking status. The design of phase detection board is optimized based on phase locking performance using an external frequency reference (Gigatronics GT 9000 frequency synthesizer). The block diagram of phase locking function is depicted in Figure F-59. The RF synthesizer works as the reference source to lock laser inter-modal output with the help of PLL board. If any phase error is detected between reference signal and inter-modal oscillation, a frequency tuning voltage signal is fed back to the PM section to lock the free-running oscillation frequency to the reference signal. The frequency locking range is recorded in Table F-13 for 50 MHz loop bandwidth. The external phase locking circuit lost locking status when frequency difference is 53 MHz, which is out of the loop bandwidth range; effectively this PLL board can successfully provide phase locking, if the instantaneous RF frequency variation is within 50 MHz.

The phase noise performance of external phase locking is provided in Figure F-60. The PLL locked RF signal quality get significant improvement compared with free-running and its phase noise in close in to the carrier is forced to follow the external reference characteristics. Its related phase noise is −85 dBc/Hz at 1 and 10 kHz offset, which is phase locked by forced PLL using external microwave reference signal. This phase noise performance is unchanged no matter what reference signal frequency is used as long as it is within 50 MHz locking range. Moreover, the stability performance is significantly improved as well. The frequency shift is reduced from 30 MHz to less than 5 kHz during 10 min period.

After evaluating optimum operation of PLL functions, performance of injection locking and phase locking combination is further studied in order to combine them together. One of important benefits of combining IL and

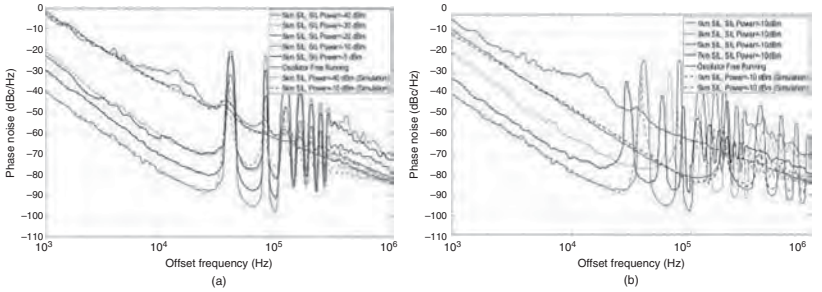


Figure F-58 Phase noise performance comparison of self-injection locking with free-running inter-modal oscillation, (a) different injection power levels, (b) different fiber delay line lengths [83, 84, 122].

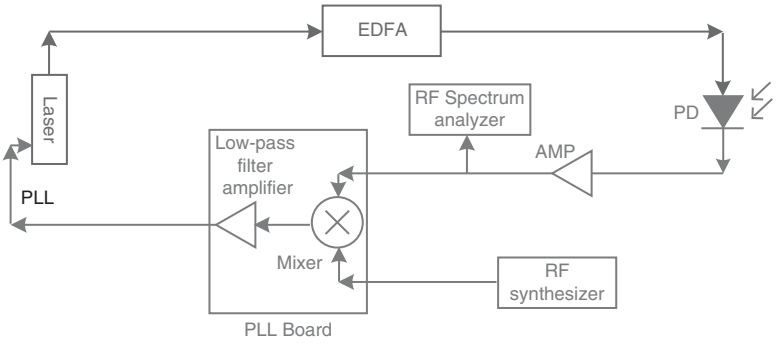


Figure F-59 External phase locking setup using external frequency reference from RF synthesizer by detection of phase error is detected and used to control PM section of multi-section laser [83, 84, 122].

Table F-13 PLL board locking range testing using external RF synthesizer source.

Laser frequency (GHz)	Loop BW = 50 MHz Reference frequency (GHz)	Locking?	Frequency shift (after 10 min)
11.540	11.540	Yes	<5 kHz
11.540	11.550	Yes	<5 kHz
11.540	11.560	Yes	<5 kHz
11.540	11.570	Yes	<5 kHz
11.540	11.580	Yes	<5 kHz
11.540	11.585	Yes	<5 kHz
11.540	11.590	Yes	<5 kHz
11.540	11.593	No	Shifting

PLL is its added benefit in pull-in time [114]. The pull-in time is used to describe how long it takes for signal with initial frequency error with reference to reach a steady status of zero frequency error; this figure of merit is measured using external reference synthesizer signal. Related expression for PLL and ILPLL pull-in time is provided in Eqs. (F-57) and (F-58) [114], where $\Delta\omega_0$ is frequency difference between inter-modal output and reference signal, ω_n is nature frequency, $\Delta\omega_i$ is locking range, and K is open loop gain. Meantime, according to [114], higher loop gain will also bring better phase noise performance. Open loop gain as high as 92 dB will introduce 10 dB phase noise reduction when comparing with 72 dB loop gain case.

$$\frac{(\Delta\omega_0)^2}{{\omega_n}^2 K} \tag{F-57}$$

$$\frac{{\Delta\omega_0}^2 - (\Delta\omega_i)^2}{{\omega_n}^2 \Delta\omega_i} \tag{F-58}$$

Comparison of the measured and simulated results is depicted in Figure F-61 for different PM offset biasing. From Figure F-61, ILPLL will provide at least 20 times faster pull-in time compared with PLL only. In addition, a smaller negative offset reverse bias voltage of PM (i.e. a larger absolute value) provides a faster pull-in time compared with larger negative offset voltage (i.e. a smaller absolute value).

Optimized performance of PLL and ILPLL in term of locking range, pull-in time is used for combination of SIL and SPLL as developed in Figure F-62. The SIL part is still kept the same while SPLL [112] part is realized by multiple delay lines to function as the reference signal in order to remove the need of external synthesizer reference in PLL structure. The high Q and energy storage characteristic of long optical delay line provides a delayed

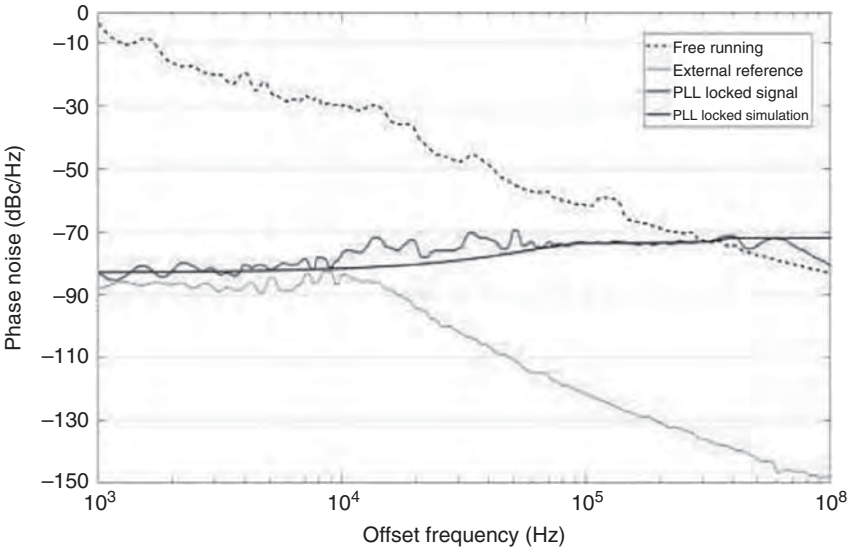


Figure F-60 Phase noise performance using external phase locking circuit (RF frequency of 11.54 GHz, RF output power of 5.39 dBm) [83, 84, 122].

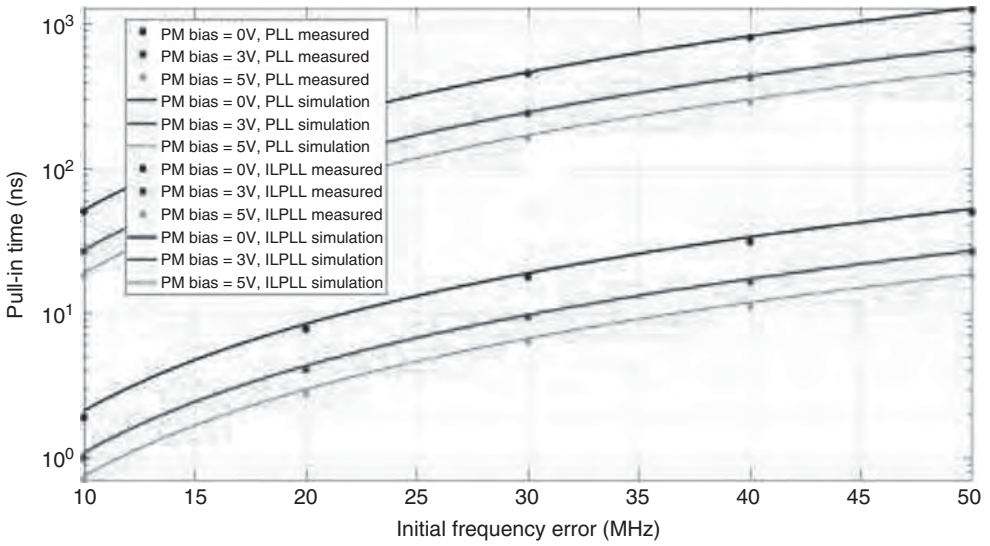


Figure F-61 Simulation and measurement results of pull-in time of PLL and ILPLL using the external frequency reference [83, 84, 122].

reference for self-stabilization of instantaneous inter-modal oscillation. The delayed and non-delayed signals are simultaneously compared using the optimized phase detector (i.e. Mixer+LPFA board of Figure F-62). Any instantaneous phase error is then detected and the low frequency component is filtered as a frequency tuning signal and feedback to PM of the semiconductor laser. This phase comparison of delayed and instantaneous signal pulls back the frequency deviation to original oscillation frequency (i.e. delayed signal as reference), which is the process of PLL. Since the natural variation of free-running laser inter-modal RF output is within 30 MHz at 20 °C, the PLL board loop bandwidth of 50 MHz is sufficient in order to completely cover any potential shift. Large phase

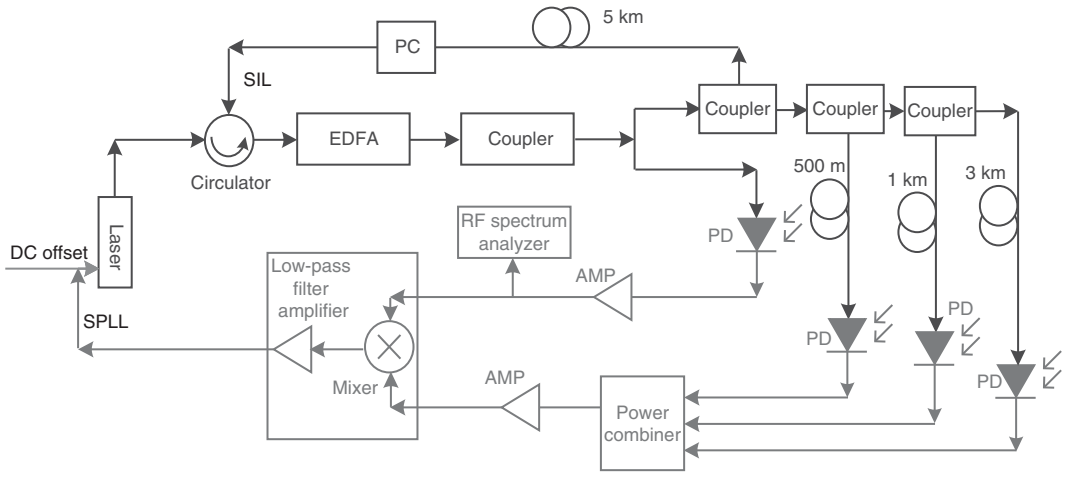


Figure F-62 Block diagram of inter-modal oscillation stabilization using a combination of self-injection locking (SIL) and triple self-phase locking (TSPLL) [83, 84, 122].

tuning sensitivity of PM (an average sensitivity of 150 MHz/V), the low frequency feedback scan range is then set at a maximum voltage swing of −1.0 to +1.0 V, which is sufficient to correct maximum 30 MHz frequency drift. Finally, the output of PLL board becomes a constant DC voltage when inter-modal oscillator is phase locked.

Different offset bias conditions of PM section are also compared using optimized self-injection locking 5 km and triple self-phase locking (TSPLL) 500 m, 1 km, and 3 km to test its related phase noise performance. Triple non-harmonically related delay loop [88] suppresses most effectively peaks of side modes generated by self-injection locking. In fact, all the significant side mode peaks are effectively suppressed (from −30 to −90 dBc) compared with self-injection locking case because of multiple loops. Moreover, shorter SPLL delay line will contribute to fast phase locking speed [114]. From the measurement results in Figure F-63, PM bias of 0 V provides the best phase noise results of −58 dBc/Hz at 1 kHz offset and −98 dBc/Hz at 10 kHz offset by avoiding any DC bias for PM. The phase noise performance comparing with free-running case shows reduction of 53 dB at 1 kHz offset and 68 dB at 10 kHz offset that also matches well with simulation prediction in Figure F-63. In the best scenario, the achieved timing jitter is 0.448 ps, which is 600 times better than free-running conditions.

F-7 DISCUSSIONS

Demand for highly stable oscillators at RF domain could be potentially addressed using optical technology. In particular, phase noise characteristics of opto-electronic oscillators have demonstrated a better performance than the electrical oscillators at frequencies above 10 GHz. In addition to the improved short term stability by reducing close-in to carrier phase noise, the long term frequency drift due to thermal variation of optical fiber index of refraction could be reduced using exotic PCFs. In fact, a composite combination of PCF with HC-PCF combined with standard SMF-28 fiber could reach passive temperature compensation. However, the high attenuation of PCF is currently a major drawback that results in reduced quality factor of the composite fiber. Nonetheless, nonlinear SRS of optical fiber could be used to compensate optical losses of HC-PCF to reach the close-in to carrier phase noise achieved using SMF-28 without the high thermal sensitivity of about 10 ppm/°C. Finally, forced fiber optic oscillation techniques of SIL, SPLL, and SILPLL are used to reduce the close-in to carrier phase noise, while reducing the side-mode suppression. This technique has been employed to develop frequency synthesizers at *X*- and *K*-band using commercially available components.

Many technological advances in opto-electronic systems will undoubtedly advance performance of the next generation of OEO. For example, integrated photonics using monolithically integrated opto-electronic solution

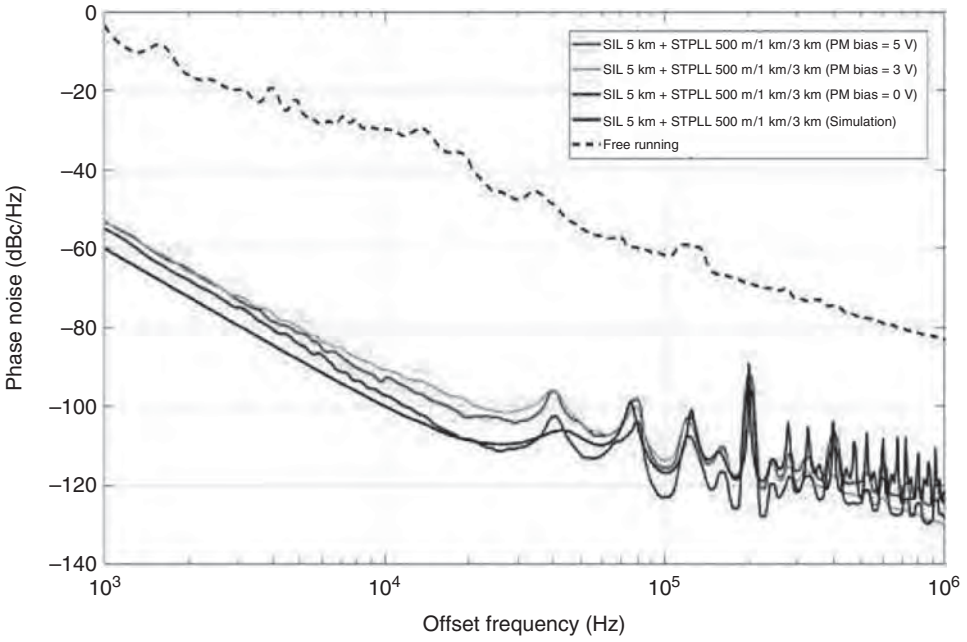


Figure F-63 Phase noise performance of SILPLL based inter-modal RF output and comparison to simulated results under different PM bias while free-running is depicted for comparison (RF = 11.54 GHz, RF power = 3.59 dBm) [83, 84, 122].

on Si chips provides practical low cost and small size solutions. Electro-optic polymer based phase modulators or multi-mode lasers are possible techniques meeting this low-cost and small-size solution. In particular custom designed phase modulators using EO polymer with Sagnac Loop based phase modulator–intensity modulator (PM–IM) interferometers that its phase modulation sensitivity are enhanced using 1D PhC. The advantage of realizing integrated OEO using Si-photonics techniques are integration of SiGe Bi-CMOS with low optical loss components, as an integrated opto-electronics. Another alternative is heterogeneously integrated Si-photonics by fusing InP multi-mode lasers on opto-electronic integrated circuits. Multimode laser with intermodal RF oscillation frequency is employed to realize small size OEO, where self-forced oscillation could be made. In addition to SILPLL of RF oscillation in multi-mode lasers, self-mode locking could be also used to improve performance of RF signal and introduce frequency tuning [115, 116]. Moreover, the large external fiber optic delay lines could be replaced by high Q factor ring [117] and WGM resonators [118] to make a small chip size integration feasible.

ACKNOWLEDGMENTS

The work presented here is as result of technical know-how of nonlinear microwave photonic devices, circuits, and systems that are established with work of many of my graduate students and colleagues in various academic and industrial institutions [85, 119, 120]. Without their contribution, this appendix would not have existed. In particular, I would like to acknowledge contribution of Dr. Xiangdong Zhang, Dr. Tsang-Der Ni, Dr. Xuesong Zhou, Dr. Jui-Yao Lin, and Dr. Harris "Chip" Moyer in analytical and experimental investigations of both RF and opto-electronic ILPLL using an external reference at Drexel University in 1990–1996. These concepts of forced-oscillations later expanded to monolithically integrated multi-section semiconductor laser diodes in collaboration with Dr. Hiroyo Ogawa and Kenji Sato during my sabbatical leave in 1996–1997 at NTT-Wireless Communications Laboratory in Yokosuka, Japan. Forced operation using both injection-locking and mode-locking of multi-section semiconductor laser were experimentally evaluated in months of November–February 1997 as part

of my sabbatical leave studies; this nonlinear process was physically understood and better explained through the PhD work of Dr. Joong-Hee Lee in 1999.

The concepts of SILPLL for both self-seeded VCO and OEO in modular and compact InP based semiconductor laser were first proposed through my experimental and analytical work during my sabbatical leave at both Universite Sciences et Technologie-Lille in collaboration with Prof. Didier Decoster, Prof. Hongwu Li, Dr. Gérard Bouwmans, and Dr. Myriam Kaba, and Thales's Research and Technology (TRT) in association with Dr. Nakita Vodjdani, Dr. Frederic Van Djik, and Dr. Jean Chazales in 2004 and 2005. It took another six years that these ideas were fully conceived.

A more comprehensive analytical and experimental work was established as part of my long standing research collaboration with Prof. Ulrich L. Rohde and Dr. Ajay K. Poddar from Synergy Microwave Corp. for more than 20 years. Particularly, the concepts of PLL (Phase Locked Loop) [34, 35], IL (Injection-Locking) [Ref. 121, Ch-10, pp. 247–340], and forced oscillation of multi-mode systems were advanced over time during these fruitful research collaborations, lead to award of three-patent applications (US9088369B2-[83], US9094133B2-[84], US62/702,970-[122]) and numerous papers, published in international conferences and journals. With their technical expertise additional contributions in terms of novel device designs and experimental verifications of SILPLL are achieved during PhD studies of my students Dr. Li Zhang, Dr. Tianchi Sun, and to be further refined with work of my current PhD student, Mr. Kai Wei. Details about this financially supported project by Synergy Microwave, specifically guided by Prof. Rohde and Dr. Poddar toward meeting the goal of commercialization, which can be found in the three-papers in the Microwave Journal (Optoelectronic Oscillators: Recent and Emerging Trends, October 2018; Computer-Controlled *K*-Band Frequency Synthesizer Using Self-Injection Locked Phase-Locked Optoelectronic Oscillator: Part 1, August 2019; and Computer-Controlled *K*-Band Frequency Synthesizer Using Self-Injection-Locked Phase-Locked Optoelectronic Oscillator: Part 2, September 2019) [61, 123, 124] and other referenced materials. The reported state-of-the-art technology is protected by multiple patents assigned to Synergy Microwave; available for licensing with mutually agreed terms and conditions.

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APPENDIX G

PHASE NOISE ANALYSIS, THEN AND TODAY

G-1 INTRODUCTION

Noise analysis of autonomous circuits (oscillators) could not be understood for many years. The modern approach, where the oscillator noise is properly analyzed as a random phase modulation, is generally credited to David B. Leeson [1].

The Leeson approach starts with the low-pass (baseband) equivalent of the resonator, which is a single-pole low-pass characterized by the time constant equal to the resonator's relaxation time. In the model, the resonator is linear. Practical resonators are satisfactorily linear, and the deviation from linearity has no noticeable effect on noise for the small perturbations present in actual oscillators. Amplifier linearity versus nonlinearity is a more complex issue that has generated a lot of confusion. We all know that gain compression is necessary to stabilize the amplitude. Therefore, the (RF) amplifier has to be described as a nonlinear device. By contrast, working out the baseband model of the amplifier in polar coordinates, and focusing on phase and amplitude fluctuation, all the nonlinearity goes in the amplitude, and the phase is linear. This is sound because the nonlinearity compresses or stretches the amplitude, not the time. Accordingly, a linear amplifier in the phase-equivalent circuit is correct. Phase noise turns into additive noise, and the difficulty of parametric modulation in the loop is gone. This is the mathematical beauty of the Leeson model. However, the orthogonal decomposition in amplitude and phase holds for high Q. With low-Q resonators, one has to use the Floquet vectors and quite a more complex formalism.

Unlike a common belief, the Leeson model actually uses a cyclostationary description of the noise. This fact, not said in the original article, is implicit in the description of the system in terms of phase fluctuations.

The strength and the weakness of the Leeson model is that it describes the oscillator as a system. Hence, amplifier and resonator are blocks described in terms of their parameters. We can predict the phase noise fairly well without knowing what is inside the blocks. With a pinch of imagination, we can work out the phase noise of the balance wheel inside a mechanical watch. By contrast, the Leeson model requires the a priori knowledge of the parameters in the actual operating conditions, based on the analysis of the circuit.

The conclusion is that the engineer designing at component level cannot use the Leeson model until the design is finished. Therefore, other analysis tools are required to start with.

A complete computation of power, loaded Q, and large-signal noise factor (often confused with the noise figure) is found in [2, pp. 131–137]. The introduction of the nodal noise analysis in a proper way was published by Hillbrand and Russer [3]. The Lee–Hajimiri noise analysis is interesting but not very practical. It is quoted very often in the literature, but its use is not practically shown [2, pp. 137–139, 4–6].

If we combine the Leeson formula with the tuning diode contribution, the following equation allows us to calculate the noise of the oscillator completely [2, p. 129]. The voltage-controlled oscillator (VCO) term was added by Rohde [2, p. 131] and the flicker term was added by Scherer [7]:

$$L(f_m) = 10\log\left\{\left[1+\frac{f_o^2}{(2f_mQ_o)^2m^2(1-m)^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P}+\frac{2kTRK_o^2}{f_m^2}\right\}\ [\text{dBc/Hz}] \qquad \text{(G-1)}$$

where

$L(f_m)$ = the phase noise ("10 log()" is omitted in Chapter 2)
f_m = frequency offset (Fourier frequency)
f_o = oscillation frequency
f_c = flicker corner frequency
Q_L = loaded Q of the tuned circuit
Q_o = unloaded Q of the tuned circuit
m = Q_L/Q_o
F = noise factor
kT = 4.1×10^{-21}, thermal energy at 300 K (room temperature)
P = average power at oscillator output
R = equivalent noise resistance of tuning diode (typically 50 Ω–10 kΩ)
K_o = oscillator voltage gain

Equation (G-1) is basically the extension of (2-144) adding the noise of the tuning diode. Another difference is that (G-1) uses f_c as the flicker parameter, instead of using b_{-1}.

Kaertner's paper [8] used a nice time domain approach and includes, probably for the first time, the noise correlation in oscillator design. At his time the now available harmonic balance (HB) method was not invented. A very good description is found in the works by Rizzoli [9–11]. While not easy to read and highly mathematical, Kaertner's calculation produced very real results.

After the linearity, another element of confusion is generated by the definition of $L(f)$. The latter is given in dBc/Hz, which recalls the definition based on the sideband power, while this definition has been superseded by $L(f) = \frac{1}{2}S_\phi(f)$. These definitions match for small phase swing, and under other conditions not discussed here. The problem is that oscillators always end up with large phase swing. In this condition, $S_\phi(f)$ is correct, the carrier-to-sideband power ratio is not. Sadly, numerous people do not trust $L(f)$ close to 0 dBc/Hz and above, and do not trust the $1/f^2$ and $1/f^3$ terms infinitely growing at low frequency, as correctly predicted by the Leeson model. They believe that this gives rise to a singularity, where the electrical power is infinity.

G-2 LARGE-SIGNAL NOISE ANALYSIS

The introduction of the "piece wise linear" HB method, which for the first time ever, was developed by Prof. Vittorio Rizzoli and team, was the perfect body to include the noise correlation method. The famous nonlinear time domain-based circuit analysis program SPICE lacks a rigorous noise correlation analysis, and the HB programs are a hybrid of linear (frequency) and nonlinear (time domain) computations [12, 13]. Rowan Gilmore worked during the "Compact Software" time. Both publications by Rizzoli and Gilmore were leading on the topic.

Rohde's team at Compact Software and the Rizzoli team were struggling a bit to validate the results, and it was complicated to get reliable measured data and maintain accuracy and speed. The Compact Software approach and the Rizzoli team were always fighting with this topic. Shortcuts and approximation had to be avoided in some algorithms because they easily produce the wrong answer. At the end, a very fast double precision multidimensional matrix inversion program was the solution. The use of FORTRAN gave the most stable results. This HB approach is also able to deal with hysteresis.

The first and most challenging circuit analysis of a low noise Texas Instruments-developed amplifier circuit was published. The details of which can be found in Appendix B [14, pp. 376–379]. For the first time ever and in

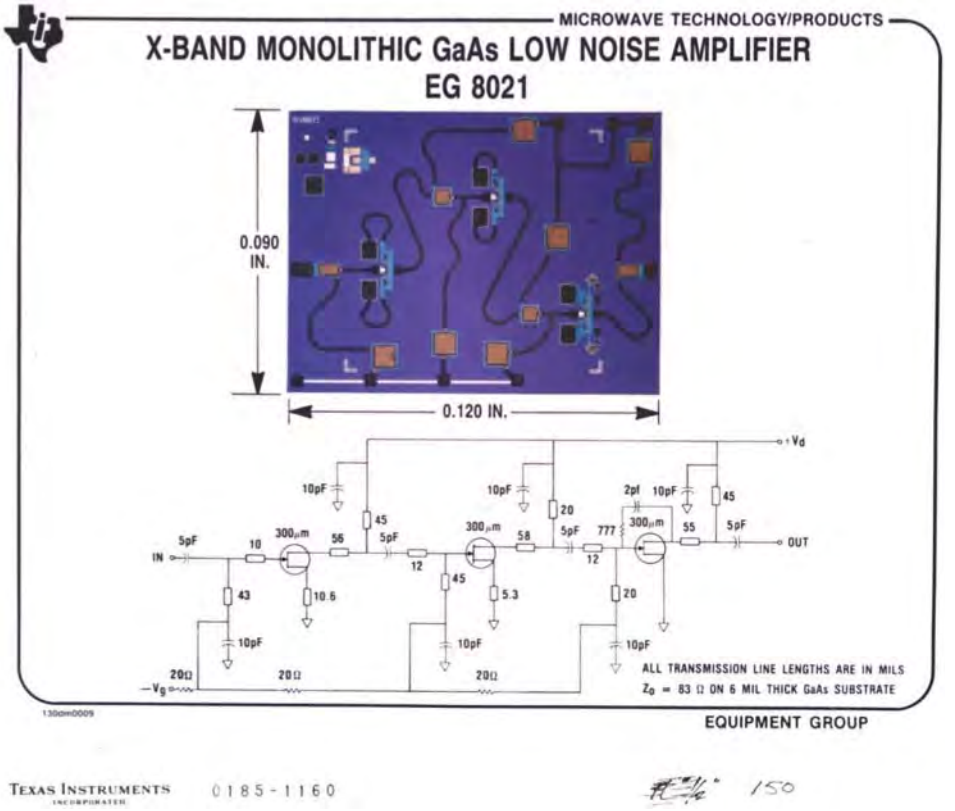

Figure G-1 Schematic of the X-band GaAs monolithic low noise amplifier (Texas Instruments) [see Appendix B].

cooperation with Robert (Bob) Pucell (Raytheon) and Tony Pavio (TI), Rohde demonstrated very accurate results using SPICE type data for GaAs field effect transistors (FETs). They were hard to come by. The team ended up using a modified Materka model [15–19]. The actual circuit was published in The *Microwave Journal* [20]. So far, it was demonstrated that the noise analysis can be done based solely on the available accurate SPICE parameters of GaAs-FET and its family members. See Figure G-1.

The large-signal circuit analysis that was really needed was the one of the oscillator. To implement the proper FET [15–19] and bipolar (BIP) [20–22] models and its derivatives was quite a task. The internal noise modeling was based on the noise correlation matrix [2] and the results were published by W. Anzill et al. [23]. Since 1987 the Microwave Harmonica program by Compact Software was already proven to be reliable [see [20]]. The next step of course was to match the measured results of practical circuits. Hewlett Packard had the first and reliable phase noise system, and Dieter Scherer was the lead engineer at the time to educate us all.

For a systematic approach, even without a simulator, as shown in [24], it is useful to have large-signal S-parameters. They are defined in [2, p. 63]. As to the large-signal parameters of bipolar transistors, which at Kaertner's time had not been derived, they are best obtained from measurements. More about the topic is found in [24]. The proper de-embedding procedure needed has been shown in [19]. It translates the external measurements to the actual chip. Actual measurements require an appropriate test fixture and a Network Analyzer is necessary with variable output power (Figures G-2 and G-3). Figures G-4–G-7 provide an example of actual large-signal S parameters in a transistor. Large-signal operation of a transistor is different form the customary low-noise application, and produce different results [18–22].

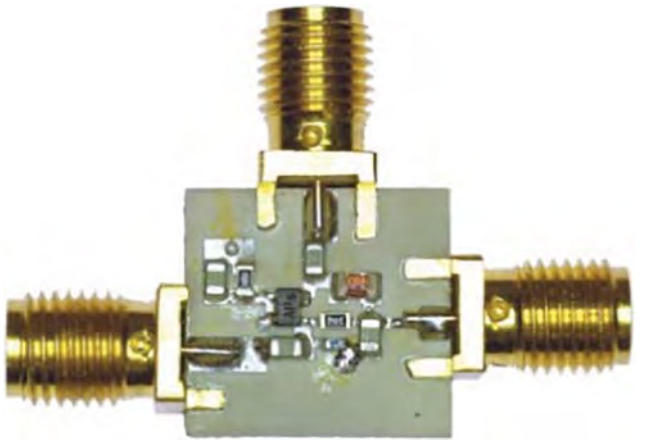

Figure G-2 Test fixture to measure large-signal *S*-parameters.

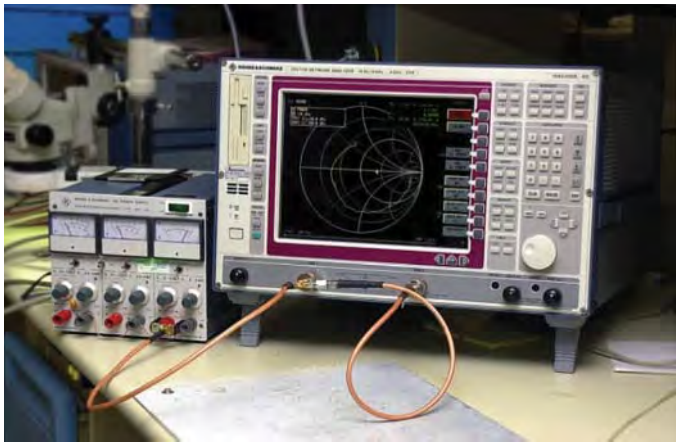

Figure G-3 Rohde & Schwarz 3 GHz network analyzer to measure the large-signal *S*-parameters at different drive levels.

Now, we analyze the circuit used by Kaertner as the basis of his brilliant paper [8, 23]. The schematic (Figure G-8) and the values shown in the following text are based on this publication. Kaertner calculated the phase noise (Figure 7 of his paper, not reproduced here), pointing out correctly that the flicker contribution is not included.

Kaertner made one simplification which in actual circuit theory is deadly: L2 was assumed to have infinite Q. Because the circuit will actually load the tank, this is permissible. With an infinite Q and with C2 = 940 pF, it will oscillate. However, once a likely Q is used (say, 100), the value of C2 has to be reduced to 100 pF for the oscillator to work. This means that feedback has to be increased to compensate for the higher loss. It is also advisable to reduce C4 to 100 pF as it is not possible to make a capacitor without parasitic inductance. The same applies to the 10 μH inductor, which is probably resonant at the operating frequency, and 1 μH seems to be a better choice. Figure G-8 shows the circuit used to analyze the phase noise with Compact Software "Microwave Harmonica." This is the Kaertner circuit, adapted as described.

The simulation results, including the AF and KF values (Figure G-9), tracks the Kaertner's phase-noise spectrum. The influence of AF and KF is clearly seen at 1 kHz.

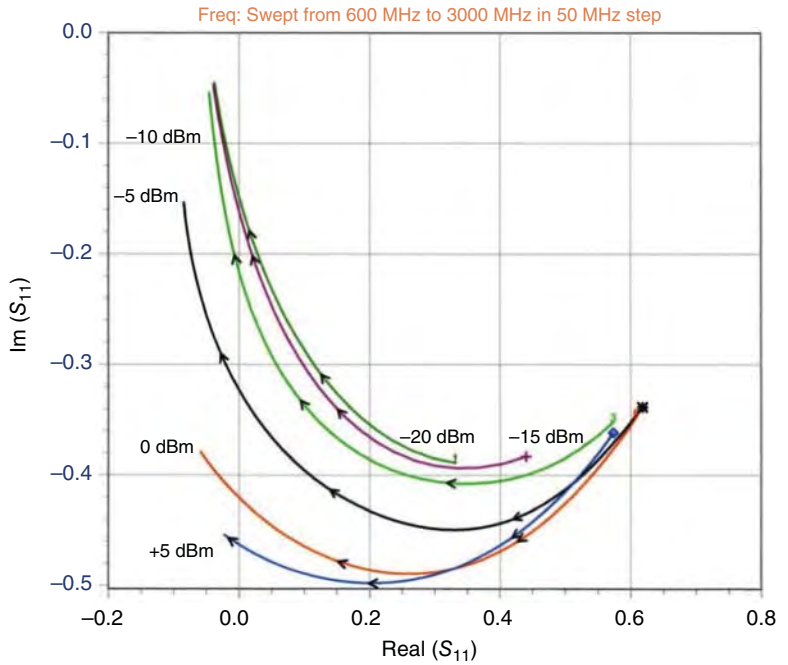

Figure G-4 Measured large-signal S_{11} of the Infineon BFP520.

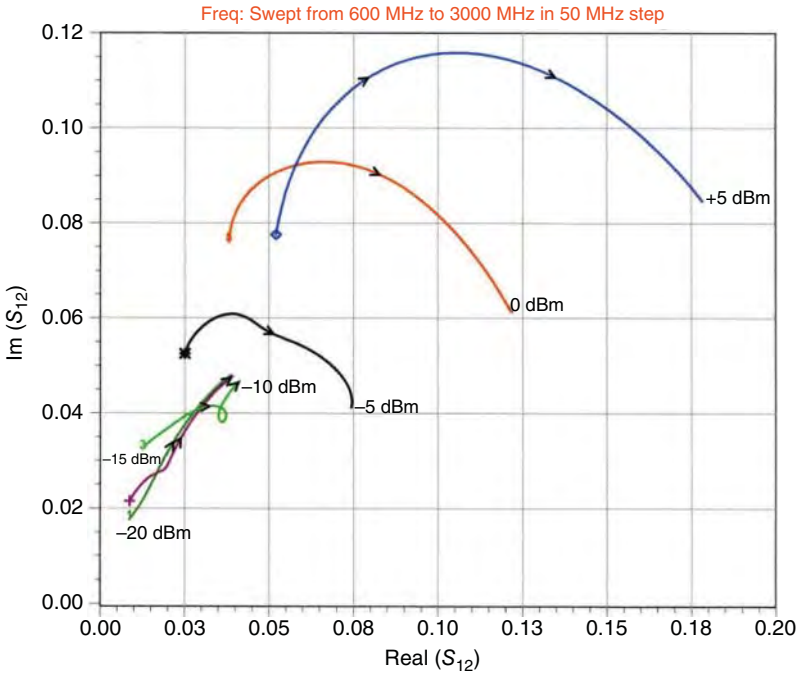

Figure G-5 Measured large-signal S_{12} of the Infineon BFP520.

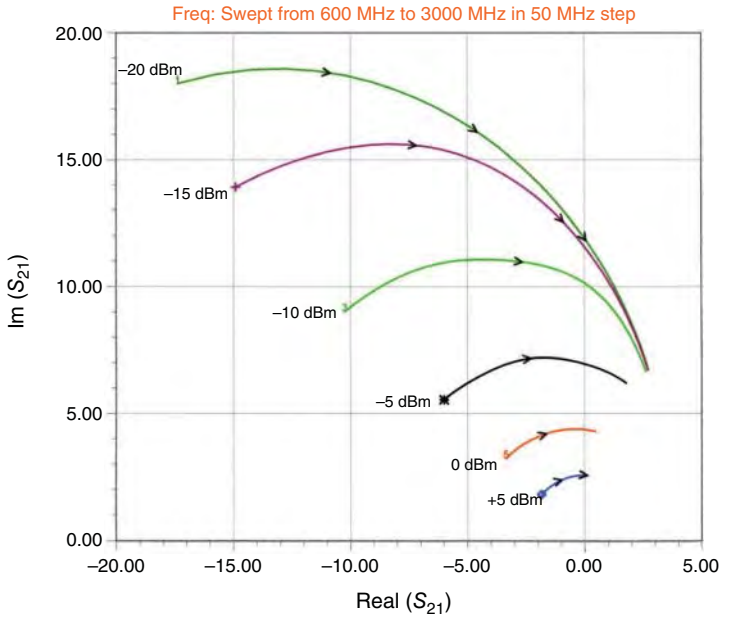

Figure G-6 Measured large-signal S_{21} of the Infineon BFP520.

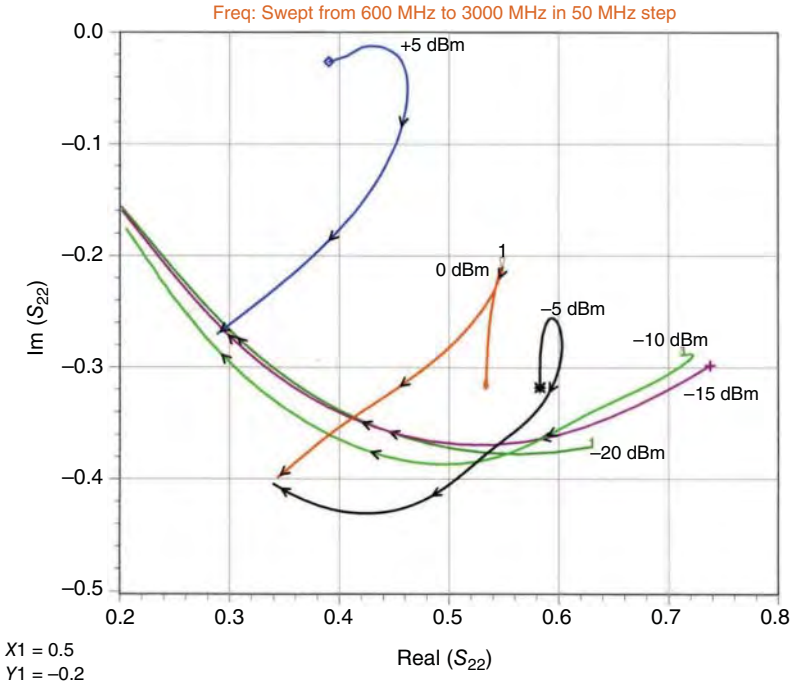

Figure G-7 Measured large-signal S_{22} of the Infineon BFP520.

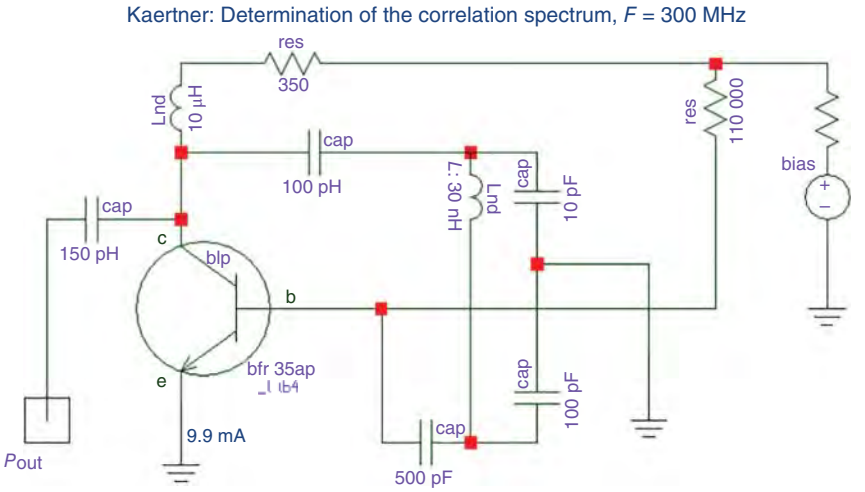

Figure G-8 Circuit schematic of the Kaertner 300 MHz oscillator.

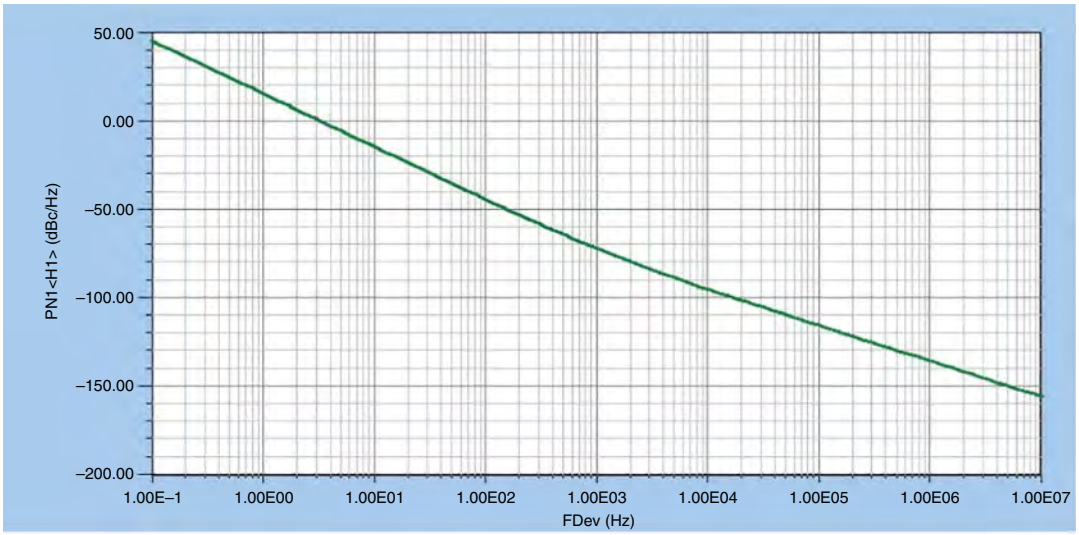

Figure G-9 Simulated phase noise of the Kaertner oscillator (Figure G-8).

The "Microwave Harmonica" software predicts the output power and the harmonic contents, shown in Figure G-10. The output power is about 16 dBm and the harmonic suppression is about 20 dB. This indicates a good operating Q of the resonant circuit.

A different approach comes from Hajimiri and Lee [5]. The HL model includes the harmonics, which brings multiple noise bands to the neighbors of the carrier frequency ω_0, and in turn contribute to phase noise (Figure G-11). The HL model shows that the oscillator's phase-noise $1/f^3$ corner frequency can be significantly lower than the device's flicker corner frequency; provided that the oscillation signals at the output of the oscillator circuits is odd-symmetric. It is worth mentioning that the HL model, correctly, uses a cyclostationary model of the electronics and derives the phase noise as an angular fluctuation.

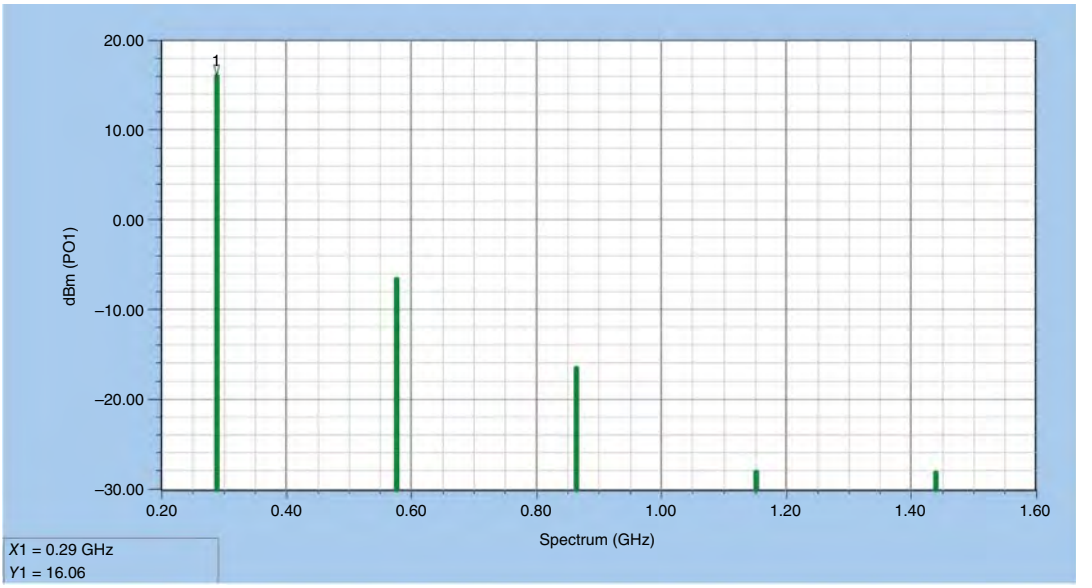

Figure G-10 Simulated output power of the Kaertner circuit.

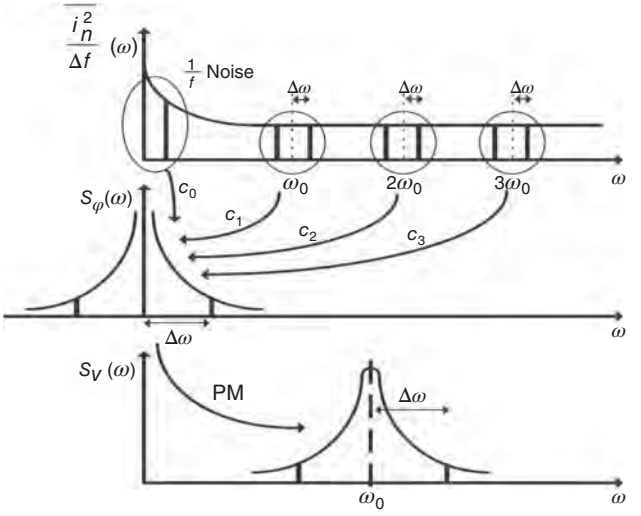

Figure G-11 Conversion process from noise $S_n(\omega)$ to phase-noise $S_\phi(f)$. Noise components from harmonically related frequencies are up-/down-converted to around carrier phase noise, Leeson's model fails to address this phenomenon [5]. Used with permission of IEEE.

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APPENDIX H

A NOVEL APPROACH TO FREQUENCY AND PHASE SETTLING TIME MEASUREMENTS ON PLL CIRCUITS

H-1 INTRODUCTION[1]

Modern radio communication systems regularly employ frequency-hopping methods to better suppress interference or prevent fading. Since such a frequency hop influences data throughput, the time for it is limited. Quick frequency settling is thus one of the key characteristics.

Up to now, complex test setups have been necessary to determine the settling time of a frequency hop. However, the time pressure on communications systems developers requires an easy and efficient measurement method.

This appendix describes different techniques for this measurement. The R&S®FSWP phase noise analyzer performs frequency and phase settling time measurements using a modern wideband concept, and results are obtained easily and conveniently with integrated transient analysis capability.

H-2 SETTLING TIME MEASUREMENT OVERVIEW

H-2-1 Theoretical Background of Frequency Settling Time

Frequency settling is typically measured during the development of components for modern communications systems such as mobile phones or radar systems. The measured quantity is the time the circuit needs to hop from one frequency to another frequency. Data transmission can start only after the circuit settles on the new frequency. In most communication systems, the internal frequency oscillators are frequency locked to a common frequency reference via a phase-locked loop (PLL) to ensure frequency accuracy and compliance with timing requirements for frequency hopping (see Figure H-1).

The characteristics of the PLL determine the phase noise of the entire system. Besides the influence on the phase noise, the loop filter in the PLL has great influence on the amount of time that the system requires for frequency and phase settling after a frequency or channel change.

A certain degree of frequency and phase deviation is acceptable after the hop. This deviation is taken into account to precisely determine the settling time.

[1]This appendix is adapted from: Kay-Uwe Sander, "Frequency and Phase settling time measurements on PLL circuits," Rohde & Schwarz Application Note 1EF102-1E, Rohde & Schwarz, Munich, Germany, June 2018. Used with permission.

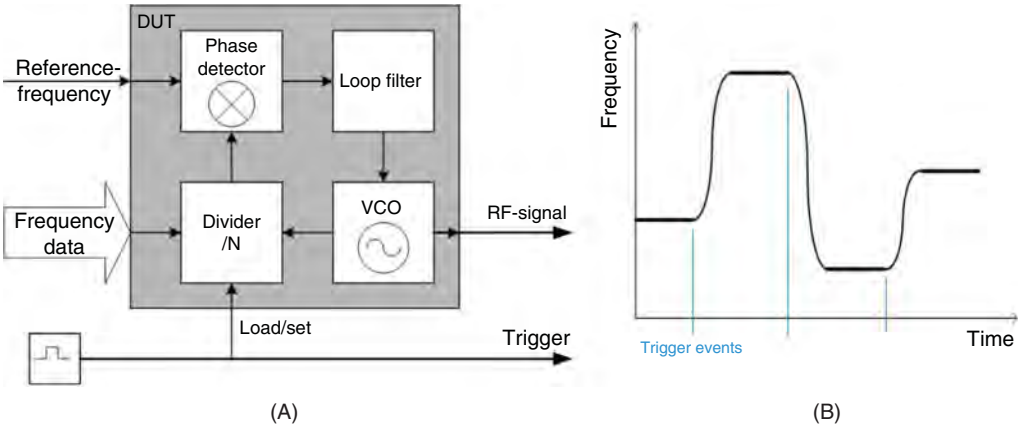

Figure H-1 Frequency-hopping synthesizer: (A) simplified block diagram, (B) trigger event waveform. Courtesy R & S.

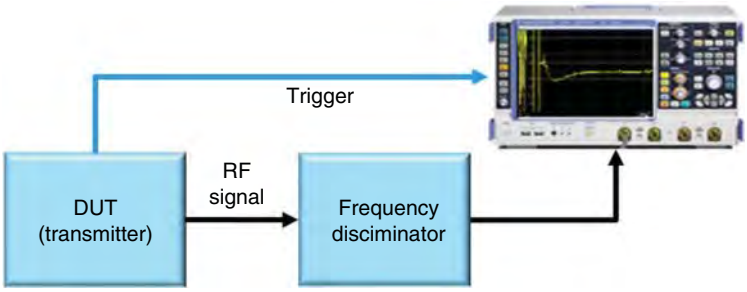

Figure H-2 Test setup with a frequency discriminator. Courtesy R & S.

H-2-2 Frequency Settling Measurement in the Past

Many standards recommend a frequency settling time measurement that is based on a frequency discriminator. The measurement of the settling time is performed on an oscilloscope connected to the video output of the discriminator, since this was the only way to get good resolution and automated measurement functions for timing measurements.

The measurement method relies on the availability of a frequency discriminator that fits to the radio frequency (RF) frequency and bandwidth of the device under test (Figure H-2).

Measurement with Signal Analyzers

As a simple way around the availability of a discriminator, the use of signal analyzers with digital sampling allows broadband measurement of wide frequency ranges. High-speed A/D converter (ADC) sample the input signal and save the measurement data (samples) in large memories. The bandwidth and sampling rate of the ADCs, plus the available memory, determine the acquisition time, possible frequency resolution, and the range over which frequency settling can be measured.

The block diagram in Figure H-3 shows the implementation of intermediate frequency (IF) sampling in a typical signal analyzer. The analog IF filter limits the IF signal to adhere to the Nyquist theorem. Typical bandwidths are in the range of 10 MHz and up to 2 GHz. The ADC samples the analog IF signal. To achieve data rate decimation and reduce the data volume, the sampling output signal is filtered digitally based on the defined bandwidth, thus reducing the sampling rate. The bandwidth determines the time resolution of the subsequent frequency settling

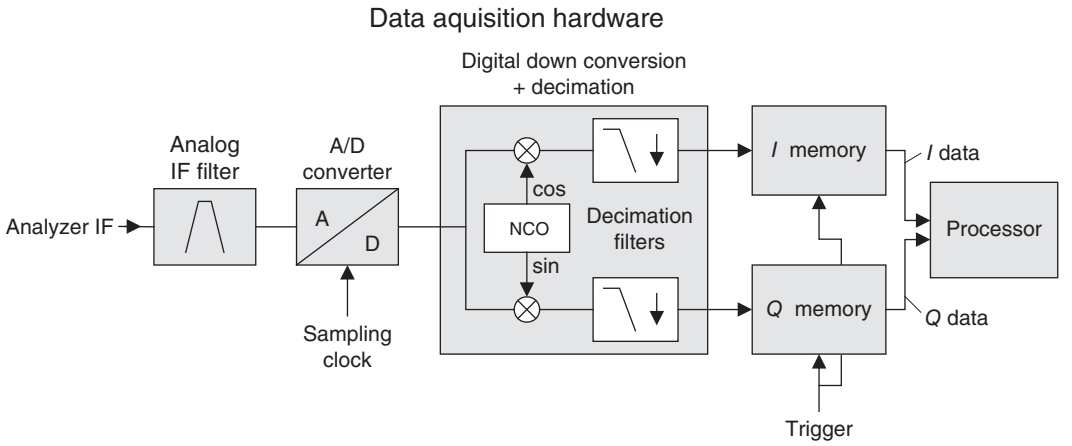

Figure H-3 Block diagram of the IF digitization in the signal analyzer.

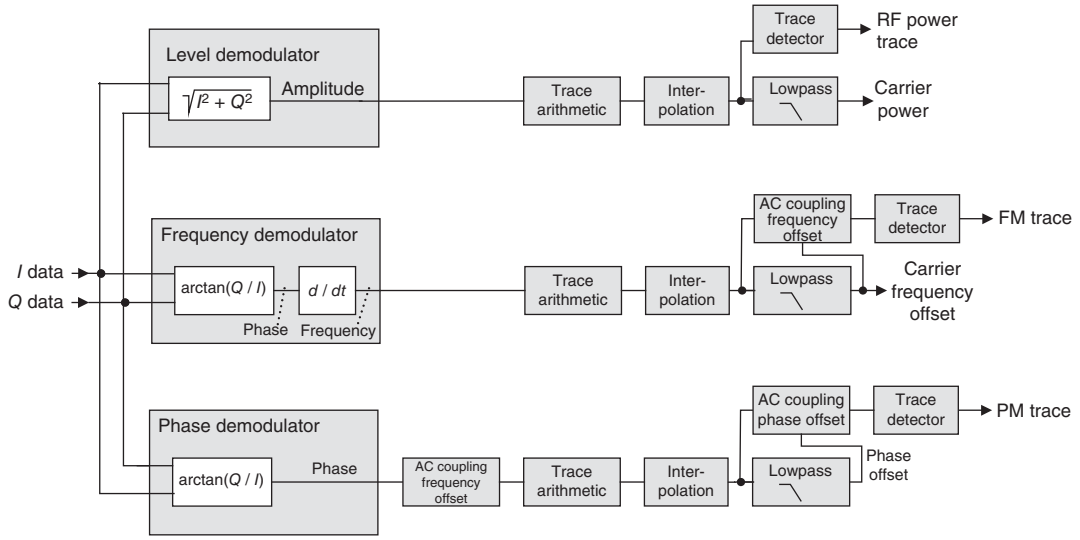

Figure H-4 Block diagram of the demodulators.

measurement. The filtered *I*/*Q* samples are stored in memory for further processing. Internal or external trigger signals can be used to control the storage process, and thus optimally adjust the available storage length to the measurement task. The processor in the signal analyzer includes software that handles the entire demodulation process. All calculations are based on the same *I*/*Q* data set stored in the measurement data memory.

Figure H-4 shows how the saved measurement data is processed to calculate frequency or phase information. The digital (*I*/*Q*) samples contain information about all signals that occur within the recorded spectral range. These samples can be used to calculate the input signal frequency versus time during acquisition time. The outputs of the digital demodulators supply information about frequency, phase, and amplitude versus time. The signal analyzer represents amplitude, phase, and frequency versus time in the form of a measurement trace, and all normal functions such as MaxHold, MinHold, and Averaging are available.

Frequency settling measurements can usually be set up in such a way that the instrument is actuated by a trigger signal that also starts the frequency hop in the device under test (DUT). Recording of measurement data is started

either directly by the trigger event or, when pre- or post-triggers are used, at an optimized, definable point in time before or after the trigger event occurs.

The strength of this architecture thus lies in the analysis of narrowband signals. It is less suited, however, for frequency-agile applications or for measurements over very large frequency ranges.

H-3 R&S FSWP PHASE NOISE ANALYZER

Modern phase noise analyzers not only are able to measure phase noise with excellent performance but also offer a transient analysis function that enables them to measure frequency and phase settling time.

The R&S®FSWP phase noise analyzer uses a signal analyzer concept based on digital signal processing techniques. The functional units used for the phase noise measurement allow frequency and phase demodulation and show frequency or phase variations over time. The advantage of this new design lies in the direct sampling of the IF and the digital conversion to the baseband (digital *I*/*Q* signals). The baseband data thus obtained allows measurements with maximum precision. The digital implementation of the demodulators makes modulation errors and drift negligible. The only sources of error that remain are the characteristics of the analog signal path in front of the ADC.

The use of a frequency divider that is available as part of the phase noise analyzer hardware increases the frequency transient measurement to a much wider bandwidth and thus captures signal transients with up to 8 GHz wide frequency hops.

In addition, the R&S®FSWP offers a real-time frequency demodulator and triggers circuit to identify the transition across a defined trigger frequency to start the measurement. This is a helpful feature for frequency hopping or phase settling time measurements, as a trigger signal that marks the frequency change is often not available from the device under test.

H-3-1 Phase Noise Analyzer Architecture

The use of signal analyzers allows broadband measurement over wide frequency ranges. This is a better approach for measuring frequency and phase settling than the use of a signal analyzer or frequency modulation (FM) discriminator. High-speed analog/digital (A/D) converters sample the input signal, and the measurement data (samples) is then processed in real-time hardware to determine the frequency and level variations of the input signal. The bandwidth and sampling rate of the ADCs determine the input frequency range over which the frequency settling can be measured.

The implementation of IF sampling in the R&S®FSWP phase noise analyzer in its narrowband transient mode (span setting <40 MHz) is shown in Figure H-5. The analog *I*/*Q* mixer uses an extremely low noise internal reference oscillator and shifts the RF input signal to a low IF frequency. The *I*/*Q* mixer outputs are fed to a very low-noise amplifier and then into 100 Ms/s ADCs. The outputs of the ADCs are then fed to an field programmable gate array (FPGA) and digital signal processing is performed in real time.

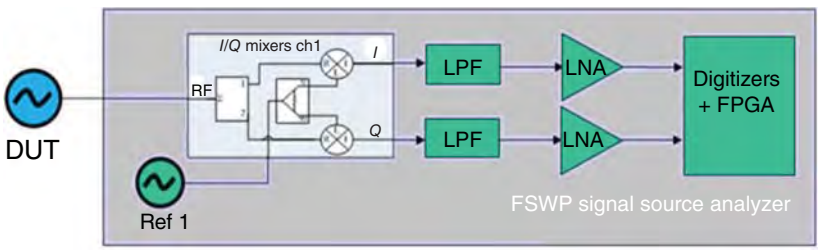

Figure H-5 Block diagram of the IF digitization in the signal analyzer.

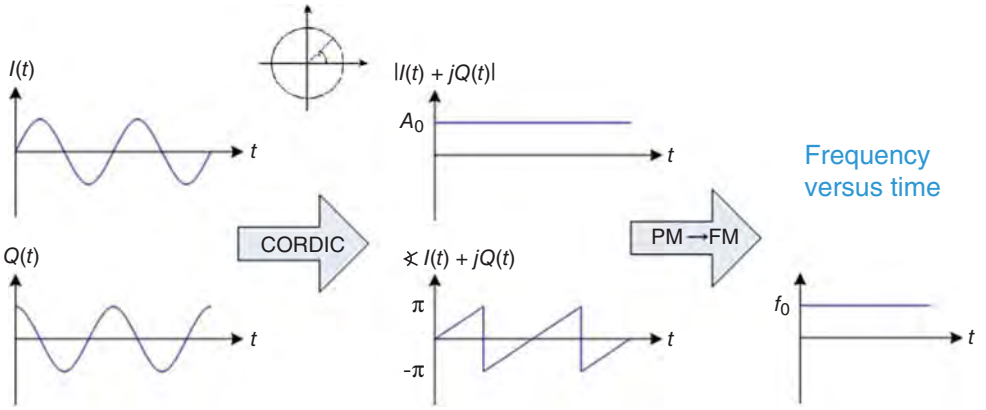

Figure H-6 Block diagram of the demodulators.

The signals from the *I* and *Q* digitizers are next equalized and fed to a digital down converter that provides an *I*/*Q* data stream for subsequent signal processing. The digital down converter provides precise *I* and *Q* signals that are not corrupted by common *I*/*Q* demodulator impairments such as *I*/*Q* imbalance and quadrature errors.

To achieve data rate decimation and reduce the data volume, the sampling output signal is digitally filtered based on the defined bandwidth, thus reducing the sampling rate. The bandwidth determines the time resolution of the subsequent frequency settling measurement. Unnecessary oversampling should be avoided, as this significantly increases noise during the measurement and increases the time required for calculations. Internal or external trigger signals can be used to control the measurement process, and thus optimally adjust the available measurement time to the task.

The block diagram of Figure H-6 shows the processing of *I*/*Q* measurement data to calculate frequency and phase information. The digital (*I*/*Q*) samples are converted into phase and amplitude versus time data, in the next step the frequency information is derived from the phase data.

While the phase noise analyzer normally uses an fast Fourier transform (FFT) to convert the level and frequency information into the phase noise and amplitude noise results, the raw frequency and phase data versus time can be used in the transient mode in the form of a measurement trace to measure frequency and phase settling.

The analog *I*/*Q*-mixer together with the 100 Ms/s ADC limits the analyzer's bandwidth to 40 MHz to fulfill to the Nyquist theorem.

Measurement with Wide Bandwidth

A special wide band signal path in the R&S®FSWP phase noise analyzer includes an RF frequency divider (see Figure H-7).

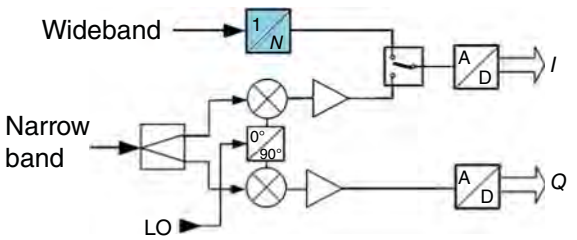

Figure H-7 Block diagram of the R&S®FSWP wideband mode.

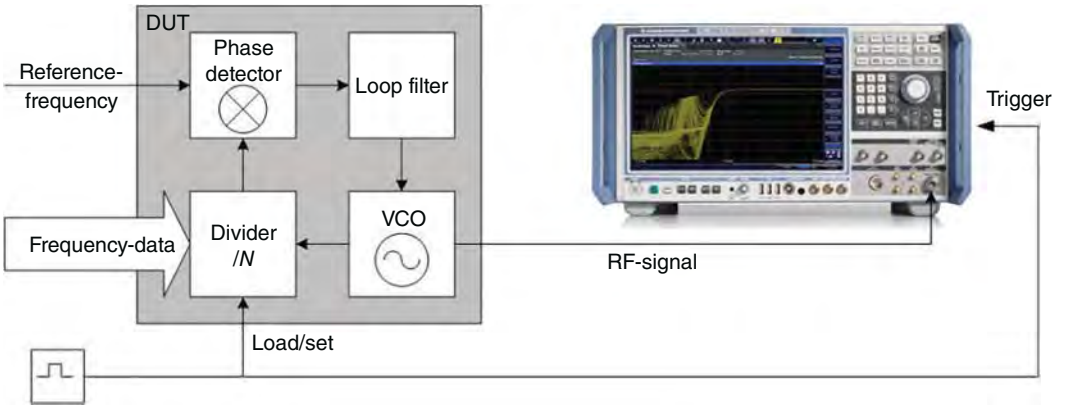

Figure H-8 Setup for measuring frequency settling on a synthesizer.

In the wideband transient mode (span setting >40 MHz), the input signal frequency range from 256 MHz to 8 GHz is divided by 256 in a first step, and the output signal from the divider (1–31.25 MHz) is then sampled and converted to perform the digital *I*/*Q* signal processing as in the narrowband mode.

H-3-2 Typical Test Setup for Settling Time Measurements

Most designs use a programmable divider in the PLL to set the frequency. The Figure H-8 shows the typical test setup for measuring frequency settling on a PLL-controlled oscillator.

The programming signal for loading the frequency divider is used directly as a trigger signal for the analyzer. It marks the start of the frequency hop. The analyzer starts to record the measurement data with the trigger event. Pre- or post-triggers can be used to adjust the start of the recording so that frequency versus time can also be observed before the hop, for example. After the measurement data is recorded, it is used to calculate and display amplitude, frequency, or phase versus time (see Figure H-9).

In case of the R&S®FSWP phase noise analyzer, the measurement can also be triggered by the signal frequency itself. The instrument monitors the output signal of the frequency demodulator and includes a trigger circuit to identify the transition across a defined trigger (frequency) to start the measurement. This feature allows the hopping time measurement for signals that do not allow accessing the trigger inside of the circuits of the device under test.

H-4 FREQUENCY HOPPING AND SETTLING TIME MEASUREMENTS IN PRACTICE

The previous sections describe the fundamentals of frequency hopping and the requirements for practical measurements on these signals. This section describes the use of the R&S®FSWP phase noise analyzer to perform measurements on frequency hopping signals and show the capabilities in RF test scenarios.

H-4-1 Trigger on Wideband Frequency Hopping Signals

To verify the performance of a frequency hopping signal, it is necessary to trigger the measurement instrument on the signal hop of interest. In many cases, the RF circuit design does not offer a trigger signal connection of the device under test.

The R&S®FSWP offers the possibility to trigger the measurement on the frequency transition through a defined trigger position (trigger frequency). Whenever the signal frequency passes this threshold, the R&S®FSWP triggers and records the frequency versus time information.

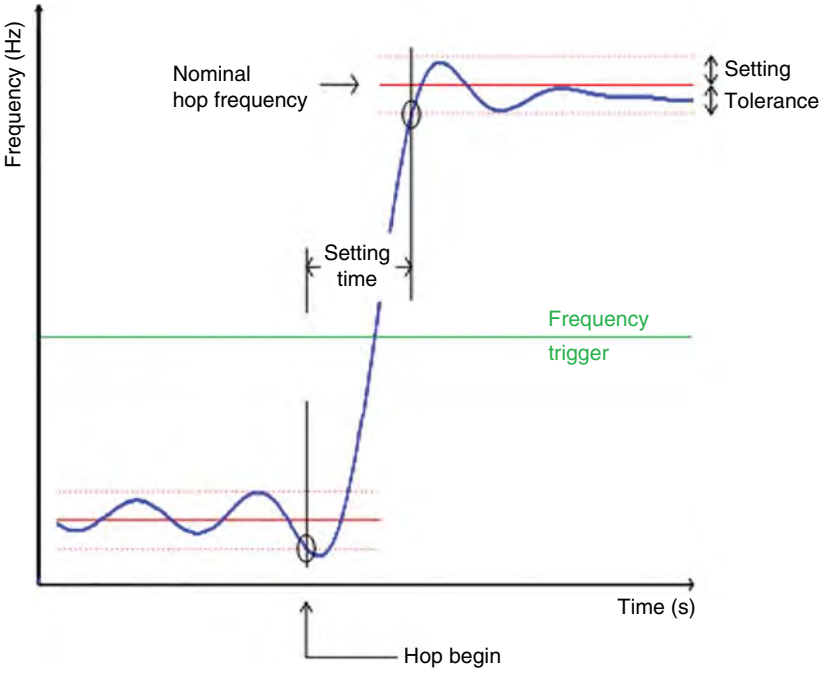

Figure H-9 Frequency trigger and timing measurements on a hopping signal.

In the example shown in Figure H-10, the oscillator generates wideband frequency hops with 200 and 800 MHz hop width. The phase noise analyzer is set to the wideband mode (with 2 GHz span on the screen) and monitors the full frequency range from 256 MHz to 8 GHz and triggers when the signal frequency passes the trigger level that is set to 5800 MHz. Markers permit readings of measured values at any time position. All measurement values are also available via remote operation.

In the next example (Figure H-11), the same signal is measured in the narrowband mode to get a more detailed view about the frequency settling process. In this case, the frequency trigger is set close to the highest frequency of 6200 MHz (see the marker position in the previous measurement).

The specification for this DUT defines a maximum settling time of 2 µs. Limit lines are used to observe these limits. The phase noise analyzer automatically monitors compliance with the limit values and outputs them as PASS/FAIL indication. The loop bandwidth of the PLL circuit is one of the main parts that define the settling time. To visualize the influence of the PLL loop bandwidth, the device under test was modified to create different frequency settling results. Settling time is illustrated in the traces shown in Figure H-11; one trace shows a slow but smooth setting with a small overshoot, while the other using a higher bandwidth settles much faster. The R&S®FSWP offers the possibility to check the measured data against a predefined limit line. In the above plot the limit verification indicates that the oscillator passes its requirement and reaches the target frequency after about 2 µs, and then settles into the target frequency after about 10 µs.

H-4-2 Frequency and Phase Settling Time Measurement

In the previous examples, all measurements were performed with the frequency trigger function of the R&S®FSWP. In this case, the measurement starts when the actual frequency of the DUT is already changing to a new value.

In many cases the designer of a synthesizer needs to know the absolute time between the frequency settling command and the real output of the DUT. In this case the programming signal for the frequency divider must be used directly as a trigger signal for the analyzer as it marks the start of the frequency change.

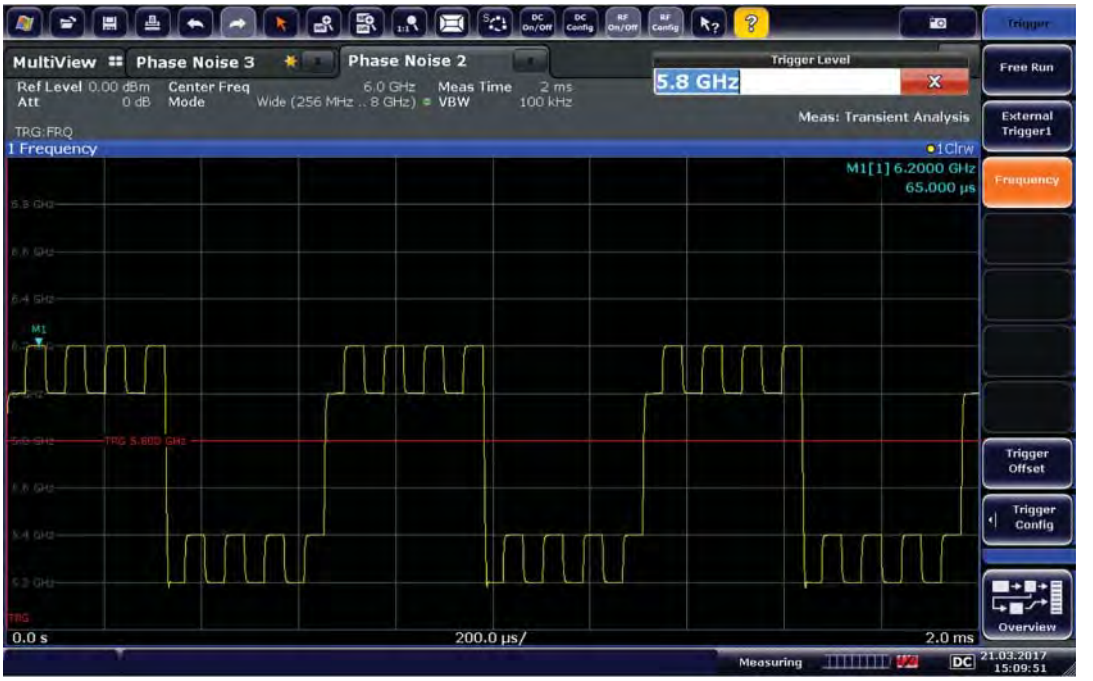

Figure H-10 Frequency trigger with the R&S®FSWP phase noise analyzer.

Figure H-11 Frequency settling time measurement with active limit verification.

Figure H-12 Frequency and phase settling time measurement in parallel.

Another important parameter of the settling time for a frequency hopping PLL is the phase settling of the RF signal. This is especially true for RF communication systems that use phase modulation, as the settling of the phase has a direct impact on the modulation quality.

In Figure H-12, the DUT is programmed to hop to a target frequency of 6000 MHz. The phase noise analyzer measures the frequency versus time in the upper screen, while the phase versus time is displayed in the lower screen. The frequency settling process seems to be almost finished within 10 µs; the phase gives a more detailed view that can reveal behavior that is not visible with any other type of view. As long as the frequency is not completely settled, the RF phase vector will rotate and the phase versus time display covers the full range from –180° to +180°. This effect is very typical for PLL circuits with large capacitors in the loop filter that need to be charged for the fully phase locked position of the oscillator.

The effect of this phase rotation may have an influence on the earliest point in time when the data transmission can reliably start. In a quadrature phase shift keying (QPSK) design, the symbol points are spaced 90° apart, and there is a tolerance of no more one-half the distance between any two quadrature points or 45°. It is important to know about the presence of the phase drift that can only be seen in the phase-versus-time analysis.

Since the phase noise analyzer starts to capture the incoming signal at a random point in time after the trigger event, the phase of the sampled signal may vary from measurement to measurement. To get a stable phase settling time measurement, a point in time needs to be defined that represents zero phase deviation in the result. On a phase settling measurement, this will usually be the point when the phase settling is expected to be finalized. This allows a direct measurement of the phase deviation relative to this point using a marker on the displayed trace data.

Finding Glitches in Settling Time Measurement

In the previous examples, all measurements are performed on a single frequency hop, with the measurement results concentrating on the final part of the frequency or phase settling phase. For frequency hopping systems, it is also important to monitor the frequency transition between the hop frequencies. The output signal of a PLL based

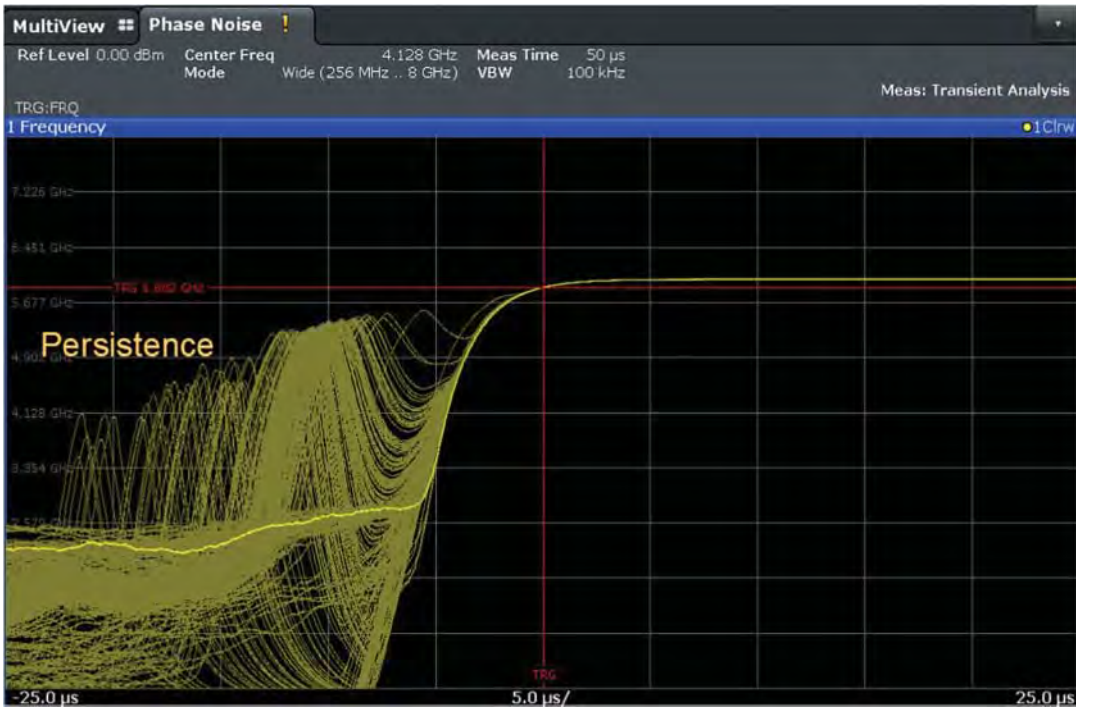

Figure H-13 Finding glitches in the frequency settling time measurement.

synthesizer might differ significantly over different hops or time. It is therefore often important to monitor many hops and overlay the time-correlated views of the frequency settling in one screen.

The R&S®FSWP offers a special trace mode called *persistence* that allows overlying indefinite amounts of measurement traces in one screen. In this mode, the actual measured trace is written in deep color saturation, while older traces fade out from the screen with a defined persistence time.

The screen shot in Figure H-13 shows an example of the persistence trace measuring the frequency settling of a synthesizer. The measurement triggers on the real-time frequency trigger to start and capture the settling of the frequency. The trigger uses a trigger offset of 25 µs to monitor the time before the frequency settles to the final value.

In the aforementioned example we see that there are events where the frequency is ringing heavily before settling to the final value. In the normal trace mode, it would be very hard to identify these bumps as the user would have to stop the measurement manually once such a result is visible on the screen. Persistence mode keeps these events on the screen for a defined amount of time before they fade out.

The persistence view is extremely helpful to find intermittent problems or rare events of a frequency settling measurement, as it makes short glitches visible even if subsequent trigger events would overwrite them in the normal clear/write trace mode.

H-5 CONCLUSION

Frequency settling time measurements were very complex with some traditional methods. For example, the resolution filter must be calibrated if it is to be used as a demodulator. The measurement range is significantly limited, and accuracy is very difficult to assess.

The new generation of phase noise analyzers (like the R&S®FSWP) performs the measurement of settling procedures with less effort and provides rapid results. In addition to measuring frequency-settling time, modern phase noise analyzers also record phase settling time—a very important measurement for phase-modulated transmission methods and one that is extremely difficult to perform using conventional methods.

Because of the digital architecture, no calibration is required; the measurement is carried out immediately, with extremely high accuracy and resolution. Modern phase noise analyzers help developers to obtain more measurement data quicker, thus allowing them to complete their tasks faster.

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INDEX

A

Acquisition
  active filter, 45
  coarse steering, 52–55
  dc amplifier and sweeping circuit, 46, 47
  frequency lock, 46, 47
  loop filter/integrator, 48
  loop stability, 54–62
  operating ranges, 44–45
  passive filter, 45
  pull-in performance, 49–52
  pull-in range, 48–49
  pull-in time, 48
  pull-out range, 47, 48
  requirements, 46
Active integrator, 585, 587
Additive noise, 82–83
Agilent counter, 94
Allan deviation (ADEV), 95
Allan variance (AVAR), 95–96
Amplifiers, phase noise
  isolation amplifiers, 103–104
  low PM noise amplifier, 102–103
  white and flicker phase noise, 100–102
Analog Devices AD9854 DDS oscillator, 124–126
Analog Devices AD9912 DDS oscillator, 125–128
  block diagram, 655
  operation modes, 661–664
  performance characteristics, 656–660
Analog Devices AD9914 DDS oscillator
  functional block diagram, 646, 647, 653, 654
  operation modes, 652
  performance characteristics, 648–651
Analog frequency dividers, 110–112
Analog phase interpolator (API), 246, 250–251
Avalanche noise, 339

B

Backward-wave materials (BWMs), 693
Barkhausen condition, 133
Beat frequency oscillator (BFO), 475, 548, 550, 551
Bias-dependent noise model
  development, 617
  Gummel–Poon bipolar transistor model, 609, 611, 615, 616
  intrinsic FET device, 612, 615
  linear equivalent circuit, 612, 614
  Materka model, 612, 615
  measured and modeled noise, 612, 614
  MESFET, 615, 616
  small-and large-signal parameters, 611, 614
  T-equivalent circuit, 609, 612
Bipolar junction transistor (BJT), 503, 512
Bit error rate (BER), 692
Bode diagram
  first-order loop, 569, 570
  loop components, 568, 569
  loop performance with added circuitry, 582
  open loop gain of PLL system, 581
  phase-noise plot calculated with the modified Leeson equation, 581
  type 1 second-order loop, 569, 578, 579
  type 2 *n*th-order loop, 569, 580
  type 2 second-order loop, 569, 579, 580
Bridge (interferometric) method
  appealing features, 187–188
  building own system, 189
  implementation intended for 8–10 GHz operation, 189–190
  phase-to-voltage gain and background noise, 188–189

C

Capture time, 7
Carmel Instruments, 94
Carrier collapse, 116
Ceramic resonator oscillators (CROs), 260, 261, 455, 457–64
  bipolar implementation, 498, 505
  measured phase noise, 497, 502
  predicted phase noise, 497, 502–503
  test circuit, 497, 501
Charge pump phase locked loop (PLL), 4
  close in phase noise, 575
  filter design constants, 571
  frequency jump lock time, 576
  linear model, 572
  negative frequency jump waveform, 576

Charge pump phase locked loop (PLL) (*Continued*)
open loop response bode plot, 572
output spectrum 100 kHz span, 575
output spectrum 200 kHz reference spurs, 575
positive frequency jump waveform, 575
2nd order passive filter, 572
Circumventing the resonator's thermal noise, 144–146
Clapp–Gouriet circuit, 259–261
Clockwise (CW) path, 743
Closed-loop transfer function, 8
Coarse-tuning loop, 483
Coherent continuous wave (CCW) path, 743
Colpitts oscillator
advantage, 259
ceramic resonators, 260, 261
Clapp–Gouriet circuit, 259–261
conventional circuit configuration, 259, 260
IC applications, 336–337
linear approach
base lead inductances and package capacitance, 262
feedback oscillator, 264
impedance analysis, 260, 261
input impedance, 262
KVL, 260
negative resistance, 260, 262
one-port oscillator design, 263
resonator oscillator's phase noise spectrum, 263
right transistor selection, 268–269
S-parameters, 265–268
semiconductors and circuits, noise in, 337–339
series feedback oscillator
configuration, 314
implementation, 318–322
output impedance, 314–317
phase noise, 318
Z-parameters, 315
350 MHz oscillator
BFG520, 269
biasing, 269–271
coupling capacitor, 276
large-signal transconductance, 271–276
parameters, 269
phase noise, 276–282
2400 MHz MOSFET-based push–pull oscillator
AM-to-PM conversion, 333–336
design calculations, 327–329
design equations, 322, 325–327
1/f noise, 330, 332–334
phase noise, 329–332
validation (*see* Validation circuits)
Colpitts–Rohde oscillator, 144, 145
Complementary metal–oxide–semiconductor (CMOS), 322, 323, 328
Complementary split-ring-resonator (CSRR) structures, 694
Complete oscillator, 139–141
Complex planes, 561, 565
lag filter, phase and frequency response, 566
RC lag filter, 566
simple RC network, 565
tuned circuit with negative resistor, 567
Complex variable functions, 559–561
CORDIC algorithm, 172
Cross-spectrum method, 180, 182
AM noise effect, 186–187
disturbing signal, 182–183
dual-channel phase-noise measurement system, 166
DUT noise, 166, 167, 173, 182, 188
measurement uncertainty, 183–184
rejection of the background noise, 167–170
thermal energy in input power divider, 184–185
Crystal oscillators, 352–354

D

Data registers, 248, 250
Dedicated frequency multiplier, 113
Device under test (DUT) noise, 166, 167, 173, 182, 188
Dielectric resonator oscillators (DROs), 444–446, 448–452, 487, 511
discriminator stabilized, 639–641
equivalent circuit, 439, 443
experimental evaluation, 535, 539
frequency function, 503, 512
high-*Q* case Microstrip, 628–629
initial current surge, switch-on time, 508, 513
Metamaterial-Möbius coupling mechanism
in disk configuration, 696
double negative materials, 693
figure of merit, 692
Mobius stacked SRR K-band oscillator, 697
permeability–permittivity pair, 693
Q-factor, 693
SDR0800-8 oscillator, 698, 699
series and parallel feedback, 697
SRR and CSRR structures, 694, 695
output power, 503, 512
start-up condition, 503, 513
super-compact file, 442–443
ultra-low phase noise (*see* Ultra-low phase noise DRO)
Differentiation, 585
Digital acquisition time, 7
Digital frequency dividers, 104–106
Digital instruments
CORDIC algorithm, 172
Jackson Labs PhaseStation 53100A, 176–178
microsemi family of phase noise and Allan deviation tester, 173–175
Nyquist zones, 171
quantization noise power, 172
Rohde & Schwarz FSWP phase noise analyzers, 178–180
Digital loops
input and output waveforms, 8–9
with mixers, 40–44
phase/frequency comparator, 7
sample/hold comparator, 7–8

Digital phase-noise analyzers, 174
Digital recursion oscillator, 210–211
Digital-to-analog converters (DACs), 52, 53, 206–208
Digital tri-state comparators
  antibacklash feature, 377, 378
  CD4046 PLL IC, 374, 375
  D flip-flops and NAND gate, 370, 371
  logic diagram, 370, 372
  Motorola MC12040, 374, 376
  output pulses, 377, 378
  output voltage as function of frequency ratio, 372, 373
  output waveforms, 370, 373
  quad-*D* circuit, 372, 374
  response of frequency/phase detector near loop lock, 377, 379
  version of, 374, 377
Digital waveform synthesizers, 220
  AD9914 of Analog Devices, 220–228
  AS9912, 220, 229
  block diagram, 203–205
  digital recursion oscillator, 210–211
  frequency spectrum, 207–208
  HF synthesizer, 220, 230
  L-band frequencies, 220, 230
  phase accumulator, 205–206, 211–215
  RAM-based synthesis, 215–219
  samples/cycle sine wave, 208, 209
  systems concerns, 209–210
Diode switches
  electronic band selection, 346–349
  frequency multiplication, 347, 350
Direct digital synthesis (DDS), 78
  dual loop synthesizer, 234–235
  fractional division *N* synthesizers (*see* Fractional division *N* synthesizers)
  phase comparators, delay line, 236–239
  phase locked SAW oscillator, 236, 238
  phase modulation, 201
  phase noise, 122–128
  signal quality
    data skew, 231
    implementation effects, 231
    nonlinear transition effects, 229, 231
    output transfer function characteristics, 231
    phase noise, 231–235
    quantization effects, 220
    two-tone intermodulation distortion, 231
  signal to quantization ratio, 118–119
  single loop phase locked DRO, 235
  single loop phase locked VCO, 235–237
  theory of operation, 117–118
  truncation spurs, 119–122
  waveform synthesizers (*see* Digital waveform synthesizers)
Direct frequency synthesis, 471–473
Distributed Bragg reflector (DBR), 744, 745
Double-balanced mixer instruments
  amplifiers and other two-port components measurement, 162–163
  asymmetric driving for low-power signals, 160
  background noise, spurs, and other experimental issues, 158
  discriminator method, 163–166
  heterodyne measurement of oscillators, 161–162
  mixer and flicker white noise, 159–160
  mixer and LNA white noise, 159
  PLL error function, 156
  tight PLL for phase noise measurement, 157
Double-balanced mixers, 355, 357
"Double-mix-divide" approach, 471–472

E

Edge-triggered JK master/slave flip-flops, 4, 368–371
Eigenmode, 671, 674, 675
Equivalent number of bit (ENOB), 119
Euler's theorem, 560
Exclusive-OR gate, 4, 358, 360–362

F

Fast Fourier transform (FFT), 69, 84–86, 96, 164, 166, 168, 183, 232, 267, 775
Field effect transistors (FETs), 259, 487, 498, 504
Field programmable gate arrays (FPGAs), 78
Fifth-order loop transient response, 36–40
Figure of merit (FOM), 129, 130, 533, 692
Filter
  active
    first order, 23
    transfer function, 25–26
  passive
    first order, 23–24
    transfer function, 26–27
Final value theorem, 585
Finite-pulse-width model, 365
Flicker frequency noise, 85
Flicker noise, 77, 83, 86, 338
Fluke model, 237, 239
Forced oscillation
  benefits, 718
  injection locked oscillator, 718–720
  phase locked loop, 723–724
  SIL, 720–723
  SILPLL (*see* Self-injection locked phase locked loop (SILPLL) oscillator)
  SPLL, 725–728
4100 MHz oscillator, 297, 300–302
Fractional division *N* synthesizers, 237
  advantages and drawbacks, 240
  average output frequency, 239
  block diagram, 202–203, 248–249
  divide-by-*N* loop, pulse remover block, 241–242
  patents, 253–255
  phase-locked loop (*see* NF loop)
Fractional frequency fluctuation, 68, 83, 86, 89, 90, 92

Frequency-conversion approach
  assumptions, 626
  autonomous circuits, 627
  conversion noise analysis, 626, 627
  modulation, 626–628
Frequency counters, 88
  Allan variance, 95–96
  AVAR, MVAR, and PVAR comparison, 97–99
  comparison of, 93–94
  conversion from spectra to two-sample variances, 96–97
  Λ counter, 90–92
  modified Allan variance, 96
  Ω counter, 92–93
  parabolic variance, 96
  Π counter, 89–90
Frequency dividers
  analog frequency dividers, 110–112
  digital frequency dividers, 104–106
  Λ divider, 106–110
  phase noise scaling, 106–107
  phase-type noise, 108
  time-type noise, 108
Frequency drift, 85
Frequency modulation (FM), 492
Frequency multipliers
  carrier collapse, 116
  dedicated frequency multiplier, 113
  locked oscillator, 113
  NLTL, 114
  step recovery diode, 114
Frequency register, 248
Frequency stability PSD, 86–87
Frequency-to-digital converters *see* Frequency counters
Friis formula, 75, 76, 144

G

Grand Repetition Period (GRP), 121
Gummel–Poon model, 609, 611, 615, 616

H

Half-hold sampling, 208
Harmonic balance (HB) method, 762
Harmonic generators, 500, 508
Heterodyning technique, 40–43
Higher-order loops, 36–40
High frequency (HF) synthesizer, 220, 230
High-performance hybrid synthesizer
  Analog Devices AD7008 DDS modulator, 545–546
  BFO synthesizer, 548, 550, 551
  block diagram, 545
  example application, 544
  ICOM IC 736 HF/6m transceiver, 545, 547
  loop filter design
    bode diagram, 551, 553
    flicker frequency noise, 548
    open-and closed-loop phase noise prediction, 551, 552
    Rohde & Schwarz multiloop synthesizer model SMK, 555
    single sideband phase noise, 551, 552, 554–555
    spectral analysis, 553, 554
    switching time, 555, 556
    synthesizer phase noise, 555, 556
    voltage supply, 555–557
  loop gain, 547, 549
  LO synthesizer, 548, 550
  output frequency, 547, 548
  single chip MC145170, 547, 550
  single-loop PLL synthesizer, 545–546
Hollow-core PCF (HC-PCF)
  passive temperature compensation, 713–714
  Raman amplification, 714–718
  temperature sensitivity improvement, 712
  thermal sensitivity analysis, 709, 710
  thermal stability *vs.* phase noise degradation, 712–713
Hybrid coupler, 383

I

Image-rejection mixers, 355, 356
Incidental FM, 26–27
Initial value theorem, 585
Injection locked oscillator (ILO), 110, 111, 718–720
Integrated circuits (ICs), 666, 668
Integration, 585
Intermediate frequency (IF) filter, 43, 44, 772, 773
Isolation amplifiers, 103–104

J

Jackson Labs PhaseStation 53100A, 176–178
Junction gate field-effect transistor (JFET), 503, 513

K

Kirchhoff's voltage law (KVL), 260

L

Λ divider, 106–110
Λ frequency counter, 90–92
Lange Electronics, 94
Laplace transform
  active integrator, 585, 587
  differentiation and integration, 585
  final value theorem, 585
  initial value theorem, 585
  linearity theorem, 584
  locking behavior of PLL, 587–589
  ramp, 584
  square wave, sine-wave contents, 582, 583
  step function, 583–584
Leeson model, 144
  oscillator loop and companion circuit, 134–135
  oscillator's phase-noise transfer function, 138–139
  phase noise of the complete oscillator, 139–141
  resonator and its impulse response, 135–138

10 MHz OCXO, 141–143
10.24 GHz DRO, 141
Left-handed materials (LHMs), 693
Linear approach, Colpitts oscillator
base lead inductances and package capacitance, 262
feedback oscillator, 264
impedance analysis, 260, 261
input impedance, 262
KVL, 260
negative resistance, 260, 262
one-port oscillator design, 263
resonator oscillator's phase noise spectrum, 263
right transistor selection, 268–269
S-parameters, 265–268
Linearity theorem, 584
Line receiver, 382
Local oscillator (LO), 2, 4, 487, 548, 550
Locked oscillator, 113
Lock-in range, 7, 45
Loop filters
active RC, 422–423
active second-order low-pass, 423–426
bode diagram, 551, 553
flicker frequency noise, 548
open-and closed-loop phase noise prediction, 551, 552
passive LC, 426–427
passive RC, 421–422
Rohde & Schwarz multiloop synthesizer model SMK, 555
single sideband phase noise, 551, 552, 554–555
spectral analysis, 553, 554
spur-suppression techniques, 427–430
switching time, 555, 556
synthesizer phase noise, 555, 556
voltage supply, 555–557
Low-noise microwave synthesizers
building blocks, 485–490
cavity-based oscillator, 497, 501
CRO, 497, 501–503
digital interfaces, 484–485
FETs, 498, 504
frequency standards, 490–492, 495
FRN synthesizer labeled module A7, 516, 521
harmonic generators, 500, 508
HP8642 generator, 512, 514, 518
isolation stage, 500, 507
measured data, 496, 500
measured phase noise, 511, 515
millimeter-wave oscillators
elements, 508, 514
harmonic output power, 503, 510
phase noise simulation, 503, 511
Texas Instrument 8132 VCO topology, 502–503, 509
39-GHz oscillator design, 503, 510
oscillators, 493, 496–499
output loop response
border diagram, 489, 492
fine-resolution system, 489, 494
optimized response, 489, 493
phase margin, 489, 493
single-sideband phase noise, 489, 491–492, 508, 514
reference frequency output, 516, 520
RF oscillator assembly, 515, 519
Rohde & Schwarz
signal generator, 534, 536–538
SMA100A, 535, 539
SMA100B, 511, 515
SMP100B, 512, 516
spectrum analyzer Series FSW, 512, 517
SPREF, 537, 539–540
SSB phase noise, 518, 522
SMHU synthesizer, 516, 521
time domain analysis, 503, 508, 511–513
very wideband oscillator, 498, 506
Low-noise oscillators
principles, 590
quarter-wavelength oscillator
capacitance required to tune, 592
rigid cable, 592
with switching diodes, 593
Rohde & Schwarz SMDU oscillator, 594
Low-pass filter (LPF), 208, 209
Low phase noise bipolar transistors (BIPTs), 487
Low PM noise amplifier, 102–103
Lumped resonator oscillator (LRO), 437, 440

M

Mach-Zehnder modulator (MZM), 731–732
Materka model, 612, 615
Mathematical expectation, 94
Metal–oxide–semiconductor field-effect transistors (MOSFETs), 594
Metal–semiconductor field-effect transistor (MESFET), 615, 616
Metamaterial-Möbius coupling mechanism
in disk configuration, 696
double negative materials, 693
figure of merit, 692
Mobius stacked SRR K-band oscillator, 697
permeability–permittivity pair, 693
Q-factor, 693
SDR0800-8 oscillator, 698, 699
series and parallel feedback, 697
SRR and CSRR structures, 694, 695
Metamaterial-Mobius Resonator (MMR), 695
Metamaterial-Möbius Strips (MMS) envisage, 692, 693
Microsemi 5120A PM noise test set, 175
Microsemi 5125, 175
Microsemi family of phase noise and Allan deviation tester, 173–175
Microstrip dielectric resonator oscillator (DRO), 628–629
Microwave oscillators
compressed Smith chart, 432–433
conditions for oscillation, 430–431
series/parallel resonance, 432–433

Microwave oscillators (*Continued*)
specifications, 431, 432
two-port design
buffered, 436
design flowchart, 437, 438
DRO file, 439, 442–444
5 GHz GaAs FET, 437, 438
LRO, 437, 440
oscillation condition, 435, 436
phase noise characteristics, 437, 439
phase noise performance, 437, 440–442
power output characteristics, 437, 440
S-parameters, 437
Spice format, 443, 445
transmission line, 437, 442
tuning parameters, 441, 444
Microwave resonators
ceramic resonators, 455, 457–46‘
dielectric resonators, 445–446, 448–452
SAW oscillator, 445–447
varactor resonators, 452–453, 455–457
YIG oscillators, 448–449, 453–455
Miller divider, 110
Millimeter-wave oscillators
applications, 636–639
design, 503, 510
elements, 508, 514
harmonic output power, 503, 510
phase noise simulation, 503, 511
Texas Instrument 8132 VCO topology, 502–503, 509
Mix-and-divide technique, 471–472
Mixer
digital loops, 40–44
double-balanced, 355, 357
image-rejection, 355, 356
single-sideband, 355
termination-insensitive, 355, 356
Moderate/low-Q (type A/C) oscillators, 146–147
Modified Allan variance (MVAR), 96
Modified Leeson equation, 319
Monolithic microwave integrated circuit (MMIC)-based synthesizers, 617, 668
frequency divider, 666, 667
IC equivalent circuit, 666, 668
Ku-band frequency synthesizer, 666, 667
regenerative frequency divider, 666, 667
VCO, 665–666
Most significant bit (MSB), 120
Motorola MC12040, 374, 376
Multiple-loop synthesizer
block diagram, 473–474
fine-resolution loop, 474, 475
noise sideband, 475
output loop, 474, 475
radio frequency, 475
SMA100B, 475–477

N

Negative index materials (NIMs), 693
900–1800 MHz half-butterfly resonator-based oscillator
coupled resonator, 308–309
layout information, 306, 307
multiple-coupled resonator, 306
phase noise, 306, 307
push–push configuration, 311–317
Q factor, 309–311
Noise contribution from power supplies, 132–133
Noise factor, 72–76, 82
Noise figure (NF) loop, 72, 244–245
accumulator, 242–244
API section, 250–251
block diagram, 240, 246–248
data registers, 248, 250
integrated currents, 251–252
integrator waveform, 251–252
of mixer circuits,–622–624
phase detector output, 241–242
phase detector sawtooth output, 241–243
phase relationship, 241
pulse remove command section, 244
requirements, 245
sequence of events, 248
structure, 248, 250
VCO frequency, 245–246
Noise-free synthesizer, 82, 123
Noise sideband
oscillator, 475, 477, 479
performance, 480–482
Noise temperature, 72–74, 76–77
Noise transfer function, 290–295
Noisy circuits, general concept, 619–622
Normalized Fourier coefficients, 597
Nyquist zones, 171

O

Ω counter, 92–93
100 MHz crystal oscillator
feedback arrangement, 284, 285
input noise power, 286–287
input noise voltage, 286
linear representation, 284, 285
noise power spectral densities, 284, 290–295
noise shaping function, 288–289
noise sources, 287–288
noise transfer function, 290–295
noisy bipolar transistor, 283
non-unity gain, 290
phase noise spectral density, 286–287
One-port negative-resistance model, 263
1000 MHz ceramic resonators
circuit arrangement, 297, 299
component values, 296
diode, 294
emitter and the capacitive feedback, 293, 294

phase noise, 297–298
real and imaginary oscillator, 297, 298
RF amplifier, 294, 296
Open-loop gain, 6
Open-loop transfer function, 365, 367
Operations for complex mathematics, 562–564
Optoelectronic oscillator (OEO)
benefits, 718
block diagram, 701–702
experimental setup, 705–708
ILO, 718–720
multi-mode semiconductor laser
inter-modal oscillation, 745–747
self-forced frequency stabilization, 747–753
structure, 744
operation principle, 704–706
passive temperature compensation, 713–714
performance comparison, 704
phase noise measurements, 708–709
PLL, 723–724
Raman amplification, 714–717
resonator technologies, 701–703
SIL, 720–723
SILPLL (*see* Self-injection locked phase locked loop (SILPLL) oscillator)
Si-photonics technique, 742–744
SPLL, 725–728
temperature sensitivity improvement, 712
temperature sensitivity measurements, 710–712
thermal sensitivity analysis, 709–710
thermal stability *vs.* phase noise degradation, 712–713
Oscillator amplitude stabilization
base-emitter RF voltage, 601
collector-emitter RF voltage, 601
current tips as function of narrow conduction angles, 598
normalized Fourier coefficients, 597
predicted output power of oscillator, 600
predicted phase noise, 600
quarter-wavelength oscillator
grounded source electrode, 595
square-law characteristic, 596
UHF oscillator, 599
small-signal theory, 594
Oscillator fluctuations, 67, 68, 94
Oscillator hacking
high-Q (type B/D) oscillators, 151–152
moderate/low-Q (type A/C) oscillators, 146–147
Rakon HSO 14 OCXO, 5 MHz, 152–153
synergy microwave DCMO 1027, 100–270 MHz VCO, 149–151
synergy microwave DRO100, 10 GHz DRO, 148–149
Oscillator noise analysis, 624–625
Overlapped Allan variance, 95

P

Parabolic variance (PVAR), 96
Parallel feedback type DRO, 676–677
Parallel resonant circuits, 340–342
Parallel spectrum analyzer, 68
Parametric frequency divider, 111
Parametric noise, 82–83
Parseval theorem, 69, 72, 106, 160
Phase accumulator method
block diagram, 211–212
delta phase register, 205, 206
design variables, 212
modulation, 215
output spectrum, 205, 206
ROM storage, 214–215
SNR, 213–214
tuning equation, 205
Phase detectors, 357, 359
output voltage, 2
quasi-digital, 3–4
sinusoidal, 3
waveform and transient characteristic, 3
Phase/frequency comparator, 7
digital tri-state comparators
antibacklash feature, 377, 378
average output voltage, 372, 373
CD4046 PLL IC, 374, 375
D flip-flops and NAND gate, 370, 371
logic diagram, 370, 372
Motorola MC12040, 374, 376
output pulses, 377, 378
quad-*D* circuit, 372, 374
response of frequency/phase detector near loop lock, 377, 379
timing diagram, 370, 373
version of, 374, 377
diode rings, 357–359
edge-triggered JK master/slave flip-flops, 368–371
exclusive-OR gate, 358, 360–362
sample/hold detectors, 362–368
types, 357
Phase/frequency detector (PFD), 129–132
Phase interpolator, 246
Phase-locked loops (PLLs), 66, 107, 111–113, 128, 314, 315, 534, 545
acquisition (*see* Acquisition)
analog, 3
analysis, 723–724
block diagram, 1–3
characteristics, 3–7
definition, 2
digital loops
input and output waveforms, 8–9
with mixers, 40–44
phase/frequency comparator, 7
sample/hold comparator, 7–8
higher-order loops, 36–40
sinusoidal phase detector, 3
type 1 first-order loop
acquisition time, 10–11

Phase-locked loops (PLLs) (*Continued*)
error function, 11
reference frequency, 11–12
transfer function, 10
type 1 second-order loop
block diagram, 12–13
error signal, 14
frequency response, 12–13
noise bandwidth, 17, 18
rise time, 13
simple resistor-capacitor *(RC)* filter, 14–16
transfer function, 12, 16
zero phase error, 19
type 2 second-order loop
active filter, 23, 25–26
lock-in characteristic, 24–25
noise bandwidth, 21
passive filter, 23–24, 26–27
pull-in characteristic, 22–23
steady-state error, 21
transfer function, 20–21
type 2 third-order loop
FM noise suppression, 35–36
loop filter, 27, 28
transfer function, 28–35
Phase noise
AD9914 block diagram, 233
additive noise, 82–83
amplifiers
isolation amplifiers, 103–104
low PM noise amplifier, 102–103
white and flicker phase noise, 100–102
artifacts, 190, 192
bridge (interferometric) method
appealing features, 187–188
building own system, 189
implementation intended for 8–10 GHz operation, 189–190
phase-to-voltage gain and background noise, 188–189
circumventing the resonator's thermal noise, 144–146
clock frequency and output frequency, 232–233
clock signal
fractional frequency fluctuation, 68
microwave spectrum of an oscillator, 66
notations, 67
time-domain representation of AM and PM noise, 67
time fluctuation/phase time fluctuation, 67
cross-spectrum method, 180, 182
AM noise effect, 186–187
disturbing signal, 182–183
dual-channel phase-noise measurement system, 166
DUT noise, 166, 167, 173, 182, 188
measurement uncertainty, 183–184
rejection of the background noise, 167–170
thermal energy in input power divider, 184–185
digital instruments
CORDIC algorithm, 172
Jackson Labs PhaseStation 53100A, 176–178
microsemi family of phase noise and Allan deviation tester, 173–175
Nyquist zones, 171
quantization noise power, 172
Rohde & Schwarz FSWP family of phase noise analyzers, 178–180
direct digital synthesizer
phase noise, 122–128
signal to quantization ratio, 118–119
theory of operation, 117–118
truncation spurs, 119–122
double-balanced mixer instruments
amplifiers and other two-port components measurement, 162–163
asymmetric driving for low-power signals, 160
background noise, spurs, and other experimental issues, 158
discriminator method, 163–166
heterodyne measurement of oscillators, 161–162
mixer and flicker white noise, 159–160
mixer and LNA white noise, 159
PLL error function, 156
tight PLL for phase noise measurement, 157
flicker noise, 77
frequency counters (*see* Frequency counters)
frequency dividers
analog frequency dividers, 110–112
digital frequency dividers, 104–106
Λ divider, 106–110
phase noise scaling, 106–107
phase-type noise, 108
time-type noise, 108
frequency multipliers
carrier collapse, 116
dedicated frequency multiplier, 113
locked oscillator, 113
NLTL, 114
step recovery diode, 114
frequency stability PSD, 86–87
heuristic derivation of L(f) and $S_\theta(f)$ in the simple case of additive noise, 79–82
HP8770A signal generator, 231–232
large-signal circuit analysis
harmonic balance method, 762
Infineon BFP520, 763, 765, 766
Kaertner oscillator, 764, 767, 768
"Microwave Harmonica" software, 767, 768
Network Analyzer, 763, 764
X-band GaAs monolithic low noise amplifier, 762, 763
Leeson model, 144
oscillator loop and companion circuit, 134–135
oscillator's phase-noise transfer function, 138–139
phase noise of the complete oscillator, 139–141
resonator and its impulse response, 135–138
10 MHz OCXO, 141–143

low-Fourier-frequency part of the phase noise PSD, 87
noise contribution from power supplies, 132–133
noise factor, 72–76, 82
noise figure, 72
noise temperature, 72–74, 76–77
oscillator hacking
  high-Q (type B/D) oscillators, 151–152
  moderate/low-Q (type A/C) oscillators, 146–147
  Rakon HSO 14 OCXO, 5 MHz, 152–153
  synergy microwave DCMO 1027, 100–270 MHz VCO, 149–151
  synergy microwave DRO100, 10 GHz DRO, 148–149
parametric noise, 82–83
phase/frequency detector noise, 129–132
phase noise spectrum
  1-GHz oscillator, 193
  100 MHz oscillator, 192
  two port device, 190, 191
polynomial law
  flicker frequency noise, 85
  flicker PM noise, 83
  frequency drift, 85
  for PM and FM noise, 84
  random walk of frequency, 85
  white frequency noise, 83
power spectral density, 68–70
quantities S_θ *(f),* S_x *(f), L(f),* and S_α *(f),* 78–79
REF CLK source, 234–235
RF spectrum of oscillator signal, 87–88
self-oscillator/autonomous oscillator, 133
Shot (Schottky) noise, 71–72
sideband, computation
  bias-dependent noise model, 609–617
  discriminator stabilized DRO, 639–641
  frequency-conversion approach, 625–628
  harmonic balance serenade program, 607, 608
  high-Q case Microstrip DRO, 628–629
  low phase noise FET oscillator, 632–637
  millimeter-wave applications, 636–639
  model derivation, 617–619
  noise figure of mixer circuits, 622–624
  noise generation in oscillators, 608–609
  noisy circuits, general concept, 619–622
  numerical approach, 628
  1-GHz ceramic resonator VCO, 630–632
  oscillator noise analysis, 624–625
  10 MHz crystal oscillator, 629–631
  workstation, 641, 642
spurs, 77–78, 190–192
Thermal (Johnson) noise, 71
350 MHz Colpitts oscillator
  discrete components, 277
  drive level, 280, 281
  inductor Q variation, 281–282
  Mathcad calculation, 277, 278
  mathematical expression, 276
  parallel-tuned Colpitts configuration, 278–280
  Y_{21}/Y_{11} large-signal condition, 280
  2400 MHz MOSFET-based push–pull oscillator, 329–332
  two-tone intermodulation, 231–232
Phase noise scaling, 106–107
Phase-noise transfer function, 138–139
Phase register, 242–245, 248, 250
Phase-type noise, 108
Π frequency counter, 89–90
Polar form, 559
Poles, 567
Polynomial law
  flicker frequency noise, 85
  flicker PM noise, 83
  frequency drift, 85
  for PM and FM noise, 84
  random walk of frequency, 85
  white frequency noise, 83
Power spectral density (PSD), 68–70
Power spectrum (PS), 69, 70
Printed circuit board (PCB), 685
Probability density function (PDF), 169
Programmable dividers
  asynchronous counters, 393–395
  implementation, 405–406
  look-ahead
    block diagram, 411
    CMOS divider chain, 412
    delays, 414–420
    division by 584, 413
    10/11 counter, 413–414
  swallow counters/dual-modulus counters, 407–410
  synchronous up-/down-counters, 394, 396–400
    application, 403
    block diagram, 402, 404
    logic diagram, 401, 403, 404
    timing table, 401, 402
Pull-in range, 7
Push–push VCO, 605

Q

Quarter-wavelength oscillator, 590–594
Quartz oscillators, 77, 112, 114, 143, 144, 146, 186, 192

R

Radio frequency (RF), 475, 515, 519 *see also* Optoelectronic oscillator (OEO)
Raman amplification (RA), 714–717
RAM-based synthesis
  applications, 219
  block diagram, 215–216
  components, 216–217
  design variables, 217–219
Ramp, 584
Random frequency fluctuation/error, 68
Random walk, 85, 554–555
Rectangular form, 559

Reference frequency standards
  crystal oscillators, 352–354
  specifying oscillators, 351–352
Regenerative frequency divider, 110, 111
Resistor-capacitor (RC) filters
  active, 422–423
  passive, 421–422
Resolution bandwidth (RBW), 69, 70, 88, 180
Rohde & Schwarz FSWP family of phase noise analyzers, 178–180
Rohde & Schwarz SMDU oscillator, 594
R&S®FSWP phase noise analyzer
  architecture, 774–776
  frequency settling
    block diagram, 771–772
    frequency trigger, 776–778
    measurement, 772–774
    test setup, 772, 776, 777
    time measurement, 777, 779–780
  phase settling, 777, 779–780

S

Sample/hold comparator, 7–8
SAW oscillator, 445–447
Schottky diode multiplier, 115
Schottky rectifiers, 115
Schottky/Shot noise, 338
SDR0800-8 oscillator, 698, 699
Self-acquisition, 7
Self-injection locked (SIL) oscillator
  analysis, 720–722
  experimental verification, 721–723
Self-injection locked phase locked loop (SILPLL) oscillator
  analysis, 728–730
  block diagram, 731
  K-band frequency synthesizer
    computer control program, 738, 739
    custom fiber mandrills, 737
    EDFA, 738, 739
    fiber laser source, 737, 738
    linear frequency modulation, 740
    measured phase noise, 740
    optical components, 737–739
    pseudo-random frequency hopped pattern, 740, 741
    results, 741
  MZM, 731–732
  X-band frequency synthesizer
    optical transversal filter, 733–737
    performances, 732, 733
    phase noise and side-modes, 732
    results, 741
    YIG filter, 733
Self-injection locking (SIL), 751, 752
Self-oscillator/autonomous oscillator, 133
Self phase locked loop (SPLL) oscillator
  analysis, 725–727
  experimental verification, 726–728
Series feedback oscillator
  configuration, 314
  implementation, 318–322
  output impedance, 314–317
  phase noise, 318
  Z-parameters, 315
Series feedback (reflection) type DRO, 675–676
Short fractional frequency, 68
Shot (Schottky) noise, 71–72
SiGe oscillator, 302, 305–306
Signal generator
  analog, 534, 536
  I/*Q* modulator, 534, 537, 538
  vector, 534, 537
Signal quality
  data skew, 231
  implementation effects, 231
  nonlinear transition effects, 229, 231
  output transfer function characteristics, 231
  phase noise, 231–235
  quantization effects, 220
  two-tone intermodulation distortion, 231
Signal-to-noise ratio (SNR), 72, 74, 213, 214
Signal to quantization ratio (SQR), 118–119
Single-sideband mixer, 355
Single-sideband (SSB) phase, 489, 491–492, 496, 522
Small-scale integration complementary MOS (CMOS) dividers, 105
Small-signal theory, 594
Smith chart, 74, 75, 432–433
Solid-core photonic crystal fiber (SC-PCF)
  phase noise measurements, 708–709
  temperature sensitivity measurements, 710–712
  thermal sensitivity analysis, 709, 710
S-parameters, 265–268
Split-ring-resonator (SRR) structures, 694
Spurious free dynamic range (SFDR), 232
Spurs, 77–78
Spur-suppression techniques, 427–430
Steady-state error, 6
Step loop, 483
Step recovery diode (SRD), 114
Swallow counters/dual-modulus counters, 407–410
Synthesizers
  digital modulation, 526–527
  direct frequency synthesis, 471–473
  information channel, 526–527
  low-noise microwave synthesizers (*see* Low-noise microwave synthesizers)
  maximum likelihood estimation, 526, 528
  microprocessor applications, 518–520, 522–523
  modulated carrier
    generation, 529–535
    representation, 527–529
  multiple loops (*see* Multiple-loop synthesizer)
  system analysis
    comb generator, 480

dual-loop synthesizer, 481
free-running oscillator, 477–478
multi-loop synthesizer, 484–485
single-loop synthesizer, 477–478
triple-loop synthesizer, 482–484
transceiver applications, 523–526

T

T-equivalent circuit, 609, 612
10 MHz OCXO, 141–143
Termination-insensitive mixers, 355, 356
Thermal (Johnson) noise, 71
350 MHz fixed-frequency Colpitts oscillator
BFG520, 269
biasing, 269–271
coupling capacitor, 276
large-signal transconductance
dc transconductance, 271
drive level, 271, 274–276
emitter–base voltage, 272
feedback factor, 272
noise, 274–276
passive components, 272
quadratic equation, 273, 274
parameters, 269
phase noise
discrete components, 277
drive level, 280, 281
inductor Q variation, 281–282
Mathcad calculation, 277, 278
mathematical expression, 276
parallel-tuned Colpitts configuration, 278–280
Y_{21}/Y_{11} large-signal condition, 280
Time fluctuation, 67, 78, 85, 89, 90, 106, 108, 113, 123, 124
Time-type noise, 108
T-notch filter, 368
Transit time and recombination noise, 338
Triple self-phase locking (TSPLL), 751, 752
TriQuint TGA2216, 388–392
Tri-state phase/frequency comparator, 4
Truncation spurs, 119–122
Tuning diodes
capacitance/voltage characteristics, 339
devices, 340
parallel capacitance, 342–343
parallel resonant circuits, 340–342
practical circuits, 344–345
Tuning equation, 205
Tuning range, 7
2400 MHz MOSFET-based push–pull oscillator
AM-to-PM conversion, 333–336
design calculations, 327–329
design equations, 322, 325–327
1/f noise, 330, 332–334
phase noise, 329–332
2000 MHz GaAs FET-based oscillator, 300, 302–304
Type 1 first-order loop
acquisition time, 10–11
error function, 11
reference frequency, 11–12
transfer function, 10
Type 1 second-order loop
block diagram, 12–13
error signal, 14
frequency response, 12–13
noise bandwidth, 17, 18
rise time, 13
simple resistor-capacitor *(RC)* filter, 14–16
transfer function, 12, 16
zero phase error, 19
Type 2 second-order loop
active filter, 23, 25–26
lock-in characteristic, 24–25
noise bandwidth, 21
passive filter, 23–24, 26–27
pull-in characteristic, 22–23
steady-state error, 21
transfer function, 20–21
Type 2 third-order loop
FM noise suppression, 35–36
loop filter, 27, 28
transfer function, 28–35

U

Ultra-low phase noise DRO
parallel feedback type DRO, 676–677
phase noise-*versus*-offset from carrier, 672
dielectrical resonator selection and characterization, 674
lumped passive components, 672–674
substrate considerations, 674
physical embodiment, 685
series feedback (reflection) type DRO, 675–676
simulated *vs*. measured results, 683–685
small signal design approach for the parallel feedback type DRO
ADS open-loop *S*-parameter simulation, 682
Agilent/EEsoft ADS strategy, 677–679
amplitude and phase noise before and after minor optimization, 689
bias stabilization circuitry, 680
CAD internal view, 690
DRO without resonator cavity and DR, 691
four-port 3D resonator model, 678, 679
gain characteristics of oscillator core, 681
large signal forward transmission, 688
large-signal open-loop *S*-parameter simulation, 687
layout component with resonator interface and matching structures, 678
noise figure and minimum noise figure *versus* frequency, 681
open-loop *S*-parameters, 684
phase noise results, 690
physical replacement, 685

Ultra-low phase noise DRO (*Continued*)
resonator cavity and DR, 691
resonator layout component, 683
resonator matching section, 688
source and load stability circles, 681
S-parameters *versus* frequency, 686
spectra and time-domain waveforms, 689
10 GHz DRO, 692
unconditional stability, 680
Unwrapped phase, 66, 680

V

Validation circuits, 282–283
4100 MHz oscillator, 297, 300–302
900–1800 MHz half-butterfly resonator-based oscillator
coupled resonator, 308–309
layout information, 306, 307
multiple-coupled resonator, 306
phase noise, 306, 307
push–push configuration, 311–317
Q factor, 309–311
100 MHz crystal oscillator, 283–293
feedback arrangement, 284, 285
input noise power, 286–287
input noise voltage, 286
linear representation, 284, 285
noise power spectral densities, 284, 290–295
noise shaping function, 288–289
noise sources, 287–288
noise transfer function, 290–295
noisy bipolar transistor, 283
non-unity gain, 290
phase noise spectral density, 286–287
1000 MHz CRO
circuit arrangement, 297, 299
component values, 296
diode, 294
emitter and the capacitive feedback, 293, 294
phase noise, 297–298
real and imaginary oscillator, 297, 298
RF amplifier, 294, 296
77 GHz SiGe oscillator, 302, 305–306
2000 MHz GaAs FET-based oscillator, 300, 302–304
Varactor resonators, 452–453, 455–457
Very large-scale integration (VLSI) integrated circuits, 78
Very low phase noise VCO for 800 MHz
frequency response, 604
high-performance VCO, 602
phase noise of signal *vs.* push–push oscillators, 604
push–push VCO, 605
simulated phase noise, 603
stepped impedance hair pin resonator with parallel coupled lines, 603
voltage distribution of the hair pin resonator, 604
Voltage-controlled oscillator (VCO), 2–3, 309
circuit configurations, 665, 666
circuit diagram, 665
fractional *N* configuration, 202–203, 242–244
frequency, 245–246
single-sideband phase noise, 666

W

White and flicker phase noise, 100–102
White frequency noise, 83
Wideband high-gain amplifiers
differential limiters, 382, 383
implementations, 387–393
isolation amplifiers, 382–387
summation amplifier, 378–382

Y

Yttrium iron garnet (YIG) oscillator, 319–322, 448–449, 453–455, 486
block diagram, 492, 495
coarse/fine steering, 492, 495
coarse tuning, 733
free-running high-*Q* YIG oscillator, 489, 491
single-sideband phase noise, 489, 491–492

Z

Zero-order data hold (ZODH), 363–365
Zeros, 567

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